Lattice Semiconductor Corporation - ICE40LP1K-SWG16TR50 Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Discontinued at Digi-Key
Number of LABs/CLBs	160
Number of Logic Elements/Cells	1280
Total RAM Bits	65536
Number of I/O	10
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	16-XFBGA, WLCSP
Supplier Device Package	16-WLCSP (1.4x1.48)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice40lp1k-swg16tr50

Routing

There are many resources provided in the iCE40 devices to route signals individually with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PLB connections are made with three different types of routing resources: Adjacent (spans two PLBs), x4 (spans five PLBs) and x12 (spans thirteen PLBs). The Adjacent, x4 and x12 connections provide fast and efficient connections in the diagonal, horizontal and vertical directions.

The design tool takes the output of the synthesis tool and places and routes the design.

Clock/Control Distribution Network

Each iCE40 device has eight global inputs, two pins on each side of the device. Note that not all GBINs are available in all packages.

These global inputs can be used as high fanout nets, clock, reset or enable signals. The dedicated global pins are identified as GBIN[7:0] and the global buffers are identified as-GBUF[7:0]. These eight inputs may be used as general purpose I/O if they are not used to drive the clock nets. Global buffer GBUF7 in I/O Bank 3 also provides an optional direct LVDS25 or subLVDS differential clock input.

Table 2-2 lists the connections between a specific global buffer and the inputs on a PLB. All global buffers optionally connect to the PLB CLK input. Any four of the eight global buffers can drive logic inputs to a PLB. Even-numbered global buffers optionally drive the Set/Reset input to a PLB. Similarly, odd-numbered buffers optionally drive the PLB clock-enable input.

Table 2-2. Global Buffer (GBUF) Connections to Programmable Logic Blocks

Global Buffer	LUT Inputs	Clock	Reset	Clock Enable
GBUF0	Yes, any 4 of 8 GBUF Inputs	Yes	Yes	
GBUF1		Yes		Yes
GBUF2		Yes	Yes	
GBUF3		Yes		Yes
GBUF4		Yes	Yes	
GBUF5		Yes		Yes
GBUF6		Yes	Yes	
GBUF7		Yes		Yes

The maximum frequency for the global buffers are shown in the iCE40 External Switching Characteristics tables later in this document.

Global Hi-Z Control

The global high-impedance control signal, GHIZ, connects to all I/O pins on the iCE40 device. This GHIZ signal is automatically asserted throughout the configuration process, forcing all user I/O pins into their high-impedance state.

Global Reset Control

The global reset control signal connects to all PLB and PIO flip-flops on the iCE40 device. The global reset signal is automatically asserted throughout the configuration process, forcing all flip-flops to their defined wake-up state. For PLB flip-flops, the wake-up state is always reset, regardless of the PLB flip-flop primitive used in the application.

sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The iCE40 devices have one or more sysCLOCK PLLs. REFERENCECLK is the reference frequency input to the PLL and its source can come from an external I/O pin or from internal routing. EXTFEEDBACK is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The PLLOUT output has an output divider, thus allowing the PLL to generate different frequencies for each output. The output divider can have a value from 1 to 6. The PLLOUT outputs can all be used to drive the iCE40 global clock network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 2-3.

The timing of the device registers can be optimized by programming a phase shift into the PLLOUT output clock which will advance or delay the output clock with reference to the REFERENCECLK clock. This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the t_{LOCK} parameter has been satisfied.

For more details on the PLL, see TN1251, iCE40 sysCLOCK PLL Design and Usage Guide.

Figure 2-3. PLL Diagram

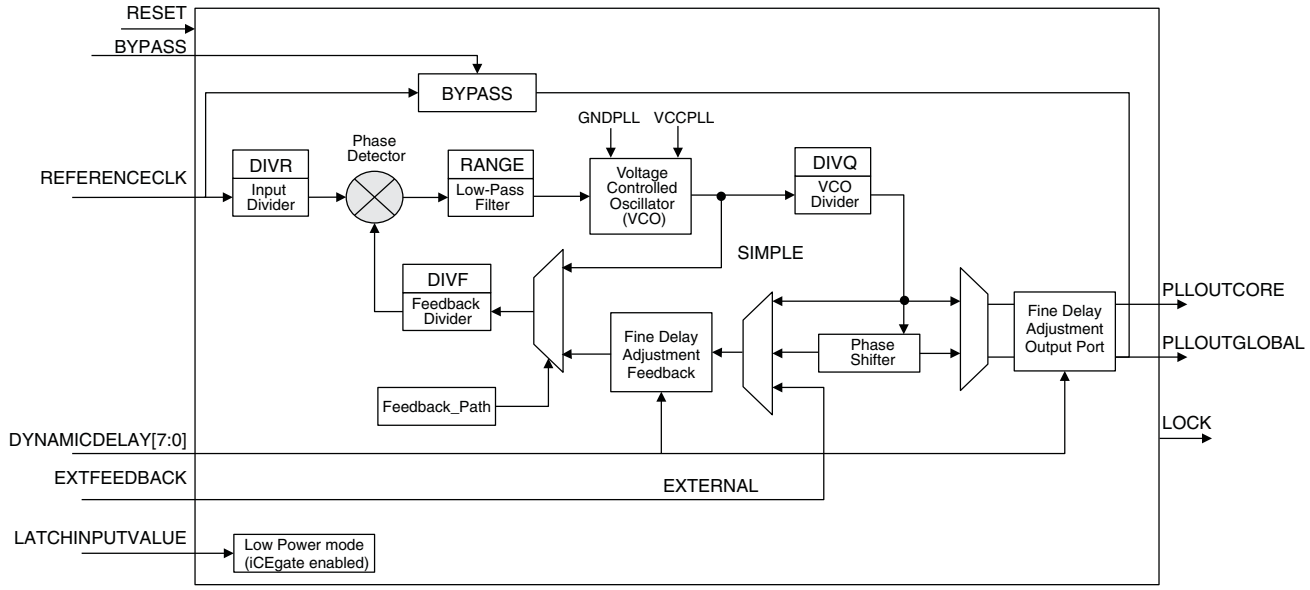


Table 2-3 provides signal descriptions of the PLL block.

Table 2-3. PLL Signal Descriptions

Signal Name	Direction	Description
REFERENCECLK	Input	Input reference clock
BYPASS	Input	When FEEDBACK_PATH is set to SIMPLE, the BYPASS control selects which clock signal connects to the PLLOUT output. 0 = PLL generated signal 1 = REFERENCECLK
EXTFEEDBACK	Input	External feedback input to PLL. Enabled when the FEEDBACK_PATH attribute is set to EXTERNAL.
DYNAMICDELAY[3:0]	Input	Fine delay adjustment control inputs. Enabled when DELAY_ADJUSTMENT_MODE is set to DYNAMIC.
LATCHINPUTVALUE	Input	When enabled, forces the PLL into low-power mode; PLL output is held static at the last input clock value. Set ENABLE ICEGATE_PORTA and PORTB to '1' to enable.
PLLOUTGLOBAL	Output	Output from the Phase-Locked Loop (PLL). Drives a global clock network on the FPGA. The port has optimal connections to global clock buffers GBUF4 and GBUF5.
PLLOUTCORE	Output	Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTLGOBAL port.
LOCK	Output	When High, indicates that the PLL output is phase aligned or locked to the input reference clock.
RESET	Input	Active low reset.

sysMEM Embedded Block RAM Memory

Larger iCE40 device includes multiple high-speed synchronous sysMEM Embedded Block RAMs (EBRs), each 4 kbit in size. This memory can be used for a wide variety of purposes including data buffering, and FIFO.

sysMEM Memory Block

The sysMEM block can implement single port, pseudo dual port, or FIFO memories with programmable logic resources. Each block can be used in a variety of depths and widths as shown in Table 2-4.

Table 2-4. sysMEM Block Configurations[1]

Block RAM Configuration	Block RAM Configuration and Size	WADDR Port Size (Bits)	WDATA Port Size (Bits)	RADDR Port Size (Bits)	RDATA Port Size (Bits)	MASK Port Size (Bits)
SB_RAM256x16 SB_RAM256x16NR SB_RAM256x16NW SB_RAM256x16NRNW	256x16 (4K)	8 [7:0]	16 [15:0]	8 [7:0]	16 [15:0]	16 [15:0]
SB_RAM512x8 SB_RAM512x8NR SB_RAM512x8NW SB_RAM512x8NRNW	512x8 (4K)	9 [8:0]	8 [7:0]	9 [8:0]	8 [7:0]	No Mask Port
SB_RAM1024x4 SB_RAM1024x4NR SB_RAM1024x4NW SB_RAM1024x4NRNW	1024x4 (4K)	10 [9:0]	4 [3:0]	10 [9:0]	4 [3:0]	No Mask Port
SB_RAM2048x2 SB_RAM2048x2NR SB_RAM2048x2NW SB_RAM2048x2NRNW	2048x2 (4K)	11 [10:0]	2 [1:0]	11 [10:0]	2 [1:0]	No Mask Port

1. For iCE40 EBR primitives with a negative-edged Read or Write clock, the base primitive name is appended with a 'N' and a 'R' or 'W' depending on the clock that is affected.

sysIO

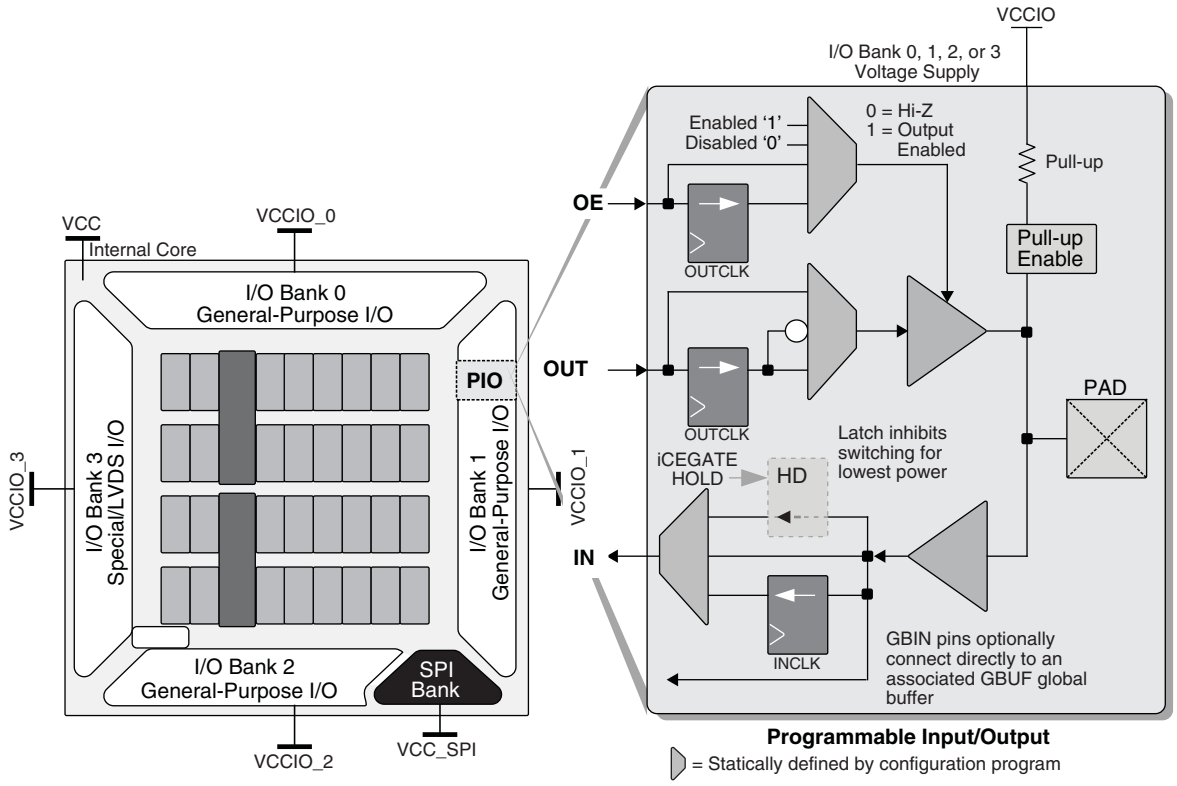
Buffer Banks

iCE40 devices have up to four I/O banks with independent V_{CCIO} rails with an additional configuration bank V_{CC_SPI} for the SPI I/Os.

Programmable I/O (PIO)

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysIO buffers and pads. The PIOs are placed on all four sides of the device.

Figure 2-5. I/O Bank and Programmable I/O Cell



The PIO contains three blocks: an input register block, output register block iCEgate™ and tri-state register block. To save power, the optional iCEgate™ latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Note that the freeze signal is common to the bank. These blocks can operate in a variety of modes along with the necessary clock and selection logic.

Input Register Block

The input register blocks for the PIOs on all edges contain registers that can be used to condition high-speed interface signals before they are passed to the device core. In Generic DDR mode, two registers are used to sample the data on the positive and negative edges of the system clock signal, creating two data streams.

Output Register Block

The output register block can optionally register signals from the core of the device before they are passed to the sysIO buffers. In Generic DDR mode, two registers are used to capture the data on the positive and negative edge of the system clock and then muxed creating one data stream.

Figure 2-6 shows the input/output register block for the PIOs.

Figure 2-6. iCE I/O Register Block Diagram

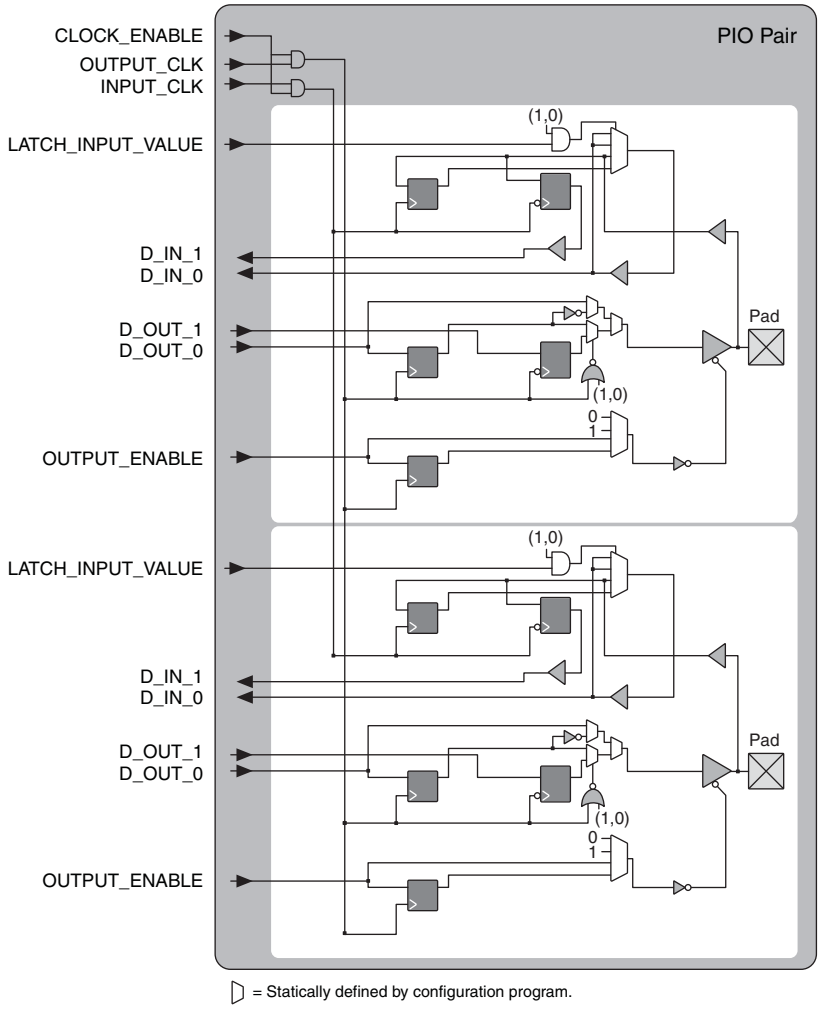


Table 2-6. PIO Signal List

Pin Name	I/O Type	Description
OUTPUT_CLK	Input	Output register clock
CLOCK_ENABLE	Input	Clock enable
INPUT_CLK	Input	Input register clock
OUTPUT_ENABLE	Input	Output enable
D_OUT_0/1	Input	Data from the core
D_IN_0/1	Output	Data to the core
LATCH_INPUT_VALUE	Input	Latches/holds the Input Value

sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysIO buffers allow users to implement a wide variety of standards that are found in today's systems including LVCMOS and LVDS25.

High Current LED Drivers combine three sysIO buffers together. This allows for programmable drive strength. This also allows for high current drivers that are ideal to drive three white LEDs, or one RGB LED. Each bank is capable of supporting multiple I/O standards including single-ended LVCMOS buffers and differential LVDS25E output buf-

iCE40 LP/HX Family Data Sheet DC and Switching Characteristics

October 2015 Data Sheet DS1040

Absolute Maximum Ratings[1, 2, 3, 4]

	iCE40 LP/HX
Supply Voltage V_{CC}	–0.5 V to 1.42 V
Output Supply Voltage V_{CCIO}, V_{CC_SPI}	–0.5 V to 3.60 V
NVCM Supply Voltage V_{PP_2V5}	–0.5 V to 3.60 V
PLL Supply Voltage V_{CCPLL}	–0.5 V to 1.30 V
I/O Tri-state Voltage Applied	–0.5 V to 3.60 V
Dedicated Input Voltage Applied	–0.5 V to 3.60 V
Storage Temperature (Ambient)	–65 °C to 150 °C
Junction Temperature (T_J)	–55 °C to 125 °C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. IOs can support a 200 mV Overshoot above the Recommend Operating Conditions V_{CCIO} (Max) and -200mV Undershoot below V_{IL} (Min). Overshoot and Undershoot is permitted for 25% duty cycle but must not exceed 1.6 ns.

Recommended Operating Conditions[1]

Symbol	Parameter		Min.	Max.	Units
V_{CC}[1]	Core Supply Voltage		1.14	1.26	V
V_{PP_2V5}	V_{PP_2V5} NVCM Programming and Operating Supply Voltage	Slave SPI Configuration	1.71	3.46	V
		Master SPI Configuration	2.30	3.46	V
		Configure from NVCM	2.30	3.46	V
		NVCM Programming	2.30	3.00	V
V_{PP_FAST}[4]	Optional fast NVCM programming supply. Leave unconnected.		N/A	N/A	V
V_{CCPLL}[5, 6]	PLL Supply Voltage		1.14	1.26	V
V_{CCIO}[1, 2, 3]	I/O Driver Supply Voltage	$V_{CCIO0-3}$	1.71	3.46	V
		V_{CC_SPI}	1.71	3.46	V
t_{JIND}	Junction Temperature Industrial Operation		–40	100	°C
t_{PROG}	Junction Temperature NVCM Programming		10	30	°C

1. Like power supplies must be tied together. For example, if V_{CCIO} and V_{CC_SPI} are both the same voltage, they must also be the same supply.
2. See recommended voltages by I/O standard in subsequent table.
3. V_{CCIO} pins of unused I/O banks should be connected to the V_{CC} power supply on boards.
4. V_{PP_FAST}, used only for fast production programming, must be left floating or unconnected in applications, except CM36 and CM49 packages MUST have the V_{PP_FAST} ball connected to V_{CCIO_0} ball externally.
5. No PLL available on the iCE40LP384 and iCE40LP640 device.
6. V_{CCPLL} is tied to V_{CC} internally in packages without PLLs pins.

Static Supply Current – HX Devices[1, 2, 3, 4]

Symbol	Parameter	Device	Typ. V_{CC}[4]	Units
I_{CC}	Core Power Supply	iCE40HX1K	296	µA
		iCE40HX4K	1140	µA
		iCE40HX8K	1140	µA
I_{CCPLL}[5]	PLL Power Supply	All devices	0.5	µA
I_{PP_2V5}	NVCM Power Supply	All devices	1.0	µA
I_{CCIO}, I_{CC_SPI}	Bank Power Supply[4] V_{CCIO} = 2.5 V	All devices	3.5	µA

1. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND, on-chip PLL is off. For more detail with your specific design, use the Power Calculator tool. Power specified with master SPI configuration mode. Other modes may be up to 25% higher.
2. Frequency = 0 MHz.
3. T_J = 25 °C, power supplies at nominal voltage.
4. Does not include pull-up.
5. V_{CCPLL} is tied to V_{CC} internally in packages without PLLs pins.

Programming NVCM Supply Current – LP Devices[1, 2, 3, 4]

Symbol	Parameter	Device	Typ. V_{CC}[5]	Units
I_{CC}	Core Power Supply	iCE40LP384	60	µA
		iCE40LP640	120	µA
		iCE40LP1K	120	µA
		iCE40LP4K	350	µA
		iCE40LP8K	350	µA
I_{CCPLL}[6, 7]	PLL Power Supply	All devices	0.5	µA
I_{PP_2V5}	NVCM Power Supply	All devices	2.5	mA
I_{CCIO}[8], I_{CC_SPI}	Bank Power Supply[5]	All devices	3.5	mA

1. Assumes all inputs are held at V_{CCIO} or GND and all outputs are tri-stated.
2. Typical user pattern.
3. SPI programming is at 8 MHz.
4. T_J = 25 °C, power supplies at nominal voltage.
5. Per bank. V_{CCIO} = 2.5 V. Does not include pull-up.
6. No PLL available on the iCE40-LP384 and iCE40-LP640 device.
7. V_{CCPLL} is tied to V_{CC} internally in packages without PLLs pins.
8. V_{PP_FAST}, used only for fast production programming, must be left floating or unconnected in applications, except CM36 and CM49 packages MUST have the V_{PP_FAST} ball connected to V_{CCIO_0} ball externally.

Programming NVCM Supply Current – HX Devices[1, 2, 3, 4]

Symbol	Parameter	Device	Typ. V_{CC}[5]	Units
I_{CC}	Core Power Supply	iCE40HX1K	278	µA
		iCE40HX4K	1174	µA
		iCE40HX8K	1174	µA
I_{CCPLL}[6]	PLL Power Supply	All devices	0.5	µA
I_{PP_2V5}	NVCM Power Supply	All devices	2.5	mA
I_{CCIO}[7], I_{CC_SPI}	Bank Power Supply[5]	All devices	3.5	mA

1. Assumes all inputs are held at V_{CCIO} or GND and all outputs are tri-stated.
2. Typical user pattern.
3. SPI programming is at 8 MHz.
4. T_J = 25 °C, power supplies at nominal voltage.
5. Per bank. V_{CCIO} = 2.5 V. Does not include pull-up.
6. V_{CCPLL} is tied to V_{CC} internally in packages without PLLs pins.
7. V_{PP_FAST}, used only for fast production programming, must be left floating or unconnected in applications.

Peak Startup Supply Current – LP Devices

Symbol	Parameter	Device	Max	Units
I_{CCPEAK}	Core Power Supply	iCE40LP384	7.7	mA
		iCELP640	6.4	mA
		iCE40LP1K	6.4	mA
		iCE40LP4K	15.7	mA
		iCE40LP8K	15.7	mA
$I_{CCPLLPEAK}$[1, 2, 4]	PLL Power Supply	iCE40LP1K	1.5	mA
		iCELP640	1.5	mA
		iCE40LP4K	8.0	mA
		iCE40LP8K	8.0	mA
$I_{PP\_2V5PEAK}$	NVCM Power Supply	iCE40LP384	3.0	mA
		iCELP640	7.7	mA
		iCE40LP1K	7.7	mA
		iCE40LP4K	4.2	mA
		iCE40LP8K	4.2	mA
$I_{PP\_FASTPEAK}$[3]	NVCM Programming Supply	iCE40LP384	5.7	mA
		iCELP640	8.1	mA
		iCE40LP1K	8.1	mA
$I_{CCIOPEAK}$[5], $I_{CC\_SPIPEAK}$	Bank Power Supply	iCE40LP384	8.4	mA
		iCELP640	3.3	mA
		iCE40LP1K	3.3	mA
		iCE40LP4K	8.2	mA
		iCE40LP8K	8.2	mA

1. No PLL available on the iCE40LP384 and iCE40LP640 device.
2. V_{CCPLL} is tied to V_{CC} internally in packages without PLLs pins.
3. V_{PP_FAST}, used only for fast production programming, must be left floating or unconnected in applications, except CM36 and CM49 packages MUST have the V_{PP_FAST} ball connected to V_{CCIO_0} ball externally.
4. While no PLL is available in the iCE40-LP640 the $I_{CCPLLPEAK}$ is additive to I_{CCPEAK}.
5. iCE40LP384 requires V_{CC} to be greater than 0.7 V when V_{CCIO} and V_{CC_SPI} are above GND.

Peak Startup Supply Current – HX Devices

Symbol	Parameter	Device	Max	Units
I_{CCPEAK}	Core Power Supply	iCE40HX1K	6.9	mA
		iCE40HX4K	22.3	mA
		iCE40HX8K	22.3	mA
$I_{CCPLLPEAK}$[1]	PLL Power Supply	iCE40HX1K	1.8	mA
		iCE40HX4K	6.4	mA
		iCE40HX8K	6.4	mA
$I_{PP\_2V5PEAK}$	NVCM Power Supply	iCE40HX1K	2.8	mA
		iCE40HX4K	4.1	mA
		iCE40HX8K	4.1	mA
$I_{CCIOPEAK}$, $I_{CC\_SPIPEAK}$	Bank Power Supply	iCE40HX1K	6.8	mA
		iCE40HX4K	6.8	mA
		iCE40HX8K	6.8	mA

1. V_{CCPLL} is tied to V_{CC} internally in packages without PLLs pins.

sysIO Recommended Operating Conditions

Standard	V_{CCIO} (V)		
	Min.	Typ.	Max.
LVCMOS 3.3	3.14	3.3	3.46
LVCMOS 2.5	2.37	2.5	2.62
LVCMOS 1.8	1.71	1.8	1.89
LVDS25E[1, 2]	2.37	2.5	2.62
subLVDSE[1, 2]	1.71	1.8	1.89

1. Inputs on-chip. Outputs are implemented with the addition of external resistors.
2. Does not apply to Configuration Bank V_{CC_SPI}.

sysIO Single-Ended DC Electrical Characteristics

Input/ Output Standard	V_{IL}		V_{IH}[1]		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} Max. (mA)	I_{OH} Max. (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3	–0.3	0.8	2.0	V_{CCIO} + 0.2 V	0.4	V_{CCIO} – 0.4	8, 16[2], 24[2]	–8, –16[2], –24[2]
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 2.5	–0.3	0.7	1.7	V_{CCIO} + 0.2 V	0.4	V_{CCIO} – 0.4	6, 12[2], 18[2]	–6, –12[2], –18[2]
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 1.8	–0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	V_{CCIO} + 0.2 V	0.4	V_{CCIO} – 0.4	4, 8[2], 12[2]	–4, –8[2], –12[2]
					0.2	V_{CCIO} – 0.2	0.1	–0.1

1. Some products are clamped to a diode when V_{IN} is larger than V_{CCIO}.
2. Only for High Drive LED outputs.

Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.

Maximum sysIO Buffer Performance[2]

I/O Standard	Max. Speed	Units
Inputs		
LVDS25[1]	400	MHz
subLVDS18[1]	400	MHz
LVCMOS33	250	MHz
LVCMOS25	250	MHz
LVCMOS18	250	MHz
Outputs		
LVDS25E	250	MHz
subLVDS18E	155	MHz
LVCMOS33	250	MHz
LVCMOS25	250	MHz
LVCMOS18	155	MHz

1. Supported in Bank 3 only.
2. Measured with a toggling pattern

iCE40 Family Timing Adders

Over Recommended Commercial Operating Conditions - LP Devices[1, 2, 3, 4, 5]

Buffer Type	Description	Timing	Units
Input Adjusters			
LVDS25	LVDS, V_{CCIO} = 2.5 V	–0.18	ns
subLVDS	subLVDS, V_{CCIO} = 1.8 V	0.82	ns
LVCMOS33	LVCMOS, V_{CCIO} = 3.3 V	0.18	ns
LVCMOS25	LVCMOS, V_{CCIO} = 2.5 V	0.00	ns
LVCMOS18	LVCMOS, V_{CCIO} = 1.8 V	0.19	ns
Output Adjusters			
LVDS25E	LVDS, Emulated, V_{CCIO} = 2.5 V	0.00	ns
subLVDSE	subLVDS, Emulated, V_{CCIO} = 1.8 V	1.32	ns
LVCMOS33	LVCMOS, V_{CCIO} = 3.3 V	–0.12	ns
LVCMOS25	LVCMOS, V_{CCIO} = 2.5 V	0.00	ns
LVCMOS18	LVCMOS, V_{CCIO} = 1.8 V	1.32	ns

1. Timing adders are relative to LVCMOS25 and characterized but not tested on every device.
2. LVCMOS timing measured with the load specified in Switching Test Condition table.
3. All other standards tested according to the appropriate specifications.
4. Commercial timing numbers are shown.
5. Not all I/O standards are supported for all banks. See the Architecture section of this data sheet for details.

Over Recommended Commercial Operating Conditions - HX Devices[1, 2, 3, 4, 5]

Buffer Type	Description	Timing	Units
Input Adjusters			
LVDS25	LVDS, V_{CCIO} = 2.5 V	0.13	ns
subLVDS	subLVDS, V_{CCIO} = 1.8 V	1.03	ns
LVCMOS33	LVCMOS, V_{CCIO} = 3.3 V	0.16	ns
LVCMOS25	LVCMOS, V_{CCIO} = 2.5 V	0.00	ns
LVCMOS18	LVCMOS, V_{CCIO} = 1.8 V	0.23	ns
Output Adjusters			
LVDS25E	LVDS, Emulated, V_{CCIO} = 2.5 V	0.00	ns
subLVDSE	subLVDS, Emulated, V_{CCIO} = 1.8 V	1.76	ns
LVCMOS33	LVCMOS, V_{CCIO} = 3.3 V	0.17	ns
LVCMOS25	LVCMOS, V_{CCIO} = 2.5 V	0.00	ns
LVCMOS18	LVCMOS, V_{CCIO} = 1.8 V	1.76	ns

1. Timing adders are relative to LVCMOS25 and characterized but not tested on every device.
2. LVCMOS timing measured with the load specified in Switching Test Condition table.
3. All other standards tested according to the appropriate specifications.
4. Commercial timing numbers are shown.
5. Not all I/O standards are supported for all banks. See the Architecture section of this data sheet for details.

iCE40 External Switching Characteristics – LP Devices [1, 2]

Over Recommended Operating Conditions

Parameter	Description	Device	Min.	Max.	Units
Clocks					
Global Clocks					
f_{MAX_GBUF}	Frequency for Global Buffer Clock network	All iCE40LP devices	—	275	MHz
t_{W_GBUF}	Clock Pulse Width for Global Buffer	All iCE40LP devices	0.92	—	ns
t_{SKEW_GBUF}	Global Buffer Clock Skew Within a Device	iCE40LP384	—	370	ps
		iCE40LP640	—	230	ps
		iCE40LP1K	—	230	ps
		iCE40LP4K	—	340	ps
		iCE40LP8K	—	340	ps
Pin-LUT-Pin Propagation Delay					
t_{PD}	Best case propagation delay through one LUT-4	All iCE40LP devices	—	9.36	ns
General I/O Pin Parameters (Using Global Buffer Clock without PLL)[3]					
t_{SKEW_IO}	Data bus skew across a bank of IOs	iCE40LP384	—	300	ps
		iCE40LP640	—	200	ps
		iCE40LP1K	—	200	ps
		iCE40LP4K	—	280	ps
		iCE40LP8K	—	280	ps
t_{CO}	Clock to Output - PIO Output Register	iCE40LP384	—	6.33	ns
		iCE40LP640	—	5.91	ns
		iCE40LP1K	—	5.91	ns
		iCE40LP4K	—	6.58	ns
		iCE40LP8K	—	6.58	ns
t_{SU}	Clock to Data Setup - PIO Input Register	iCE40LP384	–0.08	—	ns
		iCE40LP640	–0.33	—	ns
		iCE40LP1K	–0.33	—	ns
		iCE40LP4K	–0.63	—	ns
		iCE40LP8K	–0.63	—	ns
t_{H}	Clock to Data Hold - PIO Input Register	iCE40LP384	1.99	—	ns
		iCE40LP640	2.81	—	ns
		iCE40LP1K	2.81	—	ns
		iCE40LP4K	3.48	—	ns
		iCE40LP8K	3.48	—	ns
General I/O Pin Parameters (Using Global Buffer Clock with PLL)[3]					
t_{COPLL}	Clock to Output - PIO Output Register	iCE40LP1K	—	2.20	ns
		iCE40LP4K	—	2.30	ns
		iCE40LP8K	—	2.30	ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	iCE40LP1K	5.23	—	ns
		iCE40LP4K	6.13	—	ns
		iCE40LP8K	6.13	—	ns

Switching Test Conditions

Figure 3-3 shows the output test load used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-3.

Figure 3-3. Output Test Load, LVCMOS Standards

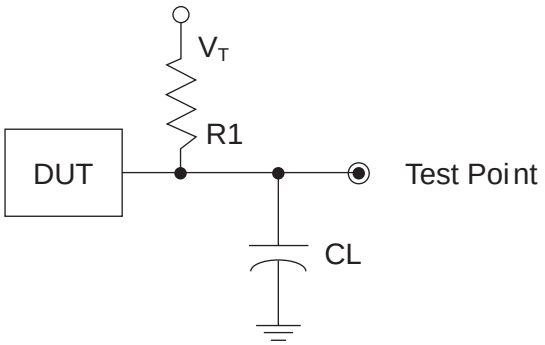


Table 3-3. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R_1	C_L	Timing Reference	V_T
LVCMOS settings (L -> H, H -> L)	∞	0 pF	LVCMOS 3.3 = 1.5 V	—
			LVCMOS 2.5 = $V_{CCIO}/2$	—
			LVCMOS 1.8 = $V_{CCIO}/2$	—
LVCMOS 3.3 (Z -> H)	188	0 pF	1.5	V_{OL}
LVCMOS 3.3 (Z -> L)			1.5	V_{OH}
Other LVCMOS (Z -> H)			$V_{CCIO}/2$	V_{OL}
Other LVCMOS (Z -> L)			$V_{CCIO}/2$	V_{OH}
LVCMOS (H -> Z)			V_{OH} - 0.15	V_{OL}
LVCMOS (L -> Z)			V_{OL} - 0.15	V_{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.

Pin Information Summary

	iCE40LP384			iCE40LP640	iCE40LP1K							
	SG32	CM36[2]	CM49[2]	SWG16	SWG16	CM36[1, 2]	CM49[1, 2]	CM81	CB81	QN84	CM121	CB121
General Purpose I/O per Bank												
Bank 0	6	4	10	3	3	4	10	17	17	17	24	24
Bank 1	5	7	7	0	0	7	7	15	16	17	25	21
Bank 2	0	4	4	1	1	4	4	11	8	11	18	19
Bank 3	6	6	12	2	2	6	10	16	17	18	24	24
Configuration	4	4	4	4	4	4	4	4	4	4	4	4
Total General Purpose Single Ended I/O	21	25	37	10	10	25	35	63	62	67	95	92
High Current Outputs per Bank												
Bank 0	0	0	0	3	3	0	0	0	0	0	0	0
Bank 1	0	0	0	0	0	0	0	0	0	0	0	0
Bank 2	0	0	0	0	0	0	0	0	0	0	0	0
Bank 3	0	0	0	0	0	0	0	0	0	0	0	0
Total Current Outputs	0	0	0	3	3	0	0	0	0	0	0	0
Differential Inputs per Bank												
Bank 0	0	0	0	0	0	0	0	0	0	0	0	0
Bank 1	0	0	0	0	0	0	0	0	0	0	0	0
Bank 2	0	0	0	0	0	0	0	0	0	0	0	0
Bank 3	3	3	6	1	1	3	5	8	9	7	12	12
Total Differential Inputs	3	3	6	1	1	3	5	8	9	7	12	12
Dedicated Inputs per Bank												
Bank 0	0	0	0	0	0	0	0	0	0	0	0	0
Bank 1	0	0	0	0	0	0	0	0	0	0	0	0
Bank 2	2	2	2	1	1	2	2	2	2	2	2	2
Bank 3	0	0	0	0	0	0	0	0	0	0	0	0
Configuration	0	0	0	0	0	0	0	0	0	0	0	0
Total Dedicated Inputs	2	2	2	1	1	2	2	2	2	2	2	2
Vccio Pins												
Bank 0	1	1	1	1	1	1	1	1	1	1	2	1
Bank 1	1	1	1	0	0	0	0	1	1	1	2	1
Bank 2	1	1	1	1	1	1	1	1	1	1	2	1
Bank 3	1	0	0	0	0	0	0	1	1	1	2	2
VCC	1	1	2	1	1	1	2	3	3	4	4	4
VCC_SPI	1	1	1	0	0	1	1	1	1	1	1	1
VPP_2V5	1	1	1	0	0	1	1	1	1	1	1	1
VPP_FAST[3]	0	0	0	0	0	1	1	1	0	1	1	1
VCCPLL	0	0	0	0	0	0	1	1	0	0	1	1
GND	2	3	3	2	2	3	4	5	8	4	8	11
NC	0	0	0	0	0	0	0	0	0	0	0	3
Total Count of Bonded Pins	32	36	49	16	16	36	49	81	81	84	121	121

1. V_{CCIO0} and V_{CCIO1} are connected together.
2. V_{CCIO2} and V_{CCIO3} are connected together.
3. V_{PP_FAST}, used only for fast production programming, must be left floating or unconnected in applications, except CM36 and CM49 packages MUST have the V_{PP_FAST} ball connected to V_{CCIO_0} ball externally.

Pin Information Summary (Continued)

	iCE40LP4K			iCE40LP8K			iCE40HX1K		
	CM81	CM121	CM225	CM81	CM121	CM225	VQ100	CB132	TQ144
General Purpose I/O per Bank									
Bank 0	17	23	46	17	23	46	19	24	23
Bank 1	15	21	42	15	21	42	19	25	25
Bank 2	9	19	40	9	19	40	12	20	20
Bank 3	18	26	46	18	26	46	18	22	24
Configuration	4	4	4	4	4	4	4	4	4
Total General Purpose Single Ended I/O	63	93	178	63	93	178	72	95	96
High Current Outputs per Bank									
Bank 0	0	0	0	0	0	0	0	0	0
Bank 1	0	0	0	0	0	0	0	0	0
Bank 2	0	0	0	0	0	0	0	0	0
Bank 3	0	0	0	0	0	0	0	0	0
Total Differential Inputs	0	0	0	0	0	0	0	0	0
Differential Inputs per Bank									
Bank 0	0	0	0	0	0	0	0	0	0
Bank 1	0	0	0	0	0	0	0	0	0
Bank 2	0	0	0	0	0	0	0	0	0
Bank 3	9	13	23	9	13	23	9	11	12
Total Differential Inputs	9	13	23	9	13	23	9	11	12
Dedicated Inputs per Bank									
Bank 0	0	0	0	0	0	0	0	0	0
Bank 1	0	0	1	0	0	1	0	1	1
Bank 2	2	2	2	2	2	2	2	2	2
Bank 3	0	0	0	0	0	0	0	0	0
Configuration	0	0	0	0	0	0	0	0	0
Total Dedicated Inputs	2	2	3	2	2	3	2	3	3
Vccio Pins									
Bank 0	1	1	3	1	1	3	2	2	2
Bank 1	1	1	3	1	1	3	2	2	2
Bank 2	1	1	3	1	1	3	2	2	2
Bank 3	1	2	4	1	2	4	3	3	2
VCC	3	4	8	3	4	8	4	5	4
VCC_SPI	1	1	1	1	1	1	1	1	1
VPP_2V5	1	1	1	1	1	1	1	1	1
VPP_FAST[1]	1	1	1	1	1	1	1	1	1
VCCPLL	1	2	2	1	2	2	0	1	1
GND	5	12	18	5	12	18	10	14	10
NC	0	0	0	0	0	0	0	2	19
Total Count of Bonded Pins	81	121	225	81	121	225	100	132	144

1. V_{PP_FAST}, used only for fast production programming, must be left floating or unconnected in applications.

Pin Information Summary (Continued)

	iCE40HX4K			iCE40HX8K			
	BG121	CB132	TQ144	BG121	CB132	CM225	CT256
General Purpose I/O per Bank							
Bank 0	23	24	27	23	24	46	52
Bank 1	21	25	29	21	25	42	52
Bank 2	19	18	19	19	18	40	46
Bank 3	26	24	28	26	24	46	52
Configuration	4	4	4	4	4	4	4
Total General Purpose Single Ended I/O	93	95	107	93	95	178	206
High Current Outputs per Bank							
Bank 0	0	0	0	0	0	0	0
Bank 1	0	0	0	0	0	0	0
Bank 2	0	0	0	0	0	0	0
Bank 3	0	0	0	0	0	0	0
Total Differential Inputs	0	0	0	0	0	0	0
Differential Inputs per Bank							
Bank 0	0	0	0	0	0	0	0
Bank 1	0	0	0	0	0	0	0
Bank 2	0	0	0	0	0	0	0
Bank 3	13	12	14	13	12	23	26
Total Differential Inputs	13	12	14	13	12	23	26
Dedicated Inputs per Bank							
Bank 0	0	0	0	0	0	0	0
Bank 1	0	1	1	0	1	1	1
Bank 2	2	2	2	2	2	2	2
Bank 3	0	0	0	0	0	0	0
Configuration	0	0	0	0	0	0	0
Total Dedicated Inputs	2	3	3	2	3	3	3
Vccio Pins							
Bank 0	1	2	2	1	2	3	4
Bank 1	1	2	2	1	2	3	4
Bank 2	1	2	2	1	2	3	4
Bank 3	2	3	2	2	3	4	4
VCC	4	5	4	4	5	8	6
VCC_SPI	1	1	1	1	1	1	1
VPP_2V5	1	1	1	1	1	1	1
VPP_FAST[1]	1	1	1	1	1	1	1
VCCPLL	2	2	2	2	2	2	2
GND	12	15	11	12	15	18	20
NC	0	0	6	0	0	0	0
Total Count of Bonded Pins	121	132	144	121	132	225	256

1. V_{PP_FAST}, used only for fast production programming, must be left floating or unconnected in applications.

iCE40 LP/HX Family Data Sheet Ordering Information

March 2017 Data Sheet DS1040

iCE40 Part Number Description

Ultra Low Power (LP) Devices

ICE40LPXXX – XXXXXXX

Device Family
iCE40 FPGA

Series
LP = Low Power Series

Logic Cells
384 = 384 Logic Cells
640 = 640 Logic Cells
1K = 1,280 Logic Cells
4K = 3,520 Logic Cells
8K = 7,680 Logic Cells

Shipping Method
TR = Tape and Reel
TR50 = Tape and Reel 50 units
TR1K = Tape and Reel 1,000 units

Package
SWG16 = 16-Ball WLCSP (0.35 mm Pitch)
CM36 = 36-Ball ucBGA (0.4 mm Pitch)
CM49 = 49-Ball ucBGA (0.4 mm Pitch)
CM81 = 81-Ball ucBGA (0.4 mm Pitch)
CB81 = 81-Ball csBGA (0.5 mm Pitch)
CM121 = 121-Ball ucBGA (0.4 mm Pitch)
CB121 = 121-Ball csBGA (0.5 mm Pitch)
CM225 = 225-Ball ucBGA (0.4 mm Pitch)
SG32 = 32-Pin QFN (0.5 mm Pitch)
QN84 = 84-Pin QFN (0.5 mm Pitch)

High Performance (HX) Devices

ICE40HXXX – XXXXXXX

Device Family
iCE40 mobileFPGA

Series
HX = High-Performance Series

Logic Cells
1K = 1,280 Logic Cells
4K = 3,520 Logic Cells
8K = 7,680 Logic Cells

Shipping Method
TR = Tape and Reel

Package
CB132 = 132-Ball csBGA (0.5 mm Pitch)
CM225 = 225-Ball ucBGA (0.4 mm Pitch)
CT256 = 256-Ball caBGA (0.8 mm Pitch)
TQ144 = 144-Pin TQFP (0.5 mm Pitch)
VQ100 = 100-Pin VQFP (0.5 mm Pitch)
BG121 = 121-Ball caBGA (0.8 mm Pitch)

All parts shipped in trays unless noted.

Ordering Information

iCE40 devices have top-side markings as shown below:

Industrial

Note: Markings are abbreviated for small packages.

Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Package	Leads	Temp.
ICE40LP384-CM36	384	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP384-CM36TR	384	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP384-CM36TR1K	384	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP384-CM49	384	1.2 V	Halogen-Free ucBGA	49	IND
ICE40LP384-CM49TR	384	1.2 V	Halogen-Free ucBGA	49	IND
ICE40LP384-CM49TR1K	384	1.2 V	Halogen-Free ucBGA	49	IND
ICE40LP384-SG32	384	1.2 V	Halogen-Free QFN	32	IND
ICE40LP384-SG32TR	384	1.2 V	Halogen-Free QFN	32	IND
ICE40LP384-SG32TR1K	384	1.2 V	Halogen-Free QFN	32	IND
ICE40LP640-SWG16TR	640	1.2 V	Halogen-Free WLCSP	16	IND
ICE40LP640-SWG16TR50	640	1.2 V	Halogen-Free WLCSP	16	IND
ICE40LP640-SWG16TR1K	640	1.2 V	Halogen-Free WLCSP	16	IND
ICE40LP1K-SWG16TR	1280	1.2 V	Halogen-Free WLCSP	16	IND
ICE40LP1K-SWG16TR50	1280	1.2 V	Halogen-Free WLCSP	16	IND
ICE40LP1K-SWG16TR1K	1280	1.2 V	Halogen-Free WLCSP	16	IND
ICE40LP1K-CM36	1280	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP1K-CM36TR	1280	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP1K-CM36TR1K	1280	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP1K-CM49	1280	1.2 V	Halogen-Free ucBGA	49	IND
ICE40LP1K-CM49TR	1280	1.2 V	Halogen-Free ucBGA	49	IND
ICE40LP1K-CM49TR1K	1280	1.2 V	Halogen-Free ucBGA	49	IND
ICE40LP1K-CM81	1280	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP1K-CM81TR	1280	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP1K-CM81TR1K	1280	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP1K-CB81	1280	1.2 V	Halogen-Free csBGA	81	IND
ICE40LP1K-CB81TR	1280	1.2 V	Halogen-Free csBGA	81	IND
ICE40LP1K-CB81TR1K	1280	1.2 V	Halogen-Free csBGA	81	IND
ICE40LP1K-CM121	1280	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP1K-CM121TR	1280	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP1K-CM121TR1K	1280	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP1K-CB121	1280	1.2 V	Halogen-Free csBGA	121	IND
ICE40LP1K-QN84	1280	1.2 V	Halogen-Free QFN	84	IND
ICE40LP4K-CM81	3520	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP4K-CM81TR	3520	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP4K-CM81TR1K	3520	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP4K-CM121	3520	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP4K-CM121TR	3520	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP4K-CM121TR1K	3520	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP4K-CM225	3520	1.2 V	Halogen-Free ucBGA	225	IND
ICE40LP8K-CM81	7680	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP8K-CM81TR	7680	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP8K-CM81TR1K	7680	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP8K-CM121	7680	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP8K-CM121TR	7680	1.2 V	Halogen-Free ucBGA	121	IND

Part Number	LUTs	Supply Voltage	Package	Leads	Temp.
ICE40LP8K-CM121TR1K	7680	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP8K-CM225	7680	1.2 V	Halogen-Free ucBGA	225	IND

High-Performance Industrial Grade Devices, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Package	Leads	Temp.
ICE40HX1K-CB132	1280	1.2 V	Halogen-Free csBGA	132	IND
ICE40HX1K-VQ100	1280	1.2 V	Halogen-Free VQFP	100	IND
ICE40HX1K-TQ144	1280	1.2 V	Halogen-Free TQFP	144	IND
ICE40HX4K-BG121	3520	1.2 V	Halogen-Free caBGA	121	IND
ICE40HX4K-BG121TR	3520	1.2 V	Halogen-Free caBGA	121	IND
ICE40HX4K-CB132	3520	1.2 V	Halogen-Free csBGA	132	IND
ICE40HX4K-TQ144	3520	1.2 V	Halogen-Free TQFP	144	IND
ICE40HX8K-BG121	7680	1.2 V	Halogen-Free caBGA	121	IND
ICE40HX8K-BG121TR	7680	1.2 V	Halogen-Free caBGA	121	IND
ICE40HX8K-CB132	7680	1.2 V	Halogen-Free csBGA	132	IND
ICE40HX8K-CM225	7680	1.2 V	Halogen-Free ucBGA	225	IND
ICE40HX8K-CT256	7680	1.2 V	Halogen-Free caBGA	256	IND

iCE40 LP/HX Family Data Sheet Revision History

March 2017 **Data Sheet DS1040**

Date	Version	Section	Change Summary
March 2017	3.3	Introduction	Updated Features section. Added 121-ball caBGA package for ICE40 HX4K/8K to Table 1-1, iCE40 Family Selection Guide.
		Architecture	Updated PLB Blocks section. Changed “subtracters” to “subtractors” in the Carry Logic description.
			Updated Clock/Control Distribution Network section. Switched the “Clock Enable“ and the “Reset” headings in Table 2-2, Global Buffer (GBUF) Connections to Programmable Logic Blocks.
		Pinout Information	Updated Pin Information Summary section. Added BG121information under iCE40HX4K and iCE40HX8K.
		Ordering Information	Updated iCE40 Part Number Description section. Added Shipping Method and BG121 package under High Performance (HX) Devices.
			Updated Ordering Information section. Added part numbers for BG121 under High-Performance Industrial Grade Devices, Halogen Free (RoHS) Packaging.
		Supplemental Information	Corrected reference to “Package Diagrams Data Sheet”.
October 2015	3.2	Introduction	Updated Features section. Added footnote to 16 WLCSP Programmable I/O: Max Inputs (LVDS25) in Table 1-1, iCE40 Family Selection Guide.
		DC and Switching Characteristics	Updated sysCLOCK PLL Timing section. Changed t_{DT} conditions.
			Updated Programming NVCM Supply Current – LP Devices section. Changed I_{PP_2V5} and I_{CCIO}, I_{CC_SPI} units.
March 2015	3.1	DC and Switching Characteristics	Updated sysIO Single-Ended DC Electrical Characteristics section. Changed LVCMOS 3.3 and LVCMOS 2. 5 V_{OH} Min. (V) from 0.5 to 0.4.
July 2014	3.0	DC and Switching Characteristics	Revised and/or added Typ. V_{CC} data in the following sections. — Static Supply Current – LP Devices — Static Supply Current – HX Devices — Programming NVCM Supply Current – LP Devices — Programming NVCM Supply Current – HX Devices In each section table, the footnote indicating Advanced device status was removed.
		Pinout Information	Updated Pin Information Summary section. Added footnote 1 to CM49 under iCE40LP1K.
April 2014	02.9	Ordering Information	Changed “i” to “I” in part number description and ordering part numbers.
			Added part numbers to the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging table.