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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	48
Number of Logic Elements/Cells	384
Total RAM Bits	-
Number of I/O	25
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	36-VFBGA
Supplier Device Package	36-UCBGA (2.5x2.5)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice40lp384-cm36

iCE40 LP/HX Family Data Sheet Introduction

March 2017 | Data Sheet DS1040

Features

- **Flexible Logic Architecture**
  - Five devices with 384 to 7,680 LUT4s and 10 to 206 I/Os
- **Ultra Low Power Devices**
  - Advanced 40 nm low power process
  - As low as 21 µA standby power
  - Programmable low swing differential I/Os
- **Embedded and Distributed Memory**
  - Up to 128 kbits sysMEM™ Embedded Block RAM
- **Pre-Engineered Source Synchronous I/O**
  - DDR registers in I/O cells
- **High Current LED Drivers**
  - Three High Current Drivers used for three different LEDs or one RGB LED
- **High Performance, Flexible I/O Buffer**
  - Programmable sysIO™ buffer supports wide range of interfaces:
    - — LVCMOS 3.3/2.5/1.8
    - — LVDS25E, subLVDS
    - — Schmitt trigger inputs, to 200 mV typical hysteresis
  - Programmable pull-up mode
- **Flexible On-Chip Clocking**
  - Eight low-skew global clock resources
  - Up to two analog PLLs per device
- **Flexible Device Configuration**
  - SRAM is configured through:
    - — Standard SPI Interface
    - — Internal Nonvolatile Configuration Memory (NVCM)
- **Broad Range of Package Options**
  - WLCSP, QFN, VQFP, TQFP, ucBGA, caBGA, and csBGA package options
  - Small footprint package options
    - — As small as 1.40 mm x 1.48 mm
  - Advanced halogen-free packaging

Table 1-1. iCE40 Family Selection Guide

Part Number		LP384	LP640	LP1K	LP4K	LP8K	HX1K	HX4K	HX8K
Logic Cells (LUT + Flip-Flop)		384	640	1,280	3,520	7,680	1,280	3,520	7,680
RAM4K Memory Blocks		0	8	16	20	32	16	20	32
RAM4K RAM bits		0	32K	64K	80K	128K	64K	80K	128K
Phase-Locked Loops (PLLs)		0	0	1[1]	2[2]	2[2]	1[1]	2	2
Maximum Programmable I/O Pins		63	25	95	167	178	95	95	206
Maximum Differential Input Pairs		8	3	12	20	23	11	12	26
High Current LED Drivers		0	3	3	0	0	0	0	0
Package	**Code**	**Programmable I/O: Max Inputs (LVDS25)**							
16 WLCSP (1.40 mm x 1.48 mm, 0.35 mm)	SWG16		10(0)[1]	10(0)[1]					
32 QFN (5 mm x 5 mm, 0.5 mm)	SG32	21(3)							
36 ucBGA (2.5 mm x 2.5 mm, 0.4 mm)	CM36	25(3)		25(3)[1]					
49 ucBGA (3 mm x 3 mm, 0.4 mm)	CM49	37(6)		35(5)[1]					
81 ucBGA (4 mm x 4 mm, 0.4 mm)	CM81			63(8)	63(9)[2]	63(9)[2]			
81 csBGA (5 mm x 5 mm, 0.5 mm)	CB81			62(9)[1]					

Table 2-3. PLL Signal Descriptions

Signal Name	Direction	Description
REFERENCECLK	Input	Input reference clock
BYPASS	Input	When FEEDBACK_PATH is set to SIMPLE, the BYPASS control selects which clock signal connects to the PLLOUT output. 0 = PLL generated signal 1 = REFERENCECLK
EXTFEEDBACK	Input	External feedback input to PLL. Enabled when the FEEDBACK_PATH attribute is set to EXTERNAL.
DYNAMICDELAY[3:0]	Input	Fine delay adjustment control inputs. Enabled when DELAY_ADJUSTMENT_MODE is set to DYNAMIC.
LATCHINPUTVALUE	Input	When enabled, forces the PLL into low-power mode; PLL output is held static at the last input clock value. Set ENABLE ICEGATE_PORTA and PORTB to '1' to enable.
PLLOUTGLOBAL	Output	Output from the Phase-Locked Loop (PLL). Drives a global clock network on the FPGA. The port has optimal connections to global clock buffers GBUF4 and GBUF5.
PLLOUTCORE	Output	Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTLGOBAL port.
LOCK	Output	When High, indicates that the PLL output is phase aligned or locked to the input reference clock.
RESET	Input	Active low reset.

sysMEM Embedded Block RAM Memory

Larger iCE40 device includes multiple high-speed synchronous sysMEM Embedded Block RAMs (EBRs), each 4 kbit in size. This memory can be used for a wide variety of purposes including data buffering, and FIFO.

sysMEM Memory Block

The sysMEM block can implement single port, pseudo dual port, or FIFO memories with programmable logic resources. Each block can be used in a variety of depths and widths as shown in Table 2-4.

Table 2-4. sysMEM Block Configurations[1]

Block RAM Configuration	Block RAM Configuration and Size	WADDR Port Size (Bits)	WDATA Port Size (Bits)	RADDR Port Size (Bits)	RDATA Port Size (Bits)	MASK Port Size (Bits)
SB_RAM256x16 SB_RAM256x16NR SB_RAM256x16NW SB_RAM256x16NRNW	256x16 (4K)	8 [7:0]	16 [15:0]	8 [7:0]	16 [15:0]	16 [15:0]
SB_RAM512x8 SB_RAM512x8NR SB_RAM512x8NW SB_RAM512x8NRNW	512x8 (4K)	9 [8:0]	8 [7:0]	9 [8:0]	8 [7:0]	No Mask Port
SB_RAM1024x4 SB_RAM1024x4NR SB_RAM1024x4NW SB_RAM1024x4NRNW	1024x4 (4K)	10 [9:0]	4 [3:0]	10 [9:0]	4 [3:0]	No Mask Port
SB_RAM2048x2 SB_RAM2048x2NR SB_RAM2048x2NW SB_RAM2048x2NRNW	2048x2 (4K)	11 [10:0]	2 [1:0]	11 [10:0]	2 [1:0]	No Mask Port

1. For iCE40 EBR primitives with a negative-edged Read or Write clock, the base primitive name is appended with a 'N' and a 'R' or 'W' depending on the clock that is affected.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Note the sysMEM Embedded Block RAM Memory address 0 cannot be initialized.

Memory Cascading

Larger and deeper blocks of RAM can be created using multiple EBR sysMEM Blocks.

RAM4k Block

Figure 2-4 shows the 256x16 memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array.

Figure 2-4. sysMEM Memory Primitives

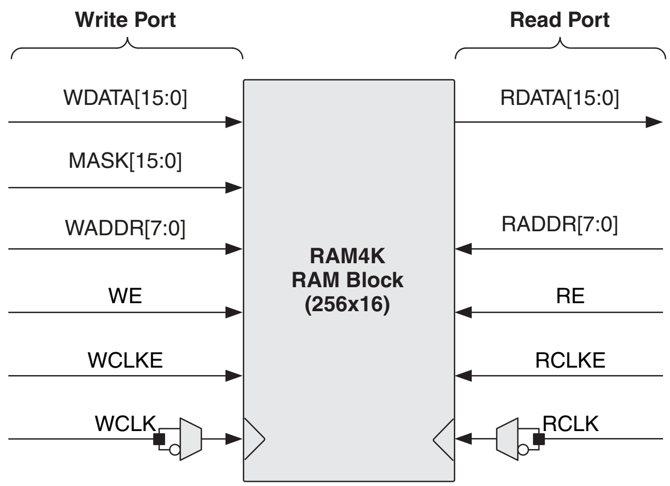


Table 2-5. EBR Signal Descriptions

Signal Name	Direction	Description
WDATA[15:0]	Input	Write Data input.
MASK[15:0]	Input	Masks write operations for individual data bit-lines. 0 = write bit; 1 = don't write bit
WADDR[7:0]	Input	Write Address input. Selects one of 256 possible RAM locations.
WE	Input	Write Enable input.
WCLKE	Input	Write Clock Enable input.
WCLK	Input	Write Clock input. Default rising-edge, but with falling-edge option.
RDATA[15:0]	Output	Read Data output.
RADDR[7:0]	Input	Read Address input. Selects one of 256 possible RAM locations.
RE	Input	Read Enable input.
RCLKE	Input	Read Clock Enable input.
RCLK	Input	Read Clock input. Default rising-edge, but with falling-edge option.

For further information on the sysMEM EBR block, please refer to TN1250, Memory Usage Guide for iCE40 Devices.

Power On Reset

iCE40 devices have power-on reset circuitry to monitor V_{CC}, V_{CCIO_2}, V_{PP_2V5}, and V_{CC_SPI} voltage levels during power-up and operation. At power-up, the POR circuitry monitors V_{CC}, V_{CCIO_2}, V_{PP_2V5}, and V_{CC_SPI} (controls configuration) voltage levels. It then triggers download from the on-chip NVCM or external Flash memory after reaching the power-up levels specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. Before and during configuration, the I/Os are held in tri-state. I/Os are released to user functionality once the device has finished configuration.

Programming and Configuration

This section describes the programming and configuration of the iCE40 family.

Device Programming
The NVCM memory can be programmed through the SPI port.

Device Configuration
There are various ways to configure the Configuration RAM (CRAM) including:

1. Internal NVCM Download
2. From a SPI Flash (Master SPI mode)
3. System microprocessor to drive a Serial Slave SPI port (SSPI mode)

The image to configure the CRAM can be selected by the user on power up (Cold Boot) or once powered up (Warm Boot).

For more details on programming and configuration, see TN1248, iCE40 Programming and Configuration Usage Guide.

Power Saving Options

iCE40 devices are available in two options for maximum flexibility: LP and HX devices. The LP devices have ultra low static and dynamic power consumption. HX devices are designed to provide high performance. Both the LP and the HX devices operate at 1.2 V V_{CC}.

iCE40 devices feature iCEGate and PLL low power mode to allow users to meet the static and dynamic power requirements of their applications. While these features are available in both device types, these features are mainly intended for use with iCE40 LP devices to manage power consumption.

Table 2-9. iCE40 Power Saving Features Description

Device Subsystem	Feature Description
PLL	When LATCHINPUTVALUE is enabled, forces the PLL into low-power mode; PLL output held static at last input clock value.
iCEGate	To save power, the optional iCEgate latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Registered inputs are effectively frozen by their associated clock or clock-enable control.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1, 3, 4, 5, 6, 7]	Input or I/O Leakage	$0V < V_{IN} < V_{CCIO} + 0.2$ V	—	—	+/–10	µA
C_1[6, 7]	I/O Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = Typ., V_{IO} = 0 to V_{CCIO} + 0.2 V	—	6	—	pf
C_2[6, 7]	Global Input Buffer Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = Typ., V_{IO} = 0 to V_{CCIO} + 0.2 V	—	6	—	pf
V_{HYST}	Input Hysteresis	V_{CCIO} = 1.8 V, 2.5 V, 3.3 V	—	200	—	mV
I_{PU}[6, 7]	Internal PIO Pull-up Current	V_{CCIO} = 1.8 V, $0 =< V_{IN} <= 0.65\ V_{CCIO}$	–3	—	–31	µA
		V_{CCIO} = 2.5 V, $0 =< V_{IN} <= 0.65\ V_{CCIO}$	–8	—	–72	µA
		V_{CCIO} = 3.3 V, $0 =< V_{IN} <= 0.65\ V_{CCIO}$	–11	—	–128	µA

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Internal pull-up resistors are disabled.
2. T_J 25°C, f = 1.0 MHz.
3. Please refer to V_{IL} and V_{IH} in the sysIO Single-Ended DC Electrical Characteristics table of this document.
4. Only applies to IOs in the SPI bank following configuration.
5. Some products are clamped to a diode when V_{IN} is larger than V_{CCIO}.
6. High current IOs has three sysIO buffers connected together.
7. The iCE40LP640 and iCE40LP1K SWG16 package has CDONE and a sysIO buffer are connected together.

Static Supply Current – LP Devices[1, 2, 3, 4]

Symbol	Parameter	Device	Typ. V_{CC}[4]	Units
I_{CC}	Core Power Supply	iCE40LP384	21	µA
		iCE40LP640	100	µA
		iCE40LP1K	100	µA
		iCE40LP4K	250	µA
		iCE40LP8K	250	µA
I_{CCPLL}[5, 6]	PLL Power Supply	All devices	0.5	µA
I_{PP_2V5}	NVCM Power Supply	All devices	1.0	µA
I_{CCIO}, I_{CC_SPI}	Bank Power Supply[4] V_{CCIO} = 2.5 V	All devices	3.5	µA

1. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND, on-chip PLL is off. For more detail with your specific design, use the Power Calculator tool. Power specified with master SPI configuration mode. Other modes may be up to 25% higher.
2. Frequency = 0 MHz.
3. T_J = 25 °C, power supplies at nominal voltage.
4. Does not include pull-up.
5. No PLL available on the iCE40LP384 and iCE40LP640 device.
6. V_{CCPLL} is tied to V_{CC} internally in packages without PLLs pins.

Programming NVCM Supply Current – HX Devices[1, 2, 3, 4]

Symbol	Parameter	Device	Typ. V_{CC}[5]	Units
I_{CC}	Core Power Supply	iCE40HX1K	278	µA
		iCE40HX4K	1174	µA
		iCE40HX8K	1174	µA
I_{CCPLL}[6]	PLL Power Supply	All devices	0.5	µA
I_{PP_2V5}	NVCM Power Supply	All devices	2.5	mA
I_{CCIO}[7], I_{CC_SPI}	Bank Power Supply[5]	All devices	3.5	mA

1. Assumes all inputs are held at V_{CCIO} or GND and all outputs are tri-stated.
2. Typical user pattern.
3. SPI programming is at 8 MHz.
4. T_J = 25 °C, power supplies at nominal voltage.
5. Per bank. V_{CCIO} = 2.5 V. Does not include pull-up.
6. V_{CCPLL} is tied to V_{CC} internally in packages without PLLs pins.
7. V_{PP_FAST}, used only for fast production programming, must be left floating or unconnected in applications.

Peak Startup Supply Current – LP Devices

Symbol	Parameter	Device	Max	Units
I_{CCPEAK}	Core Power Supply	iCE40LP384	7.7	mA
		iCELP640	6.4	mA
		iCE40LP1K	6.4	mA
		iCE40LP4K	15.7	mA
		iCE40LP8K	15.7	mA
$I_{CCPLLPEAK}$[1, 2, 4]	PLL Power Supply	iCE40LP1K	1.5	mA
		iCELP640	1.5	mA
		iCE40LP4K	8.0	mA
		iCE40LP8K	8.0	mA
$I_{PP\_2V5PEAK}$	NVCM Power Supply	iCE40LP384	3.0	mA
		iCELP640	7.7	mA
		iCE40LP1K	7.7	mA
		iCE40LP4K	4.2	mA
		iCE40LP8K	4.2	mA
$I_{PP\_FASTPEAK}$[3]	NVCM Programming Supply	iCE40LP384	5.7	mA
		iCELP640	8.1	mA
		iCE40LP1K	8.1	mA
$I_{CCIOPEAK}$[5], $I_{CC\_SPIPEAK}$	Bank Power Supply	iCE40LP384	8.4	mA
		iCELP640	3.3	mA
		iCE40LP1K	3.3	mA
		iCE40LP4K	8.2	mA
		iCE40LP8K	8.2	mA

1. No PLL available on the iCE40LP384 and iCE40LP640 device.
2. V_{CCPLL} is tied to V_{CC} internally in packages without PLLs pins.
3. V_{PP_FAST}, used only for fast production programming, must be left floating or unconnected in applications, except CM36 and CM49 packages MUST have the V_{PP_FAST} ball connected to V_{CCIO_0} ball externally.
4. While no PLL is available in the iCE40-LP640 the $I_{CCPLLPEAK}$ is additive to I_{CCPEAK}.
5. iCE40LP384 requires V_{CC} to be greater than 0.7 V when V_{CCIO} and V_{CC_SPI} are above GND.

Peak Startup Supply Current – HX Devices

Symbol	Parameter	Device	Max	Units
I_{CCPEAK}	Core Power Supply	iCE40HX1K	6.9	mA
		iCE40HX4K	22.3	mA
		iCE40HX8K	22.3	mA
$I_{CCPLLPEAK}$[1]	PLL Power Supply	iCE40HX1K	1.8	mA
		iCE40HX4K	6.4	mA
		iCE40HX8K	6.4	mA
$I_{PP\_2V5PEAK}$	NVCM Power Supply	iCE40HX1K	2.8	mA
		iCE40HX4K	4.1	mA
		iCE40HX8K	4.1	mA
$I_{CCIOPEAK}$, $I_{CC\_SPIPEAK}$	Bank Power Supply	iCE40HX1K	6.8	mA
		iCE40HX4K	6.8	mA
		iCE40HX8K	6.8	mA

1. V_{CCPLL} is tied to V_{CC} internally in packages without PLLs pins.

sysIO Recommended Operating Conditions

Standard	V_{CCIO} (V)		
	Min.	Typ.	Max.
LVCMOS 3.3	3.14	3.3	3.46
LVCMOS 2.5	2.37	2.5	2.62
LVCMOS 1.8	1.71	1.8	1.89
LVDS25E[1, 2]	2.37	2.5	2.62
subLVDSE[1, 2]	1.71	1.8	1.89

1. Inputs on-chip. Outputs are implemented with the addition of external resistors.
2. Does not apply to Configuration Bank V_{CC_SPI}.

sysIO Single-Ended DC Electrical Characteristics

Input/ Output Standard	V_{IL}		V_{IH}[1]		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} Max. (mA)	I_{OH} Max. (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3	–0.3	0.8	2.0	V_{CCIO} + 0.2 V	0.4	V_{CCIO} – 0.4	8, 16[2], 24[2]	–8, –16[2], –24[2]
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 2.5	–0.3	0.7	1.7	V_{CCIO} + 0.2 V	0.4	V_{CCIO} – 0.4	6, 12[2], 18[2]	–6, –12[2], –18[2]
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 1.8	–0.3	0.35V_{CCIO}	0.65V_{CCIO}	V_{CCIO} + 0.2 V	0.4	V_{CCIO} – 0.4	4, 8[2], 12[2]	–4, –8[2], –12[2]
					0.2	V_{CCIO} – 0.2	0.1	–0.1

1. Some products are clamped to a diode when V_{IN} is larger than V_{CCIO}.
2. Only for High Drive LED outputs.

SubLVDS Emulation

The iCE40 family supports the differential subLVDS standard. The output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all banks of the devices. The subLVDS input standard is supported by the LVDS25 differential input buffer. The scheme shown in Figure 3-2 is one possible solution for subLVDSE output standard implementation. Use LVDS25E mode with suggested resistors for subLVDSE operation. Resistor values in Figure 3-2 are industry standard values for 1% resistors.

Figure 3-2. subLVDSE

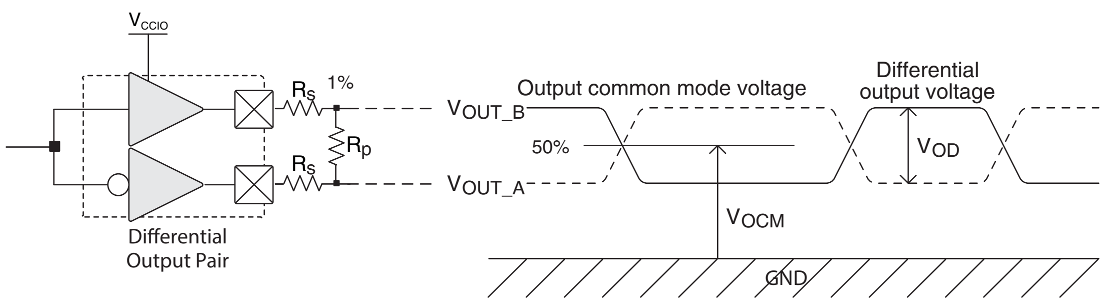


Table 3-2. subLVDSE DC Conditions

Over Recommended Operating Conditions

Parameter	Description	Typ.	Units
Z_{OUT}	Output impedance	20	Ohms
R_S	Driver series resistor	270	Ohms
R_P	Driver parallel resistor	120	Ohms
R_T	Receiver termination	100	Ohms
V_{OH}	Output high voltage	1.43	V
V_{OL}	Output low voltage	1.07	V
V_{OD}	Output differential voltage	0.35	V
V_{CM}	Output common mode voltage	0.9	V
Z_{BACK}	Back impedance	100.5	Ohms
I_{DC}	DC output current	2.8	mA

Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.

Maximum sysIO Buffer Performance[2]

I/O Standard	Max. Speed	Units
Inputs		
LVDS25[1]	400	MHz
subLVDS18[1]	400	MHz
LVCMOS33	250	MHz
LVCMOS25	250	MHz
LVCMOS18	250	MHz
Outputs		
LVDS25E	250	MHz
subLVDS18E	155	MHz
LVCMOS33	250	MHz
LVCMOS25	250	MHz
LVCMOS18	155	MHz

1. Supported in Bank 3 only.
2. Measured with a toggling pattern

iCE40 Family Timing Adders

Over Recommended Commercial Operating Conditions - LP Devices[1, 2, 3, 4, 5]

Buffer Type	Description	Timing	Units
Input Adjusters			
LVDS25	LVDS, V_{CCIO} = 2.5 V	–0.18	ns
subLVDS	subLVDS, V_{CCIO} = 1.8 V	0.82	ns
LVCMOS33	LVCMOS, V_{CCIO} = 3.3 V	0.18	ns
LVCMOS25	LVCMOS, V_{CCIO} = 2.5 V	0.00	ns
LVCMOS18	LVCMOS, V_{CCIO} = 1.8 V	0.19	ns
Output Adjusters			
LVDS25E	LVDS, Emulated, V_{CCIO} = 2.5 V	0.00	ns
subLVDSE	subLVDS, Emulated, V_{CCIO} = 1.8 V	1.32	ns
LVCMOS33	LVCMOS, V_{CCIO} = 3.3 V	–0.12	ns
LVCMOS25	LVCMOS, V_{CCIO} = 2.5 V	0.00	ns
LVCMOS18	LVCMOS, V_{CCIO} = 1.8 V	1.32	ns

1. Timing adders are relative to LVCMOS25 and characterized but not tested on every device.
2. LVCMOS timing measured with the load specified in Switching Test Condition table.
3. All other standards tested according to the appropriate specifications.
4. Commercial timing numbers are shown.
5. Not all I/O standards are supported for all banks. See the Architecture section of this data sheet for details.

Over Recommended Commercial Operating Conditions - HX Devices[1, 2, 3, 4, 5]

Buffer Type	Description	Timing	Units
Input Adjusters			
LVDS25	LVDS, V_{CCIO} = 2.5 V	0.13	ns
subLVDS	subLVDS, V_{CCIO} = 1.8 V	1.03	ns
LVCMOS33	LVCMOS, V_{CCIO} = 3.3 V	0.16	ns
LVCMOS25	LVCMOS, V_{CCIO} = 2.5 V	0.00	ns
LVCMOS18	LVCMOS, V_{CCIO} = 1.8 V	0.23	ns
Output Adjusters			
LVDS25E	LVDS, Emulated, V_{CCIO} = 2.5 V	0.00	ns
subLVDSE	subLVDS, Emulated, V_{CCIO} = 1.8 V	1.76	ns
LVCMOS33	LVCMOS, V_{CCIO} = 3.3 V	0.17	ns
LVCMOS25	LVCMOS, V_{CCIO} = 2.5 V	0.00	ns
LVCMOS18	LVCMOS, V_{CCIO} = 1.8 V	1.76	ns

1. Timing adders are relative to LVCMOS25 and characterized but not tested on every device.
2. LVCMOS timing measured with the load specified in Switching Test Condition table.
3. All other standards tested according to the appropriate specifications.
4. Commercial timing numbers are shown.
5. Not all I/O standards are supported for all banks. See the Architecture section of this data sheet for details.

iCE40 External Switching Characteristics – HX Devices [1, 2]

Over Recommended Operating Conditions

Parameter	Description	Device	Min.	Max.	Units
Clocks					
Primary Clocks					
f_{MAX_GBUF}	Frequency for Global Buffer Clock network	All iCE40HX devices	—	275	MHz
t_{W_GBUF}	Clock Pulse Width for Global Buffer	All iCE40HX devices	0.88	—	ns
t_{SKEW_GBUF}	Global Buffer Clock Skew Within a Device	iCE40HX1K	—	727	ps
		iCE40HX4K	—	300	ps
		iCE40HX8K	—	300	ps
Pin-LUT-Pin Propagation Delay					
t_{PD}	Best case propagation delay through one LUT-4	All iCE40 HX devices	—	7.30	ns
General I/O Pin Parameters (Using Global Buffer Clock without PLL)					
t_{SKEW_IO}	Data bus skew across a bank of IOs	iCE40HX1K	—	696	ps
		iCE40HX4K	—	290	ps
		iCE40HX8K	—	290	ps
t_{CO}	Clock to Output - PIO Output Register	iCE40HX1K	—	5.00	ns
		iCE40HX4K	—	5.41	ns
		iCE40HX8K	—	5.41	ns
t_{SU}	Clock to Data Setup - PIO Input Register	iCE40HX1K	–0.23	—	ns
		iCE40HX4K	–0.43	—	ns
		iCE40HX8K	–0.43	—	ns
t_H	Clock to Data Hold - PIO Input Register	iCE40HX1K	1.92	—	ns
		iCE40HX4K	2.38	—	ns
		iCE40HX8K	2.38	—	ns
General I/O Pin Parameters (Using Global Buffer Clock with PLL)[3]					
t_{COPLL}	Clock to Output - PIO Output Register	iCE40HX1K	—	2.96	ns
		iCE40HX4K	—	2.51	ns
		iCE40HX8K	—	2.51	ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	iCE40HX1K	3.10	—	ns
		iCE40HX4K	4.16	—	ns
		iCE40HX8K	4.16	—	ns
t_{HPLL}	Clock to Data Hold - PIO Input Register	iCE40HX1K	–0.60	—	ns
		iCE40HX4K	–0.53	—	ns
		iCE40HX8K	–0.53	—	ns

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the iCECube2 software.
2. General I/O timing numbers based on LVCMOS 2.5, 0pf load.
3. Supported on devices with a PLL.

SPI Master or NVCM Configuration Time[1, 2]

Symbol	Parameter	Conditions	Typ.	Units
t_{CONFIG}	POR/CRESET_B to Device I/O Active	iCE40LP384 - Low Frequency (Default)	25	ms
		iCE40LP384 - Medium Frequency	15	ms
		iCE40LP384 - High Frequency	11	ms
		iCE40LP640 - Low Frequency (Default)	53	ms
		iCE40LP640 - Medium Frequency	25	ms
		iCE40LP640 - High Frequency	13	ms
		iCE40LP/HX1K - Low Frequency (Default)	53	ms
		iCE40LP/HX1K - Medium Frequency	25	ms
		iCE40LP/HX1K - High Frequency	13	ms
		iCE40LP/HX4K - Low Frequency (Default)	230	ms
		iCE40LP/HX4K - Medium Frequency	110	ms
		iCE40LP/HX4K - High Frequency	70	ms
		iCE40LP/HX8K - Low Frequency (Default)	230	ms
		iCE40LP/HX8K - Medium Frequency	110	ms
		iCE40LP/HX8K - High Frequency	70	ms

1. Assumes sysMEM Block is initialized to an all zero pattern if they are used.
2. The NVCM download time is measured with a fast ramp rate starting from the maximum voltage of POR trip point.

sysCONFIG Port Timing Specifications[1] (Continued)

Symbol	Parameter		Min.	Typ.	Max.	Units
t_{MCLK}	CRESET_B high to first MCLK edge	iCE40LP384 - Low Frequency (Default)	600	—	—	us
		iCE40LP384 - Medium Frequency	600	—	—	us
		iCE40LP384 - High Frequency	600	—	—	us
		iCE40LP640, iCE40LP/HX1K - Low Frequency (Default)	800	—	—	us
		iCE40LP640, iCE40LP/HX1K - Medium Frequency	800	—	—	us
		iCE40LP640, iCE40LP/HX1K - High Frequency	800	—	—	us
		iCE40LP/HX1K -Low Frequency (Default)	800	—	—	us
		iCE40LP/HX1K - Medium Frequency	800	—	—	us
		iCE40LP/HX1K - High Frequency	800	—	—	us
		iCE40LP/HX4K - Low Frequency (Default)	1200	—	—	us
		iCE40LP/HX4K - Medium Frequency	1200	—	—	us
		iCE40LP/HX4K - high frequency	1200	—	—	us
		iCE40LP/HX8K - Low Frequency (Default)	1200	—	—	us
		iCE40LP/HX8K - Medium Frequency	1200	—	—	us
		iCE40LP/HX8K - High Frequency	1200	—	—	us

1. Does not apply for NVCM.
2. Supported only with 1.2 V V_{CC} and at 25 °C.
3. Extended range f_{MAX} Write operations support up to 53 MHz only with 1.2 V V_{CC} and at 25 °C.

Switching Test Conditions

Figure 3-3 shows the output test load used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-3.

Figure 3-3. Output Test Load, LVCMOS Standards

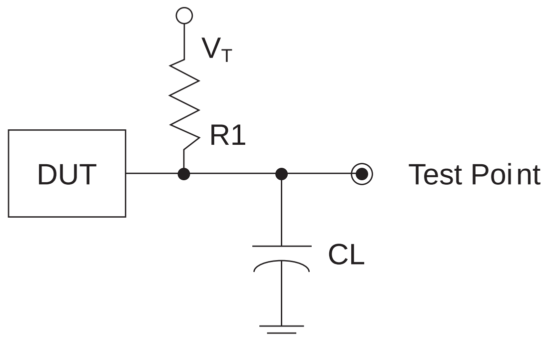


Table 3-3. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R_1	C_L	Timing Reference	V_T
LVCMOS settings (L -> H, H -> L)	∞	0 pF	LVCMOS 3.3 = 1.5 V	—
			LVCMOS 2.5 = $V_{CCIO}/2$	—
			LVCMOS 1.8 = $V_{CCIO}/2$	—
LVCMOS 3.3 (Z -> H)	188	0 pF	1.5	V_{OL}
LVCMOS 3.3 (Z -> L)			1.5	V_{OH}
Other LVCMOS (Z -> H)			$V_{CCIO}/2$	V_{OL}
Other LVCMOS (Z -> L)			$V_{CCIO}/2$	V_{OH}
LVCMOS (H -> Z)			V_{OH} - 0.15	V_{OL}
LVCMOS (L -> Z)			V_{OL} - 0.15	V_{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.

Signal Descriptions

Signal Name	I/O	Descriptions
General Purpose		
IO[Bank]_[Row/Column Number][A/B]	I/O	[Bank] indicates the bank of the device on which the pad is located. [Number] indicates IO number on the device.
IO[Bank]_[Row/Column Number][A/B]	I/O	[Bank] indicates the bank of the device on which the pad is located. [Number] indicates IO number on the device. [A/B] indicates the differential I/O. 'A' = negative input. 'B' = positive input.
HCIO[Bank]_[Number]	I/O	High Current IO. [Bank] indicates the bank of the device on which the pad is located. [Number] indicates IO number.
NC	—	No connect
GND	—	GND – Ground. Dedicated pins. It is recommended that all GNDs are tied together.
VCC	—	VCC – The power supply pins for core logic. Dedicated pins. It is recommended that all VCCs are tied to the same supply.
VCCIO_x	—	VCCIO – The power supply pins for I/O Bank x. Dedicated pins. All VCCIOs located in the same bank are tied to the same supply.
PLL and Global Functions (Used as user-programmable I/O pins when not used for PLL or clock pins)		
VCCPLLx	—	PLL VCC – Power. Dedicated pins. The PLL requires a separate power and ground that is quiet and stable to reduce the output clock jitter of the PLL.
GNDPLLx	—	PLL GND – Ground. Dedicated pins. The sysCLOCK PLL has the DC ground connection made on the FPGA, so the external PLL ground connection (GNDPLL) must NOT be connected to the board's ground.
GBINx	—	Global pads. Two per side.
Programming and Configuration		
CBSEL[0:1]	I/O	Dual function pins. I/Os when not used as CBSEL. Optional ColdBoot configuration SELect input, if ColdBoot mode is enabled.
CRESET_B	I	Configuration Reset, active Low. Dedicated input. No internal pull-up resistor. Either actively drive externally or connect a 10 KOhm pull-up resistor to VCCIO_2.
CDONE	I/O	Configuration Done. Includes a permanent weak pull-up resistor to VCCIO_2. If driving external devices with CDONE output, an external pull-up resistor to VCCIO_2 may be required. Refer to the TN1248, iCE40 Programming and Configuration for more details. Following device configuration the iCE40LP640 and iCE40LP1K in the SWG16 package CDONE pin can be used as a user output.
VCC_SPI	—	SPI interface voltage supply input. Must have a valid voltage even if configuring from NVCM.
SPI_SCK	I/O	Input Configuration Clock for configuring an FPGA in Slave SPI mode. Output Configuration Clock for configuring an FPGA configuration modes.
SPI_SS_B	I/O	SPI Slave Select. Active Low. Includes an internal weak pull-up resistor to VCC_SPI during configuration. During configuration, the logic level sampled on this pin determines the configuration mode used by the iCE40 device. An input when sampled at the start of configuration. An input when in SPI Peripheral configuration mode (SPI_SS_B = Low). An output when in Master SPI Flash configuration mode.
SPI_SI	I/O	Slave SPI serial data input and master SPI serial data output
SPI_SO	I/O	Slave SPI serial data output and master SPI serial data input

Pin Information Summary

	iCE40LP384			iCE40LP640	iCE40LP1K							
	SG32	CM36[2]	CM49[2]	SWG16	SWG16	CM36[1, 2]	CM49[1, 2]	CM81	CB81	QN84	CM121	CB121
General Purpose I/O per Bank												
Bank 0	6	4	10	3	3	4	10	17	17	17	24	24
Bank 1	5	7	7	0	0	7	7	15	16	17	25	21
Bank 2	0	4	4	1	1	4	4	11	8	11	18	19
Bank 3	6	6	12	2	2	6	10	16	17	18	24	24
Configuration	4	4	4	4	4	4	4	4	4	4	4	4
Total General Purpose Single Ended I/O	21	25	37	10	10	25	35	63	62	67	95	92
High Current Outputs per Bank												
Bank 0	0	0	0	3	3	0	0	0	0	0	0	0
Bank 1	0	0	0	0	0	0	0	0	0	0	0	0
Bank 2	0	0	0	0	0	0	0	0	0	0	0	0
Bank 3	0	0	0	0	0	0	0	0	0	0	0	0
Total Current Outputs	0	0	0	3	3	0	0	0	0	0	0	0
Differential Inputs per Bank												
Bank 0	0	0	0	0	0	0	0	0	0	0	0	0
Bank 1	0	0	0	0	0	0	0	0	0	0	0	0
Bank 2	0	0	0	0	0	0	0	0	0	0	0	0
Bank 3	3	3	6	1	1	3	5	8	9	7	12	12
Total Differential Inputs	3	3	6	1	1	3	5	8	9	7	12	12
Dedicated Inputs per Bank												
Bank 0	0	0	0	0	0	0	0	0	0	0	0	0
Bank 1	0	0	0	0	0	0	0	0	0	0	0	0
Bank 2	2	2	2	1	1	2	2	2	2	2	2	2
Bank 3	0	0	0	0	0	0	0	0	0	0	0	0
Configuration	0	0	0	0	0	0	0	0	0	0	0	0
Total Dedicated Inputs	2	2	2	1	1	2	2	2	2	2	2	2
Vccio Pins												
Bank 0	1	1	1	1	1	1	1	1	1	1	2	1
Bank 1	1	1	1	0	0	0	0	1	1	1	2	1
Bank 2	1	1	1	1	1	1	1	1	1	1	2	1
Bank 3	1	0	0	0	0	0	0	1	1	1	2	2
VCC	1	1	2	1	1	1	2	3	3	4	4	4
VCC_SPI	1	1	1	0	0	1	1	1	1	1	1	1
VPP_2V5	1	1	1	0	0	1	1	1	1	1	1	1
VPP_FAST[3]	0	0	0	0	0	1	1	1	0	1	1	1
VCCPLL	0	0	0	0	0	0	1	1	0	0	1	1
GND	2	3	3	2	2	3	4	5	8	4	8	11
NC	0	0	0	0	0	0	0	0	0	0	0	3
Total Count of Bonded Pins	32	36	49	16	16	36	49	81	81	84	121	121

1. V_{CCIO0} and V_{CCIO1} are connected together.
2. V_{CCIO2} and V_{CCIO3} are connected together.
3. V_{PP_FAST}, used only for fast production programming, must be left floating or unconnected in applications, except CM36 and CM49 packages MUST have the V_{PP_FAST} ball connected to V_{CCIO_0} ball externally.

Pin Information Summary (Continued)

	iCE40LP4K			iCE40LP8K			iCE40HX1K		
	CM81	CM121	CM225	CM81	CM121	CM225	VQ100	CB132	TQ144
General Purpose I/O per Bank									
Bank 0	17	23	46	17	23	46	19	24	23
Bank 1	15	21	42	15	21	42	19	25	25
Bank 2	9	19	40	9	19	40	12	20	20
Bank 3	18	26	46	18	26	46	18	22	24
Configuration	4	4	4	4	4	4	4	4	4
Total General Purpose Single Ended I/O	63	93	178	63	93	178	72	95	96
High Current Outputs per Bank									
Bank 0	0	0	0	0	0	0	0	0	0
Bank 1	0	0	0	0	0	0	0	0	0
Bank 2	0	0	0	0	0	0	0	0	0
Bank 3	0	0	0	0	0	0	0	0	0
Total Differential Inputs	0	0	0	0	0	0	0	0	0
Differential Inputs per Bank									
Bank 0	0	0	0	0	0	0	0	0	0
Bank 1	0	0	0	0	0	0	0	0	0
Bank 2	0	0	0	0	0	0	0	0	0
Bank 3	9	13	23	9	13	23	9	11	12
Total Differential Inputs	9	13	23	9	13	23	9	11	12
Dedicated Inputs per Bank									
Bank 0	0	0	0	0	0	0	0	0	0
Bank 1	0	0	1	0	0	1	0	1	1
Bank 2	2	2	2	2	2	2	2	2	2
Bank 3	0	0	0	0	0	0	0	0	0
Configuration	0	0	0	0	0	0	0	0	0
Total Dedicated Inputs	2	2	3	2	2	3	2	3	3
Vccio Pins									
Bank 0	1	1	3	1	1	3	2	2	2
Bank 1	1	1	3	1	1	3	2	2	2
Bank 2	1	1	3	1	1	3	2	2	2
Bank 3	1	2	4	1	2	4	3	3	2
VCC	3	4	8	3	4	8	4	5	4
VCC_SPI	1	1	1	1	1	1	1	1	1
VPP_2V5	1	1	1	1	1	1	1	1	1
VPP_FAST[1]	1	1	1	1	1	1	1	1	1
VCCPLL	1	2	2	1	2	2	0	1	1
GND	5	12	18	5	12	18	10	14	10
NC	0	0	0	0	0	0	0	2	19
Total Count of Bonded Pins	81	121	225	81	121	225	100	132	144

1. V_{PP_FAST}, used only for fast production programming, must be left floating or unconnected in applications.

Pin Information Summary (Continued)

	iCE40HX4K			iCE40HX8K			
	BG121	CB132	TQ144	BG121	CB132	CM225	CT256
General Purpose I/O per Bank							
Bank 0	23	24	27	23	24	46	52
Bank 1	21	25	29	21	25	42	52
Bank 2	19	18	19	19	18	40	46
Bank 3	26	24	28	26	24	46	52
Configuration	4	4	4	4	4	4	4
Total General Purpose Single Ended I/O	93	95	107	93	95	178	206
High Current Outputs per Bank							
Bank 0	0	0	0	0	0	0	0
Bank 1	0	0	0	0	0	0	0
Bank 2	0	0	0	0	0	0	0
Bank 3	0	0	0	0	0	0	0
Total Differential Inputs	0	0	0	0	0	0	0
Differential Inputs per Bank							
Bank 0	0	0	0	0	0	0	0
Bank 1	0	0	0	0	0	0	0
Bank 2	0	0	0	0	0	0	0
Bank 3	13	12	14	13	12	23	26
Total Differential Inputs	13	12	14	13	12	23	26
Dedicated Inputs per Bank							
Bank 0	0	0	0	0	0	0	0
Bank 1	0	1	1	0	1	1	1
Bank 2	2	2	2	2	2	2	2
Bank 3	0	0	0	0	0	0	0
Configuration	0	0	0	0	0	0	0
Total Dedicated Inputs	2	3	3	2	3	3	3
Vccio Pins							
Bank 0	1	2	2	1	2	3	4
Bank 1	1	2	2	1	2	3	4
Bank 2	1	2	2	1	2	3	4
Bank 3	2	3	2	2	3	4	4
VCC	4	5	4	4	5	8	6
VCC_SPI	1	1	1	1	1	1	1
VPP_2V5	1	1	1	1	1	1	1
VPP_FAST[1]	1	1	1	1	1	1	1
VCCPLL	2	2	2	2	2	2	2
GND	12	15	11	12	15	18	20
NC	0	0	6	0	0	0	0
Total Count of Bonded Pins	121	132	144	121	132	225	256

1. V_{PP_FAST}, used only for fast production programming, must be left floating or unconnected in applications.

iCE40 Part Number Description

Ultra Low Power (LP) Devices

ICE40LPXXX – XXXXXXX

Device Family
iCE40 FPGA

Series
LP = Low Power Series

Logic Cells
384 = 384 Logic Cells
640 = 640 Logic Cells
1K = 1,280 Logic Cells
4K = 3,520 Logic Cells
8K = 7,680 Logic Cells

Shipping Method
TR = Tape and Reel
TR50 = Tape and Reel 50 units
TR1K = Tape and Reel 1,000 units

Package
SWG16 = 16-Ball WLCSP (0.35 mm Pitch)
CM36 = 36-Ball ucBGA (0.4 mm Pitch)
CM49 = 49-Ball ucBGA (0.4 mm Pitch)
CM81 = 81-Ball ucBGA (0.4 mm Pitch)
CB81 = 81-Ball csBGA (0.5 mm Pitch)
CM121 = 121-Ball ucBGA (0.4 mm Pitch)
CB121 = 121-Ball csBGA (0.5 mm Pitch)
CM225 = 225-Ball ucBGA (0.4 mm Pitch)
SG32 = 32-Pin QFN (0.5 mm Pitch)
QN84 = 84-Pin QFN (0.5 mm Pitch)

High Performance (HX) Devices

ICE40HXXX – XXXXXXX

Device Family
iCE40 mobileFPGA

Series
HX = High-Performance Series

Logic Cells
1K = 1,280 Logic Cells
4K = 3,520 Logic Cells
8K = 7,680 Logic Cells

Shipping Method
TR = Tape and Reel

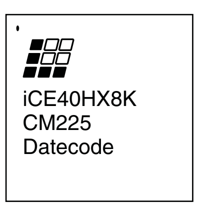
Package
CB132 = 132-Ball csBGA (0.5 mm Pitch)
CM225 = 225-Ball ucBGA (0.4 mm Pitch)
CT256 = 256-Ball caBGA (0.8 mm Pitch)
TQ144 = 144-Pin TQFP (0.5 mm Pitch)
VQ100 = 100-Pin VQFP (0.5 mm Pitch)
BG121 = 121-Ball caBGA (0.8 mm Pitch)

All parts shipped in trays unless noted.

Ordering Information

iCE40 devices have top-side markings as shown below:

Industrial



Note: Markings are abbreviated for small packages.

Part Number	LUTs	Supply Voltage	Package	Leads	Temp.
ICE40LP8K-CM121TR1K	7680	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP8K-CM225	7680	1.2 V	Halogen-Free ucBGA	225	IND

High-Performance Industrial Grade Devices, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Package	Leads	Temp.
ICE40HX1K-CB132	1280	1.2 V	Halogen-Free csBGA	132	IND
ICE40HX1K-VQ100	1280	1.2 V	Halogen-Free VQFP	100	IND
ICE40HX1K-TQ144	1280	1.2 V	Halogen-Free TQFP	144	IND
ICE40HX4K-BG121	3520	1.2 V	Halogen-Free caBGA	121	IND
ICE40HX4K-BG121TR	3520	1.2 V	Halogen-Free caBGA	121	IND
ICE40HX4K-CB132	3520	1.2 V	Halogen-Free csBGA	132	IND
ICE40HX4K-TQ144	3520	1.2 V	Halogen-Free TQFP	144	IND
ICE40HX8K-BG121	7680	1.2 V	Halogen-Free caBGA	121	IND
ICE40HX8K-BG121TR	7680	1.2 V	Halogen-Free caBGA	121	IND
ICE40HX8K-CB132	7680	1.2 V	Halogen-Free csBGA	132	IND
ICE40HX8K-CM225	7680	1.2 V	Halogen-Free ucBGA	225	IND
ICE40HX8K-CT256	7680	1.2 V	Halogen-Free caBGA	256	IND