Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	48
Number of Logic Elements/Cells	384
Total RAM Bits	-
Number of I/O	25
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	36-VFBGA
Supplier Device Package	36-UCBGA (2.5x2.5)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice40lp384-cm36tr1k

iCE40 LP/HX Family Data Sheet Introduction

March 2017 **Data Sheet DS1040**

Features

- **Flexible Logic Architecture**
  - Five devices with 384 to 7,680 LUT4s and 10 to 206 I/Os
- **Ultra Low Power Devices**
  - Advanced 40 nm low power process
  - As low as 21 µA standby power
  - Programmable low swing differential I/Os
- **Embedded and Distributed Memory**
  - Up to 128 kbits sysMEM™ Embedded Block RAM
- **Pre-Engineered Source Synchronous I/O**
  - DDR registers in I/O cells
- **High Current LED Drivers**
  - Three High Current Drivers used for three different LEDs or one RGB LED
- **High Performance, Flexible I/O Buffer**
  - Programmable sysIO™ buffer supports wide range of interfaces:
    - — LVCMOS 3.3/2.5/1.8
    - — LVDS25E, subLVDS
    - — Schmitt trigger inputs, to 200 mV typical hysteresis
  - Programmable pull-up mode
- **Flexible On-Chip Clocking**
  - Eight low-skew global clock resources
  - Up to two analog PLLs per device
- **Flexible Device Configuration**
  - SRAM is configured through:
    - — Standard SPI Interface
    - — Internal Nonvolatile Configuration Memory (NVCM)
- **Broad Range of Package Options**
  - WLCSP, QFN, VQFP, TQFP, ucBGA, caBGA, and csBGA package options
  - Small footprint package options
    - — As small as 1.40 mm x 1.48 mm
  - Advanced halogen-free packaging

Table 1-1. iCE40 Family Selection Guide

Part Number		LP384	LP640	LP1K	LP4K	LP8K	HX1K	HX4K	HX8K
Logic Cells (LUT + Flip-Flop)		384	640	1,280	3,520	7,680	1,280	3,520	7,680
RAM4K Memory Blocks		0	8	16	20	32	16	20	32
RAM4K RAM bits		0	32K	64K	80K	128K	64K	80K	128K
Phase-Locked Loops (PLLs)		0	0	1[1]	2[2]	2[2]	1[1]	2	2
Maximum Programmable I/O Pins		63	25	95	167	178	95	95	206
Maximum Differential Input Pairs		8	3	12	20	23	11	12	26
High Current LED Drivers		0	3	3	0	0	0	0	0
Package	**Code**	**Programmable I/O: Max Inputs (LVDS25)**							
16 WLCSP (1.40 mm x 1.48 mm, 0.35 mm)	SWG16		10(0)[1]	10(0)[1]					
32 QFN (5 mm x 5 mm, 0.5 mm)	SG32	21(3)							
36 ucBGA (2.5 mm x 2.5 mm, 0.4 mm)	CM36	25(3)		25(3)[1]					
49 ucBGA (3 mm x 3 mm, 0.4 mm)	CM49	37(6)		35(5)[1]					
81 ucBGA (4 mm x 4 mm, 0.4 mm)	CM81			63(8)	63(9)[2]	63(9)[2]			
81 csBGA (5 mm x 5 mm, 0.5 mm)	CB81			62(9)[1]					

Global Reset Control

The global reset control signal connects to all PLB and PIO flip-flops on the iCE40 device. The global reset signal is automatically asserted throughout the configuration process, forcing all flip-flops to their defined wake-up state. For PLB flip-flops, the wake-up state is always reset, regardless of the PLB flip-flop primitive used in the application.

sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The iCE40 devices have one or more sysCLOCK PLLs. REFERENCECLK is the reference frequency input to the PLL and its source can come from an external I/O pin or from internal routing. EXTFEEDBACK is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The PLLOUT output has an output divider, thus allowing the PLL to generate different frequencies for each output. The output divider can have a value from 1 to 6. The PLLOUT outputs can all be used to drive the iCE40 global clock network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 2-3.

The timing of the device registers can be optimized by programming a phase shift into the PLLOUT output clock which will advance or delay the output clock with reference to the REFERENCECLK clock. This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the t_{LOCK} parameter has been satisfied.

For more details on the PLL, see TN1251, iCE40 sysCLOCK PLL Design and Usage Guide.

Figure 2-3. PLL Diagram

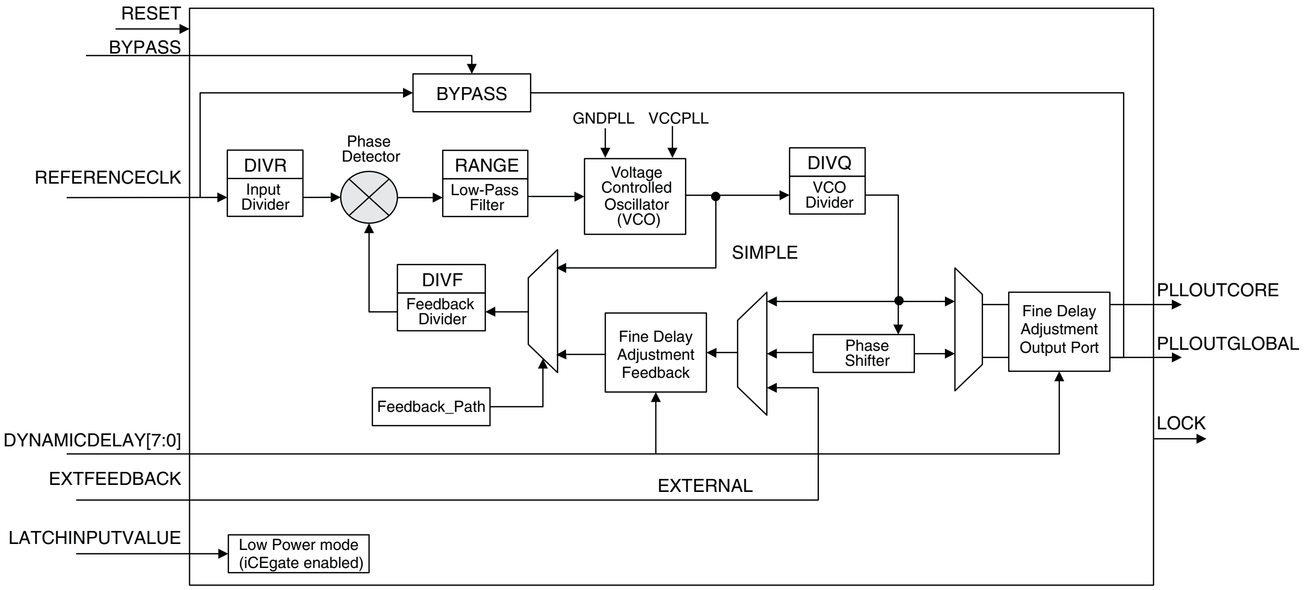


Table 2-3 provides signal descriptions of the PLL block.

Table 2-3. PLL Signal Descriptions

Signal Name	Direction	Description
REFERENCECLK	Input	Input reference clock
BYPASS	Input	When FEEDBACK_PATH is set to SIMPLE, the BYPASS control selects which clock signal connects to the PLLOUT output. 0 = PLL generated signal 1 = REFERENCECLK
EXTFEEDBACK	Input	External feedback input to PLL. Enabled when the FEEDBACK_PATH attribute is set to EXTERNAL.
DYNAMICDELAY[3:0]	Input	Fine delay adjustment control inputs. Enabled when DELAY_ADJUSTMENT_MODE is set to DYNAMIC.
LATCHINPUTVALUE	Input	When enabled, forces the PLL into low-power mode; PLL output is held static at the last input clock value. Set ENABLE ICEGATE_PORTA and PORTB to ‘1’ to enable.
PLLOUTGLOBAL	Output	Output from the Phase-Locked Loop (PLL). Drives a global clock network on the FPGA. The port has optimal connections to global clock buffers GBUF4 and GBUF5.
PLLOUTCORE	Output	Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTLGOBAL port.
LOCK	Output	When High, indicates that the PLL output is phase aligned or locked to the input reference clock.
RESET	Input	Active low reset.

sysMEM Embedded Block RAM Memory

Larger iCE40 device includes multiple high-speed synchronous sysMEM Embedded Block RAMs (EBRs), each 4 kbit in size. This memory can be used for a wide variety of purposes including data buffering, and FIFO.

sysMEM Memory Block

The sysMEM block can implement single port, pseudo dual port, or FIFO memories with programmable logic resources. Each block can be used in a variety of depths and widths as shown in Table 2-4.

Table 2-4. sysMEM Block Configurations[1]

Block RAM Configuration	Block RAM Configuration and Size	WADDR Port Size (Bits)	WDATA Port Size (Bits)	RADDR Port Size (Bits)	RDATA Port Size (Bits)	MASK Port Size (Bits)
SB_RAM256x16 SB_RAM256x16NR SB_RAM256x16NW SB_RAM256x16NRNW	256x16 (4K)	8 [7:0]	16 [15:0]	8 [7:0]	16 [15:0]	16 [15:0]
SB_RAM512x8 SB_RAM512x8NR SB_RAM512x8NW SB_RAM512x8NRNW	512x8 (4K)	9 [8:0]	8 [7:0]	9 [8:0]	8 [7:0]	No Mask Port
SB_RAM1024x4 SB_RAM1024x4NR SB_RAM1024x4NW SB_RAM1024x4NRNW	1024x4 (4K)	10 [9:0]	4 [3:0]	10 [9:0]	4 [3:0]	No Mask Port
SB_RAM2048x2 SB_RAM2048x2NR SB_RAM2048x2NW SB_RAM2048x2NRNW	2048x2 (4K)	11 [10:0]	2 [1:0]	11 [10:0]	2 [1:0]	No Mask Port

1. For iCE40 EBR primitives with a negative-edged Read or Write clock, the base primitive name is appended with a ‘N’ and a ‘R’ or ‘W’ depending on the clock that is affected.

sysIO

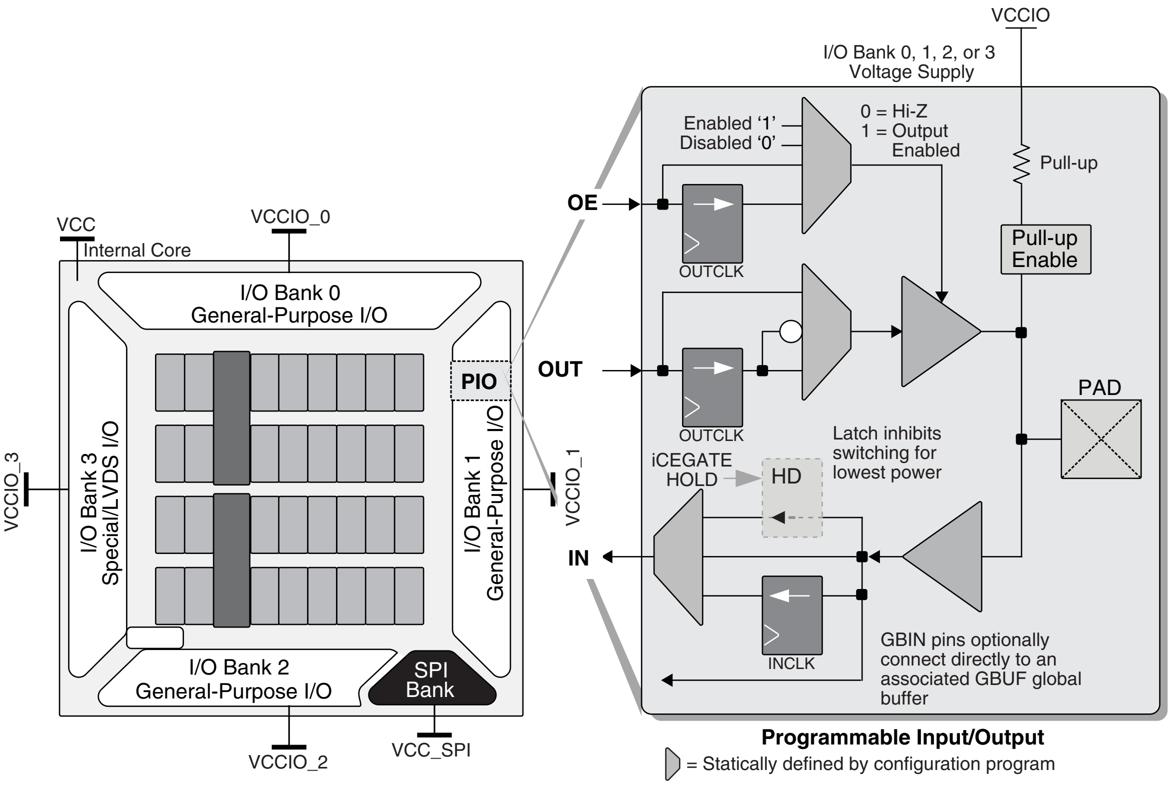
Buffer Banks

iCE40 devices have up to four I/O banks with independent V_{CCIO} rails with an additional configuration bank V_{CC_SPI} for the SPI I/Os.

Programmable I/O (PIO)

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysIO buffers and pads. The PIOs are placed on all four sides of the device.

Figure 2-5. I/O Bank and Programmable I/O Cell



The PIO contains three blocks: an input register block, output register block iCEgate™ and tri-state register block. To save power, the optional iCEgate™ latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Note that the freeze signal is common to the bank. These blocks can operate in a variety of modes along with the necessary clock and selection logic.

Input Register Block

The input register blocks for the PIOs on all edges contain registers that can be used to condition high-speed interface signals before they are passed to the device core. In Generic DDR mode, two registers are used to sample the data on the positive and negative edges of the system clock signal, creating two data streams.

Output Register Block

The output register block can optionally register signals from the core of the device before they are passed to the sysIO buffers. In Generic DDR mode, two registers are used to capture the data on the positive and negative edge of the system clock and then muxed creating one data stream.

Figure 2-6 shows the input/output register block for the PIOs.

fers. Bank 3 additionally supports differential LVDS25 input buffers. Each sysIO bank has its own dedicated power supply.

Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC}, V_{CCIO_2}, V_{PP_2V5}, and V_{CC_SPI} have reached the level defined in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. The default configuration of the I/O pins in a device prior to configuration is tri-stated with a weak pull-up to V_{CCIO}. The I/O pins will maintain the pre-configuration state until V_{CC} and V_{CCIO} (for I/O banks containing configuration I/Os) have reached levels, at which time the I/Os will take on the software user-configured settings only after a proper download/configuration. Unused IOs are automatically blocked and the pullup termination is disabled.

Supported Standards

The iCE40 sysIO buffer supports both single-ended and differential input standards. The single-ended standard supported is LVCMOS. The buffer supports the LVCMOS 1.8, 2.5, and 3.3 V standards. The buffer has individually configurable options for bus maintenance (weak pull-up or none). The High Current output buffer have individually configurable options for drive strength.

Table 2-7 and Table 2-8 show the I/O standards (together with their supply and reference voltages) supported by the iCE40 devices.

Table 2-7. Supported Input Standards

Input Standard	V_{CCIO} (Typical)		
	3.3 V	**2.5 V**	**1.8 V**
Single-Ended Interfaces			
LVCMOS33	Yes		
LVCMOS25		Yes	
LVCMOS18			Yes
Differential Interfaces			
LVDS25[1]		Yes	
subLVDS[1]			Yes

1. Bank 3 only.

Table 2-8. Supported Output Standards

Output Standard	V_{CCIO} (Typical)
Single-Ended Interfaces	
LVCMOS33	3.3
LVCMOS25	2.5
LVCMOS18	1.8
Differential Interfaces	
LVDS25E[1]	2.5
subLVDSE[1]	1.8

1. These interfaces can be emulated with external resistors in all devices.

Non-Volatile Configuration Memory

All iCE40 devices provide a Non-Volatile Configuration Memory (NVCM) block which can be used to configure the device.

For more information on the NVCM, please refer to TN1248, iCE40 Programming and Configuration Usage Guide.

Power Supply Ramp Rates[1, 2]

Symbol	Parameter		Min.	Max.	Units
t_{RAMP}	Power supply ramp rates for all power supplies.	All configuration modes. No power supply sequencing.	0.40	10	V/ms
		Configuring from Slave SPI. No power supply sequencing,	0.01	10	V/ms
		Configuring from NVCM. V_{CC} and V_{PP_2V5} to be powered 0.25 ms before V_{CC_SPI}.	0.01	10	V/ms
		Configuring from MSPI. V_{CC} and V_{PP_SPI} to be powered 0.25 ms before V_{PP_2V5}.	0.01	10	V/ms

1. Assumes monotonic ramp rates.
2. iCE40LP384 requires V_{CC} to be greater than 0.7V when V_{CCIO} and V_{CC_SPI} are above GND.

Power-On-Reset Voltage Levels[1]

Symbol	Device	Parameter		Min.	Max.	Units
V_{PORUP}	iCE40LP384	Power-On-Reset ramp-up trip point (band gap based circuit monitoring VCC, VCCIO_2, VCC_SPI and VPP_2V5)	VCC	0.67	0.99	V
			VCCIO_2	0.70	1.59	V
			VCC_SPI	0.70	1.59	V
			VPP_2V5	0.70	1.59	V
	iCE40LP640, iCE40LP/HX1K, iCE40LP/HX4K, iCE40LP/HX8K	Power-On-Reset ramp-up trip point (band gap based circuit monitoring VCC, VCCIO_2, VCC_SPI and VPP_2V5)	VCC	0.55	0.75	V
			VCCIO_2	0.86	1.29	V
			VCC_SPI	0.86	1.29	V
			VPP_2V5	0.86	1.33	V
V_{PORDN}	iCE40LP384	Power-On-Reset ramp-down trip point (band gap based circuit monitoring VCC, VCCIO_2, VCC_SPI and VPP_2V5)	VCC	—	0.64	V
			VCCIO_2	—	1.59	V
			VCC_SPI	—	1.59	V
			VPP_2V5	—	1.59	V
	iCE40LP640, iCE40LP/HX1K, iCE40LP/HX4K, iCE40LP/HX8K	Power-On-Reset ramp-down trip point (band gap based circuit monitoring VCC, VCCIO_2, VCC_SPI and VPP_2V5)	VCC	—	0.75	V
			VCCIO_2	—	1.29	V
			VCC_SPI	—	1.29	V
			VPP_2V5	—	1.33	V

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.

ESD Performance

Please refer to the iCE40 Product Family Qualification Summary for complete qualification data, including ESD performance.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1, 3, 4, 5, 6, 7]	Input or I/O Leakage	0V < V_{IN} < V_{CCIO} + 0.2 V	—	—	+/–10	µA
C_1[6, 7]	I/O Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = Typ., V_{IO} = 0 to V_{CCIO} + 0.2 V	—	6	—	pf
C_2[6, 7]	Global Input Buffer Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = Typ., V_{IO} = 0 to V_{CCIO} + 0.2 V	—	6	—	pf
V_{HYST}	Input Hysteresis	V_{CCIO} = 1.8 V, 2.5 V, 3.3 V	—	200	—	mV
I_{PU}[6, 7]	Internal PIO Pull-up Current	V_{CCIO} = 1.8 V, 0=<V_{IN}<=0.65 V_{CCIO}	–3	—	–31	µA
		V_{CCIO} = 2.5 V, 0=<V_{IN}<=0.65 V_{CCIO}	–8	—	–72	µA
		V_{CCIO} = 3.3 V, 0=<V_{IN}<=0.65 V_{CCIO}	–11	—	–128	µA

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Internal pull-up resistors are disabled.
2. T_J 25°C, f = 1.0 MHz.
3. Please refer to V_{IL} and V_{IH} in the sysIO Single-Ended DC Electrical Characteristics table of this document.
4. Only applies to IOs in the SPI bank following configuration.
5. Some products are clamped to a diode when V_{IN} is larger than V_{CCIO}.
6. High current IOs has three sysIO buffers connected together.
7. The iCE40LP640 and iCE40LP1K SWG16 package has CDONE and a sysIO buffer are connected together.

Static Supply Current – LP Devices[1, 2, 3, 4]

Symbol	Parameter	Device	Typ. V_{CC}[4]	Units
I_{CC}	Core Power Supply	iCE40LP384	21	µA
		iCE40LP640	100	µA
		iCE40LP1K	100	µA
		iCE40LP4K	250	µA
		iCE40LP8K	250	µA
I_{CCPLL}[5, 6]	PLL Power Supply	All devices	0.5	µA
I_{PP_2V5}	NVCM Power Supply	All devices	1.0	µA
I_{CCIO}, I_{CC_SPI}	Bank Power Supply[4] V_{CCIO} = 2.5 V	All devices	3.5	µA

1. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND, on-chip PLL is off. For more detail with your specific design, use the Power Calculator tool. Power specified with master SPI configuration mode. Other modes may be up to 25% higher.
2. Frequency = 0 MHz.
3. T_J = 25 °C, power supplies at nominal voltage.
4. Does not include pull-up.
5. No PLL available on the iCE40LP384 and iCE40LP640 device.
6. V_{CCPLL} is tied to V_{CC} internally in packages without PLLs pins.

Peak Startup Supply Current – HX Devices

Symbol	Parameter	Device	Max	Units
I_{CCPEAK}	Core Power Supply	iCE40HX1K	6.9	mA
		iCE40HX4K	22.3	mA
		iCE40HX8K	22.3	mA
$I_{CCPLLPEAK}$[1]	PLL Power Supply	iCE40HX1K	1.8	mA
		iCE40HX4K	6.4	mA
		iCE40HX8K	6.4	mA
$I_{PP\_2V5PEAK}$	NVCM Power Supply	iCE40HX1K	2.8	mA
		iCE40HX4K	4.1	mA
		iCE40HX8K	4.1	mA
$I_{CCIOPEAK}$, $I_{CC\_SPIPEAK}$	Bank Power Supply	iCE40HX1K	6.8	mA
		iCE40HX4K	6.8	mA
		iCE40HX8K	6.8	mA

1. V_{CCPLL} is tied to V_{CC} internally in packages without PLLs pins.

sysIO Recommended Operating Conditions

Standard	V_{CCIO} (V)		
	Min.	Typ.	Max.
LVCMOS 3.3	3.14	3.3	3.46
LVCMOS 2.5	2.37	2.5	2.62
LVCMOS 1.8	1.71	1.8	1.89
LVDS25E[1, 2]	2.37	2.5	2.62
subLVDSE[1, 2]	1.71	1.8	1.89

1. Inputs on-chip. Outputs are implemented with the addition of external resistors.
2. Does not apply to Configuration Bank V_{CC_SPI}.

sysIO Single-Ended DC Electrical Characteristics

Input/ Output Standard	V_{IL}		V_{IH}[1]		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} Max. (mA)	I_{OH} Max. (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3	–0.3	0.8	2.0	V_{CCIO} + 0.2 V	0.4	V_{CCIO} – 0.4	8, 16[2], 24[2]	–8, –16[2], –24[2]
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 2.5	–0.3	0.7	1.7	V_{CCIO} + 0.2 V	0.4	V_{CCIO} – 0.4	6, 12[2], 18[2]	–6, –12[2], –18[2]
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 1.8	–0.3	0.35V_{CCIO}	0.65V_{CCIO}	V_{CCIO} + 0.2 V	0.4	V_{CCIO} – 0.4	4, 8[2], 12[2]	–4, –8[2], –12[2]
					0.2	V_{CCIO} – 0.2	0.1	–0.1

1. Some products are clamped to a diode when V_{IN} is larger than V_{CCIO}.
2. Only for High Drive LED outputs.

LVDS25E Emulation

iCE40 devices can support LVDSE outputs via emulation on all banks. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all devices. The scheme shown in Figure 3-1 is one possible solution for LVDS25E standard implementation. Resistor values in Figure 3-1 are industry standard values for 1% resistors.

Figure 3-1. LVDS25E Using External Resistors

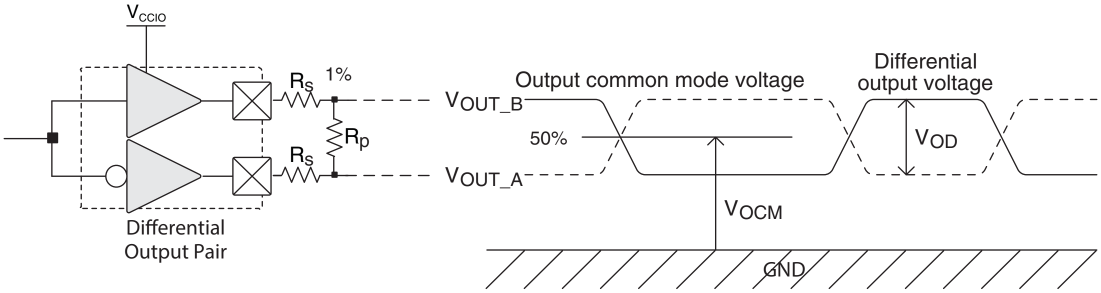


Table 3-1. LVDS25E DC Conditions

Over Recommended Operating Conditions

Parameter	Description	Typ.	Units
Z_{OUT}	Output impedance	20	Ohms
R_S	Driver series resistor	150	Ohms
R_P	Driver parallel resistor	140	Ohms
R_T	Receiver termination	100	Ohms
V_{OH}	Output high voltage	1.43	V
V_{OL}	Output low voltage	1.07	V
V_{OD}	Output differential voltage	0.30	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	100.5	Ohms
I_{DC}	DC output current	6.03	mA

Over Recommended Commercial Operating Conditions - HX Devices[1, 2, 3, 4, 5]

Buffer Type	Description	Timing	Units
Input Adjusters			
LVDS25	LVDS, V_{CCIO} = 2.5 V	0.13	ns
subLVDS	subLVDS, V_{CCIO} = 1.8 V	1.03	ns
LVCMOS33	LVCMOS, V_{CCIO} = 3.3 V	0.16	ns
LVCMOS25	LVCMOS, V_{CCIO} = 2.5 V	0.00	ns
LVCMOS18	LVCMOS, V_{CCIO} = 1.8 V	0.23	ns
Output Adjusters			
LVDS25E	LVDS, Emulated, V_{CCIO} = 2.5 V	0.00	ns
subLVDSE	subLVDS, Emulated, V_{CCIO} = 1.8 V	1.76	ns
LVCMOS33	LVCMOS, V_{CCIO} = 3.3 V	0.17	ns
LVCMOS25	LVCMOS, V_{CCIO} = 2.5 V	0.00	ns
LVCMOS18	LVCMOS, V_{CCIO} = 1.8 V	1.76	ns

1. Timing adders are relative to LVCMOS25 and characterized but not tested on every device.
2. LVCMOS timing measured with the load specified in Switching Test Condition table.
3. All other standards tested according to the appropriate specifications.
4. Commercial timing numbers are shown.
5. Not all I/O standards are supported for all banks. See the Architecture section of this data sheet for details.

iCE40 External Switching Characteristics – LP Devices [1, 2]

Over Recommended Operating Conditions

Parameter	Description	Device	Min.	Max.	Units
Clocks					
Global Clocks					
f_{MAX_GBUF}	Frequency for Global Buffer Clock network	All iCE40LP devices	—	275	MHz
t_{W_GBUF}	Clock Pulse Width for Global Buffer	All iCE40LP devices	0.92	—	ns
t_{SKEW_GBUF}	Global Buffer Clock Skew Within a Device	iCE40LP384	—	370	ps
		iCE40LP640	—	230	ps
		iCE40LP1K	—	230	ps
		iCE40LP4K	—	340	ps
		iCE40LP8K	—	340	ps
Pin-LUT-Pin Propagation Delay					
t_{PD}	Best case propagation delay through one LUT-4	All iCE40LP devices	—	9.36	ns
General I/O Pin Parameters (Using Global Buffer Clock without PLL)[3]					
t_{SKEW_IO}	Data bus skew across a bank of IOs	iCE40LP384	—	300	ps
		iCE40LP640	—	200	ps
		iCE40LP1K	—	200	ps
		iCE40LP4K	—	280	ps
		iCE40LP8K	—	280	ps
t_{CO}	Clock to Output - PIO Output Register	iCE40LP384	—	6.33	ns
		iCE40LP640	—	5.91	ns
		iCE40LP1K	—	5.91	ns
		iCE40LP4K	—	6.58	ns
		iCE40LP8K	—	6.58	ns
t_{SU}	Clock to Data Setup - PIO Input Register	iCE40LP384	–0.08	—	ns
		iCE40LP640	–0.33	—	ns
		iCE40LP1K	–0.33	—	ns
		iCE40LP4K	–0.63	—	ns
		iCE40LP8K	–0.63	—	ns
t_{H}	Clock to Data Hold - PIO Input Register	iCE40LP384	1.99	—	ns
		iCE40LP640	2.81	—	ns
		iCE40LP1K	2.81	—	ns
		iCE40LP4K	3.48	—	ns
		iCE40LP8K	3.48	—	ns
General I/O Pin Parameters (Using Global Buffer Clock with PLL)[3]					
t_{COPLL}	Clock to Output - PIO Output Register	iCE40LP1K	—	2.20	ns
		iCE40LP4K	—	2.30	ns
		iCE40LP8K	—	2.30	ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	iCE40LP1K	5.23	—	ns
		iCE40LP4K	6.13	—	ns
		iCE40LP8K	6.13	—	ns

iCE40 External Switching Characteristics – HX Devices [1, 2]

Over Recommended Operating Conditions

Parameter	Description	Device	Min.	Max.	Units
Clocks					
Primary Clocks					
f_{MAX_GBUF}	Frequency for Global Buffer Clock network	All iCE40HX devices	—	275	MHz
t_{W_GBUF}	Clock Pulse Width for Global Buffer	All iCE40HX devices	0.88	—	ns
t_{SKEW_GBUF}	Global Buffer Clock Skew Within a Device	iCE40HX1K	—	727	ps
		iCE40HX4K	—	300	ps
		iCE40HX8K	—	300	ps
Pin-LUT-Pin Propagation Delay					
t_{PD}	Best case propagation delay through one LUT-4	All iCE40 HX devices	—	7.30	ns
General I/O Pin Parameters (Using Global Buffer Clock without PLL)					
t_{SKEW_IO}	Data bus skew across a bank of IOs	iCE40HX1K	—	696	ps
		iCE40HX4K	—	290	ps
		iCE40HX8K	—	290	ps
t_{CO}	Clock to Output - PIO Output Register	iCE40HX1K	—	5.00	ns
		iCE40HX4K	—	5.41	ns
		iCE40HX8K	—	5.41	ns
t_{SU}	Clock to Data Setup - PIO Input Register	iCE40HX1K	–0.23	—	ns
		iCE40HX4K	–0.43	—	ns
		iCE40HX8K	–0.43	—	ns
t_H	Clock to Data Hold - PIO Input Register	iCE40HX1K	1.92	—	ns
		iCE40HX4K	2.38	—	ns
		iCE40HX8K	2.38	—	ns
General I/O Pin Parameters (Using Global Buffer Clock with PLL)[3]					
t_{COPLL}	Clock to Output - PIO Output Register	iCE40HX1K	—	2.96	ns
		iCE40HX4K	—	2.51	ns
		iCE40HX8K	—	2.51	ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	iCE40HX1K	3.10	—	ns
		iCE40HX4K	4.16	—	ns
		iCE40HX8K	4.16	—	ns
t_{HPLL}	Clock to Data Hold - PIO Input Register	iCE40HX1K	–0.60	—	ns
		iCE40HX4K	–0.53	—	ns
		iCE40HX8K	–0.53	—	ns

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the iCECube2 software.
2. General I/O timing numbers based on LVCMOS 2.5, 0pf load.
3. Supported on devices with a PLL.

sysCONFIG Port Timing Specifications[1]

Symbol	Parameter		Min.	Typ.	Max.	Units
All Configuration Modes						
t_{CRESET_B}	Minimum CRESET_B Low pulse width required to restart configuration, from falling edge to rising edge		200	—	—	ns
t_{DONE_IO}	Number of configuration clock cycles after CDONE goes High before the PIO pins are activated		49	—	—	Clock Cycles
Slave SPI						
t_{CR_SCK}	Minimum time from a rising edge on CRESET_B until the first SPI write operation, first SPI_SCK. During this time, the iCE40 device is clearing its internal configuration memory	iCE40LP384	600	-	—	us
		iCE40LP640, iCE40LP/HX1K	800	-	—	us
		iCE40LP/HX4K	1200	-	—	us
		iCE40LP/HX8K	1200	-	—	us
f_{MAX}[1]	CCLK clock frequency	Write	1	-	25	MHz
		Read iCE40LP384[2]	-	15	-	MHz
		Read iCE40LP640, iCE40LP/HX1K[2]	-	15	-	MHz
		Read iCE40LP/HX4K[2]	-	15	-	MHz
		Read iCE40LP/HX8K[2]	-	15	-	MHz
t_{CCLKH}	CCLK clock pulse width high		20	—	—	ns
t_{CCLKL}	CCLK clock pulse width low		20	—	—	ns
t_{STSU}	CCLK setup time		12		—	ns
t_{STH}	CCLK hold time		12	—	—	ns
t_{STCO}	CCLK falling edge to valid output		13	—	—	ns
Master SPI						
f_{MCLK}	MCLK clock frequency	Off	—	0	—	MHz
		Low Frequency (Default)	—	7.5	—	MHz
		Medium Frequency[3]	—	24	—	MHz
		High Frequency[3]	—	40	—	MHz

Switching Test Conditions

Figure 3-3 shows the output test load used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-3.

Figure 3-3. Output Test Load, LVCMOS Standards

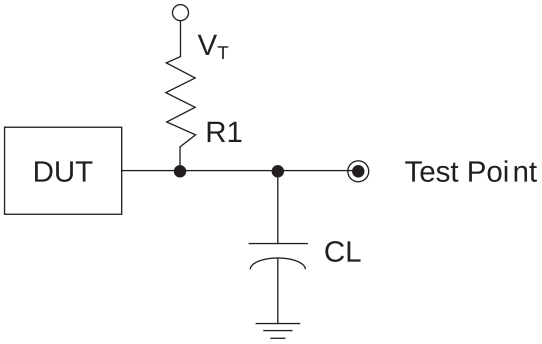


Table 3-3. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R_1	C_L	Timing Reference	V_T
LVCMOS settings (L -> H, H -> L)	∞	0 pF	LVCMOS 3.3 = 1.5 V	—
			LVCMOS 2.5 = $V_{CCIO}/2$	—
			LVCMOS 1.8 = $V_{CCIO}/2$	—
LVCMOS 3.3 (Z -> H)	188	0 pF	1.5	V_{OL}
LVCMOS 3.3 (Z -> L)			1.5	V_{OH}
Other LVCMOS (Z -> H)			$V_{CCIO}/2$	V_{OL}
Other LVCMOS (Z -> L)			$V_{CCIO}/2$	V_{OH}
LVCMOS (H -> Z)			V_{OH} - 0.15	V_{OL}
LVCMOS (L -> Z)			V_{OL} - 0.15	V_{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.

iCE40 LP/HX Family Data Sheet
Pinout Information

March 2017 **Data Sheet DS1040**

Signal Descriptions

Signal Name	I/O	Descriptions
General Purpose		
IO[Bank]_[Row/Column Number][A/B]	I/O	[Bank] indicates the bank of the device on which the pad is located. [Number] indicates IO number on the device.
IO[Bank]_[Row/Column Number][A/B]	I/O	[Bank] indicates the bank of the device on which the pad is located. [Number] indicates IO number on the device. [A/B] indicates the differential I/O. 'A' = negative input. 'B' = positive input.
HCIO[Bank]_[Number]	I/O	High Current IO. [Bank] indicates the bank of the device on which the pad is located. [Number] indicates IO number.
NC	—	No connect
GND	—	GND – Ground. Dedicated pins. It is recommended that all GNDs are tied together.
VCC	—	VCC – The power supply pins for core logic. Dedicated pins. It is recommended that all VCCs are tied to the same supply.
VCCIO_x	—	VCCIO – The power supply pins for I/O Bank x. Dedicated pins. All VCCIOs located in the same bank are tied to the same supply.
PLL and Global Functions (Used as user-programmable I/O pins when not used for PLL or clock pins)		
VCCPLLx	—	PLL VCC – Power. Dedicated pins. The PLL requires a separate power and ground that is quiet and stable to reduce the output clock jitter of the PLL.
GNDPLLx	—	PLL GND – Ground. Dedicated pins. The sysCLOCK PLL has the DC ground connection made on the FPGA, so the external PLL ground connection (GNDPLL) must NOT be connected to the board's ground.
GBINx	—	Global pads. Two per side.
Programming and Configuration		
CBSEL[0:1]	I/O	Dual function pins. I/Os when not used as CBSEL. Optional ColdBoot configuration SELect input, if ColdBoot mode is enabled.
CRESET_B	I	Configuration Reset, active Low. Dedicated input. No internal pull-up resistor. Either actively drive externally or connect a 10 KOhm pull-up resistor to VCCIO_2.
CDONE	I/O	Configuration Done. Includes a permanent weak pull-up resistor to VCCIO_2. If driving external devices with CDONE output, an external pull-up resistor to VCCIO_2 may be required. Refer to the TN1248, iCE40 Programming and Configuration for more details. Following device configuration the iCE40LP640 and iCE40LP1K in the SWG16 package CDONE pin can be used as a user output.
VCC_SPI	—	SPI interface voltage supply input. Must have a valid voltage even if configuring from NVCM.
SPI_SCK	I/O	Input Configuration Clock for configuring an FPGA in Slave SPI mode. Output Configuration Clock for configuring an FPGA configuration modes.
SPI_SS_B	I/O	SPI Slave Select. Active Low. Includes an internal weak pull-up resistor to VCC_SPI during configuration. During configuration, the logic level sampled on this pin determines the configuration mode used by the iCE40 device. An input when sampled at the start of configuration. An input when in SPI Peripheral configuration mode (SPI_SS_B = Low). An output when in Master SPI Flash configuration mode.
SPI_SI	I/O	Slave SPI serial data input and master SPI serial data output
SPI_SO	I/O	Slave SPI serial data output and master SPI serial data input

Pin Information Summary (Continued)

	iCE40LP4K			iCE40LP8K			iCE40HX1K		
	CM81	**CM121**	**CM225**	**CM81**	**CM121**	**CM225**	**VQ100**	**CB132**	**TQ144**
General Purpose I/O per Bank									
Bank 0	17	23	46	17	23	46	19	24	23
Bank 1	15	21	42	15	21	42	19	25	25
Bank 2	9	19	40	9	19	40	12	20	20
Bank 3	18	26	46	18	26	46	18	22	24
Configuration	4	4	4	4	4	4	4	4	4
Total General Purpose Single Ended I/O	63	93	178	63	93	178	72	95	96
High Current Outputs per Bank									
Bank 0	0	0	0	0	0	0	0	0	0
Bank 1	0	0	0	0	0	0	0	0	0
Bank 2	0	0	0	0	0	0	0	0	0
Bank 3	0	0	0	0	0	0	0	0	0
Total Differential Inputs	0	0	0	0	0	0	0	0	0
Differential Inputs per Bank									
Bank 0	0	0	0	0	0	0	0	0	0
Bank 1	0	0	0	0	0	0	0	0	0
Bank 2	0	0	0	0	0	0	0	0	0
Bank 3	9	13	23	9	13	23	9	11	12
Total Differential Inputs	9	13	23	9	13	23	9	11	12
Dedicated Inputs per Bank									
Bank 0	0	0	0	0	0	0	0	0	0
Bank 1	0	0	1	0	0	1	0	1	1
Bank 2	2	2	2	2	2	2	2	2	2
Bank 3	0	0	0	0	0	0	0	0	0
Configuration	0	0	0	0	0	0	0	0	0
Total Dedicated Inputs	2	2	3	2	2	3	2	3	3
Vccio Pins									
Bank 0	1	1	3	1	1	3	2	2	2
Bank 1	1	1	3	1	1	3	2	2	2
Bank 2	1	1	3	1	1	3	2	2	2
Bank 3	1	2	4	1	2	4	3	3	2
VCC	3	4	8	3	4	8	4	5	4
VCC_SPI	1	1	1	1	1	1	1	1	1
VPP_2V5	1	1	1	1	1	1	1	1	1
VPP_FAST[1]	1	1	1	1	1	1	1	1	1
VCCPLL	1	2	2	1	2	2	0	1	1
GND	5	12	18	5	12	18	10	14	10
NC	0	0	0	0	0	0	0	2	19
Total Count of Bonded Pins	81	121	225	81	121	225	100	132	144

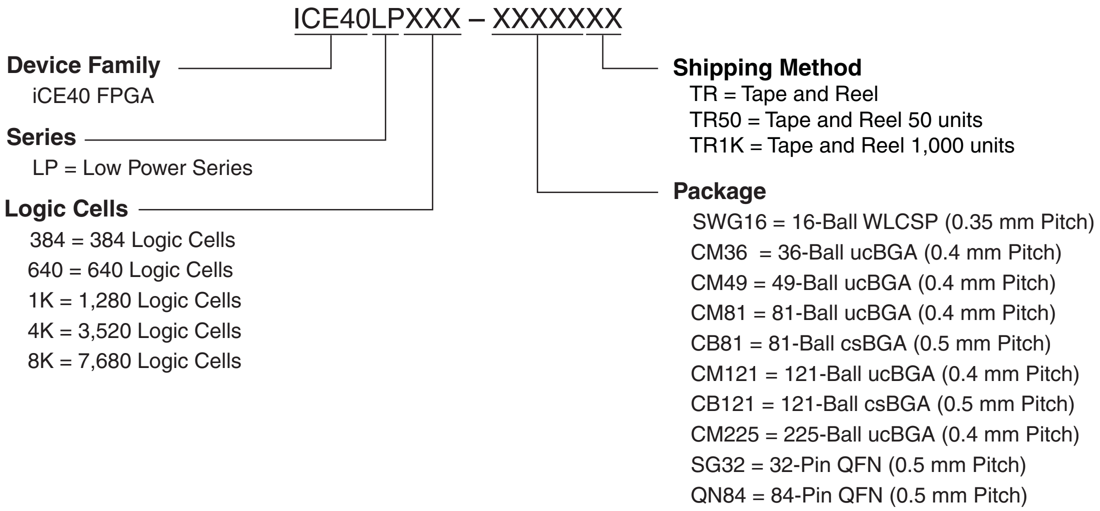
1. V_{PP_FAST}, used only for fast production programming, must be left floating or unconnected in applications.

iCE40 LP/HX Family Data Sheet
Ordering Information

March 2017 **Data Sheet DS1040**

iCE40 Part Number Description

Ultra Low Power (LP) Devices



ICE40LPXXX – XXXXXXX

Device Family
iCE40 FPGA

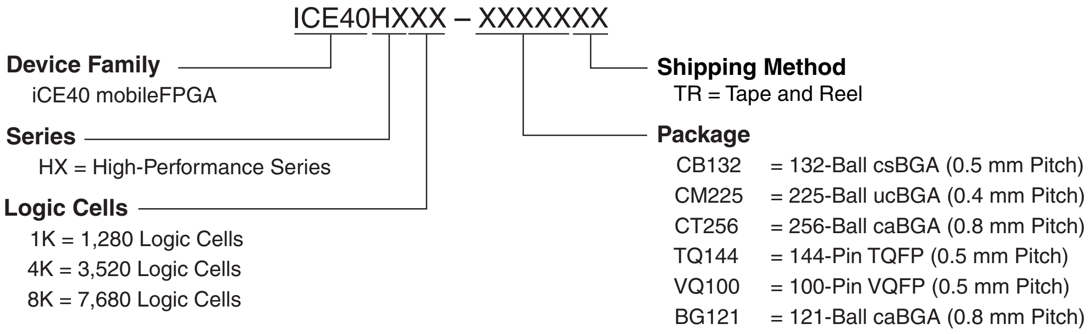
Series
LP = Low Power Series

Logic Cells
384 = 384 Logic Cells
640 = 640 Logic Cells
1K = 1,280 Logic Cells
4K = 3,520 Logic Cells
8K = 7,680 Logic Cells

Shipping Method
TR = Tape and Reel
TR50 = Tape and Reel 50 units
TR1K = Tape and Reel 1,000 units

Package
SWG16 = 16-Ball WLCSP (0.35 mm Pitch)
CM36 = 36-Ball ucBGA (0.4 mm Pitch)
CM49 = 49-Ball ucBGA (0.4 mm Pitch)
CM81 = 81-Ball ucBGA (0.4 mm Pitch)
CB81 = 81-Ball csBGA (0.5 mm Pitch)
CM121 = 121-Ball ucBGA (0.4 mm Pitch)
CB121 = 121-Ball csBGA (0.5 mm Pitch)
CM225 = 225-Ball ucBGA (0.4 mm Pitch)
SG32 = 32-Pin QFN (0.5 mm Pitch)
QN84 = 84-Pin QFN (0.5 mm Pitch)

High Performance (HX) Devices



ICE40HXXX – XXXXXXX

Device Family
iCE40 mobileFPGA

Series
HX = High-Performance Series

Logic Cells
1K = 1,280 Logic Cells
4K = 3,520 Logic Cells
8K = 7,680 Logic Cells

Shipping Method
TR = Tape and Reel

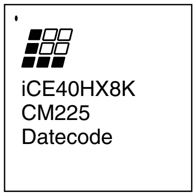
Package
CB132 = 132-Ball csBGA (0.5 mm Pitch)
CM225 = 225-Ball ucBGA (0.4 mm Pitch)
CT256 = 256-Ball caBGA (0.8 mm Pitch)
TQ144 = 144-Pin TQFP (0.5 mm Pitch)
VQ100 = 100-Pin VQFP (0.5 mm Pitch)
BG121 = 121-Ball caBGA (0.8 mm Pitch)

All parts shipped in trays unless noted.

Ordering Information

iCE40 devices have top-side markings as shown below:

Industrial



Note: Markings are abbreviated for small packages.

Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Package	Leads	Temp.
ICE40LP384-CM36	384	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP384-CM36TR	384	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP384-CM36TR1K	384	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP384-CM49	384	1.2 V	Halogen-Free ucBGA	49	IND
ICE40LP384-CM49TR	384	1.2 V	Halogen-Free ucBGA	49	IND
ICE40LP384-CM49TR1K	384	1.2 V	Halogen-Free ucBGA	49	IND
ICE40LP384-SG32	384	1.2 V	Halogen-Free QFN	32	IND
ICE40LP384-SG32TR	384	1.2 V	Halogen-Free QFN	32	IND
ICE40LP384-SG32TR1K	384	1.2 V	Halogen-Free QFN	32	IND
ICE40LP640-SWG16TR	640	1.2 V	Halogen-Free WLCSP	16	IND
ICE40LP640-SWG16TR50	640	1.2 V	Halogen-Free WLCSP	16	IND
ICE40LP640-SWG16TR1K	640	1.2 V	Halogen-Free WLCSP	16	IND
ICE40LP1K-SWG16TR	1280	1.2 V	Halogen-Free WLCSP	16	IND
ICE40LP1K-SWG16TR50	1280	1.2 V	Halogen-Free WLCSP	16	IND
ICE40LP1K-SWG16TR1K	1280	1.2 V	Halogen-Free WLCSP	16	IND
ICE40LP1K-CM36	1280	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP1K-CM36TR	1280	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP1K-CM36TR1K	1280	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP1K-CM49	1280	1.2 V	Halogen-Free ucBGA	49	IND
ICE40LP1K-CM49TR	1280	1.2 V	Halogen-Free ucBGA	49	IND
ICE40LP1K-CM49TR1K	1280	1.2 V	Halogen-Free ucBGA	49	IND
ICE40LP1K-CM81	1280	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP1K-CM81TR	1280	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP1K-CM81TR1K	1280	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP1K-CB81	1280	1.2 V	Halogen-Free csBGA	81	IND
ICE40LP1K-CB81TR	1280	1.2 V	Halogen-Free csBGA	81	IND
ICE40LP1K-CB81TR1K	1280	1.2 V	Halogen-Free csBGA	81	IND
ICE40LP1K-CM121	1280	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP1K-CM121TR	1280	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP1K-CM121TR1K	1280	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP1K-CB121	1280	1.2 V	Halogen-Free csBGA	121	IND
ICE40LP1K-QN84	1280	1.2 V	Halogen-Free QFN	84	IND
ICE40LP4K-CM81	3520	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP4K-CM81TR	3520	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP4K-CM81TR1K	3520	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP4K-CM121	3520	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP4K-CM121TR	3520	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP4K-CM121TR1K	3520	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP4K-CM225	3520	1.2 V	Halogen-Free ucBGA	225	IND
ICE40LP8K-CM81	7680	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP8K-CM81TR	7680	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP8K-CM81TR1K	7680	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP8K-CM121	7680	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP8K-CM121TR	7680	1.2 V	Halogen-Free ucBGA	121	IND

iCE40 LP/HX Family Data Sheet Revision History

March 2017 **Data Sheet DS1040**

Date	Version	Section	Change Summary
March 2017	3.3	Introduction	Updated Features section. Added 121-ball caBGA package for ICE40 HX4K/8K to Table 1-1, iCE40 Family Selection Guide.
		Architecture	Updated PLB Blocks section. Changed “subtracters” to “subtractors” in the Carry Logic description.
			Updated Clock/Control Distribution Network section. Switched the “Clock Enable“ and the “Reset” headings in Table 2-2, Global Buffer (GBUF) Connections to Programmable Logic Blocks.
		Pinout Information	Updated Pin Information Summary section. Added BG121information under iCE40HX4K and iCE40HX8K.
		Ordering Information	Updated iCE40 Part Number Description section. Added Shipping Method and BG121 package under High Performance (HX) Devices.
			Updated Ordering Information section. Added part numbers for BG121 under High-Performance Industrial Grade Devices, Halogen Free (RoHS) Packaging.
		Supplemental Information	Corrected reference to “Package Diagrams Data Sheet”.
October 2015	3.2	Introduction	Updated Features section. Added footnote to 16 WLCSP Programmable I/O: Max Inputs (LVDS25) in Table 1-1, iCE40 Family Selection Guide.
		DC and Switching Characteristics	Updated sysCLOCK PLL Timing section. Changed t_{DT} conditions.
			Updated Programming NVCM Supply Current – LP Devices section. Changed I_{PP_2V5} and I_{CCIO}, I_{CC_SPI} units.
March 2015	3.1	DC and Switching Characteristics	Updated sysIO Single-Ended DC Electrical Characteristics section. Changed LVCMOS 3.3 and LVCMOS 2. 5 V_{OH} Min. (V) from 0.5 to 0.4.
July 2014	3.0	DC and Switching Characteristics	Revised and/or added Typ. V_{CC} data in the following sections. — Static Supply Current – LP Devices — Static Supply Current – HX Devices — Programming NVCM Supply Current – LP Devices — Programming NVCM Supply Current – HX Devices In each section table, the footnote indicating Advanced device status was removed.
		Pinout Information	Updated Pin Information Summary section. Added footnote 1 to CM49 under iCE40LP1K.
April 2014	02.9	Ordering Information	Changed “i” to “I” in part number description and ordering part numbers.
			Added part numbers to the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging table.

Date	Version	Section	Change Summary
April 2013	02.2	Introduction	Added the LP8K 81 ucBGA.
		Architecture	Corrected typos.
		DC and Switching Characteristics	Corrected typos. Added 7:1 LVDS waveforms.
		Pinout Information	Corrected typos in signal descriptions. Added the LP8K 81 ucBGA.
		Ordering Information	Added the LP8K 81 ucBGA.
March 2013	02.1	DC and Switching Characteristics	Recommended operating conditions added requirement for Master SPI.
			Updated Recommended Operating Conditions for V_{PP_2V5}.
			Updated Power-On-Reset Voltage Levels and sequence requirements.
			Updated Static Supply Current conditions.
			Changed unit for t_{SKEW_IO} from ns to ps.
			Updated range of CCLK f_{MAX}.
		Ordering Information	Updated ordering information to include tape and reel part numbers.
September 2012	02.0	—	Merged SiliconBlue iCE40 LP and HX data sheets and updated to Lattice format.
	01.31	—	Updated Table 1.
	01.3	—	Production release.
			Updated notes on Table 3: Recommended Operating Conditions.
			Updated values in Table 4, Table 5, Table 12, Table 13 and Table 17.
	01.21	—	Updated Figure 3 and Figure 4 to specify iCE40.
Aug 2012	01.2	—	Updated company name.
July 2011	01.1	—	Moved package specifications to iCE40 pinout Excel files.
			Updated Table 1 maximum I/Os.
	01.01	—	Added 640, 1K and 4K to Table 13 configuration times. Updated Table 1 maximum I/Os.
	01.0	—	Initial release.