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## Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

### Details

Product Status	Active
Number of LABs/CLBs	48
Number of Logic Elements/Cells	384
Total RAM Bits	-
Number of I/O	37
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	49-VFBGA
Supplier Device Package	49-UCBGA (3x3)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/ice40lp384-cm49">https://www.e-xfl.com/product-detail/lattice-semiconductor/ice40lp384-cm49</a>

**Table 1-1. iCE40 Family Selection Guide (continued)**

84 QFN (7 mm x 7 mm, 0.5 mm)	QN84			67(7) <sup>1</sup>					
100 VQFP (14 mm x 14 mm, 0.5 mm)	VQ100						72(9) <sup>1</sup>		
121 ucBGA (5 mm x 5 mm, 0.4 mm)	CM121			95(12)	93(13)	93(13)			
121 csBGA (6 mm x 6 mm, 0.5 mm)	CB121			92(12)					
121 caBGA (9 mm x 9 mm, 0.8 mm)	BG121							93(13)	93(13)
132 csBGA (8 mm x 8 mm, 0.5 mm)	CB132						95(11)	95(12)	95(12)
144 TQFP (20 mm x 20 mm, 0.5 mm)	TQ144						96(12)	107(14)	
225 ucBGA (7 mm x 7 mm, 0.4 mm)	CM225				178(23)	178(23)			178(23)
256-ball caBGA (14 mm x 14 mm, 0.8 mm)	CT256								206(26)

1. No PLL available on the 16 WLCSP, 36 ucBGA, 81 csBGA, 84 QFN and 100 VQFP packages.

2. Only one PLL available on the 81 ucBGA package.

3. High Current I/Os only available on the 16 WLCSP package.

## Introduction

The iCE40 family of ultra-low power, non-volatile FPGAs has five devices with densities ranging from 384 to 7680 Look-Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic, these devices feature Embedded Block RAM (EBR), Non-volatile Configuration Memory (NVCM) and Phase Locked Loops (PLLs). These features allow the devices to be used in low-cost, high-volume consumer and system applications. Select packages offer High-Current drivers that are ideal to drive three white LEDs, or one RGB LED.

The iCE40 devices are fabricated on a 40 nm CMOS low power process. The device architecture has several features such as programmable low-swing differential I/Os and the ability to turn off on-chip PLLs dynamically. These features help manage static and dynamic power consumption, resulting in low static power for all members of the family. The iCE40 devices are available in two versions – ultra low power (LP) and high performance (HX) devices.

The iCE40 FPGAs are available in a broad range of advanced halogen-free packages ranging from the space saving 1.40x1.48 mm WLCSP to the PCB-friendly 20x20 mm TQFP. Table 1-1 shows the LUT densities, package and I/O options, along with other key parameters.

The iCE40 devices offer enhanced I/O features such as pull-up resistors. Pull-up features are controllable on a “per-pin” basis.

The iCE40 devices also provide flexible, reliable and secure configuration from on-chip NVCM. These devices can also configure themselves from external SPI Flash or be configured by an external master such as a CPU.

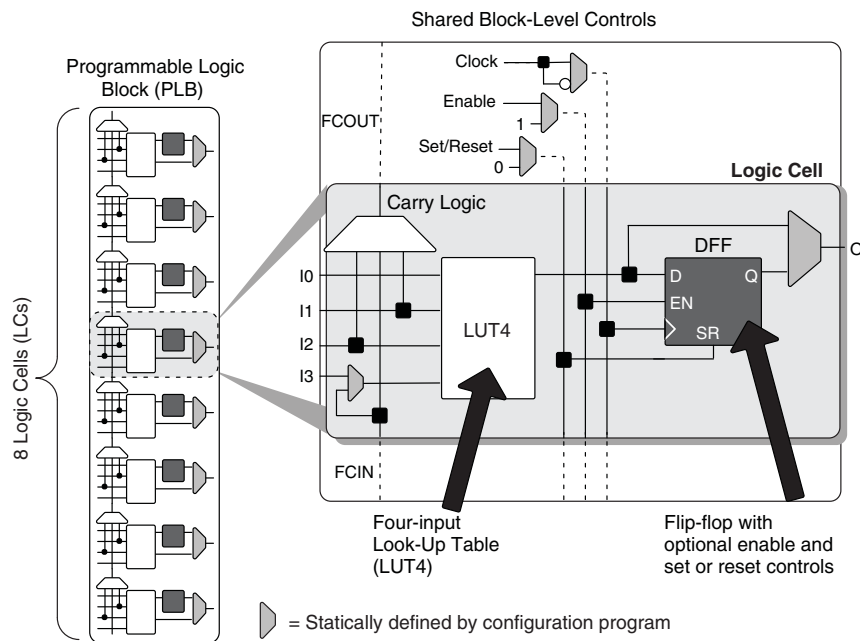
Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the iCE40 family of devices. Popular logic synthesis tools provide synthesis library support for iCE40. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the iCE40 device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules, including a number of reference designs, licensed free of charge, optimized for the iCE40 FPGA family. By using these configurable soft core IP cores as standardized blocks, users are free to concentrate on the unique aspects of their design, increasing their productivity.

### PLB Blocks

The core of the iCE40 device consists of Programmable Logic Blocks (PLB) which can be programmed to perform logic and arithmetic functions. Each PLB consists of eight interconnected Logic Cells (LC) as shown in Figure 2-2. Each LC contains one LUT and one register.

**Figure 2-2. PLB Block Diagram**



### Logic Cells

Each Logic Cell includes three primary logic elements shown in Figure 2-2.

- A four-input Look-Up Table (LUT4) builds any combinational logic function, of any complexity, requiring up to four inputs. Similarly, the LUT4 element behaves as a 16x1 Read-Only Memory (ROM). Combine and cascade multiple LUT4s to create wider logic functions.
- A 'D'-style Flip-Flop (DFF), with an optional clock-enable and reset control input, builds sequential logic functions. Each DFF also connects to a global reset signal that is automatically asserted immediately following device configuration.
- Carry Logic boosts the logic efficiency and performance of arithmetic functions, including adders, subtractors, comparators, binary counters and some wide, cascaded logic functions.

**Table 2-1. Logic Cell Signal Descriptions**

Function	Type	Signal Names	Description
Input	Data signal	I0, I1, I2, I3	Inputs to LUT4
Input	Control signal	Enable	Clock enable shared by all LCs in the PLB
Input	Control signal	Set/Reset <sup>1</sup>	Asynchronous or synchronous local set/reset shared by all LCs in the PLB.
Input	Control signal	Clock	Clock one of the eight Global Buffers, or from the general-purpose interconnects fabric shared by all LCs in the PLB
Input	Inter-PLB signal	FCIN	Fast carry in
Output	Data signals	O	LUT4 or registered output
Output	Inter-PFU signal	FCOUT	Fast carry out

1. If Set/Reset is not used, then the flip-flop is never set/reset, except when cleared immediately after configuration.

**Table 2-3. PLL Signal Descriptions**

Signal Name	Direction	Description
REFERENCECLK	Input	Input reference clock
BYPASS	Input	When FEEDBACK_PATH is set to SIMPLE, the BYPASS control selects which clock signal connects to the PLLOUT output. 0 = PLL generated signal 1 = REFERENCECLK
EXTFEEDBACK	Input	External feedback input to PLL. Enabled when the FEEDBACK_PATH attribute is set to EXTERNAL.
DYNAMICDELAY[3:0]	Input	Fine delay adjustment control inputs. Enabled when DELAY_ADJUSTMENT_MODE is set to DYNAMIC.
LATCHINPUTVALUE	Input	When enabled, forces the PLL into low-power mode; PLL output is held static at the last input clock value. Set ENABLE ICEGATE_PORTA and PORTB to '1' to enable.
PLLOUTGLOBAL	Output	Output from the Phase-Locked Loop (PLL). Drives a global clock network on the FPGA. The port has optimal connections to global clock buffers GBUF4 and GBUF5.
PLLOUTCORE	Output	Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTGLOBAL port.
LOCK	Output	When High, indicates that the PLL output is phase aligned or locked to the input reference clock.
RESET	Input	Active low reset.

## sysMEM Embedded Block RAM Memory

Larger iCE40 device includes multiple high-speed synchronous sysMEM Embedded Block RAMs (EBRs), each 4 kbit in size. This memory can be used for a wide variety of purposes including data buffering, and FIFO.

### sysMEM Memory Block

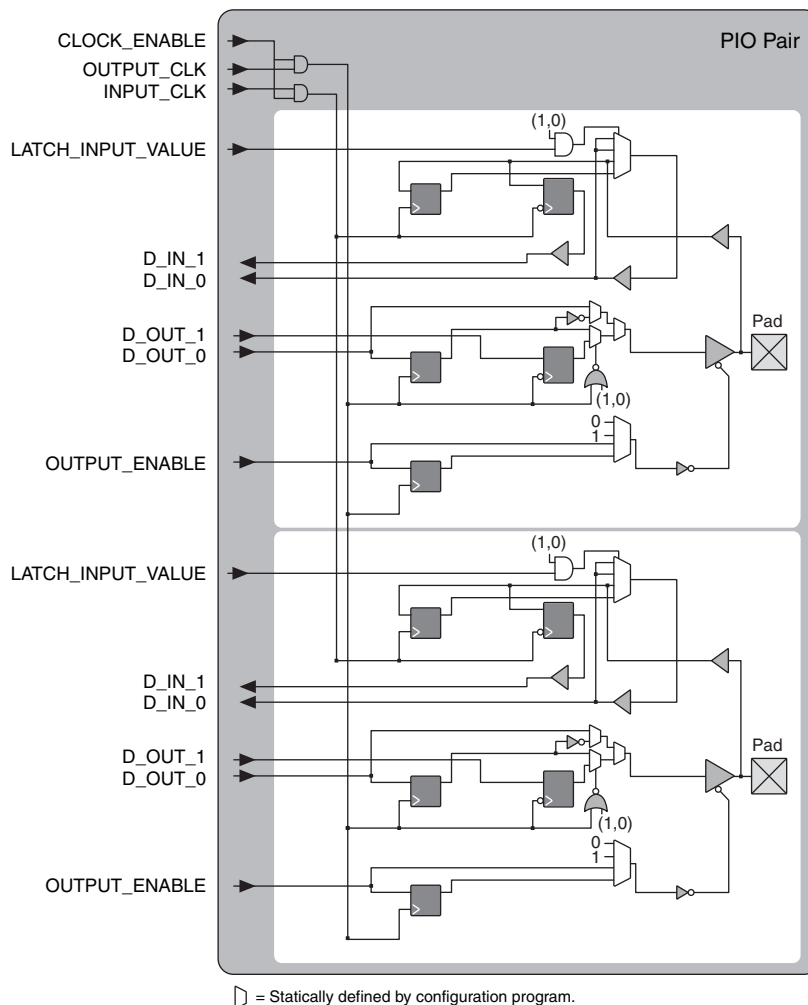
The sysMEM block can implement single port, pseudo dual port, or FIFO memories with programmable logic resources. Each block can be used in a variety of depths and widths as shown in Table 2-4.

**Table 2-4. sysMEM Block Configurations<sup>1</sup>**

Block RAM Configuration	Block RAM Configuration and Size	WADDR Port Size (Bits)	WDATA Port Size (Bits)	RADDR Port Size (Bits)	RDATA Port Size (Bits)	MASK Port Size (Bits)
SB_RAM256x16 SB_RAM256x16NR SB_RAM256x16NW SB_RAM256x16NRNW	256x16 (4K)	8 [7:0]	16 [15:0]	8 [7:0]	16 [15:0]	16 [15:0]
SB_RAM512x8 SB_RAM512x8NR SB_RAM512x8NW SB_RAM512x8NRNW	512x8 (4K)	9 [8:0]	8 [7:0]	9 [8:0]	8 [7:0]	No Mask Port
SB_RAM1024x4 SB_RAM1024x4NR SB_RAM1024x4NW SB_RAM1024x4NRNW	1024x4 (4K)	10 [9:0]	4 [3:0]	10 [9:0]	4 [3:0]	No Mask Port
SB_RAM2048x2 SB_RAM2048x2NR SB_RAM2048x2NW SB_RAM2048x2NRNW	2048x2 (4K)	11 [10:0]	2 [1:0]	11 [10:0]	2 [1:0]	No Mask Port

1. For iCE40 EBR primitives with a negative-edged Read or Write clock, the base primitive name is appended with a 'N' and a 'R' or 'W' depending on the clock that is affected.

**Figure 2-6. iCE I/O Register Block Diagram**



**Table 2-6. PIO Signal List**

Pin Name	I/O Type	Description
OUTPUT_CLK	Input	Output register clock
CLOCK_ENABLE	Input	Clock enable
INPUT_CLK	Input	Input register clock
OUTPUT_ENABLE	Input	Output enable
D_OUT_0/1	Input	Data from the core
D_IN_0/1	Output	Data to the core
LATCH_INPUT_VALUE	Input	Latches/holds the Input Value

## sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysIO buffers allow users to implement a wide variety of standards that are found in today's systems including LVCMOS and LVDS25.

High Current LED Drivers combine three sysIO buffers together. This allows for programmable drive strength. This also allows for high current drivers that are ideal to drive three white LEDs, or one RGB LED. Each bank is capable of supporting multiple I/O standards including single-ended LVCMOS buffers and differential LVDS25E output buf-

**Static Supply Current – HX Devices<sup>1, 2, 3, 4</sup>**

Symbol	Parameter	Device	Typ. $V_{CC}^4$	Units
$I_{CC}$	Core Power Supply	iCE40HX1K	296	$\mu A$
		iCE40HX4K	1140	$\mu A$
		iCE40HX8K	1140	$\mu A$
$I_{CCPLL}^5$	PLL Power Supply	All devices	0.5	$\mu A$
$I_{PP\_2V5}$	NVCM Power Supply	All devices	1.0	$\mu A$
$I_{CCIO}, I_{CC\_SPI}$	Bank Power Supply <sup>4</sup> $V_{CCIO} = 2.5 V$	All devices	3.5	$\mu A$

1. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at  $V_{CCIO}$  or GND, on-chip PLL is off. For more detail with your specific design, use the Power Calculator tool. Power specified with master SPI configuration mode. Other modes may be up to 25% higher.
2. Frequency = 0 MHz.
3.  $T_J = 25^\circ C$ , power supplies at nominal voltage.
4. Does not include pull-up.
5.  $V_{CCPLL}$  is tied to  $V_{CC}$  internally in packages without PLLs pins.

**Programming NVCM Supply Current – LP Devices<sup>1, 2, 3, 4</sup>**

Symbol	Parameter	Device	Typ. $V_{CC}^5$	Units
$I_{CC}$	Core Power Supply	iCE40LP384	60	$\mu A$
		iCE40LP640	120	$\mu A$
		iCE40LP1K	120	$\mu A$
		iCE40LP4K	350	$\mu A$
		iCE40LP8K	350	$\mu A$
$I_{CCPLL}^{6, 7}$	PLL Power Supply	All devices	0.5	$\mu A$
$I_{PP\_2V5}$	NVCM Power Supply	All devices	2.5	mA
$I_{CCIO}^8, I_{CC\_SPI}$	Bank Power Supply <sup>5</sup>	All devices	3.5	mA

1. Assumes all inputs are held at  $V_{CCIO}$  or GND and all outputs are tri-stated.
2. Typical user pattern.
3. SPI programming is at 8 MHz.
4.  $T_J = 25^\circ C$ , power supplies at nominal voltage.
5. Per bank.  $V_{CCIO} = 2.5 V$ . Does not include pull-up.
6. No PLL available on the iCE40-LP384 and iCE40-LP640 device.
7.  $V_{CCPLL}$  is tied to  $V_{CC}$  internally in packages without PLLs pins.
8.  $V_{PP\_FAST}$ , used only for fast production programming, must be left floating or unconnected in applications, except CM36 and CM49 packages MUST have the  $V_{PP\_FAST}$  ball connected to  $V_{CCIO\_0}$  ball externally.

### Programming NVCM Supply Current – HX Devices<sup>1, 2, 3, 4</sup>

Symbol	Parameter	Device	Typ. $V_{CC}^5$	Units
$I_{CC}$	Core Power Supply	iCE40HX1K	278	$\mu A$
		iCE40HX4K	1174	$\mu A$
		iCE40HX8K	1174	$\mu A$
$I_{CCPLL}^6$	PLL Power Supply	All devices	0.5	$\mu A$
$I_{PP\_2V5}$	NVCM Power Supply	All devices	2.5	mA
$I_{CCIO}^7, I_{CC\_SPI}$	Bank Power Supply <sup>5</sup>	All devices	3.5	mA

1. Assumes all inputs are held at  $V_{CCIO}$  or GND and all outputs are tri-stated.

2. Typical user pattern.

3. SPI programming is at 8 MHz.

4.  $T_J = 25^\circ C$ , power supplies at nominal voltage.

5. Per bank.  $V_{CCIO} = 2.5 V$ . Does not include pull-up.

6.  $V_{CCPLL}$  is tied to  $V_{CC}$  internally in packages without PLLs pins.

7.  $V_{PP\_FAST}$ , used only for fast production programming, must be left floating or unconnected in applications.

### Peak Startup Supply Current – LP Devices

Symbol	Parameter	Device	Max	Units
$I_{CCPEAK}$	Core Power Supply	iCE40LP384	7.7	mA
		iCELP640	6.4	mA
		iCE40LP1K	6.4	mA
		iCE40LP4K	15.7	mA
		iCE40LP8K	15.7	mA
$I_{CCPLLPEAK}^{1, 2, 4}$	PLL Power Supply	iCE40LP1K	1.5	mA
		iCELP640	1.5	mA
		iCE40LP4K	8.0	mA
		iCE40LP8K	8.0	mA
$I_{PP\_2V5PEAK}$	NVCM Power Supply	iCE40LP384	3.0	mA
		iCELP640	7.7	mA
		iCE40LP1K	7.7	mA
		iCE40LP4K	4.2	mA
		iCE40LP8K	4.2	mA
$I_{PP\_FASTPEAK}^3$	NVCM Programming Supply	iCE40LP384	5.7	mA
		iCELP640	8.1	mA
		iCE40LP1K	8.1	mA
$I_{CCIOPEAK}^5, I_{CC\_SPIPEAK}$	Bank Power Supply	iCE40LP384	8.4	mA
		iCELP640	3.3	mA
		iCE40LP1K	3.3	mA
		iCE40LP4K	8.2	mA
		iCE40LP8K	8.2	mA

1. No PLL available on the iCE40LP384 and iCE40LP640 device.

2.  $V_{CCPLL}$  is tied to  $V_{CC}$  internally in packages without PLLs pins.

3.  $V_{PP\_FAST}$ , used only for fast production programming, must be left floating or unconnected in applications, except CM36 and CM49 packages MUST have the  $V_{PP\_FAST}$  ball connected to  $V_{CCIO\_0}$  ball externally.

4. While no PLL is available in the iCE40-LP640 the  $I_{CCPLLPEAK}$  is additive to  $I_{CCPEAK}$ .

5. iCE40LP384 requires  $V_{CC}$  to be greater than 0.7 V when  $V_{CCIO}$  and  $V_{CC\_SPI}$  are above GND.

## sysIO Differential Electrical Characteristics

The LVDS25E/subLVDS differential output buffers are available on all banks but the LVDS/subLVDS input buffers are only available on Bank 3 of iCE40 devices.

### LVDS25

#### Over Recommended Operating Conditions

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
$V_{INP}, V_{INM}$	Input Voltage	$V_{CCIO}^1 = 2.5$	0	—	2.5	V
$V_{THD}$	Differential Input Threshold		250	350	450	mV
$V_{CM}$	Input Common Mode Voltage	$V_{CCIO}^1 = 2.5$	$(V_{CCIO}/2) - 0.3$	$V_{CCIO}/2$	$(V_{CCIO}/2) + 0.3$	V
$I_{IN}$	Input Current	Power on	—	—	$\pm 10$	$\mu A$

1. Typical.

### subLVDS

#### Over Recommended Operating Conditions

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
$V_{INP}, V_{INM}$	Input Voltage	$V_{CCIO}^1 = 1.8$	0	—	1.8	V
$V_{THD}$	Differential Input Threshold		100	150	200	mV
$V_{CM}$	Input Common Mode Voltage	$V_{CCIO}^1 = 1.8$	$(V_{CCIO}/2) - 0.25$	$V_{CCIO}/2$	$(V_{CCIO}/2) + 0.25$	V
$I_{IN}$	Input Current	Power on	—	—	$\pm 10$	$\mu A$

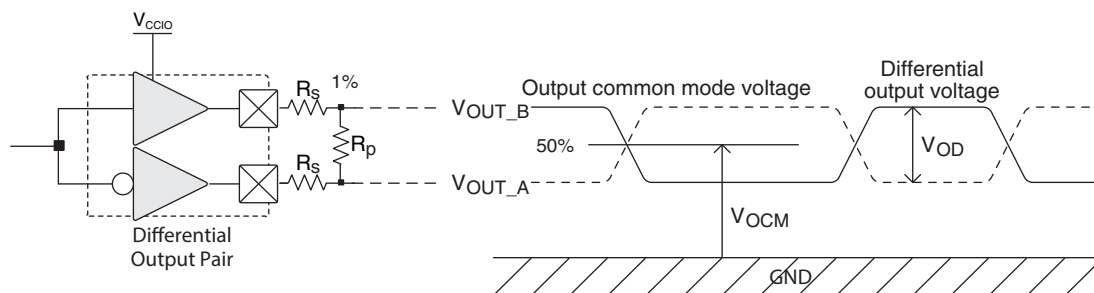
1. Typical.



### SubLVDS Emulation

The iCE40 family supports the differential subLVDS standard. The output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all banks of the devices. The subLVDS input standard is supported by the LVDS25 differential input buffer. The scheme shown in Figure 3-2 is one possible solution for subLVDS output standard implementation. Use LVDS25E mode with suggested resistors for subLVDS operation. Resistor values in Figure 3-2 are industry standard values for 1% resistors.

**Figure 3-2. subLVDS**



**Table 3-2. subLVDS DC Conditions**

#### Over Recommended Operating Conditions

Parameter	Description	Typ.	Units
$Z_{OUT}$	Output impedance	20	Ohms
$R_S$	Driver series resistor	270	Ohms
$R_P$	Driver parallel resistor	120	Ohms
$R_T$	Receiver termination	100	Ohms
$V_{OH}$	Output high voltage	1.43	V
$V_{OL}$	Output low voltage	1.07	V
$V_{OD}$	Output differential voltage	0.35	V
$V_{CM}$	Output common mode voltage	0.9	V
$Z_{BACK}$	Back impedance	100.5	Ohms
$I_{DC}$	DC output current	2.8	mA

## Typical Building Block Function Performance – LP Devices<sup>1, 2</sup>

### Pin-to-Pin Performance (LVCMOS25)

Function	Timing	Units
<b>Basic Functions</b>		
16-bit decoder	11.0	ns
4:1 MUX	12.0	ns
16:1 MUX	13.0	ns

### Register-to-Register Performance

Function	Timing	Units
<b>Basic Functions</b>		
16:1 MUX	190	MHz
16-bit adder	160	MHz
16-bit counter	175	MHz
64-bit counter	65	MHz
<b>Embedded Memory Functions</b>		
256x16 Pseudo-Dual Port RAM	240	MHz

1. The above timing numbers are generated using the iCECube2 design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.
2. Using a  $V_{CC}$  of 1.14 V at Junction Temp 85 °C.

## Typical Building Block Function Performance – HX Devices<sup>1, 2</sup>

### Pin-to-Pin Performance (LVCMOS25)

Function	Timing	Units
<b>Basic Functions</b>		
16-bit decoder	10.0	ns
4:1 MUX	9.0	ns
16:1 MUX	9.5	ns

### Register-to-Register Performance

Function	Timing	Units
<b>Basic Functions</b>		
16:1 MUX	305	MHz
16-bit adder	220	MHz
16-bit counter	255	MHz
64-bit counter	105	MHz
<b>Embedded Memory Functions</b>		
256x16 Pseudo-Dual Port RAM	403	MHz

1. The above timing numbers are generated using the iCECube2 design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.
2. Using a  $V_{CC}$  of 1.14 V at Junction Temp 85 °C.

### iCE40 External Switching Characteristics – LP Devices <sup>1, 2</sup>

#### Over Recommended Operating Conditions

Parameter	Description	Device	Min.	Max.	Units
Clocks					
Global Clocks					
t <sub>MAX_GBUF</sub>	Frequency for Global Buffer Clock network	All iCE40LP devices	—	275	MHz
t <sub>W_GBUF</sub>	Clock Pulse Width for Global Buffer	All iCE40LP devices	0.92	—	ns
t <sub>SKEW_GBUF</sub>	Global Buffer Clock Skew Within a Device	iCE40LP384	—	370	ps
		iCE40LP640	—	230	ps
		iCE40LP1K	—	230	ps
		iCE40LP4K	—	340	ps
		iCE40LP8K	—	340	ps
Pin-LUT-Pin Propagation Delay					
t <sub>PD</sub>	Best case propagation delay through one LUT-4	All iCE40LP devices	—	9.36	ns
General I/O Pin Parameters (Using Global Buffer Clock without PLL) <sup>3</sup>					
t <sub>SKEW_IO</sub>	Data bus skew across a bank of IOs	iCE40LP384	—	300	ps
		iCE40LP640	—	200	ps
		iCE40LP1K	—	200	ps
		iCE40LP4K	—	280	ps
		iCE40LP8K	—	280	ps
t <sub>CO</sub>	Clock to Output - PIO Output Register	iCE40LP384	—	6.33	ns
		iCE40LP640	—	5.91	ns
		iCE40LP1K	—	5.91	ns
		iCE40LP4K	—	6.58	ns
		iCE40LP8K	—	6.58	ns
t <sub>SU</sub>	Clock to Data Setup - PIO Input Register	iCE40LP384	−0.08	—	ns
		iCE40LP640	−0.33	—	ns
		iCE40LP1K	−0.33	—	ns
		iCE40LP4K	−0.63	—	ns
		iCE40LP8K	−0.63	—	ns
t <sub>H</sub>	Clock to Data Hold - PIO Input Register	iCE40LP384	1.99	—	ns
		iCE40LP640	2.81	—	ns
		iCE40LP1K	2.81	—	ns
		iCE40LP4K	3.48	—	ns
		iCE40LP8K	3.48	—	ns
General I/O Pin Parameters (Using Global Buffer Clock with PLL) <sup>3</sup>					
t <sub>COPLL</sub>	Clock to Output - PIO Output Register	iCE40LP1K	—	2.20	ns
		iCE40LP4K	—	2.30	ns
		iCE40LP8K	—	2.30	ns
t <sub>SUPLL</sub>	Clock to Data Setup - PIO Input Register	iCE40LP1K	5.23	—	ns
		iCE40LP4K	6.13	—	ns
		iCE40LP8K	6.13	—	ns

**iCE40 External Switching Characteristics – LP Devices (Continued)<sup>1, 2</sup>**
**Over Recommended Operating Conditions**

Parameter	Description	Device	Min.	Max.	Units
t <sub>HPLL</sub>	Clock to Data Hold - PIO Input Register	iCE40LP1K	–0.90	—	ns
		iCE40LP4K	–0.80	—	ns
		iCE40LP8K	–0.80	—	ns

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions can be extracted from the iCECube2 software.

2. General I/O timing numbers based on LVCMOS 2.5, 0pf load.

3. Supported on devices with a PLL.

**SPI Master or NVCM Configuration Time<sup>1, 2</sup>**

Symbol	Parameter	Conditions	Typ.	Units
$t_{\text{CONFIG}}$	POR/CRESET_B to Device I/O Active	iCE40LP384 - Low Frequency (Default)	25	ms
		iCE40LP384 - Medium Frequency	15	ms
		iCE40LP384 - High Frequency	11	ms
		iCE40LP640 - Low Frequency (Default)	53	ms
		iCE40LP640 - Medium Frequency	25	ms
		iCE40LP640 - High Frequency	13	ms
		iCE40LP/HX1K - Low Frequency (Default)	53	ms
		iCE40LP/HX1K - Medium Frequency	25	ms
		iCE40LP/HX1K - High Frequency	13	ms
		iCE40LP/HX4K - Low Frequency (Default)	230	ms
		iCE40LP/HX4K - Medium Frequency	110	ms
		iCE40LP/HX4K - High Frequency	70	ms
		iCE40LP/HX8K - Low Frequency (Default)	230	ms
		iCE40LP/HX8K - Medium Frequency	110	ms
		iCE40LP/HX8K - High Frequency	70	ms

1. Assumes sysMEM Block is initialized to an all zero pattern if they are used.

2. The NVCM download time is measured with a fast ramp rate starting from the maximum voltage of POR trip point.

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**Signal Descriptions (Continued)**

Signal Name	I/O	Descriptions
VPP_FAST	—	Optional fast NVCM programming supply. V <sub>PP_FAST</sub> , used only for fast production programming, must be left floating or unconnected in applications, except CM36 and CM49 packages MUST have the V <sub>PP_FAST</sub> ball connected to V <sub>CCIO_0</sub> ball externally.
VPP_2V5	—	VPP_2V5 NVCM programming and operating supply

### Pin Information Summary

	iCE40LP384			iCE40LP640	iCE40LP1K							
	SG32	CM36 <sup>2</sup>	CM49 <sup>2</sup>	SWG16	SWG16	CM36 <sup>1,2</sup>	CM49 <sup>1,2</sup>	CM81	CB81	QN84	CM121	CB121
<b>General Purpose I/O per Bank</b>												
Bank 0	6	4	10	3	3	4	10	17	17	17	24	24
Bank 1	5	7	7	0	0	7	7	15	16	17	25	21
Bank 2	0	4	4	1	1	4	4	11	8	11	18	19
Bank 3	6	6	12	2	2	6	10	16	17	18	24	24
Configuration	4	4	4	4	4	4	4	4	4	4	4	4
Total General Purpose Single Ended I/O	21	25	37	10	10	25	35	63	62	67	95	92
<b>High Current Outputs per Bank</b>												
Bank 0	0	0	0	3	3	0	0	0	0	0	0	0
Bank 1	0	0	0	0	0	0	0	0	0	0	0	0
Bank 2	0	0	0	0	0	0	0	0	0	0	0	0
Bank 3	0	0	0	0	0	0	0	0	0	0	0	0
Total Current Outputs	0	0	0	3	3	0	0	0	0	0	0	0
<b>Differential Inputs per Bank</b>												
Bank 0	0	0	0	0	0	0	0	0	0	0	0	0
Bank 1	0	0	0	0	0	0	0	0	0	0	0	0
Bank 2	0	0	0	0	0	0	0	0	0	0	0	0
Bank 3	3	3	6	1	1	3	5	8	9	7	12	12
Total Differential Inputs	3	3	6	1	1	3	5	8	9	7	12	12
<b>Dedicated Inputs per Bank</b>												
Bank 0	0	0	0	0	0	0	0	0	0	0	0	0
Bank 1	0	0	0	0	0	0	0	0	0	0	0	0
Bank 2	2	2	2	1	1	2	2	2	2	2	2	2
Bank 3	0	0	0	0	0	0	0	0	0	0	0	0
Configuration	0	0	0	0	0	0	0	0	0	0	0	0
Total Dedicated Inputs	2	2	2	1	1	2	2	2	2	2	2	2
<b>Vccio Pins</b>												
Bank 0	1	1	1	1	1	1	1	1	1	1	2	1
Bank 1	1	1	1	0	0	0	0	1	1	1	2	1
Bank 2	1	1	1	1	1	1	1	1	1	1	2	1
Bank 3	1	0	0	0	0	0	0	1	1	1	2	2
VCC	1	1	2	1	1	1	2	3	3	4	4	4
VCC_SPI	1	1	1	0	0	1	1	1	1	1	1	1
VPP_2V5	1	1	1	0	0	1	1	1	1	1	1	1
VPP_FAST <sup>3</sup>	0	0	0	0	0	1	1	1	0	1	1	1
VCCPLL	0	0	0	0	0	0	1	1	0	0	1	1
GND	2	3	3	2	2	3	4	5	8	4	8	11
NC	0	0	0	0	0	0	0	0	0	0	0	3
Total Count of Bonded Pins	32	36	49	16	16	36	49	81	81	84	121	121

1. V<sub>CCIO0</sub> and V<sub>CCIO1</sub> are connected together.
2. V<sub>CCIO2</sub> and V<sub>CCIO3</sub> are connected together.
3. V<sub>PP\_FAST</sub>: used only for fast production programming, must be left floating or unconnected in applications, except CM36 and CM49 packages MUST have the V<sub>PP\_FAST</sub> ball connected to V<sub>CCIO\_0</sub> ball externally.

### Pin Information Summary (Continued)

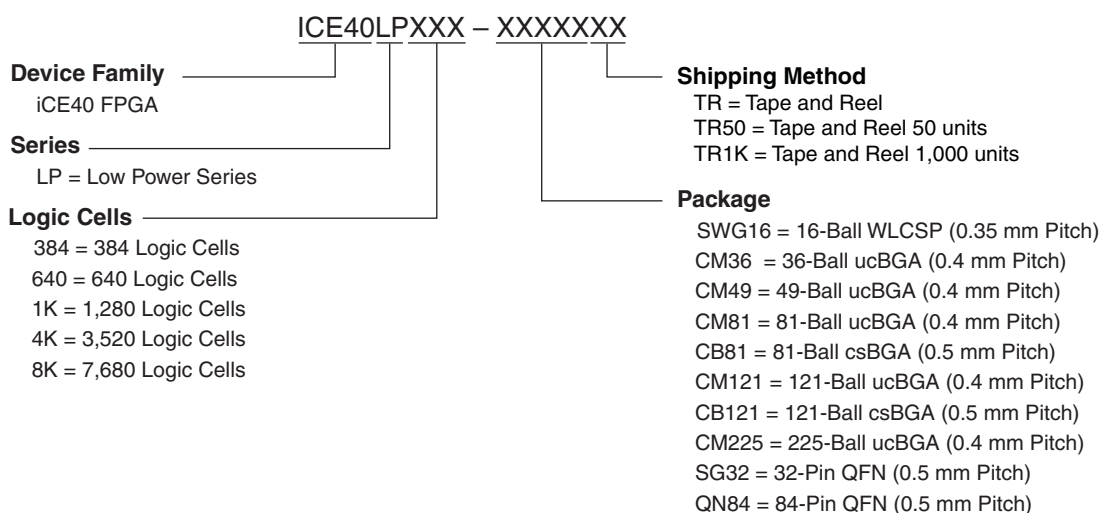
	iCE40LP4K			iCE40LP8K			iCE40HX1K		
	CM81	CM121	CM225	CM81	CM121	CM225	VQ100	CB132	TQ144
<b>General Purpose I/O per Bank</b>									
Bank 0	17	23	46	17	23	46	19	24	23
Bank 1	15	21	42	15	21	42	19	25	25
Bank 2	9	19	40	9	19	40	12	20	20
Bank 3	18	26	46	18	26	46	18	22	24
Configuration	4	4	4	4	4	4	4	4	4
Total General Purpose Single Ended I/O	63	93	178	63	93	178	72	95	96
<b>High Current Outputs per Bank</b>									
Bank 0	0	0	0	0	0	0	0	0	0
Bank 1	0	0	0	0	0	0	0	0	0
Bank 2	0	0	0	0	0	0	0	0	0
Bank 3	0	0	0	0	0	0	0	0	0
Total Differential Inputs	0	0	0	0	0	0	0	0	0
<b>Differential Inputs per Bank</b>									
Bank 0	0	0	0	0	0	0	0	0	0
Bank 1	0	0	0	0	0	0	0	0	0
Bank 2	0	0	0	0	0	0	0	0	0
Bank 3	9	13	23	9	13	23	9	11	12
Total Differential Inputs	9	13	23	9	13	23	9	11	12
<b>Dedicated Inputs per Bank</b>									
Bank 0	0	0	0	0	0	0	0	0	0
Bank 1	0	0	1	0	0	1	0	1	1
Bank 2	2	2	2	2	2	2	2	2	2
Bank 3	0	0	0	0	0	0	0	0	0
Configuration	0	0	0	0	0	0	0	0	0
Total Dedicated Inputs	2	2	3	2	2	3	2	3	3
<b>Vccio Pins</b>									
Bank 0	1	1	3	1	1	3	2	2	2
Bank 1	1	1	3	1	1	3	2	2	2
Bank 2	1	1	3	1	1	3	2	2	2
Bank 3	1	2	4	1	2	4	3	3	2
VCC	3	4	8	3	4	8	4	5	4
VCC_SPI	1	1	1	1	1	1	1	1	1
VPP_2V5	1	1	1	1	1	1	1	1	1
VPP_FAST <sup>1</sup>	1	1	1	1	1	1	1	1	1
VCCPLL	1	2	2	1	2	2	0	1	1
GND	5	12	18	5	12	18	10	14	10
NC	0	0	0	0	0	0	0	2	19
Total Count of Bonded Pins	81	121	225	81	121	225	100	132	144

1. VPP\_FAST<sup>1</sup> used only for fast production programming, must be left floating or unconnected in applications.

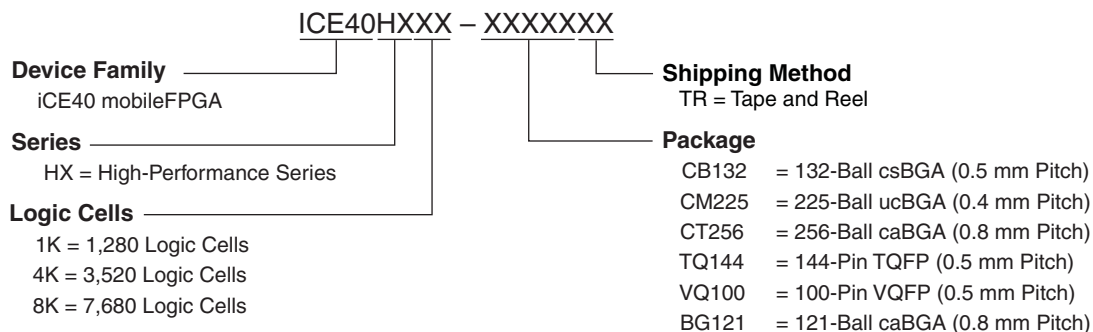


### iCE40 Part Number Description

#### Ultra Low Power (LP) Devices



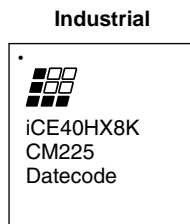
#### High Performance (HX) Devices



All parts shipped in trays unless noted.

### Ordering Information

iCE40 devices have top-side markings as shown below:



Note: Markings are abbreviated for small packages.

**Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging**

Part Number	LUTs	Supply Voltage	Package	Leads	Temp.
ICE40LP384-CM36	384	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP384-CM36TR	384	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP384-CM36TR1K	384	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP384-CM49	384	1.2 V	Halogen-Free ucBGA	49	IND
ICE40LP384-CM49TR	384	1.2 V	Halogen-Free ucBGA	49	IND
ICE40LP384-CM49TR1K	384	1.2 V	Halogen-Free ucBGA	49	IND
ICE40LP384-SG32	384	1.2 V	Halogen-Free QFN	32	IND
ICE40LP384-SG32TR	384	1.2 V	Halogen-Free QFN	32	IND
ICE40LP384-SG32TR1K	384	1.2 V	Halogen-Free QFN	32	IND
ICE40LP640-SWG16TR	640	1.2 V	Halogen-Free WLCSP	16	IND
ICE40LP640-SWG16TR50	640	1.2 V	Halogen-Free WLCSP	16	IND
ICE40LP640-SWG16TR1K	640	1.2 V	Halogen-Free WLCSP	16	IND
ICE40LP1K-SWG16TR	1280	1.2 V	Halogen-Free WLCSP	16	IND
ICE40LP1K-SWG16TR50	1280	1.2 V	Halogen-Free WLCSP	16	IND
ICE40LP1K-SWG16TR1K	1280	1.2 V	Halogen-Free WLCSP	16	IND
ICE40LP1K-CM36	1280	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP1K-CM36TR	1280	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP1K-CM36TR1K	1280	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP1K-CM49	1280	1.2 V	Halogen-Free ucBGA	49	IND
ICE40LP1K-CM49TR	1280	1.2 V	Halogen-Free ucBGA	49	IND
ICE40LP1K-CM49TR1K	1280	1.2 V	Halogen-Free ucBGA	49	IND
ICE40LP1K-CM81	1280	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP1K-CM81TR	1280	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP1K-CM81TR1K	1280	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP1K-CB81	1280	1.2 V	Halogen-Free csBGA	81	IND
ICE40LP1K-CB81TR	1280	1.2 V	Halogen-Free csBGA	81	IND
ICE40LP1K-CB81TR1K	1280	1.2 V	Halogen-Free csBGA	81	IND
ICE40LP1K-CM121	1280	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP1K-CM121TR	1280	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP1K-CM121TR1K	1280	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP1K-CB121	1280	1.2 V	Halogen-Free csBGA	121	IND
ICE40LP1K-QN84	1280	1.2 V	Halogen-Free QFN	84	IND
ICE40LP4K-CM81	3520	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP4K-CM81TR	3520	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP4K-CM81TR1K	3520	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP4K-CM121	3520	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP4K-CM121TR	3520	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP4K-CM121TR1K	3520	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP4K-CM225	3520	1.2 V	Halogen-Free ucBGA	225	IND
ICE40LP8K-CM81	7680	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP8K-CM81TR	7680	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP8K-CM81TR1K	7680	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP8K-CM121	7680	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP8K-CM121TR	7680	1.2 V	Halogen-Free ucBGA	121	IND

Part Number	LUTs	Supply Voltage	Package	Leads	Temp.
ICE40LP8K-CM121TR1K	7680	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP8K-CM225	7680	1.2 V	Halogen-Free ucBGA	225	IND

**High-Performance Industrial Grade Devices, Halogen Free (RoHS) Packaging**

Part Number	LUTs	Supply Voltage	Package	Leads	Temp.
ICE40HX1K-CB132	1280	1.2 V	Halogen-Free csBGA	132	IND
ICE40HX1K-VQ100	1280	1.2 V	Halogen-Free VQFP	100	IND
ICE40HX1K-TQ144	1280	1.2 V	Halogen-Free TQFP	144	IND
ICE40HX4K-BG121	3520	1.2 V	Halogen-Free caBGA	121	IND
ICE40HX4K-BG121TR	3520	1.2 V	Halogen-Free caBGA	121	IND
ICE40HX4K-CB132	3520	1.2 V	Halogen-Free csBGA	132	IND
ICE40HX4K-TQ144	3520	1.2 V	Halogen-Free TQFP	144	IND
ICE40HX8K-BG121	7680	1.2 V	Halogen-Free caBGA	121	IND
ICE40HX8K-BG121TR	7680	1.2 V	Halogen-Free caBGA	121	IND
ICE40HX8K-CB132	7680	1.2 V	Halogen-Free csBGA	132	IND
ICE40HX8K-CM225	7680	1.2 V	Halogen-Free ucBGA	225	IND
ICE40HX8K-CT256	7680	1.2 V	Halogen-Free caBGA	256	IND

Date	Version	Section	Change Summary
February 2014	02.8	Introduction	Updated Features section. — Corrected standby power units. — Included High Current LED Drivers
			Updated Table 1-1, iCE40 Family Selection Guide. — Removed LP384 Programmable I/O for 81 ucBGA package.
		Architecture	Updated Supported Standards section. Added information on High Current LED drivers.
		DC and Switching Characteristics	Corrected typos.
			Added footnote to the Peak Startup Supply Current – LP Devices table.
		Ordering Information	Updated part number description in the Ultra Low Power (LP) Devices section.
			Added part numbers to the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging table.
October 2013	02.7	Introduction	Updated Features list and iCE40 Family Selection Guide table.
		Architecture	Revised iCE40-1K device to iCE40LP/HX1K device.
		DC and Switching Characteristics	Added iCE40LP640 device information.
		Pinout Information	Added iCE40LP640 and iCE40LP1K information.
		Ordering Information	Added iCE40LP640 and iCE40LP1K information.
September 2013	02.6	DC and Switching Characteristics	Updated Absolute Maximum Ratings section.
			Updated sysCLOCK PLL Timing – Preliminary table.
		Pinout Information	Updated Pin Information Summary table.
August 2013	02.5	Introduction	Updated the iCE40 Family Selection Guide table.
		DC and Switching Characteristics	Updated the following tables: — Absolute Maximum Ratings — Power-On-Reset Voltage Levels — Static Supply Current – LP Devices — Static Supply Current – HX Devices — Programming NVCM Supply Current – LP Devices — Programming NVCM Supply Current – HX Devices — Peak Startup Supply Current – LP Devices — sysIO Recommended Operating Conditions — Typical Building Block Function Performance – HX Devices — iCE40 External Switching Characteristics – HX Devices — sysCLOCK PLL Timing – Preliminary — SPI Master or NVCM Configuration Time
		Pinout Information	Updated the Pin Information Summary table.
July 2013	02.4	Introduction	Updated the iCE40 Family Selection Guide table.
		DC and Switching Characteristics	Updated the sysCONFIG Port Timing Specifications table.
			Updated footnote in DC Electrical Characteristics table.
			GDDR tables removed. Support to be provided in a technical note.
		Pinout Information	Updated the Pin Information Summary table.
		Ordering Information	Updated the top-side markings figure.
			Updated the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging table.
May 2013	02.3	DC and Switching Characteristics	Added new data from Characterization.

Date	Version	Section	Change Summary
April 2013	02.2	Introduction	Added the LP8K 81 ucBGA.
		Architecture	Corrected typos.
		DC and Switching Characteristics	Corrected typos. Added 7:1 LVDS waveforms.
		Pinout Information	Corrected typos in signal descriptions. Added the LP8K 81 ucBGA.
		Ordering Information	Added the LP8K 81 ucBGA.
March 2013	02.1	DC and Switching Characteristics	Recommended operating conditions added requirement for Master SPI.
			Updated Recommended Operating Conditions for $V_{PP\_2V5}$ .
			Updated Power-On-Reset Voltage Levels and sequence requirements.
			Updated Static Supply Current conditions.
			Changed unit for $t_{SKEW\_IO}$ from ns to ps.
			Updated range of CCLK $f_{MAX}$ .
		Ordering Information	Updated ordering information to include tape and reel part numbers.
September 2012	02.0	—	Merged SiliconBlue iCE40 LP and HX data sheets and updated to Lattice format.
	01.31	—	Updated Table 1.
	01.3	—	Production release.
			Updated notes on Table 3: Recommended Operating Conditions.
			Updated values in Table 4, Table 5, Table 12, Table 13 and Table 17.
	01.21	—	Updated Figure 3 and Figure 4 to specify iCE40.
Aug 2012	01.2	—	Updated company name.
July 2011	01.1	—	Moved package specifications to iCE40 pinout Excel files.
			Updated Table 1 maximum I/Os.
	01.01	—	Added 640, 1K and 4K to Table 13 configuration times. Updated Table 1 maximum I/Os.
	01.0	—	Initial release.