# Lattice Semiconductor Corporation - ICE40LP4K-CM121TR1K Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 440 |
| Number of Logic Elements/Cells | 3520 |
| Total RAM Bits | 81920 |
| Number of I/O | 93 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 121-VFBGA |
| Supplier Device Package | 121-UCBGA (5x5) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/ice40lp4k-cm121tr1k |

# iCE40 LP/HX Family Data Sheet Introduction

March 2017 Data Sheet DS1040

## Features

- **Flexible Logic Architecture**
  - Five devices with 384 to 7,680 LUT4s and 10 to 206 I/Os
- **Ultra Low Power Devices**
  - Advanced 40 nm low power process
  - As low as 21 µA standby power
  - Programmable low swing differential I/Os
- **Embedded and Distributed Memory**
  - Up to 128 kbits sysMEM™ Embedded Block RAM
- **Pre-Engineered Source Synchronous I/O**
  - DDR registers in I/O cells
- **High Current LED Drivers**
  - Three High Current Drivers used for three different LEDs or one RGB LED
- **High Performance, Flexible I/O Buffer**
  - Programmable sysIO™ buffer supports wide range of interfaces:
    - LVCMOS 3.3/2.5/1.8
    - LVDS25E, subLVDS
    - Schmitt trigger inputs, to 200 mV typical hysteresis
  - Programmable pull-up mode
- **Flexible On-Chip Clocking**
  - Eight low-skew global clock resources
  - Up to two analog PLLs per device
- **Flexible Device Configuration**
  - SRAM is configured through:
    - Standard SPI Interface
    - Internal Nonvolatile Configuration Memory (NVCM)
- **Broad Range of Package Options**
  - WLCSP, QFN, VQFP, TQFP, ucBGA, caBGA, and csBGA package options
  - Small footprint package options
    - As small as 1.40 mm x 1.48 mm
  - Advanced halogen-free packaging

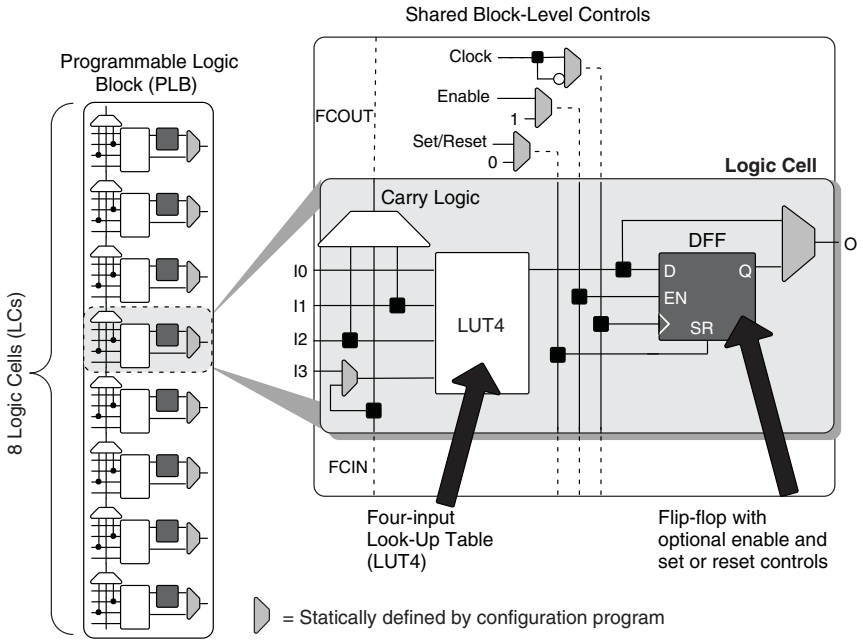
***Table 1-1. iCE40 Family Selection Guide***

| Part Number | | LP384 | LP640 | LP1K | LP4K | LP8K | HX1K | HX4K | HX8K |
|---|---|---|---|---|---|---|---|---|---|
| Logic Cells (LUT + Flip-Flop) | | 384 | 640 | 1,280 | 3,520 | 7,680 | 1,280 | 3,520 | 7,680 |
| RAM4K Memory Blocks | | 0 | 8 | 16 | 20 | 32 | 16 | 20 | 32 |
| RAM4K RAM bits | | 0 | 32K | 64K | 80K | 128K | 64K | 80K | 128K |
| Phase-Locked Loops (PLLs) | | 0 | 0 | 1[1] | 2[2] | 2[2] | 1[1] | 2 | 2 |
| Maximum Programmable I/O Pins | | 63 | 25 | 95 | 167 | 178 | 95 | 95 | 206 |
| Maximum Differential Input Pairs | | 8 | 3 | 12 | 20 | 23 | 11 | 12 | 26 |
| High Current LED Drivers | | 0 | 3 | 3 | 0 | 0 | 0 | 0 | 0 |
| **Package** | **Code** | **Programmable I/O: Max Inputs (LVDS25)** | | | | | | | |
| 16 WLCSP (1.40 mm x 1.48 mm, 0.35 mm) | SWG16 | | 10(0)[1] | 10(0)[1] | | | | | |
| 32 QFN (5 mm x 5 mm, 0.5 mm) | SG32 | 21(3) | | | | | | | |
| 36 ucBGA (2.5 mm x 2.5 mm, 0.4 mm) | CM36 | 25(3) | | 25(3)[1] | | | | | |
| 49 ucBGA (3 mm x 3 mm, 0.4 mm) | CM49 | 37(6) | | 35(5)[1] | | | | | |
| 81 ucBGA (4 mm x 4 mm, 0.4 mm) | CM81 | | | 63(8) | 63(9)[2] | 63(9)[2] | | | |
| 81 csBGA (5 mm x 5 mm, 0.5 mm) | CB81 | | | 62(9)[1] | | | | | |

## PLB Blocks

The core of the iCE40 device consists of Programmable Logic Blocks (PLB) which can be programmed to perform logic and arithmetic functions. Each PLB consists of eight interconnected Logic Cells (LC) as shown in Figure 2-2. Each LC contains one LUT and one register.

***Figure 2-2. PLB Block Diagram***




### Logic Cells

Each Logic Cell includes three primary logic elements shown in Figure 2-2.

- A four-input Look-Up Table (LUT4) builds any combinational logic function, of any complexity, requiring up to four inputs. Similarly, the LUT4 element behaves as a 16x1 Read-Only Memory (ROM). Combine and cascade multiple LUT4s to create wider logic functions.
- A 'D'-style Flip-Flop (DFF), with an optional clock-enable and reset control input, builds sequential logic functions. Each DFF also connects to a global reset signal that is automatically asserted immediately following device configuration.
- Carry Logic boosts the logic efficiency and performance of arithmetic functions, including adders, subtractors, comparators, binary counters and some wide, cascaded logic functions.

***Table 2-1. Logic Cell Signal Descriptions***

| Function | Type | Signal Names | Description |
|---|---|---|---|
| Input | Data signal | I0, I1, I2, I3 | Inputs to LUT4 |
| Input | Control signal | Enable | Clock enable shared by all LCs in the PLB |
| Input | Control signal | Set/Reset[1] | Asynchronous or synchronous local set/reset shared by all LCs in the PLB. |
| Input | Control signal | Clock | Clock one of the eight Global Buffers, or from the general-purpose interconnects fabric shared by all LCs in the PLB |
| Input | Inter-PLB signal | FCIN | Fast carry in |
| Output | Data signals | O | LUT4 or registered output |
| Output | Inter-PFU signal | FCOUT | Fast carry out |

1. If Set/Reset is not used, then the flip-flop is never set/reset, except when cleared immediately after configuration.

### Global Reset Control

The global reset control signal connects to all PLB and PIO flip-flops on the iCE40 device. The global reset signal is automatically asserted throughout the configuration process, forcing all flip-flops to their defined wake-up state. For PLB flip-flops, the wake-up state is always reset, regardless of the PLB flip-flop primitive used in the application.

## sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The iCE40 devices have one or more sysCLOCK PLLs. REFERENCECLK is the reference frequency input to the PLL and its source can come from an external I/O pin or from internal routing. EXTFEEDBACK is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The PLLOUT output has an output divider, thus allowing the PLL to generate different frequencies for each output. The output divider can have a value from 1 to 6. The PLLOUT outputs can all be used to drive the iCE40 global clock network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 2-3.

The timing of the device registers can be optimized by programming a phase shift into the PLLOUT output clock which will advance or delay the output clock with reference to the REFERENCECLK clock. This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the $t_{LOCK}$ parameter has been satisfied.

For more details on the PLL, see TN1251, iCE40 sysCLOCK PLL Design and Usage Guide.

***Figure 2-3. PLL Diagram***

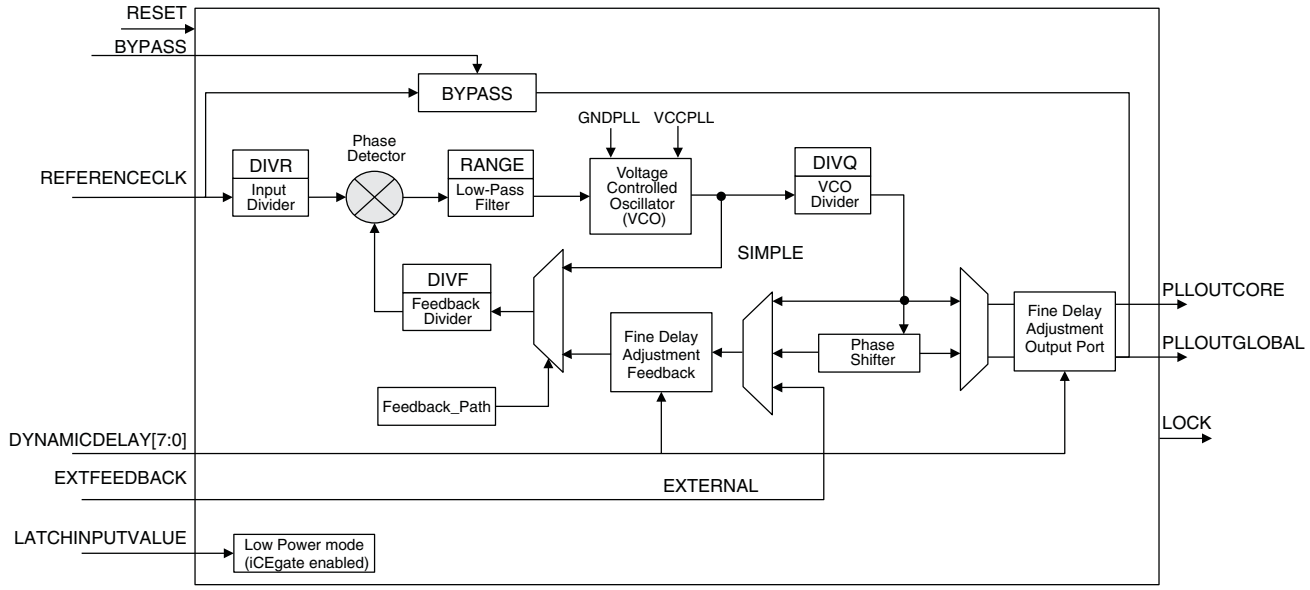



Table 2-3 provides signal descriptions of the PLL block.

## sysIO

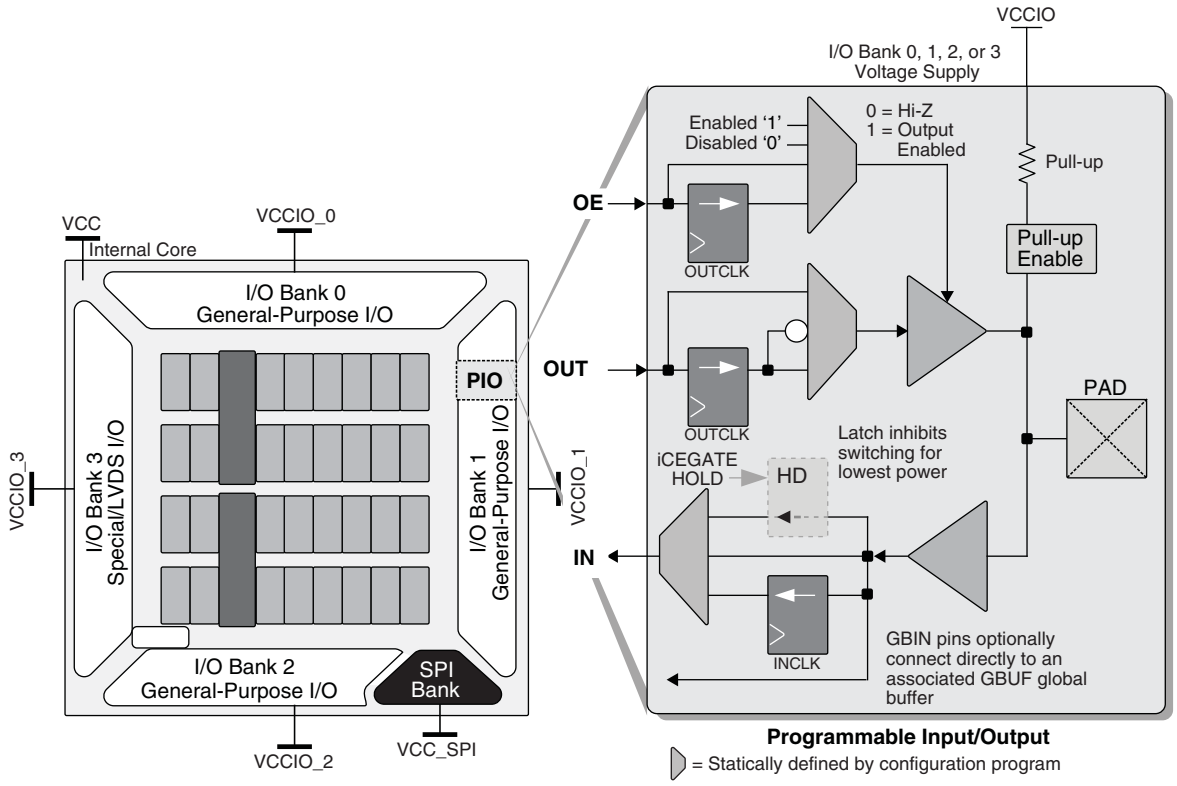
### Buffer Banks

iCE40 devices have up to four I/O banks with independent $V_{CCIO}$ rails with an additional configuration bank $V_{CC\_SPI}$ for the SPI I/Os.

### Programmable I/O (PIO)

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysIO buffers and pads. The PIOs are placed on all four sides of the device.

***Figure 2-5. I/O Bank and Programmable I/O Cell***




The PIO contains three blocks: an input register block, output register block iCEgate™ and tri-state register block. To save power, the optional iCEgate™ latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Note that the freeze signal is common to the bank. These blocks can operate in a variety of modes along with the necessary clock and selection logic.

### Input Register Block

The input register blocks for the PIOs on all edges contain registers that can be used to condition high-speed interface signals before they are passed to the device core. In Generic DDR mode, two registers are used to sample the data on the positive and negative edges of the system clock signal, creating two data streams.

### Output Register Block

The output register block can optionally register signals from the core of the device before they are passed to the sysIO buffers. In Generic DDR mode, two registers are used to capture the data on the positive and negative edge of the system clock and then muxed creating one data stream.

Figure 2-6 shows the input/output register block for the PIOs.

*Figure 2-6. iCE I/O Register Block Diagram*

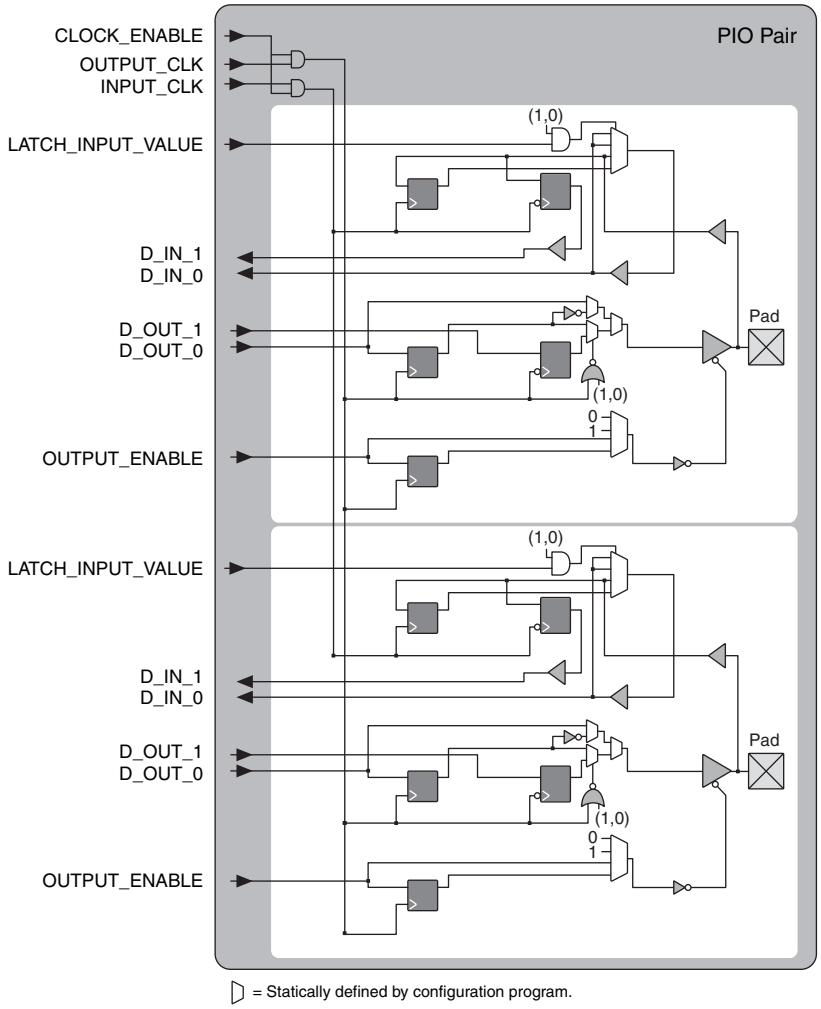



*Table 2-6. PIO Signal List*

| Pin Name | I/O Type | Description |
|---|---|---|
| OUTPUT_CLK | Input | Output register clock |
| CLOCK_ENABLE | Input | Clock enable |
| INPUT_CLK | Input | Input register clock |
| OUTPUT_ENABLE | Input | Output enable |
| D_OUT_0/1 | Input | Data from the core |
| D_IN_0/1 | Output | Data to the core |
| LATCH_INPUT_VALUE | Input | Latches/holds the Input Value |

## sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysIO buffers allow users to implement a wide variety of standards that are found in today's systems including LVCMOS and LVDS25.

High Current LED Drivers combine three sysIO buffers together. This allows for programmable drive strength. This also allows for high current drivers that are ideal to drive three white LEDs, or one RGB LED. Each bank is capable of supporting multiple I/O standards including single-ended LVCMOS buffers and differential LVDS25E output buf-

fers. Bank 3 additionally supports differential LVDS25 input buffers. Each sysIO bank has its own dedicated power supply.

**Typical I/O Behavior During Power-up**

The internal power-on-reset (POR) signal is deactivated when $V_{CC}$, $V_{CCIO\_2}$, $V_{PP\_2V5}$, and $V_{CC\_SPI}$ have reached the level defined in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all $V_{CCIO}$ banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. The default configuration of the I/O pins in a device prior to configuration is tri-stated with a weak pull-up to $V_{CCIO}$. The I/O pins will maintain the pre-configuration state until $V_{CC}$ and $V_{CCIO}$ (for I/O banks containing configuration I/Os) have reached levels, at which time the I/Os will take on the software user-configured settings only after a proper download/configuration. Unused IOs are automatically blocked and the pullup termination is disabled.

**Supported Standards**

The iCE40 sysIO buffer supports both single-ended and differential input standards. The single-ended standard supported is LVCMOS. The buffer supports the LVCMOS 1.8, 2.5, and 3.3 V standards. The buffer has individually configurable options for bus maintenance (weak pull-up or none). The High Current output buffer have individually configurable options for drive strength.

Table 2-7 and Table 2-8 show the I/O standards (together with their supply and reference voltages) supported by the iCE40 devices.

***Table 2-7. Supported Input Standards***

| Input Standard | $V_{CCIO}$ (Typical) | | |
|---|---|---|---|
| | 3.3 V | 2.5 V | 1.8 V |
| **Single-Ended Interfaces** | | | |
| LVCMOS33 | Yes | | |
| LVCMOS25 | | Yes | |
| LVCMOS18 | | | Yes |
| **Differential Interfaces** | | | |
| LVDS25[1] | | Yes | |
| subLVDS[1] | | | Yes |

1. Bank 3 only.

***Table 2-8. Supported Output Standards***

| Output Standard | $V_{CCIO}$ (Typical) |
|---|---|
| **Single-Ended Interfaces** | |
| LVCMOS33 | 3.3 |
| LVCMOS25 | 2.5 |
| LVCMOS18 | 1.8 |
| **Differential Interfaces** | |
| LVDS25E[1] | 2.5 |
| subLVDSE[1] | 1.8 |

1. These interfaces can be emulated with external resistors in all devices.

## Non-Volatile Configuration Memory

All iCE40 devices provide a Non-Volatile Configuration Memory (NVCM) block which can be used to configure the device.

For more information on the NVCM, please refer to TN1248, iCE40 Programming and Configuration Usage Guide.

# iCE40 LP/HX Family Data Sheet DC and Switching Characteristics

October 2015 Data Sheet DS1040

## Absolute Maximum Ratings[1, 2, 3, 4]

| | iCE40 LP/HX |
|---|---|
| Supply Voltage $V_{CC}$ | –0.5 V to 1.42 V |
| Output Supply Voltage $V_{CCIO}$, $V_{CC\_SPI}$ | –0.5 V to 3.60 V |
| NVCM Supply Voltage $V_{PP\_2V5}$ | –0.5 V to 3.60 V |
| PLL Supply Voltage $V_{CCPLL}$ | –0.5 V to 1.30 V |
| I/O Tri-state Voltage Applied | –0.5 V to 3.60 V |
| Dedicated Input Voltage Applied | –0.5 V to 3.60 V |
| Storage Temperature (Ambient) | –65 °C to 150 °C |
| Junction Temperature ($T_J$) | –55 °C to 125 °C |

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. IOs can support a 200 mV Overshoot above the Recommend Operating Conditions $V_{CCIO}$ (Max) and -200mV Undershoot below $V_{IL}$ (Min). Overshoot and Undershoot is permitted for 25% duty cycle but must not exceed 1.6 ns.

## Recommended Operating Conditions[1]

| Symbol | Parameter | | Min. | Max. | Units |
|---|---|---|---|---|---|
| $V_{CC}$[1] | Core Supply Voltage | | 1.14 | 1.26 | V |
| $V_{PP\_2V5}$ | $V_{PP\_2V5}$ NVCM Programming and Operating Supply Voltage | Slave SPI Configuration | 1.71 | 3.46 | V |
| | | Master SPI Configuration | 2.30 | 3.46 | V |
| | | Configure from NVCM | 2.30 | 3.46 | V |
| | | NVCM Programming | 2.30 | 3.00 | V |
| $V_{PP\_FAST}$[4] | Optional fast NVCM programming supply. Leave unconnected. | | N/A | N/A | V |
| $V_{CCPLL}$[5, 6] | PLL Supply Voltage | | 1.14 | 1.26 | V |
| $V_{CCIO}$[1, 2, 3] | I/O Driver Supply Voltage | $V_{CCIO0-3}$ | 1.71 | 3.46 | V |
| | | $V_{CC\_SPI}$ | 1.71 | 3.46 | V |
| $t_{JIND}$ | Junction Temperature Industrial Operation | | –40 | 100 | °C |
| $t_{PROG}$ | Junction Temperature NVCM Programming | | 10 | 30 | °C |

1. Like power supplies must be tied together. For example, if $V_{CCIO}$ and $V_{CC\_SPI}$ are both the same voltage, they must also be the same supply.
2. See recommended voltages by I/O standard in subsequent table.
3. $V_{CCIO}$ pins of unused I/O banks should be connected to the $V_{CC}$ power supply on boards.
4. $V_{PP\_FAST}$, used only for fast production programming, must be left floating or unconnected in applications, except CM36 and CM49 packages MUST have the $V_{PP\_FAST}$ ball connected to $V_{CCIO\_0}$ ball externally.
5. No PLL available on the iCE40LP384 and iCE40LP640 device.
6. $V_{CCPLL}$ is tied to $V_{CC}$ internally in packages without PLLs pins.

## Power Supply Ramp Rates[1, 2]

| Symbol | Parameter | | Min. | Max. | Units |
|---|---|---|---|---|---|
| $t_{RAMP}$ | Power supply ramp rates for all power supplies. | All configuration modes. No power supply sequencing. | 0.40 | 10 | V/ms |
| | | Configuring from Slave SPI. No power supply sequencing, | 0.01 | 10 | V/ms |
| | | Configuring from NVCM. $V_{CC}$ and $V_{PP\_2V5}$ to be powered 0.25 ms before $V_{CC\_SPI}$. | 0.01 | 10 | V/ms |
| | | Configuring from MSPI. $V_{CC}$ and $V_{PP\_SPI}$ to be powered 0.25 ms before $V_{PP\_2V5}$. | 0.01 | 10 | V/ms |

1. Assumes monotonic ramp rates.
2. iCE40LP384 requires $V_{CC}$ to be greater than 0.7V when $V_{CCIO}$ and $V_{CC\_SPI}$ are above GND.

## Power-On-Reset Voltage Levels[1]

| Symbol | Device | Parameter | | Min. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{PORUP}$ | iCE40LP384 | Power-On-Reset ramp-up trip point (band gap based circuit monitoring VCC, VCCIO_2, VCC_SPI and VPP_2V5) | VCC | 0.67 | 0.99 | V |
| | | | VCCIO_2 | 0.70 | 1.59 | V |
| | | | VCC_SPI | 0.70 | 1.59 | V |
| | | | VPP_2V5 | 0.70 | 1.59 | V |
| | iCE40LP640, iCE40LP/HX1K, iCE40LP/HX4K, iCE40LP/HX8K | Power-On-Reset ramp-up trip point (band gap based circuit monitoring VCC, VCCIO_2, VCC_SPI and VPP_2V5) | VCC | 0.55 | 0.75 | V |
| | | | VCCIO_2 | 0.86 | 1.29 | V |
| | | | VCC_SPI | 0.86 | 1.29 | V |
| | | | VPP_2V5 | 0.86 | 1.33 | V |
| $V_{PORDN}$ | iCE40LP384 | Power-On-Reset ramp-down trip point (band gap based circuit monitoring VCC, VCCIO_2, VCC_SPI and VPP_2V5) | VCC | — | 0.64 | V |
| | | | VCCIO_2 | — | 1.59 | V |
| | | | VCC_SPI | — | 1.59 | V |
| | | | VPP_2V5 | — | 1.59 | V |
| | iCE40LP640, iCE40LP/HX1K, iCE40LP/HX4K, iCE40LP/HX8K | Power-On-Reset ramp-down trip point (band gap based circuit monitoring VCC, VCCIO_2, VCC_SPI and VPP_2V5) | VCC | — | 0.75 | V |
| | | | VCCIO_2 | — | 1.29 | V |
| | | | VCC_SPI | — | 1.29 | V |
| | | | VPP_2V5 | — | 1.33 | V |

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.

## ESD Performance

Please refer to the iCE40 Product Family Qualification Summary for complete qualification data, including ESD performance.

# DC Electrical Characteristics

**Over Recommended Operating Conditions**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{IL}$, $I_{IH}$ [1, 3, 4, 5, 6, 7] | Input or I/O Leakage | $0V < V_{IN} < V_{CCIO} + 0.2$ V | — | — | +/–10 | µA |
| $C_1$ [6, 7] | I/O Capacitance[2] | $V_{CCIO}$ = 3.3 V, 2.5 V, 1.8 V<br>$V_{CC}$ = Typ., $V_{IO}$ = 0 to $V_{CCIO}$ + 0.2 V | — | 6 | — | pf |
| $C_2$ [6, 7] | Global Input Buffer Capacitance[2] | $V_{CCIO}$ = 3.3 V, 2.5 V, 1.8 V<br>$V_{CC}$ = Typ., $V_{IO}$ = 0 to $V_{CCIO}$ + 0.2 V | — | 6 | — | pf |
| $V_{HYST}$ | Input Hysteresis | $V_{CCIO}$ = 1.8 V, 2.5 V, 3.3 V | — | 200 | — | mV |
| $I_{PU}$ [6, 7] | Internal PIO Pull-up Current | $V_{CCIO}$ = 1.8 V, 0=<$V_{IN}$<=0.65 $V_{CCIO}$ | –3 | — | –31 | µA |
| | | $V_{CCIO}$ = 2.5 V, 0=<$V_{IN}$<=0.65 $V_{CCIO}$ | –8 | — | –72 | µA |
| | | $V_{CCIO}$ = 3.3 V, 0=<$V_{IN}$<=0.65 $V_{CCIO}$ | –11 | — | –128 | µA |

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Internal pull-up resistors are disabled.
2. $T_J$ 25°C, f = 1.0 MHz.
3. Please refer to $V_{IL}$ and $V_{IH}$ in the sysIO Single-Ended DC Electrical Characteristics table of this document.
4. Only applies to IOs in the SPI bank following configuration.
5. Some products are clamped to a diode when $V_{IN}$ is larger than $V_{CCIO}$.
6. High current IOs has three sysIO buffers connected together.
7. The iCE40LP640 and iCE40LP1K SWG16 package has CDONE and a sysIO buffer are connected together.

# Static Supply Current – LP Devices[1, 2, 3, 4]

| Symbol | Parameter | Device | Typ. $V_{CC}$[4] | Units |
|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply | iCE40LP384 | 21 | µA |
| | | iCE40LP640 | 100 | µA |
| | | iCE40LP1K | 100 | µA |
| | | iCE40LP4K | 250 | µA |
| | | iCE40LP8K | 250 | µA |
| $I_{CCPLL}$ [5, 6] | PLL Power Supply | All devices | 0.5 | µA |
| $I_{PP\_2V5}$ | NVCM Power Supply | All devices | 1.0 | µA |
| $I_{CCIO}$, $I_{CC\_SPI}$ | Bank Power Supply[4]<br>$V_{CCIO}$ = 2.5 V | All devices | 3.5 | µA |

1. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at $V_{CCIO}$ or GND, on-chip PLL is off. For more detail with your specific design, use the Power Calculator tool. Power specified with master SPI configuration mode. Other modes may be up to 25% higher.
2. Frequency = 0 MHz.
3. $T_J$ = 25 °C, power supplies at nominal voltage.
4. Does not include pull-up.
5. No PLL available on the iCE40LP384 and iCE40LP640 device.
6. $V_{CCPLL}$ is tied to $V_{CC}$ internally in packages without PLLs pins.

## sysIO Differential Electrical Characteristics

The LVDS25E/subLVDSE differential output buffers are available on all banks but the LVDS/subLVDS input buffers are only available on Bank 3 of iCE40 devices.

### LVDS25

**Over Recommended Operating Conditions**

| Parameter Symbol | Parameter Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{INP}$, $V_{INM}$ | Input Voltage | $V_{CCIO}$[1] = 2.5 | 0 | — | 2.5 | V |
| $V_{THD}$ | Differential Input Threshold | | 250 | 350 | 450 | mV |
| $V_{CM}$ | Input Common Mode Voltage | $V_{CCIO}$[1] = 2.5 | ($V_{CCIO}$/2) - 0.3 | $V_{CCIO}$/2 | ($V_{CCIO}$/2) + 0.3 | V |
| $I_{IN}$ | Input Current | Power on | — | — | ±10 | µA |

1. Typical.

### subLVDS

**Over Recommended Operating Conditions**

| Parameter Symbol | Parameter Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{INP}$, $V_{INM}$ | Input Voltage | $V_{CCIO}$[1] = 1.8 | 0 | — | 1.8 | V |
| $V_{THD}$ | Differential Input Threshold | | 100 | 150 | 200 | mV |
| $V_{CM}$ | Input Common Mode Voltage | $V_{CCIO}$[1] = 1.8 | ($V_{CCIO}$/2) - 0.25 | $V_{CCIO}$/2 | ($V_{CCIO}$/2) + 0.25 | V |
| $I_{IN}$ | Input Current | Power on | — | — | ±10 | µA |

1. Typical.

## LVDS25E Emulation

iCE40 devices can support LVDSE outputs via emulation on all banks. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all devices. The scheme shown in Figure 3-1 is one possible solution for LVDS25E standard implementation. Resistor values in Figure 3-1 are industry standard values for 1% resistors.

***Figure 3-1. LVDS25E Using External Resistors***

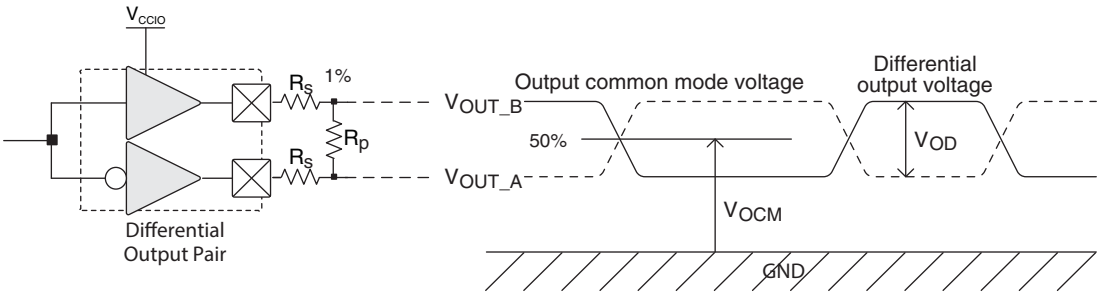



***Table 3-1. LVDS25E DC Conditions***

**Over Recommended Operating Conditions**

| Parameter | Description | Typ. | Units |
|---|---|---|---|
| $Z_{OUT}$ | Output impedance | 20 | Ohms |
| $R_S$ | Driver series resistor | 150 | Ohms |
| $R_P$ | Driver parallel resistor | 140 | Ohms |
| $R_T$ | Receiver termination | 100 | Ohms |
| $V_{OH}$ | Output high voltage | 1.43 | V |
| $V_{OL}$ | Output low voltage | 1.07 | V |
| $V_{OD}$ | Output differential voltage | 0.30 | V |
| $V_{CM}$ | Output common mode voltage | 1.25 | V |
| $Z_{BACK}$ | Back impedance | 100.5 | Ohms |
| $I_{DC}$ | DC output current | 6.03 | mA |

## SubLVDS Emulation

The iCE40 family supports the differential subLVDS standard. The output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all banks of the devices. The subLVDS input standard is supported by the LVDS25 differential input buffer. The scheme shown in Figure 3-2 is one possible solution for subLVDSE output standard implementation. Use LVDS25E mode with suggested resistors for subLVDSE operation. Resistor values in Figure 3-2 are industry standard values for 1% resistors.

***Figure 3-2. subLVDSE***

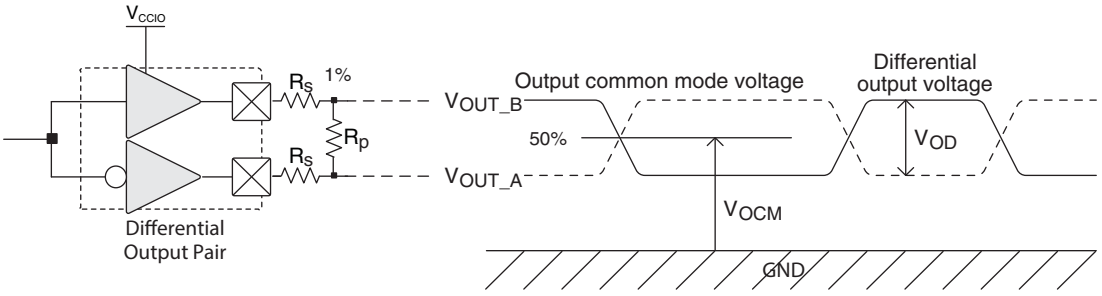



***Table 3-2. subLVDSE DC Conditions***

**Over Recommended Operating Conditions**

| Parameter | Description | Typ. | Units |
|---|---|---|---|
| $Z_{OUT}$ | Output impedance | 20 | Ohms |
| $R_S$ | Driver series resistor | 270 | Ohms |
| $R_P$ | Driver parallel resistor | 120 | Ohms |
| $R_T$ | Receiver termination | 100 | Ohms |
| $V_{OH}$ | Output high voltage | 1.43 | V |
| $V_{OL}$ | Output low voltage | 1.07 | V |
| $V_{OD}$ | Output differential voltage | 0.35 | V |
| $V_{CM}$ | Output common mode voltage | 0.9 | V |
| $Z_{BACK}$ | Back impedance | 100.5 | Ohms |
| $I_{DC}$ | DC output current | 2.8 | mA |

# Typical Building Block Function Performance – LP Devices[1, 2]

## Pin-to-Pin Performance (LVCMOS25)

| Function | Timing | Units |
|---|---|---|
| **Basic Functions** | | |
| 16-bit decoder | 11.0 | ns |
| 4:1 MUX | 12.0 | ns |
| 16:1 MUX | 13.0 | ns |

## Register-to-Register Performance

| Function | Timing | Units |
|---|---|---|
| **Basic Functions** | | |
| 16:1 MUX | 190 | MHz |
| 16-bit adder | 160 | MHz |
| 16-bit counter | 175 | MHz |
| 64-bit counter | 65 | MHz |
| **Embedded Memory Functions** | | |
| 256x16 Pseudo-Dual Port RAM | 240 | MHz |

1. The above timing numbers are generated using the iCECube2 design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.
2. Using a $V_{CC}$ of 1.14 V at Junction Temp 85 °C.

# Typical Building Block Function Performance – HX Devices[1, 2]

## Pin-to-Pin Performance (LVCMOS25)

| Function | Timing | Units |
|---|---|---|
| **Basic Functions** | | |
| 16-bit decoder | 10.0 | ns |
| 4:1 MUX | 9.0 | ns |
| 16:1 MUX | 9.5 | ns |

## Register-to-Register Performance

| Function | Timing | Units |
|---|---|---|
| **Basic Functions** | | |
| 16:1 MUX | 305 | MHz |
| 16-bit adder | 220 | MHz |
| 16-bit counter | 255 | MHz |
| 64-bit counter | 105 | MHz |
| **Embedded Memory Functions** | | |
| 256x16 Pseudo-Dual Port RAM | 403 | MHz |

1. The above timing numbers are generated using the iCECube2 design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.
2. Using a $V_{CC}$ of 1.14 V at Junction Temp 85 °C.

## sysCONFIG Port Timing Specifications[1] (Continued)

| Symbol | Parameter | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{MCLK}$ | CRESET_B high to first MCLK edge | iCE40LP384 - Low Frequency (Default) | 600 | — | — | us |
| | | iCE40LP384 - Medium Frequency | 600 | — | — | us |
| | | iCE40LP384 - High Frequency | 600 | — | — | us |
| | | iCE40LP640, iCE40LP/HX1K - Low Frequency (Default) | 800 | — | — | us |
| | | iCE40LP640, iCE40LP/HX1K - Medium Frequency | 800 | — | — | us |
| | | iCE40LP640, iCE40LP/HX1K - High Frequency | 800 | — | — | us |
| | | iCE40LP/HX1K -Low Frequency (Default) | 800 | — | — | us |
| | | iCE40LP/HX1K - Medium Frequency | 800 | — | — | us |
| | | iCE40LP/HX1K - High Frequency | 800 | — | — | us |
| | | iCE40LP/HX4K - Low Frequency (Default) | 1200 | — | — | us |
| | | iCE40LP/HX4K - Medium Frequency | 1200 | — | — | us |
| | | iCE40LP/HX4K - high frequency | 1200 | — | — | us |
| | | iCE40LP/HX8K - Low Frequency (Default) | 1200 | — | — | us |
| | | iCE40LP/HX8K - Medium Frequency | 1200 | — | — | us |
| | | iCE40LP/HX8K - High Frequency | 1200 | — | — | us |

1. Does not apply for NVCM.
2. Supported only with 1.2 V $V_{CC}$ and at 25 °C.
3. Extended range $f_{MAX}$ Write operations support up to 53 MHz only with 1.2 V $V_{CC}$ and at 25 °C.

## Signal Descriptions

| Signal Name | I/O | Descriptions |
|---|---|---|
| **General Purpose** | | |
| IO[Bank]_[Row/Column Number][A/B] | I/O | [Bank] indicates the bank of the device on which the pad is located. [Number] indicates IO number on the device. |
| IO[Bank]_[Row/Column Number][A/B] | I/O | [Bank] indicates the bank of the device on which the pad is located. [Number] indicates IO number on the device. [A/B] indicates the differential I/O. 'A' = negative input. 'B' = positive input. |
| HCIO[Bank]_[Number] | I/O | High Current IO. [Bank] indicates the bank of the device on which the pad is located. [Number] indicates IO number. |
| NC | — | No connect |
| GND | — | GND – Ground. Dedicated pins. It is recommended that all GNDs are tied together. |
| VCC | — | VCC – The power supply pins for core logic. Dedicated pins. It is recommended that all VCCs are tied to the same supply. |
| VCCIO_x | — | VCCIO – The power supply pins for I/O Bank x. Dedicated pins. All VCCIOs located in the same bank are tied to the same supply. |
| **PLL and Global Functions (Used as user-programmable I/O pins when not used for PLL or clock pins)** | | |
| VCCPLLx | — | PLL VCC – Power. Dedicated pins. The PLL requires a separate power and ground that is quiet and stable to reduce the output clock jitter of the PLL. |
| GNDPLLx | — | PLL GND – Ground. Dedicated pins. The sysCLOCK PLL has the DC ground connection made on the FPGA, so the external PLL ground connection (GNDPLL) must NOT be connected to the board's ground. |
| GBINx | — | Global pads. Two per side. |
| **Programming and Configuration** | | |
| CBSEL[0:1] | I/O | Dual function pins. I/Os when not used as CBSEL. Optional ColdBoot configuration SELect input, if ColdBoot mode is enabled. |
| CRESET_B | I | Configuration Reset, active Low. Dedicated input. No internal pull-up resistor. Either actively drive externally or connect a 10 KOhm pull-up resistor to VCCIO_2. |
| CDONE | I/O | Configuration Done. Includes a permanent weak pull-up resistor to VCCIO_2. If driving external devices with CDONE output, an external pull-up resistor to VCCIO_2 may be required. Refer to the TN1248, iCE40 Programming and Configuration for more details. Following device configuration the iCE40LP640 and iCE40LP1K in the SWG16 package CDONE pin can be used as a user output. |
| VCC_SPI | — | SPI interface voltage supply input. Must have a valid voltage even if configuring from NVCM. |
| SPI_SCK | I/O | Input Configuration Clock for configuring an FPGA in Slave SPI mode. Output Configuration Clock for configuring an FPGA configuration modes. |
| SPI_SS_B | I/O | SPI Slave Select. Active Low. Includes an internal weak pull-up resistor to VCC_SPI during configuration. During configuration, the logic level sampled on this pin determines the configuration mode used by the iCE40 device. An input when sampled at the start of configuration. An input when in SPI Peripheral configuration mode (SPI_SS_B = Low). An output when in Master SPI Flash configuration mode. |
| SPI_SI | I/O | Slave SPI serial data input and master SPI serial data output |
| SPI_SO | I/O | Slave SPI serial data output and master SPI serial data input |

## Pin Information Summary

| | iCE40LP384 | | | iCE40LP640 | iCE40LP1K | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | SG32 | CM36[2] | CM49[2] | SWG16 | SWG16 | CM36[1, 2] | CM49[1, 2] | CM81 | CB81 | QN84 | CM121 | CB121 |
| **General Purpose I/O per Bank** | | | | | | | | | | | | |
| Bank 0 | 6 | 4 | 10 | 3 | 3 | 4 | 10 | 17 | 17 | 17 | 24 | 24 |
| Bank 1 | 5 | 7 | 7 | 0 | 0 | 7 | 7 | 15 | 16 | 17 | 25 | 21 |
| Bank 2 | 0 | 4 | 4 | 1 | 1 | 4 | 4 | 11 | 8 | 11 | 18 | 19 |
| Bank 3 | 6 | 6 | 12 | 2 | 2 | 6 | 10 | 16 | 17 | 18 | 24 | 24 |
| Configuration | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 |
| Total General Purpose Single Ended I/O | 21 | 25 | 37 | 10 | 10 | 25 | 35 | 63 | 62 | 67 | 95 | 92 |
| **High Current Outputs per Bank** | | | | | | | | | | | | |
| Bank 0 | 0 | 0 | 0 | 3 | 3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bank 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bank 2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bank 3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Total Current Outputs | 0 | 0 | 0 | 3 | 3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **Differential Inputs per Bank** | | | | | | | | | | | | |
| Bank 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bank 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bank 2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bank 3 | 3 | 3 | 6 | 1 | 1 | 3 | 5 | 8 | 9 | 7 | 12 | 12 |
| Total Differential Inputs | 3 | 3 | 6 | 1 | 1 | 3 | 5 | 8 | 9 | 7 | 12 | 12 |
| **Dedicated Inputs per Bank** | | | | | | | | | | | | |
| Bank 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bank 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bank 2 | 2 | 2 | 2 | 1 | 1 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| Bank 3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Configuration | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Total Dedicated Inputs | 2 | 2 | 2 | 1 | 1 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| **Vccio Pins** | | | | | | | | | | | | |
| Bank 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 2 | 1 |
| Bank 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 2 | 1 |
| Bank 2 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 2 | 1 |
| Bank 3 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 2 | 2 |
| VCC | 1 | 1 | 2 | 1 | 1 | 1 | 2 | 3 | 3 | 4 | 4 | 4 |
| VCC_SPI | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| VPP_2V5 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| VPP_FAST[3] | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| VCCPLL | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| GND | 2 | 3 | 3 | 2 | 2 | 3 | 4 | 5 | 8 | 4 | 8 | 11 |
| NC | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 3 |
| Total Count of Bonded Pins | 32 | 36 | 49 | 16 | 16 | 36 | 49 | 81 | 81 | 84 | 121 | 121 |

1. $V_{CCIO0}$ and $V_{CCIO1}$ are connected together.
2. $V_{CCIO2}$ and $V_{CCIO3}$ are connected together.
3. $V_{PP\_FAST}$, used only for fast production programming, must be left floating or unconnected in applications, except CM36 and CM49 packages MUST have the $V_{PP\_FAST}$ ball connected to $V_{CCIO\_0}$ ball externally.

## Pin Information Summary (Continued)

| | iCE40LP4K | | | iCE40LP8K | | | iCE40HX1K | | |
|---|---|---|---|---|---|---|---|---|---|
| | CM81 | CM121 | CM225 | CM81 | CM121 | CM225 | VQ100 | CB132 | TQ144 |
| **General Purpose I/O per Bank** | | | | | | | | | |
| Bank 0 | 17 | 23 | 46 | 17 | 23 | 46 | 19 | 24 | 23 |
| Bank 1 | 15 | 21 | 42 | 15 | 21 | 42 | 19 | 25 | 25 |
| Bank 2 | 9 | 19 | 40 | 9 | 19 | 40 | 12 | 20 | 20 |
| Bank 3 | 18 | 26 | 46 | 18 | 26 | 46 | 18 | 22 | 24 |
| Configuration | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 |
| Total General Purpose Single Ended I/O | 63 | 93 | 178 | 63 | 93 | 178 | 72 | 95 | 96 |
| **High Current Outputs per Bank** | | | | | | | | | |
| Bank 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bank 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bank 2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bank 3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Total Differential Inputs | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **Differential Inputs per Bank** | | | | | | | | | |
| Bank 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bank 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bank 2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bank 3 | 9 | 13 | 23 | 9 | 13 | 23 | 9 | 11 | 12 |
| Total Differential Inputs | 9 | 13 | 23 | 9 | 13 | 23 | 9 | 11 | 12 |
| **Dedicated Inputs per Bank** | | | | | | | | | |
| Bank 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bank 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| Bank 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| Bank 3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Configuration | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Total Dedicated Inputs | 2 | 2 | 3 | 2 | 2 | 3 | 2 | 3 | 3 |
| **Vccio Pins** | | | | | | | | | |
| Bank 0 | 1 | 1 | 3 | 1 | 1 | 3 | 2 | 2 | 2 |
| Bank 1 | 1 | 1 | 3 | 1 | 1 | 3 | 2 | 2 | 2 |
| Bank 2 | 1 | 1 | 3 | 1 | 1 | 3 | 2 | 2 | 2 |
| Bank 3 | 1 | 2 | 4 | 1 | 2 | 4 | 3 | 3 | 2 |
| VCC | 3 | 4 | 8 | 3 | 4 | 8 | 4 | 5 | 4 |
| VCC_SPI | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| VPP_2V5 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| VPP_FAST[1] | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| VCCPLL | 1 | 2 | 2 | 1 | 2 | 2 | 0 | 1 | 1 |
| GND | 5 | 12 | 18 | 5 | 12 | 18 | 10 | 14 | 10 |
| NC | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 2 | 19 |
| Total Count of Bonded Pins | 81 | 121 | 225 | 81 | 121 | 225 | 100 | 132 | 144 |

1. $V_{PP\_FAST}$, used only for fast production programming, must be left floating or unconnected in applications.

## Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging

| Part Number | LUTs | Supply Voltage | Package | Leads | Temp. |
|---|---|---|---|---|---|
| ICE40LP384-CM36 | 384 | 1.2 V | Halogen-Free ucBGA | 36 | IND |
| ICE40LP384-CM36TR | 384 | 1.2 V | Halogen-Free ucBGA | 36 | IND |
| ICE40LP384-CM36TR1K | 384 | 1.2 V | Halogen-Free ucBGA | 36 | IND |
| ICE40LP384-CM49 | 384 | 1.2 V | Halogen-Free ucBGA | 49 | IND |
| ICE40LP384-CM49TR | 384 | 1.2 V | Halogen-Free ucBGA | 49 | IND |
| ICE40LP384-CM49TR1K | 384 | 1.2 V | Halogen-Free ucBGA | 49 | IND |
| ICE40LP384-SG32 | 384 | 1.2 V | Halogen-Free QFN | 32 | IND |
| ICE40LP384-SG32TR | 384 | 1.2 V | Halogen-Free QFN | 32 | IND |
| ICE40LP384-SG32TR1K | 384 | 1.2 V | Halogen-Free QFN | 32 | IND |
| ICE40LP640-SWG16TR | 640 | 1.2 V | Halogen-Free WLCSP | 16 | IND |
| ICE40LP640-SWG16TR50 | 640 | 1.2 V | Halogen-Free WLCSP | 16 | IND |
| ICE40LP640-SWG16TR1K | 640 | 1.2 V | Halogen-Free WLCSP | 16 | IND |
| ICE40LP1K-SWG16TR | 1280 | 1.2 V | Halogen-Free WLCSP | 16 | IND |
| ICE40LP1K-SWG16TR50 | 1280 | 1.2 V | Halogen-Free WLCSP | 16 | IND |
| ICE40LP1K-SWG16TR1K | 1280 | 1.2 V | Halogen-Free WLCSP | 16 | IND |
| ICE40LP1K-CM36 | 1280 | 1.2 V | Halogen-Free ucBGA | 36 | IND |
| ICE40LP1K-CM36TR | 1280 | 1.2 V | Halogen-Free ucBGA | 36 | IND |
| ICE40LP1K-CM36TR1K | 1280 | 1.2 V | Halogen-Free ucBGA | 36 | IND |
| ICE40LP1K-CM49 | 1280 | 1.2 V | Halogen-Free ucBGA | 49 | IND |
| ICE40LP1K-CM49TR | 1280 | 1.2 V | Halogen-Free ucBGA | 49 | IND |
| ICE40LP1K-CM49TR1K | 1280 | 1.2 V | Halogen-Free ucBGA | 49 | IND |
| ICE40LP1K-CM81 | 1280 | 1.2 V | Halogen-Free ucBGA | 81 | IND |
| ICE40LP1K-CM81TR | 1280 | 1.2 V | Halogen-Free ucBGA | 81 | IND |
| ICE40LP1K-CM81TR1K | 1280 | 1.2 V | Halogen-Free ucBGA | 81 | IND |
| ICE40LP1K-CB81 | 1280 | 1.2 V | Halogen-Free csBGA | 81 | IND |
| ICE40LP1K-CB81TR | 1280 | 1.2 V | Halogen-Free csBGA | 81 | IND |
| ICE40LP1K-CB81TR1K | 1280 | 1.2 V | Halogen-Free csBGA | 81 | IND |
| ICE40LP1K-CM121 | 1280 | 1.2 V | Halogen-Free ucBGA | 121 | IND |
| ICE40LP1K-CM121TR | 1280 | 1.2 V | Halogen-Free ucBGA | 121 | IND |
| ICE40LP1K-CM121TR1K | 1280 | 1.2 V | Halogen-Free ucBGA | 121 | IND |
| ICE40LP1K-CB121 | 1280 | 1.2 V | Halogen-Free csBGA | 121 | IND |
| ICE40LP1K-QN84 | 1280 | 1.2 V | Halogen-Free QFN | 84 | IND |
| ICE40LP4K-CM81 | 3520 | 1.2 V | Halogen-Free ucBGA | 81 | IND |
| ICE40LP4K-CM81TR | 3520 | 1.2 V | Halogen-Free ucBGA | 81 | IND |
| ICE40LP4K-CM81TR1K | 3520 | 1.2 V | Halogen-Free ucBGA | 81 | IND |
| ICE40LP4K-CM121 | 3520 | 1.2 V | Halogen-Free ucBGA | 121 | IND |
| ICE40LP4K-CM121TR | 3520 | 1.2 V | Halogen-Free ucBGA | 121 | IND |
| ICE40LP4K-CM121TR1K | 3520 | 1.2 V | Halogen-Free ucBGA | 121 | IND |
| ICE40LP4K-CM225 | 3520 | 1.2 V | Halogen-Free ucBGA | 225 | IND |
| ICE40LP8K-CM81 | 7680 | 1.2 V | Halogen-Free ucBGA | 81 | IND |
| ICE40LP8K-CM81TR | 7680 | 1.2 V | Halogen-Free ucBGA | 81 | IND |
| ICE40LP8K-CM81TR1K | 7680 | 1.2 V | Halogen-Free ucBGA | 81 | IND |
| ICE40LP8K-CM121 | 7680 | 1.2 V | Halogen-Free ucBGA | 121 | IND |
| ICE40LP8K-CM121TR | 7680 | 1.2 V | Halogen-Free ucBGA | 121 | IND |

# iCE40 LP/HX Family Data Sheet Supplemental Information



## For Further Information

A variety of technical notes for the iCE40 family are available on the Lattice web site.

- TN1248, iCE40 Programming and Configuration
- TN1250, Memory Usage Guide for iCE40 Devices
- TN1251, iCE40 sysCLOCK PLL Design and Usage Guide
- TN1252, iCE40 Hardware Checklist
- TN1253, Using Differential I/O (LVDS, Sub-LVDS) in iCE40 Devices
- TN1074, PCB Layout Recommendations for BGA Packages
- iCE40 Pinout Files
- Thermal Management document
- Lattice design tools
- IBIS
- Package Diagrams Data Sheet
- Schematic Symbols

# iCE40 LP/HX Family Data Sheet Revision History

**March 2017** **Data Sheet DS1040**

| Date | Version | Section | Change Summary |
|---|---|---|---|
| March 2017 | 3.3 | Introduction | Updated Features section. Added 121-ball caBGA package for ICE40 HX4K/8K to Table 1-1, iCE40 Family Selection Guide. |
| | | Architecture | Updated PLB Blocks section. Changed “subtracters” to “subtractors” in the Carry Logic description. |
| | | | Updated Clock/Control Distribution Network section. Switched the “Clock Enable“ and the “Reset” headings in Table 2-2, Global Buffer (GBUF) Connections to Programmable Logic Blocks. |
| | | Pinout Information | Updated Pin Information Summary section. Added BG121information under iCE40HX4K and iCE40HX8K. |
| | | Ordering Information | Updated iCE40 Part Number Description section. Added Shipping Method and BG121 package under High Performance (HX) Devices. |
| | | | Updated Ordering Information section. Added part numbers for BG121 under High-Performance Industrial Grade Devices, Halogen Free (RoHS) Packaging. |
| | | Supplemental Information | Corrected reference to “Package Diagrams Data Sheet”. |
| October 2015 | 3.2 | Introduction | Updated Features section. Added footnote to 16 WLCSP Programmable I/O: Max Inputs (LVDS25) in Table 1-1, iCE40 Family Selection Guide. |
| | | DC and Switching Characteristics | Updated sysCLOCK PLL Timing section. Changed $t_{DT}$ conditions. |
| | | | Updated Programming NVCM Supply Current – LP Devices section. Changed $I_{PP\_2V5}$ and $I_{CCIO}$, $I_{CC\_SPI}$ units. |
| March 2015 | 3.1 | DC and Switching Characteristics | Updated sysIO Single-Ended DC Electrical Characteristics section. Changed LVCMOS 3.3 and LVCMOS 2. 5 $V_{OH}$ Min. (V) from 0.5 to 0.4. |
| July 2014 | 3.0 | DC and Switching Characteristics | Revised and/or added Typ. $V_{CC}$ data in the following sections.<br>— Static Supply Current – LP Devices<br>— Static Supply Current – HX Devices<br>— Programming NVCM Supply Current – LP Devices<br>— Programming NVCM Supply Current – HX Devices<br>In each section table, the footnote indicating Advanced device status was removed. |
| | | Pinout Information | Updated Pin Information Summary section. Added footnote 1 to CM49 under iCE40LP1K. |
| April 2014 | 02.9 | Ordering Information | Changed “i” to “I” in part number description and ordering part numbers. |
| | | | Added part numbers to the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging table. |