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## Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

### Details

Product Status	Active
Number of LABs/CLBs	80
Number of Logic Elements/Cells	640
Total RAM Bits	32768
Number of I/O	10
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	16-XFBGA, WLCSP
Supplier Device Package	16-WLCSP (1.4x1.48)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/ice40lp640-swg16tr1k">https://www.e-xfl.com/product-detail/lattice-semiconductor/ice40lp640-swg16tr1k</a>

## Features

- Flexible Logic Architecture**
  - Five devices with 384 to 7,680 LUT4s and 10 to 206 I/Os
- Ultra Low Power Devices**
  - Advanced 40 nm low power process
  - As low as 21  $\mu$ A standby power
  - Programmable low swing differential I/Os
- Embedded and Distributed Memory**
  - Up to 128 kbits sysMEM™ Embedded Block RAM
- Pre-Engineered Source Synchronous I/O**
  - DDR registers in I/O cells
- High Current LED Drivers**
  - Three High Current Drivers used for three different LEDs or one RGB LED
- High Performance, Flexible I/O Buffer**
  - Programmable sysIO™ buffer supports wide range of interfaces:
    - LVCMOS 3.3/2.5/1.8
    - LVDS25E, subLVDS
    - Schmitt trigger inputs, to 200 mV typical hysteresis
- Flexible On-Chip Clocking**
  - Programmable pull-up mode
  - Eight low-skew global clock resources
  - Up to two analog PLLs per device
- Flexible Device Configuration**
  - SRAM is configured through:
    - Standard SPI Interface
    - Internal Nonvolatile Configuration Memory (NVCM)
- Broad Range of Package Options**
  - WLCSP, QFN, VQFP, TQFP, ucBGA, caBGA, and csBGA package options
  - Small footprint package options
    - As small as 1.40 mm x 1.48 mm
  - Advanced halogen-free packaging

**Table 1-1. iCE40 Family Selection Guide**

Part Number	LP384	LP640	LP1K	LP4K	LP8K	HX1K	HX4K	HX8K
Logic Cells (LUT + Flip-Flop)	384	640	1,280	3,520	7,680	1,280	3,520	7,680
RAM4K Memory Blocks	0	8	16	20	32	16	20	32
RAM4K RAM bits	0	32K	64K	80K	128K	64K	80K	128K
Phase-Locked Loops (PLLs)	0	0	1 <sup>1</sup>	2 <sup>2</sup>	2 <sup>2</sup>	1 <sup>1</sup>	2	2
Maximum Programmable I/O Pins	63	25	95	167	178	95	95	206
Maximum Differential Input Pairs	8	3	12	20	23	11	12	26
High Current LED Drivers	0	3	3	0	0	0	0	0
Package	Code	Programmable I/O: Max Inputs (LVDS25)						
16 WLCSP (1.40 mm x 1.48 mm, 0.35 mm)	SWG16		10(0) <sup>1</sup>	10(0) <sup>1</sup>				
32 QFN (5 mm x 5 mm, 0.5 mm)	SG32	21(3)						
36 ucBGA (2.5 mm x 2.5 mm, 0.4 mm)	CM36	25(3)		25(3) <sup>1</sup>				
49 ucBGA (3 mm x 3 mm, 0.4 mm)	CM49	37(6)		35(5) <sup>1</sup>				
81 ucBGA (4 mm x 4 mm, 0.4 mm)	CM81			63(8)	63(9) <sup>2</sup>	63(9) <sup>2</sup>		
81 csBGA (5 mm x 5 mm, 0.5 mm)	CB81			62(9) <sup>1</sup>				

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**Table 1-1. iCE40 Family Selection Guide (continued)**

84 QFN (7 mm x 7 mm, 0.5 mm)	QN84			67(7) <sup>1</sup>					
100 VQFP (14 mm x 14 mm, 0.5 mm)	VQ100						72(9) <sup>1</sup>		
121 ucBGA (5 mm x 5 mm, 0.4 mm)	CM121			95(12)	93(13)	93(13)			
121 csBGA (6 mm x 6 mm, 0.5 mm)	CB121			92(12)					
121 caBGA (9 mm x 9 mm, 0.8 mm)	BG121							93(13)	93(13)
132 csBGA (8 mm x 8 mm, 0.5 mm)	CB132						95(11)	95(12)	95(12)
144 TQFP (20 mm x 20 mm, 0.5 mm)	TQ144						96(12)	107(14)	
225 ucBGA (7 mm x 7 mm, 0.4 mm)	CM225				178(23)	178(23)			178(23)
256-ball caBGA (14 mm x 14 mm, 0.8 mm)	CT256								206(26)

1. No PLL available on the 16 WLCSP, 36 ucBGA, 81 csBGA, 84 QFN and 100 VQFP packages.

2. Only one PLL available on the 81 ucBGA package.

3. High Current I/Os only available on the 16 WLCSP package.

## Introduction

The iCE40 family of ultra-low power, non-volatile FPGAs has five devices with densities ranging from 384 to 7680 Look-Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic, these devices feature Embedded Block RAM (EBR), Non-volatile Configuration Memory (NVCM) and Phase Locked Loops (PLLs). These features allow the devices to be used in low-cost, high-volume consumer and system applications. Select packages offer High-Current drivers that are ideal to drive three white LEDs, or one RGB LED.

The iCE40 devices are fabricated on a 40 nm CMOS low power process. The device architecture has several features such as programmable low-swing differential I/Os and the ability to turn off on-chip PLLs dynamically. These features help manage static and dynamic power consumption, resulting in low static power for all members of the family. The iCE40 devices are available in two versions – ultra low power (LP) and high performance (HX) devices.

The iCE40 FPGAs are available in a broad range of advanced halogen-free packages ranging from the space saving 1.40x1.48 mm WLCSP to the PCB-friendly 20x20 mm TQFP. Table 1-1 shows the LUT densities, package and I/O options, along with other key parameters.

The iCE40 devices offer enhanced I/O features such as pull-up resistors. Pull-up features are controllable on a “per-pin” basis.

The iCE40 devices also provide flexible, reliable and secure configuration from on-chip NVCM. These devices can also configure themselves from external SPI Flash or be configured by an external master such as a CPU.

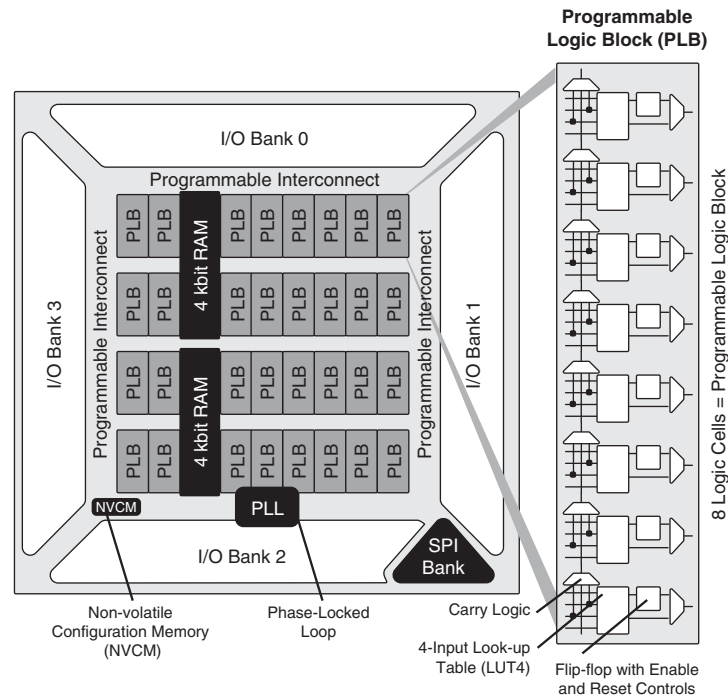
Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the iCE40 family of devices. Popular logic synthesis tools provide synthesis library support for iCE40. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the iCE40 device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules, including a number of reference designs, licensed free of charge, optimized for the iCE40 FPGA family. By using these configurable soft core IP cores as standardized blocks, users are free to concentrate on the unique aspects of their design, increasing their productivity.

## Architecture Overview

The iCE40 family architecture contains an array of Programmable Logic Blocks (PLB), sysCLOCK™ PLLs, Non-volatile Programmable Configuration Memory (NVCM) and blocks of sysMEM™ Embedded Block RAM (EBR) surrounded by Programmable I/O (PIO). Figure 2-1 shows the block diagram of the iCE40LP/HX1K device.

**Figure 2-1. iCE40LP/HX1K Device, Top View**



The logic blocks, Programmable Logic Blocks (PLB) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each column has either logic blocks or EBR blocks. The PIO cells are located at the periphery of the device, arranged in banks. The PLB contains the building blocks for logic, arithmetic, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the iCE40 family, there are up to four independent sysIO banks. Note on some packages  $V_{CCIO}$  banks are tied together. There are different types of I/O buffers on the different banks. Refer to the details in later sections of this document. The sysMEM EBRs are large 4 kbit, dedicated fast memory blocks. These blocks can be configured as RAM, ROM or FIFO.

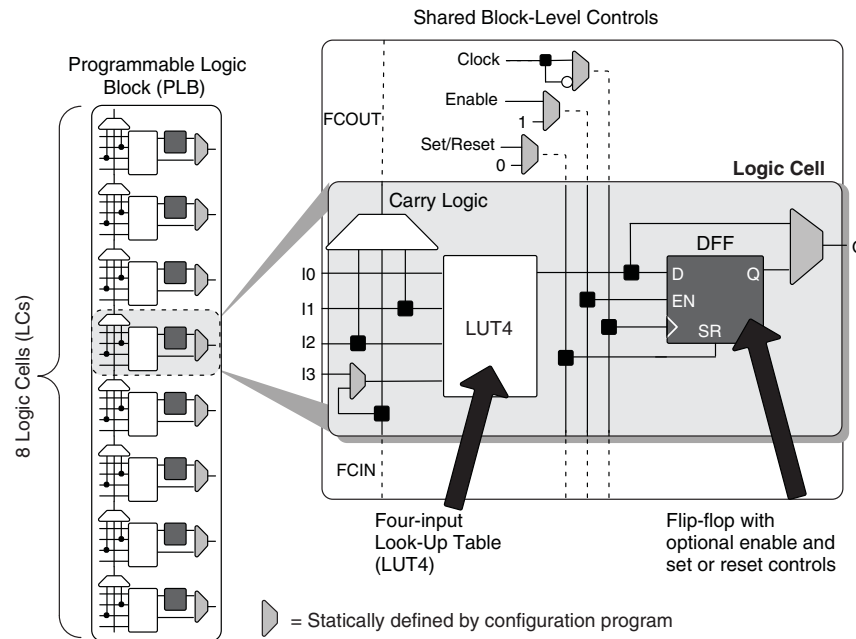
The iCE40 architecture also provides up to two sysCLOCK Phase Locked Loop (PLL) blocks. The PLLs have multiply, divide, and phase shifting capabilities that are used to manage the frequency and phase relationships of the clocks.

Every device in the family has a SPI port that supports programming and configuration of the device. The iCE40 includes on-chip, Nonvolatile Configuration Memory (NVCM).

## PLB Blocks

The core of the iCE40 device consists of Programmable Logic Blocks (PLB) which can be programmed to perform logic and arithmetic functions. Each PLB consists of eight interconnected Logic Cells (LC) as shown in Figure 2-2. Each LC contains one LUT and one register.

**Figure 2-2. PLB Block Diagram**



## Logic Cells

Each Logic Cell includes three primary logic elements shown in Figure 2-2.

- A four-input Look-Up Table (LUT4) builds any combinational logic function, of any complexity, requiring up to four inputs. Similarly, the LUT4 element behaves as a 16x1 Read-Only Memory (ROM). Combine and cascade multiple LUT4s to create wider logic functions.
- A 'D'-style Flip-Flop (DFF), with an optional clock-enable and reset control input, builds sequential logic functions. Each DFF also connects to a global reset signal that is automatically asserted immediately following device configuration.
- Carry Logic boosts the logic efficiency and performance of arithmetic functions, including adders, subtractors, comparators, binary counters and some wide, cascaded logic functions.

**Table 2-1. Logic Cell Signal Descriptions**

Function	Type	Signal Names	Description
Input	Data signal	I0, I1, I2, I3	Inputs to LUT4
Input	Control signal	Enable	Clock enable shared by all LCs in the PLB
Input	Control signal	Set/Reset <sup>1</sup>	Asynchronous or synchronous local set/reset shared by all LCs in the PLB.
Input	Control signal	Clock	Clock one of the eight Global Buffers, or from the general-purpose interconnects fabric shared by all LCs in the PLB
Input	Inter-PLB signal	FCIN	Fast carry in
Output	Data signals	O	LUT4 or registered output
Output	Inter-PFU signal	FCOUT	Fast carry out

1. If Set/Reset is not used, then the flip-flop is never set/reset, except when cleared immediately after configuration.

## Routing

There are many resources provided in the iCE40 devices to route signals individually with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PLB connections are made with three different types of routing resources: Adjacent (spans two PLBs), x4 (spans five PLBs) and x12 (spans thirteen PLBs). The Adjacent, x4 and x12 connections provide fast and efficient connections in the diagonal, horizontal and vertical directions.

The design tool takes the output of the synthesis tool and places and routes the design.

## Clock/Control Distribution Network

Each iCE40 device has eight global inputs, two pins on each side of the device. Note that not all GBINs are available in all packages.

These global inputs can be used as high fanout nets, clock, reset or enable signals. The dedicated global pins are identified as GBIN[7:0] and the global buffers are identified as-GBUF[7:0]. These eight inputs may be used as general purpose I/O if they are not used to drive the clock nets. Global buffer GBUF7 in I/O Bank 3 also provides an optional direct LVDS25 or subLVDS differential clock input.

Table 2-2 lists the connections between a specific global buffer and the inputs on a PLB. All global buffers optionally connect to the PLB CLK input. Any four of the eight global buffers can drive logic inputs to a PLB. Even-numbered global buffers optionally drive the Set/Reset input to a PLB. Similarly, odd-numbered buffers optionally drive the PLB clock-enable input.

**Table 2-2. Global Buffer (GBUF) Connections to Programmable Logic Blocks**

Global Buffer	LUT Inputs	Clock	Reset	Clock Enable
GBUF0	Yes, any 4 of 8 GBUF Inputs	Yes	Yes	
GBUF1		Yes		Yes
GBUF2		Yes	Yes	
GBUF3		Yes		Yes
GBUF4		Yes	Yes	
GBUF5		Yes		Yes
GBUF6		Yes	Yes	
GBUF7		Yes		Yes

The maximum frequency for the global buffers are shown in the iCE40 External Switching Characteristics tables later in this document.

## Global Hi-Z Control

The global high-impedance control signal, GHIZ, connects to all I/O pins on the iCE40 device. This GHIZ signal is automatically asserted throughout the configuration process, forcing all user I/O pins into their high-impedance state.

## sysIO

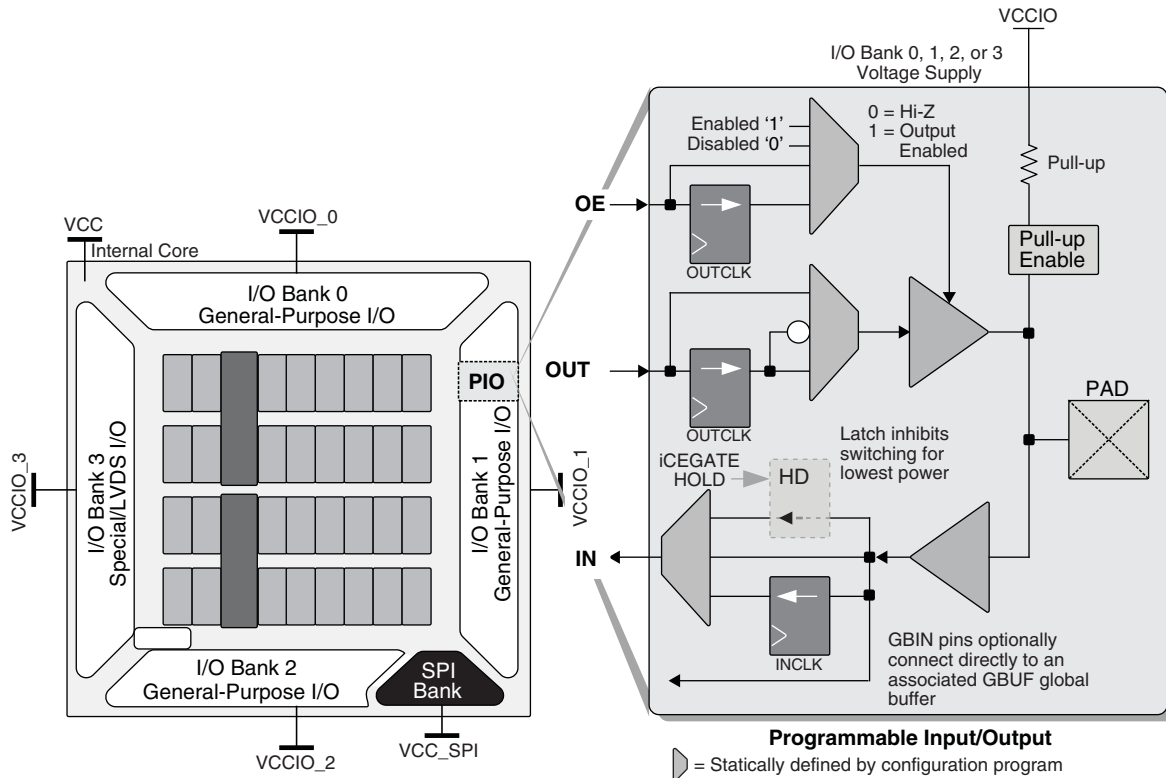
### Buffer Banks

iCE40 devices have up to four I/O banks with independent  $V_{CCIO}$  rails with an additional configuration bank  $V_{CC\_SPI}$  for the SPI I/Os.

### Programmable I/O (PIO)

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysIO buffers and pads. The PIOs are placed on all four sides of the device.

**Figure 2-5. I/O Bank and Programmable I/O Cell**



The PIO contains three blocks: an input register block, output register block iCEgate™ and tri-state register block. To save power, the optional iCEgate™ latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Note that the freeze signal is common to the bank. These blocks can operate in a variety of modes along with the necessary clock and selection logic.

### Input Register Block

The input register blocks for the PIOs on all edges contain registers that can be used to condition high-speed interface signals before they are passed to the device core. In Generic DDR mode, two registers are used to sample the data on the positive and negative edges of the system clock signal, creating two data streams.

### Output Register Block

The output register block can optionally register signals from the core of the device before they are passed to the sysIO buffers. In Generic DDR mode, two registers are used to capture the data on the positive and negative edge of the system clock and then muxed creating one data stream.

Figure 2-6 shows the input/output register block for the PIOs.

Figure 2-6. iCE I/O Register Block Diagram

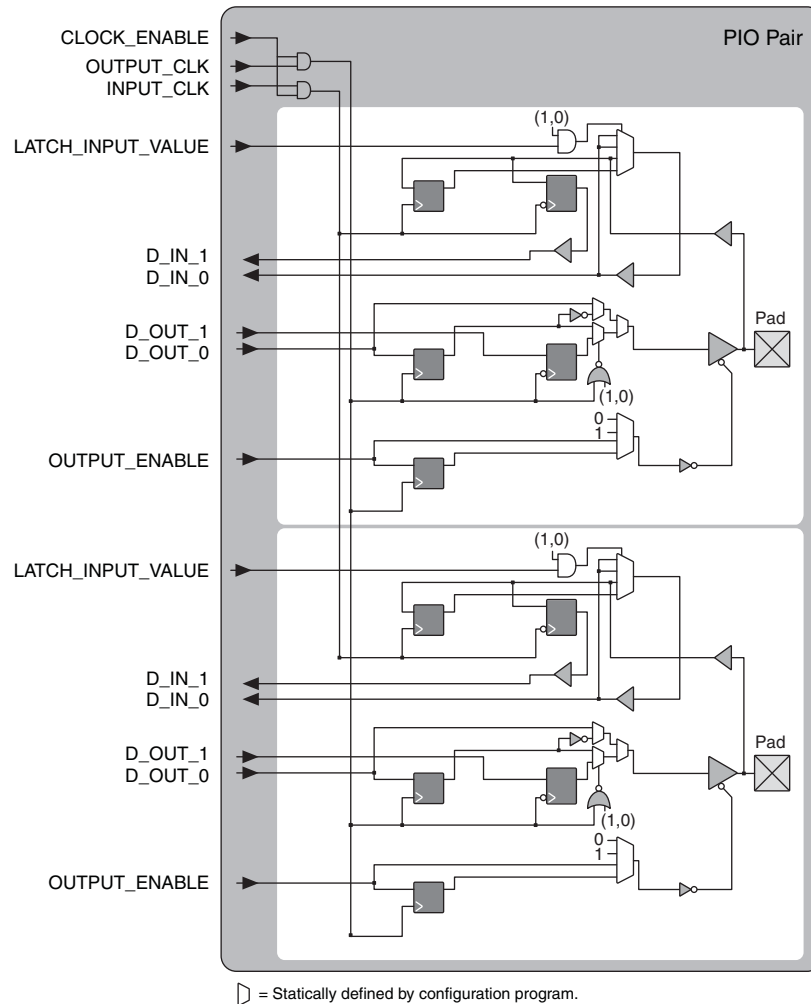


Table 2-6. PIO Signal List

Pin Name	I/O Type	Description
OUTPUT_CLK	Input	Output register clock
CLOCK_ENABLE	Input	Clock enable
INPUT_CLK	Input	Input register clock
OUTPUT_ENABLE	Input	Output enable
D_OUT_0/1	Input	Data from the core
D_IN_0/1	Output	Data to the core
LATCH_INPUT_VALUE	Input	Latches/holds the Input Value

### sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysIO buffers allow users to implement a wide variety of standards that are found in today's systems including LVCMOS and LVDS25.

High Current LED Drivers combine three sysIO buffers together. This allows for programmable drive strength. This also allows for high current drivers that are ideal to drive three white LEDs, or one RGB LED. Each bank is capable of supporting multiple I/O standards including single-ended LVCMOS buffers and differential LVDS25E output buf-



fers. Bank 3 additionally supports differential LVDS25 input buffers. Each sysIO bank has its own dedicated power supply.

**Typical I/O Behavior During Power-up**

The internal power-on-reset (POR) signal is deactivated when  $V_{CC}$ ,  $V_{CCIO\_2}$ ,  $V_{PP\_2V5}$ , and  $V_{CC\_SPI}$  have reached the level defined in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user’s responsibility to ensure that all  $V_{CCIO}$  banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. The default configuration of the I/O pins in a device prior to configuration is tri-stated with a weak pull-up to  $V_{CCIO}$ . The I/O pins will maintain the pre-configuration state until  $V_{CC}$  and  $V_{CCIO}$  (for I/O banks containing configuration I/Os) have reached levels, at which time the I/Os will take on the software user-configured settings only after a proper download/configuration. Unused IOs are automatically blocked and the pullup termination is disabled.

**Supported Standards**

The iCE40 sysIO buffer supports both single-ended and differential input standards. The single-ended standard supported is LVCMOS. The buffer supports the LVCMOS 1.8, 2.5, and 3.3 V standards. The buffer has individually configurable options for bus maintenance (weak pull-up or none). The High Current output buffer have individually configurable options for drive strength.

Table 2-7 and Table 2-8 show the I/O standards (together with their supply and reference voltages) supported by the iCE40 devices.

**Table 2-7. Supported Input Standards**

Input Standard	$V_{CCIO}$ (Typical)		
	3.3 V	2.5 V	1.8 V
<b>Single-Ended Interfaces</b>			
LVCMOS33	Yes		
LVCMOS25		Yes	
LVCMOS18			Yes
<b>Differential Interfaces</b>			
LVDS25 <sup>1</sup>		Yes	
subLVDS <sup>1</sup>			Yes

1. Bank 3 only.

**Table 2-8. Supported Output Standards**

Output Standard	$V_{CCIO}$ (Typical)
<b>Single-Ended Interfaces</b>	
LVCMOS33	3.3
LVCMOS25	2.5
LVCMOS18	1.8
<b>Differential Interfaces</b>	
LVDS25E <sup>1</sup>	2.5
subLVDSE <sup>1</sup>	1.8

1. These interfaces can be emulated with external resistors in all devices.

**Non-Volatile Configuration Memory**

All iCE40 devices provide a Non-Volatile Configuration Memory (NVCM) block which can be used to configure the device.

For more information on the NVCM, please refer to TN1248, [iCE40 Programming and Configuration Usage Guide](#).

## Power On Reset

iCE40 devices have power-on reset circuitry to monitor  $V_{CC}$ ,  $V_{CCIO\_2}$ ,  $V_{PP\_2V5}$ , and  $V_{CC\_SPI}$  voltage levels during power-up and operation. At power-up, the POR circuitry monitors  $V_{CC}$ ,  $V_{CCIO\_2}$ ,  $V_{PP\_2V5}$ , and  $V_{CC\_SPI}$  (controls configuration) voltage levels. It then triggers download from the on-chip NVCM or external Flash memory after reaching the power-up levels specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. Before and during configuration, the I/Os are held in tri-state. I/Os are released to user functionality once the device has finished configuration.

## Programming and Configuration

This section describes the programming and configuration of the iCE40 family.

### Device Programming

The NVCM memory can be programmed through the SPI port.

### Device Configuration

There are various ways to configure the Configuration RAM (CRAM) including:

1. Internal NVCM Download
2. From a SPI Flash (Master SPI mode)
3. System microprocessor to drive a Serial Slave SPI port (SSPI mode)

The image to configure the CRAM can be selected by the user on power up (Cold Boot) or once powered up (Warm Boot).

For more details on programming and configuration, see TN1248, [iCE40 Programming and Configuration Usage Guide](#).

## Power Saving Options

iCE40 devices are available in two options for maximum flexibility: LP and HX devices. The LP devices have ultra low static and dynamic power consumption. HX devices are designed to provide high performance. Both the LP and the HX devices operate at 1.2 V  $V_{CC}$ .

iCE40 devices feature iCEGate and PLL low power mode to allow users to meet the static and dynamic power requirements of their applications. While these features are available in both device types, these features are mainly intended for use with iCE40 LP devices to manage power consumption.

**Table 2-9. iCE40 Power Saving Features Description**

Device Subsystem	Feature Description
PLL	When LATCHINPUTVALUE is enabled, forces the PLL into low-power mode; PLL output held static at last input clock value.
iCEGate	To save power, the optional iCEgate latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Registered inputs are effectively frozen by their associated clock or clock-enable control.

## Peak Startup Supply Current – HX Devices

Symbol	Parameter	Device	Max	Units
$I_{CCPEAK}$	Core Power Supply	iCE40HX1K	6.9	mA
		iCE40HX4K	22.3	mA
		iCE40HX8K	22.3	mA
$I_{CCPLLPEAK}^1$	PLL Power Supply	iCE40HX1K	1.8	mA
		iCE40HX4K	6.4	mA
		iCE40HX8K	6.4	mA
$I_{PP\_2V5PEAK}$	NVCM Power Supply	iCE40HX1K	2.8	mA
		iCE40HX4K	4.1	mA
		iCE40HX8K	4.1	mA
$I_{CCIOPEAK}, I_{CC\_SPIPEAK}$	Bank Power Supply	iCE40HX1K	6.8	mA
		iCE40HX4K	6.8	mA
		iCE40HX8K	6.8	mA

1.  $V_{CCPLL}$  is tied to  $V_{CC}$  internally in packages without PLLs pins.

## sysIO Recommended Operating Conditions

Standard	$V_{CCIO}$ (V)		
	Min.	Typ.	Max.
LVC MOS 3.3	3.14	3.3	3.46
LVC MOS 2.5	2.37	2.5	2.62
LVC MOS 1.8	1.71	1.8	1.89
LVDS25E <sup>1,2</sup>	2.37	2.5	2.62
subLV DSE <sup>1,2</sup>	1.71	1.8	1.89

1. Inputs on-chip. Outputs are implemented with the addition of external resistors.

2. Does not apply to Configuration Bank  $V_{CC\_SPI}$ .

## sysIO Single-Ended DC Electrical Characteristics

Input/ Output Standard	$V_{IL}$		$V_{IH}^1$		$V_{OL}$ Max. (V)	$V_{OH}$ Min. (V)	$I_{OL}$ Max. (mA)	$I_{OH}$ Max. (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVC MOS 3.3	-0.3	0.8	2.0	$V_{CCIO} + 0.2$ V	0.4	$V_{CCIO} - 0.4$	8, 16 <sup>2</sup> , 24 <sup>2</sup>	-8, -16 <sup>2</sup> , -24 <sup>2</sup>
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVC MOS 2.5	-0.3	0.7	1.7	$V_{CCIO} + 0.2$ V	0.4	$V_{CCIO} - 0.4$	6, 12 <sup>2</sup> , 18 <sup>2</sup>	-6, -12 <sup>2</sup> , -18 <sup>2</sup>
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVC MOS 1.8	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	$V_{CCIO} + 0.2$ V	0.4	$V_{CCIO} - 0.4$	4, 8 <sup>2</sup> , 12 <sup>2</sup>	-4, -8 <sup>2</sup> , -12 <sup>2</sup>
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1

1. Some products are clamped to a diode when  $V_{IN}$  is larger than  $V_{CCIO}$ .

2. Only for High Drive LED outputs.

## LVDS25E Emulation

iCE40 devices can support LVDS25E outputs via emulation on all banks. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all devices. The scheme shown in Figure 3-1 is one possible solution for LVDS25E standard implementation. Resistor values in Figure 3-1 are industry standard values for 1% resistors.

Figure 3-1. LVDS25E Using External Resistors

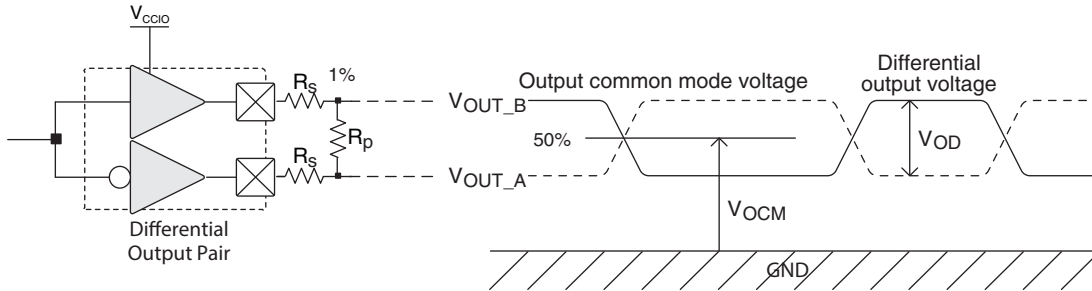


Table 3-1. LVDS25E DC Conditions

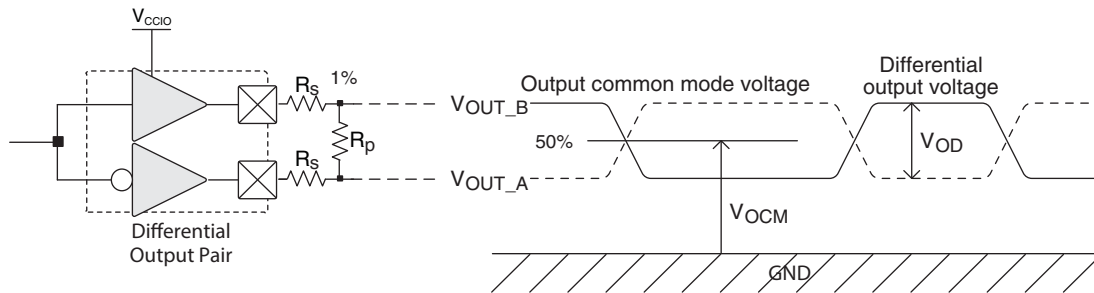
### Over Recommended Operating Conditions

Parameter	Description	Typ.	Units
Z <sub>OUT</sub>	Output impedance	20	Ohms
R <sub>S</sub>	Driver series resistor	150	Ohms
R <sub>P</sub>	Driver parallel resistor	140	Ohms
R <sub>T</sub>	Receiver termination	100	Ohms
V <sub>OH</sub>	Output high voltage	1.43	V
V <sub>OL</sub>	Output low voltage	1.07	V
V <sub>OD</sub>	Output differential voltage	0.30	V
V <sub>CM</sub>	Output common mode voltage	1.25	V
Z <sub>BACK</sub>	Back impedance	100.5	Ohms
I <sub>DC</sub>	DC output current	6.03	mA

## SubLVDS Emulation

The iCE40 family supports the differential subLVDS standard. The output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all banks of the devices. The subLVDS input standard is supported by the LVDS25 differential input buffer. The scheme shown in Figure 3-2 is one possible solution for subLVDS output standard implementation. Use LVDS25E mode with suggested resistors for subLVDS operation. Resistor values in Figure 3-2 are industry standard values for 1% resistors.

**Figure 3-2. subLVDS**



**Table 3-2. subLVDS DC Conditions**

### Over Recommended Operating Conditions

Parameter	Description	Typ.	Units
Z <sub>OUT</sub>	Output impedance	20	Ohms
R <sub>S</sub>	Driver series resistor	270	Ohms
R <sub>P</sub>	Driver parallel resistor	120	Ohms
R <sub>T</sub>	Receiver termination	100	Ohms
V <sub>OH</sub>	Output high voltage	1.43	V
V <sub>OL</sub>	Output low voltage	1.07	V
V <sub>OD</sub>	Output differential voltage	0.35	V
V <sub>CM</sub>	Output common mode voltage	0.9	V
Z <sub>BACK</sub>	Back impedance	100.5	Ohms
I <sub>DC</sub>	DC output current	2.8	mA

**iCE40 External Switching Characteristics – LP Devices** <sup>1, 2</sup>

Over Recommended Operating Conditions

Parameter	Description	Device	Min.	Max.	Units
<b>Clocks</b>					
<b>Global Clocks</b>					
f <sub>MAX_GBUF</sub>	Frequency for Global Buffer Clock network	All iCE40LP devices	—	275	MHz
t <sub>W_GBUF</sub>	Clock Pulse Width for Global Buffer	All iCE40LP devices	0.92	—	ns
t <sub>SKEW_GBUF</sub>	Global Buffer Clock Skew Within a Device	iCE40LP384	—	370	ps
		iCE40LP640	—	230	ps
		iCE40LP1K	—	230	ps
		iCE40LP4K	—	340	ps
		iCE40LP8K	—	340	ps
<b>Pin-LUT-Pin Propagation Delay</b>					
t <sub>PD</sub>	Best case propagation delay through one LUT-4	All iCE40LP devices	—	9.36	ns
<b>General I/O Pin Parameters (Using Global Buffer Clock without PLL)<sup>3</sup></b>					
t <sub>SKEW_IO</sub>	Data bus skew across a bank of IOs	iCE40LP384	—	300	ps
		iCE40LP640	—	200	ps
		iCE40LP1K	—	200	ps
		iCE40LP4K	—	280	ps
		iCE40LP8K	—	280	ps
t <sub>CO</sub>	Clock to Output - PIO Output Register	iCE40LP384	—	6.33	ns
		iCE40LP640	—	5.91	ns
		iCE40LP1K	—	5.91	ns
		iCE40LP4K	—	6.58	ns
		iCE40LP8K	—	6.58	ns
t <sub>SU</sub>	Clock to Data Setup - PIO Input Register	iCE40LP384	-0.08	—	ns
		iCE40LP640	-0.33	—	ns
		iCE40LP1K	-0.33	—	ns
		iCE40LP4K	-0.63	—	ns
		iCE40LP8K	-0.63	—	ns
t <sub>H</sub>	Clock to Data Hold - PIO Input Register	iCE40LP384	1.99	—	ns
		iCE40LP640	2.81	—	ns
		iCE40LP1K	2.81	—	ns
		iCE40LP4K	3.48	—	ns
		iCE40LP8K	3.48	—	ns
<b>General I/O Pin Parameters (Using Global Buffer Clock with PLL)<sup>3</sup></b>					
t <sub>COPLL</sub>	Clock to Output - PIO Output Register	iCE40LP1K	—	2.20	ns
		iCE40LP4K	—	2.30	ns
		iCE40LP8K	—	2.30	ns
t <sub>SUPLL</sub>	Clock to Data Setup - PIO Input Register	iCE40LP1K	5.23	—	ns
		iCE40LP4K	6.13	—	ns
		iCE40LP8K	6.13	—	ns

## sysCLOCK PLL Timing

### Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Min.	Max.	Units
$f_{IN}$	Input Clock Frequency (REFERENCECLK, EXTFEEDBACK)		10	133	MHz
$f_{OUT}$	Output Clock Frequency (PLLOUT)		16	275	MHz
$f_{VCO}$	PLL VCO Frequency		533	1066	MHz
$f_{PFD}$	Phase Detector Input Frequency		10	133	MHz
<b>AC Characteristics</b>					
$t_{DT}$	Output Clock Duty Cycle	$f_{OUT} < 175$ MHz	40	50	%
		175 MHz < $f_{OUT} < 275$ MHz	35	65	"%
$t_{PH}$	Output Phase Accuracy		—	+/-12	deg
$t_{OPJIT}^{1,5}$	Output Clock Period Jitter	$f_{OUT} \leq 100$ MHz	—	450	ps p-p
		$f_{OUT} > 100$ MHz	—	0.05	UIPP
	Output Clock Cycle-to-cycle Jitter	$f_{OUT} \leq 100$ MHz	—	750	ps p-p
		$f_{OUT} > 100$ MHz	—	0.10	UIPP
	Output Clock Phase Jitter	$f_{PFD} \leq 25$ MHz	—	275	ps p-p
		$f_{PFD} > 25$ MHz	—	0.05	UIPP
$t_W$	Output Clock Pulse Width	At 90% or 10%	1.3	—	ns
$t_{LOCK}^{2,3}$	PLL Lock-in Time		—	50	us
$t_{UNLOCK}$	PLL Unlock Time		—	50	ns
$t_{IPJIT}^4$	Input Clock Period Jitter	$f_{PFD} \geq 20$ MHz	—	1000	ps p-p
		$f_{PFD} < 20$ MHz	—	0.02	UIPP
$t_{FDTAP}$	Fine Delay adjustment, per Tap		147	195	ps
$t_{STABLE}^3$	LATCHINPUTVALUE LOW to PLL Stable		—	500	ns
$t_{STABLE\_PW}^3$	LATCHINPUTVALUE Pulse Width		—	100	ns
$t_{RST}$	RESET Pulse Width		10	—	ns
$t_{RSTREC}$	RESET Recovery Time		10	—	us
$t_{DYNAMIC\_WD}$	DYNAMICDELAY Pulse Width		100	—	VCO Cycles
$t_{PDBYPASS}$	Propagation delay with the PLL in bypass mode	iCE40LP	1.18	4.68	ns
		iCE40HX	1.73	4.07	ns

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.
2. Output clock is valid after  $t_{LOCK}$  for PLL reset and dynamic delay adjustment.
3. At minimum  $f_{PFD}$ . As the  $f_{PFD}$  increases the time will decrease to approximately 60% the value listed.
4. Maximum limit to prevent PLL unlock from occurring. Does not imply the PLL will operate within the output specifications listed in this table.
5. The jitter values will increase with loading of the PLD fabric and in the presence of SSO noise.

### sysCONFIG Port Timing Specifications<sup>1</sup>

Symbol	Parameter		Min.	Typ.	Max.	Units
<b>All Configuration Modes</b>						
t <sub>CRESET_B</sub>	Minimum CRESET_B Low pulse width required to restart configuration, from falling edge to rising edge		200	—	—	ns
t <sub>DONE_IO</sub>	Number of configuration clock cycles after CDONE goes High before the PIO pins are activated		49	—	—	Clock Cycles
<b>Slave SPI</b>						
t <sub>CR_SCK</sub>	Minimum time from a rising edge on CRESET_B until the first SPI write operation, first SPI_SCK. During this time, the iCE40 device is clearing its internal configuration memory	iCE40LP384	600	-	—	us
		iCE40LP640, iCE40LP/HX1K	800	-	—	us
		iCE40LP/HX4K	1200	-	—	us
		iCE40LP/HX8K	1200	-	—	us
f <sub>MAX</sub> <sup>1</sup>	CCLK clock frequency	Write	1	-	25	MHz
		Read iCE40LP384 <sup>2</sup>	-	15	-	MHz
		Read iCE40LP640, iCE40LP/HX1K <sup>2</sup>	-	15	-	MHz
		Read iCE40LP/HX4K <sup>2</sup>	-	15	-	MHz
		Read iCE40LP/HX8K <sup>2</sup>	-	15	-	MHz
t <sub>CCLKH</sub>	CCLK clock pulse width high		20	—	—	ns
t <sub>CCLKL</sub>	CCLK clock pulse width low		20	—	—	ns
t <sub>STSU</sub>	CCLK setup time		12	—	—	ns
t <sub>STH</sub>	CCLK hold time		12	—	—	ns
t <sub>STCO</sub>	CCLK falling edge to valid output		13	—	—	ns
<b>Master SPI</b>						
f <sub>MCLK</sub>	MCLK clock frequency	Off	—	0	—	MHz
		Low Frequency (Default)	—	7.5	—	MHz
		Medium Frequency <sup>3</sup>	—	24	—	MHz
		High Frequency <sup>3</sup>	—	40	—	MHz



**sysCONFIG Port Timing Specifications<sup>1</sup> (Continued)**

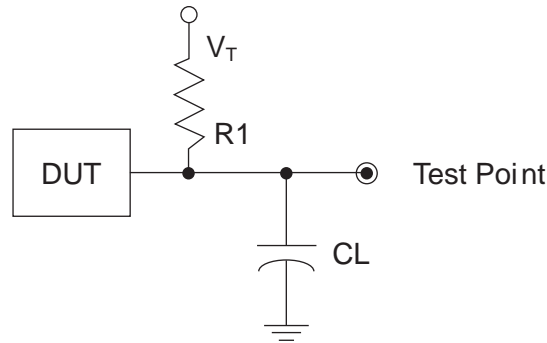
Symbol	Parameter		Min.	Typ.	Max.	Units
t <sub>MCLK</sub>	CRESET_B high to first MCLK edge	iCE40LP384 - Low Frequency (Default)	600	—	—	us
		iCE40LP384 - Medium Frequency	600	—	—	us
		iCE40LP384 - High Frequency	600	—	—	us
		iCE40LP640, iCE40LP/HX1K - Low Frequency (Default)	800	—	—	us
		iCE40LP640, iCE40LP/HX1K - Medium Frequency	800	—	—	us
		iCE40LP640, iCE40LP/HX1K - High Frequency	800	—	—	us
		iCE40LP/HX1K - Low Frequency (Default)	800	—	—	us
		iCE40LP/HX1K - Medium Frequency	800	—	—	us
		iCE40LP/HX1K - High Frequency	800	—	—	us
		iCE40LP/HX4K - Low Frequency (Default)	1200	—	—	us
		iCE40LP/HX4K - Medium Frequency	1200	—	—	us
		iCE40LP/HX4K - high frequency	1200	—	—	us
		iCE40LP/HX8K - Low Frequency (Default)	1200	—	—	us
		iCE40LP/HX8K - Medium Frequency	1200	—	—	us
		iCE40LP/HX8K - High Frequency	1200	—	—	us

1. Does not apply for NVCM.
2. Supported only with 1.2 V V<sub>CC</sub> and at 25 °C.
3. Extended range f<sub>MAX</sub> Write operations support up to 53 MHz only with 1.2 V V<sub>CC</sub> and at 25 °C.

## Switching Test Conditions

Figure 3-3 shows the output test load used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-3.

**Figure 3-3. Output Test Load, LVCMOS Standards**



**Table 3-3. Test Fixture Required Components, Non-Terminated Interfaces**

Test Condition	R <sub>1</sub>	C <sub>L</sub>	Timing Reference	V <sub>T</sub>
LVCMOS settings (L -> H, H -> L)	∞	0 pF	LVCMOS 3.3 = 1.5 V	—
			LVCMOS 2.5 = V <sub>CCIO</sub> /2	—
			LVCMOS 1.8 = V <sub>CCIO</sub> /2	—
LVCMOS 3.3 (Z -> H)	188	0 pF	1.5	V <sub>OL</sub>
LVCMOS 3.3 (Z -> L)			1.5	V <sub>OH</sub>
Other LVCMOS (Z -> H)			V <sub>CCIO</sub> /2	V <sub>OL</sub>
Other LVCMOS (Z -> L)			V <sub>CCIO</sub> /2	V <sub>OH</sub>
LVCMOS (H -> Z)			V <sub>OH</sub> - 0.15	V <sub>OL</sub>
LVCMOS (L -> Z)			V <sub>OL</sub> - 0.15	V <sub>OH</sub>

Note: Output test conditions for all other interfaces are determined by the respective standards.

Part Number	LUTs	Supply Voltage	Package	Leads	Temp.
ICE40LP8K-CM121TR1K	7680	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP8K-CM225	7680	1.2 V	Halogen-Free ucBGA	225	IND

**High-Performance Industrial Grade Devices, Halogen Free (RoHS) Packaging**

Part Number	LUTs	Supply Voltage	Package	Leads	Temp.
ICE40HX1K-CB132	1280	1.2 V	Halogen-Free csBGA	132	IND
ICE40HX1K-VQ100	1280	1.2 V	Halogen-Free VQFP	100	IND
ICE40HX1K-TQ144	1280	1.2 V	Halogen-Free TQFP	144	IND
ICE40HX4K-BG121	3520	1.2 V	Halogen-Free caBGA	121	IND
ICE40HX4K-BG121TR	3520	1.2 V	Halogen-Free caBGA	121	IND
ICE40HX4K-CB132	3520	1.2 V	Halogen-Free csBGA	132	IND
ICE40HX4K-TQ144	3520	1.2 V	Halogen-Free TQFP	144	IND
ICE40HX8K-BG121	7680	1.2 V	Halogen-Free caBGA	121	IND
ICE40HX8K-BG121TR	7680	1.2 V	Halogen-Free caBGA	121	IND
ICE40HX8K-CB132	7680	1.2 V	Halogen-Free csBGA	132	IND
ICE40HX8K-CM225	7680	1.2 V	Halogen-Free ucBGA	225	IND
ICE40HX8K-CT256	7680	1.2 V	Halogen-Free caBGA	256	IND

Date	Version	Section	Change Summary
March 2017	3.3	Introduction	Updated <a href="#">Features</a> section. Added 121-ball caBGA package for ICE40 HX4K/8K to Table 1-1, iCE40 Family Selection Guide.
		Architecture	Updated <a href="#">PLB Blocks</a> section. Changed “subtractors” to “subtractors” in the Carry Logic description.
			Updated <a href="#">Clock/Control Distribution Network</a> section. Switched the “Clock Enable” and the “Reset” headings in Table 2-2, Global Buffer (GBUF) Connections to Programmable Logic Blocks.
		Pinout Information	Updated <a href="#">Pin Information Summary</a> section. Added BG121 information under iCE40HX4K and iCE40HX8K.
		Ordering Information	Updated <a href="#">iCE40 Part Number Description</a> section. Added Shipping Method and BG121 package under High Performance (HX) Devices.
			Updated <a href="#">Ordering Information</a> section. Added part numbers for BG121 under High-Performance Industrial Grade Devices, Halogen Free (RoHS) Packaging.
Supplemental Information	Corrected reference to “Package Diagrams Data Sheet”.		
October 2015	3.2	Introduction	Updated Features section. Added footnote to 16 WLCSP Programmable I/O: Max Inputs (LVDS25) in Table 1-1, iCE40 Family Selection Guide.
		DC and Switching Characteristics	Updated sysCLOCK PLL Timing section. Changed $t_{DT}$ conditions. Updated Programming NVCM Supply Current – LP Devices section. Changed $I_{PP\_2V5}$ and $I_{CCIO}$ , $I_{CC\_SPI}$ units.
March 2015	3.1	DC and Switching Characteristics	Updated sysIO Single-Ended DC Electrical Characteristics section. Changed LVCMOS 3.3 and LVCMOS 2.5 $V_{OH}$ Min. (V) from 0.5 to 0.4.
July 2014	3.0	DC and Switching Characteristics	Revised and/or added Typ. $V_{CC}$ data in the following sections. — Static Supply Current – LP Devices — Static Supply Current – HX Devices — Programming NVCM Supply Current – LP Devices — Programming NVCM Supply Current – HX Devices In each section table, the footnote indicating Advanced device status was removed.
		Pinout Information	Updated Pin Information Summary section. Added footnote 1 to CM49 under iCE40LP1K.
April 2014	02.9	Ordering Information	Changed “I” to “l” in part number description and ordering part numbers.
			Added part numbers to the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging table.

Date	Version	Section	Change Summary
February 2014	02.8	Introduction	Updated Features section. — Corrected standby power units. — Included High Current LED Drivers
			Updated Table 1-1, iCE40 Family Selection Guide. — Removed LP384 Programmable I/O for 81 ucBGA package.
		Architecture	Updated Supported Standards section. Added information on High Current LED drivers.
		DC and Switching Characteristics	Corrected typos.
			Added footnote to the Peak Startup Supply Current – LP Devices table.
Ordering Information	Updated part number description in the Ultra Low Power (LP) Devices section.		
	Added part numbers to the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging table.		
October 2013	02.7	Introduction	Updated Features list and iCE40 Family Selection Guide table.
		Architecture	Revised iCE40-1K device to iCE40LP/HX1K device.
		DC and Switching Characteristics	Added iCE40LP640 device information.
		Pinout Information	Added iCE40LP640 and iCE40LP1K information.
		Ordering Information	Added iCE40LP640 and iCE40LP1K information.
September 2013	02.6	DC and Switching Characteristics	Updated Absolute Maximum Ratings section.
			Updated sysCLOCK PLL Timing – Preliminary table.
		Pinout Information	Updated Pin Information Summary table.
August 2013	02.5	Introduction	Updated the iCE40 Family Selection Guide table.
		DC and Switching Characteristics	Updated the following tables: — Absolute Maximum Ratings — Power-On-Reset Voltage Levels — Static Supply Current – LP Devices — Static Supply Current – HX Devices — Programming NVCM Supply Current – LP Devices — Programming NVCM Supply Current – HX Devices — Peak Startup Supply Current – LP Devices — sysIO Recommended Operating Conditions — Typical Building Block Function Performance – HX Devices — iCE40 External Switching Characteristics – HX Devices — sysCLOCK PLL Timing – Preliminary — SPI Master or NVCM Configuration Time
			Pinout Information
July 2013	02.4	Introduction	Updated the iCE40 Family Selection Guide table.
		DC and Switching Characteristics	Updated the sysCONFIG Port Timing Specifications table.
			Updated footnote in DC Electrical Characteristics table.
			GDDR tables removed. Support to be provided in a technical note.
		Pinout Information	Updated the Pin Information Summary table.
Ordering Information	Updated the top-side markings figure.		
	Updated the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging table.		
May 2013	02.3	DC and Switching Characteristics	Added new data from Characterization.