# Lattice Semiconductor Corporation - ICE40LP8K-CM121TR Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 960 |
| Number of Logic Elements/Cells | 7680 |
| Total RAM Bits | 131072 |
| Number of I/O | 93 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 121-VFBGA |
| Supplier Device Package | 121-UCBGA (5x5) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/ice40lp8k-cm121tr |

*Table 1-1. iCE40 Family Selection Guide (continued)*

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 84 QFN<br>(7 mm x 7 mm, 0.5 mm) | QN84 | | | 67(7)[1] | | | | | |
| 100 VQFP<br>(14 mm x 14 mm, 0.5 mm) | VQ100 | | | | | | 72(9)[1] | | |
| 121 ucBGA<br>(5 mm x 5 mm, 0.4 mm) | CM121 | | | 95(12) | 93(13) | 93(13) | | | |
| 121 csBGA<br>(6 mm x 6 mm, 0.5 mm) | CB121 | | | 92(12) | | | | | |
| 121 caBGA<br>(9 mm x 9 mm, 0.8 mm) | BG121 | | | | | | | 93(13) | 93(13) |
| 132 csBGA<br>(8 mm x 8 mm, 0.5 mm) | CB132 | | | | | | 95(11) | 95(12) | 95(12) |
| 144 TQFP<br>(20 mm x 20 mm, 0.5 mm) | TQ144 | | | | | | 96(12) | 107(14) | |
| 225 ucBGA<br>(7 mm x 7 mm, 0.4 mm) | CM225 | | | | 178(23) | 178(23) | | | 178(23) |
| 256-ball caBGA<br>(14 mm x 14 mm, 0.8 mm) | CT256 | | | | | | | | 206(26) |

1. No PLL available on the 16 WLCSP, 36 ucBGA, 81 csBGA, 84 QFN and 100 VQFP packages.
2. Only one PLL available on the 81 ucBGA package.
3. High Current I/Os only available on the 16 WLCSP package.

## Introduction

The iCE40 family of ultra-low power, non-volatile FPGAs has five devices with densities ranging from 384 to 7680 Look-Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic, these devices feature Embedded Block RAM (EBR), Non-volatile Configuration Memory (NVCM) and Phase Locked Loops (PLLs). These features allow the devices to be used in low-cost, high-volume consumer and system applications. Select packages offer High-Current drivers that are ideal to drive three white LEDs, or one RGB LED.

The iCE40 devices are fabricated on a 40 nm CMOS low power process. The device architecture has several features such as programmable low-swing differential I/Os and the ability to turn off on-chip PLLs dynamically. These features help manage static and dynamic power consumption, resulting in low static power for all members of the family. The iCE40 devices are available in two versions – ultra low power (LP) and high performance (HX) devices.

The iCE40 FPGAs are available in a broad range of advanced halogen-free packages ranging from the space saving 1.40x1.48 mm WLCSP to the PCB-friendly 20x20 mm TQFP. Table 1-1 shows the LUT densities, package and I/O options, along with other key parameters.

The iCE40 devices offer enhanced I/O features such as pull-up resistors. Pull-up features are controllable on a “per-pin” basis.

The iCE40 devices also provide flexible, reliable and secure configuration from on-chip NVCM. These devices can also configure themselves from external SPI Flash or be configured by an external master such as a CPU.

Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the iCE40 family of devices. Popular logic synthesis tools provide synthesis library support for iCE40. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the iCE40 device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules, including a number of reference designs, licensed free of charge, optimized for the iCE40 FPGA family. By using these configurable soft core IP cores as standardized blocks, users are free to concentrate on the unique aspects of their design, increasing their productivity.

### Global Reset Control

The global reset control signal connects to all PLB and PIO flip-flops on the iCE40 device. The global reset signal is automatically asserted throughout the configuration process, forcing all flip-flops to their defined wake-up state. For PLB flip-flops, the wake-up state is always reset, regardless of the PLB flip-flop primitive used in the application.

## sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The iCE40 devices have one or more sysCLOCK PLLs. REFERENCECLK is the reference frequency input to the PLL and its source can come from an external I/O pin or from internal routing. EXTFEEDBACK is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The PLLOUT output has an output divider, thus allowing the PLL to generate different frequencies for each output. The output divider can have a value from 1 to 6. The PLLOUT outputs can all be used to drive the iCE40 global clock network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 2-3.

The timing of the device registers can be optimized by programming a phase shift into the PLLOUT output clock which will advance or delay the output clock with reference to the REFERENCECLK clock. This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the $t_{LOCK}$ parameter has been satisfied.

For more details on the PLL, see TN1251, iCE40 sysCLOCK PLL Design and Usage Guide.

***Figure 2-3. PLL Diagram***

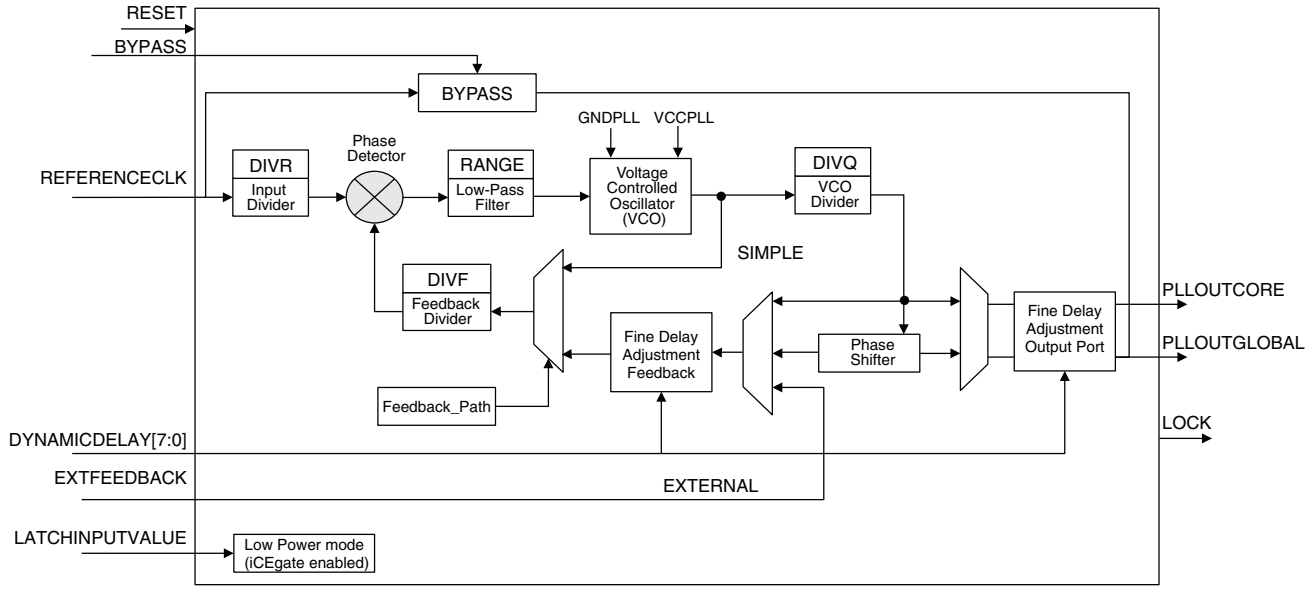


Table 2-3 provides signal descriptions of the PLL block.

### RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Note the sysMEM Embedded Block RAM Memory address 0 cannot be initialized.

### Memory Cascading

Larger and deeper blocks of RAM can be created using multiple EBR sysMEM Blocks.

### RAM4k Block

Figure 2-4 shows the 256x16 memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array.

***Figure 2-4. sysMEM Memory Primitives***

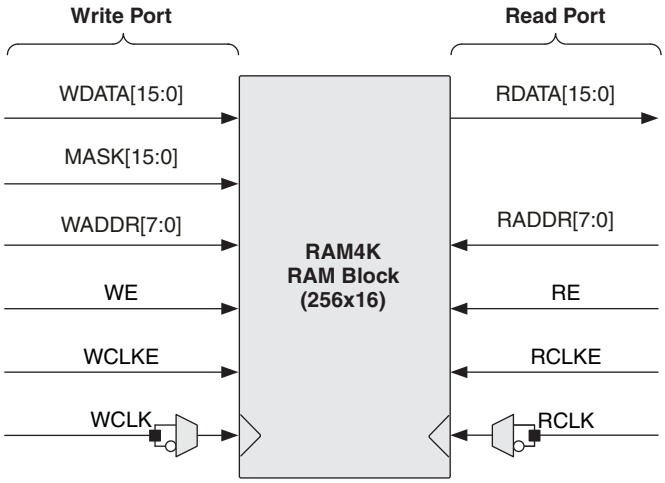


***Table 2-5. EBR Signal Descriptions***

| Signal Name | Direction | Description |
|---|---|---|
| WDATA[15:0] | Input | Write Data input. |
| MASK[15:0] | Input | Masks write operations for individual data bit-lines.<br>0 = write bit; 1 = don't write bit |
| WADDR[7:0] | Input | Write Address input. Selects one of 256 possible RAM locations. |
| WE | Input | Write Enable input. |
| WCLKE | Input | Write Clock Enable input. |
| WCLK | Input | Write Clock input. Default rising-edge, but with falling-edge option. |
| RDATA[15:0] | Output | Read Data output. |
| RADDR[7:0] | Input | Read Address input. Selects one of 256 possible RAM locations. |
| RE | Input | Read Enable input. |
| RCLKE | Input | Read Clock Enable input. |
| RCLK | Input | Read Clock input. Default rising-edge, but with falling-edge option. |

For further information on the sysMEM EBR block, please refer to TN1250, Memory Usage Guide for iCE40 Devices.

*Figure 2-6. iCE I/O Register Block Diagram*

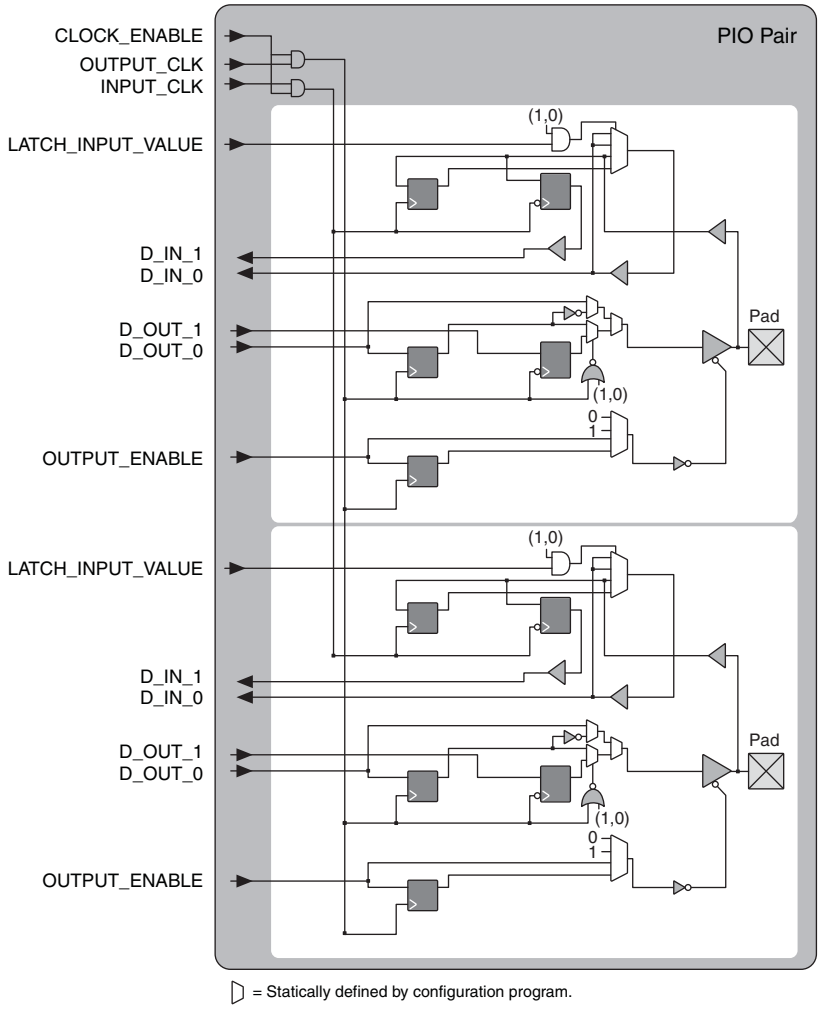


*Table 2-6. PIO Signal List*

| Pin Name | I/O Type | Description |
|---|---|---|
| OUTPUT_CLK | Input | Output register clock |
| CLOCK_ENABLE | Input | Clock enable |
| INPUT_CLK | Input | Input register clock |
| OUTPUT_ENABLE | Input | Output enable |
| D_OUT_0/1 | Input | Data from the core |
| D_IN_0/1 | Output | Data to the core |
| LATCH_INPUT_VALUE | Input | Latches/holds the Input Value |

## sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysIO buffers allow users to implement a wide variety of standards that are found in today's systems including LVCMOS and LVDS25.

High Current LED Drivers combine three sysIO buffers together. This allows for programmable drive strength. This also allows for high current drivers that are ideal to drive three white LEDs, or one RGB LED. Each bank is capable of supporting multiple I/O standards including single-ended LVCMOS buffers and differential LVDS25E output buf-

# DC Electrical Characteristics

**Over Recommended Operating Conditions**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{IL}$, $I_{IH}$ [1, 3, 4, 5, 6, 7] | Input or I/O Leakage | $0V < V_{IN} < V_{CCIO} + 0.2$ V | — | — | +/–10 | µA |
| $C_1$ [6, 7] | I/O Capacitance[2] | $V_{CCIO}$ = 3.3 V, 2.5 V, 1.8 V<br>$V_{CC}$ = Typ., $V_{IO}$ = 0 to $V_{CCIO}$ + 0.2 V | — | 6 | — | pf |
| $C_2$ [6, 7] | Global Input Buffer Capacitance[2] | $V_{CCIO}$ = 3.3 V, 2.5 V, 1.8 V<br>$V_{CC}$ = Typ., $V_{IO}$ = 0 to $V_{CCIO}$ + 0.2 V | — | 6 | — | pf |
| $V_{HYST}$ | Input Hysteresis | $V_{CCIO}$ = 1.8 V, 2.5 V, 3.3 V | — | 200 | — | mV |
| $I_{PU}$ [6, 7] | Internal PIO Pull-up Current | $V_{CCIO}$ = 1.8 V, 0=<$V_{IN}$<=0.65 $V_{CCIO}$ | –3 | — | –31 | µA |
| | | $V_{CCIO}$ = 2.5 V, 0=<$V_{IN}$<=0.65 $V_{CCIO}$ | –8 | — | –72 | µA |
| | | $V_{CCIO}$ = 3.3 V, 0=<$V_{IN}$<=0.65 $V_{CCIO}$ | –11 | — | –128 | µA |

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Internal pull-up resistors are disabled.
2. $T_J$ 25°C, f = 1.0 MHz.
3. Please refer to $V_{IL}$ and $V_{IH}$ in the sysIO Single-Ended DC Electrical Characteristics table of this document.
4. Only applies to IOs in the SPI bank following configuration.
5. Some products are clamped to a diode when $V_{IN}$ is larger than $V_{CCIO}$.
6. High current IOs has three sysIO buffers connected together.
7. The iCE40LP640 and iCE40LP1K SWG16 package has CDONE and a sysIO buffer are connected together.

# Static Supply Current – LP Devices[1, 2, 3, 4]

| Symbol | Parameter | Device | Typ. $V_{CC}$[4] | Units |
|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply | iCE40LP384 | 21 | µA |
| | | iCE40LP640 | 100 | µA |
| | | iCE40LP1K | 100 | µA |
| | | iCE40LP4K | 250 | µA |
| | | iCE40LP8K | 250 | µA |
| $I_{CCPLL}$ [5, 6] | PLL Power Supply | All devices | 0.5 | µA |
| $I_{PP\_2V5}$ | NVCM Power Supply | All devices | 1.0 | µA |
| $I_{CCIO}$, $I_{CC\_SPI}$ | Bank Power Supply[4]<br>$V_{CCIO}$ = 2.5 V | All devices | 3.5 | µA |

1. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at $V_{CCIO}$ or GND, on-chip PLL is off. For more detail with your specific design, use the Power Calculator tool. Power specified with master SPI configuration mode. Other modes may be up to 25% higher.
2. Frequency = 0 MHz.
3. $T_J$ = 25 °C, power supplies at nominal voltage.
4. Does not include pull-up.
5. No PLL available on the iCE40LP384 and iCE40LP640 device.
6. $V_{CCPLL}$ is tied to $V_{CC}$ internally in packages without PLLs pins.

## Static Supply Current – HX Devices[1, 2, 3, 4]

| Symbol | Parameter | Device | Typ. $V_{CC}$[4] | Units |
|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply | iCE40HX1K | 296 | µA |
| | | iCE40HX4K | 1140 | µA |
| | | iCE40HX8K | 1140 | µA |
| $I_{CCPLL}$[5] | PLL Power Supply | All devices | 0.5 | µA |
| $I_{PP\_2V5}$ | NVCM Power Supply | All devices | 1.0 | µA |
| $I_{CCIO}$, $I_{CC\_SPI}$ | Bank Power Supply[4] $V_{CCIO}$ = 2.5 V | All devices | 3.5 | µA |

1. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at $V_{CCIO}$ or GND, on-chip PLL is off. For more detail with your specific design, use the Power Calculator tool. Power specified with master SPI configuration mode. Other modes may be up to 25% higher.
2. Frequency = 0 MHz.
3. $T_J$ = 25 °C, power supplies at nominal voltage.
4. Does not include pull-up.
5. $V_{CCPLL}$ is tied to $V_{CC}$ internally in packages without PLLs pins.

## Programming NVCM Supply Current – LP Devices[1, 2, 3, 4]

| Symbol | Parameter | Device | Typ. $V_{CC}$[5] | Units |
|---|---|---|---|---|
| $I_{CC}$ | Core Power Supply | iCE40LP384 | 60 | µA |
| | | iCE40LP640 | 120 | µA |
| | | iCE40LP1K | 120 | µA |
| | | iCE40LP4K | 350 | µA |
| | | iCE40LP8K | 350 | µA |
| $I_{CCPLL}$[6, 7] | PLL Power Supply | All devices | 0.5 | µA |
| $I_{PP\_2V5}$ | NVCM Power Supply | All devices | 2.5 | mA |
| $I_{CCIO}$[8], $I_{CC\_SPI}$ | Bank Power Supply[5] | All devices | 3.5 | mA |

1. Assumes all inputs are held at $V_{CCIO}$ or GND and all outputs are tri-stated.
2. Typical user pattern.
3. SPI programming is at 8 MHz.
4. $T_J$ = 25 °C, power supplies at nominal voltage.
5. Per bank. $V_{CCIO}$ = 2.5 V. Does not include pull-up.
6. No PLL available on the iCE40-LP384 and iCE40-LP640 device.
7. $V_{CCPLL}$ is tied to $V_{CC}$ internally in packages without PLLs pins.
8. $V_{PP\_FAST}$, used only for fast production programming, must be left floating or unconnected in applications, except CM36 and CM49 packages MUST have the $V_{PP\_FAST}$ ball connected to $V_{CCIO\_0}$ ball externally.

## Peak Startup Supply Current – HX Devices

| Symbol | Parameter | Device | Max | Units |
|---|---|---|---|---|
| $I_{CCPEAK}$ | Core Power Supply | iCE40HX1K | 6.9 | mA |
| | | iCE40HX4K | 22.3 | mA |
| | | iCE40HX8K | 22.3 | mA |
| $I_{CCPLLPEAK}$[1] | PLL Power Supply | iCE40HX1K | 1.8 | mA |
| | | iCE40HX4K | 6.4 | mA |
| | | iCE40HX8K | 6.4 | mA |
| $I_{PP\_2V5PEAK}$ | NVCM Power Supply | iCE40HX1K | 2.8 | mA |
| | | iCE40HX4K | 4.1 | mA |
| | | iCE40HX8K | 4.1 | mA |
| $I_{CCIOPEAK}$, $I_{CC\_SPIPEAK}$ | Bank Power Supply | iCE40HX1K | 6.8 | mA |
| | | iCE40HX4K | 6.8 | mA |
| | | iCE40HX8K | 6.8 | mA |

1. $V_{CCPLL}$ is tied to $V_{CC}$ internally in packages without PLLs pins.

## sysIO Recommended Operating Conditions

| Standard | $V_{CCIO}$ (V) | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| LVCMOS 3.3 | 3.14 | 3.3 | 3.46 |
| LVCMOS 2.5 | 2.37 | 2.5 | 2.62 |
| LVCMOS 1.8 | 1.71 | 1.8 | 1.89 |
| LVDS25E[1, 2] | 2.37 | 2.5 | 2.62 |
| subLVDSE[1, 2] | 1.71 | 1.8 | 1.89 |

1. Inputs on-chip. Outputs are implemented with the addition of external resistors.
2. Does not apply to Configuration Bank $V_{CC\_SPI}$.

## sysIO Single-Ended DC Electrical Characteristics

| Input/ Output Standard | $V_{IL}$ | | $V_{IH}$[1] | | $V_{OL}$ Max. (V) | $V_{OH}$ Min. (V) | $I_{OL}$ Max. (mA) | $I_{OH}$ Max. (mA) |
|---|---|---|---|---|---|---|---|---|
| | Min. (V) | Max. (V) | Min. (V) | Max. (V) | | | | |
| LVCMOS 3.3 | –0.3 | 0.8 | 2.0 | $V_{CCIO}$ + 0.2 V | 0.4 | $V_{CCIO}$ – 0.4 | 8, 16[2], 24[2] | –8, –16[2], –24[2] |
| | | | | | 0.2 | $V_{CCIO}$ – 0.2 | 0.1 | –0.1 |
| LVCMOS 2.5 | –0.3 | 0.7 | 1.7 | $V_{CCIO}$ + 0.2 V | 0.4 | $V_{CCIO}$ – 0.4 | 6, 12[2], 18[2] | –6, –12[2], –18[2] |
| | | | | | 0.2 | $V_{CCIO}$ – 0.2 | 0.1 | –0.1 |
| LVCMOS 1.8 | –0.3 | $0.35V_{CCIO}$ | $0.65V_{CCIO}$ | $V_{CCIO}$ + 0.2 V | 0.4 | $V_{CCIO}$ – 0.4 | 4, 8[2], 12[2] | –4, –8[2], –12[2] |
| | | | | | 0.2 | $V_{CCIO}$ – 0.2 | 0.1 | –0.1 |

1. Some products are clamped to a diode when $V_{IN}$ is larger than $V_{CCIO}$.
2. Only for High Drive LED outputs.

## sysIO Differential Electrical Characteristics

The LVDS25E/subLVDSE differential output buffers are available on all banks but the LVDS/subLVDS input buffers are only available on Bank 3 of iCE40 devices.

### LVDS25

**Over Recommended Operating Conditions**

| Parameter Symbol | Parameter Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{INP}$, $V_{INM}$ | Input Voltage | $V_{CCIO}$[1] = 2.5 | 0 | — | 2.5 | V |
| $V_{THD}$ | Differential Input Threshold | | 250 | 350 | 450 | mV |
| $V_{CM}$ | Input Common Mode Voltage | $V_{CCIO}$[1] = 2.5 | ($V_{CCIO}$/2) - 0.3 | $V_{CCIO}$/2 | ($V_{CCIO}$/2) + 0.3 | V |
| $I_{IN}$ | Input Current | Power on | — | — | ±10 | µA |

1. Typical.

### subLVDS

**Over Recommended Operating Conditions**

| Parameter Symbol | Parameter Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{INP}$, $V_{INM}$ | Input Voltage | $V_{CCIO}$[1] = 1.8 | 0 | — | 1.8 | V |
| $V_{THD}$ | Differential Input Threshold | | 100 | 150 | 200 | mV |
| $V_{CM}$ | Input Common Mode Voltage | $V_{CCIO}$[1] = 1.8 | ($V_{CCIO}$/2) - 0.25 | $V_{CCIO}$/2 | ($V_{CCIO}$/2) + 0.25 | V |
| $I_{IN}$ | Input Current | Power on | — | — | ±10 | µA |

1. Typical.

## LVDS25E Emulation

iCE40 devices can support LVDSE outputs via emulation on all banks. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all devices. The scheme shown in Figure 3-1 is one possible solution for LVDS25E standard implementation. Resistor values in Figure 3-1 are industry standard values for 1% resistors.

***Figure 3-1. LVDS25E Using External Resistors***

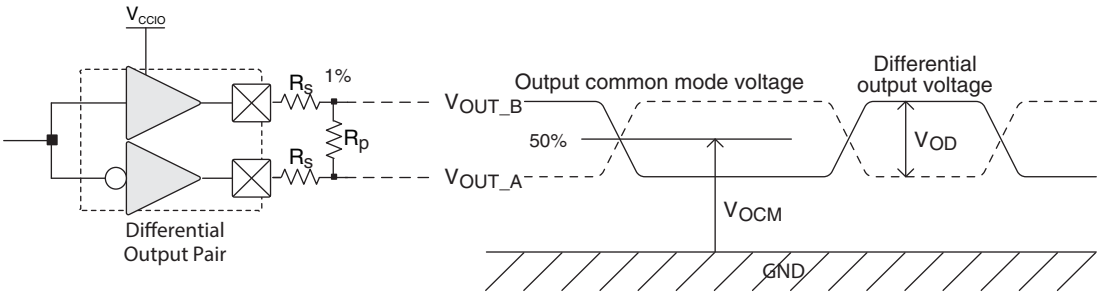


***Table 3-1. LVDS25E DC Conditions***

**Over Recommended Operating Conditions**

| Parameter | Description | Typ. | Units |
|---|---|---|---|
| $Z_{OUT}$ | Output impedance | 20 | Ohms |
| $R_S$ | Driver series resistor | 150 | Ohms |
| $R_P$ | Driver parallel resistor | 140 | Ohms |
| $R_T$ | Receiver termination | 100 | Ohms |
| $V_{OH}$ | Output high voltage | 1.43 | V |
| $V_{OL}$ | Output low voltage | 1.07 | V |
| $V_{OD}$ | Output differential voltage | 0.30 | V |
| $V_{CM}$ | Output common mode voltage | 1.25 | V |
| $Z_{BACK}$ | Back impedance | 100.5 | Ohms |
| $I_{DC}$ | DC output current | 6.03 | mA |

## SubLVDS Emulation

The iCE40 family supports the differential subLVDS standard. The output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all banks of the devices. The subLVDS input standard is supported by the LVDS25 differential input buffer. The scheme shown in Figure 3-2 is one possible solution for subLVDSE output standard implementation. Use LVDS25E mode with suggested resistors for subLVDSE operation. Resistor values in Figure 3-2 are industry standard values for 1% resistors.

***Figure 3-2. subLVDSE***

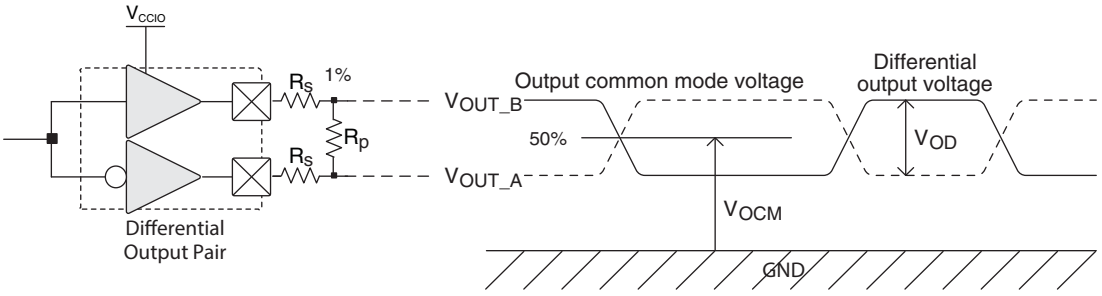


***Table 3-2. subLVDSE DC Conditions***

**Over Recommended Operating Conditions**

| Parameter | Description | Typ. | Units |
|---|---|---|---|
| $Z_{OUT}$ | Output impedance | 20 | Ohms |
| $R_S$ | Driver series resistor | 270 | Ohms |
| $R_P$ | Driver parallel resistor | 120 | Ohms |
| $R_T$ | Receiver termination | 100 | Ohms |
| $V_{OH}$ | Output high voltage | 1.43 | V |
| $V_{OL}$ | Output low voltage | 1.07 | V |
| $V_{OD}$ | Output differential voltage | 0.35 | V |
| $V_{CM}$ | Output common mode voltage | 0.9 | V |
| $Z_{BACK}$ | Back impedance | 100.5 | Ohms |
| $I_{DC}$ | DC output current | 2.8 | mA |

## Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.

## Maximum sysIO Buffer Performance[2]

| I/O Standard | Max. Speed | Units |
|---|---|---|
| **Inputs** | | |
| LVDS25[1] | 400 | MHz |
| subLVDS18[1] | 400 | MHz |
| LVCMOS33 | 250 | MHz |
| LVCMOS25 | 250 | MHz |
| LVCMOS18 | 250 | MHz |
| **Outputs** | | |
| LVDS25E | 250 | MHz |
| subLVDS18E | 155 | MHz |
| LVCMOS33 | 250 | MHz |
| LVCMOS25 | 250 | MHz |
| LVCMOS18 | 155 | MHz |

1. Supported in Bank 3 only.
2. Measured with a toggling pattern

## iCE40 Family Timing Adders

**Over Recommended Commercial Operating Conditions - LP Devices[1, 2, 3, 4, 5]**

| Buffer Type | Description | Timing | Units |
|---|---|---|---|
| **Input Adjusters** | | | |
| LVDS25 | LVDS, $V_{CCIO}$ = 2.5 V | –0.18 | ns |
| subLVDS | subLVDS, $V_{CCIO}$ = 1.8 V | 0.82 | ns |
| LVCMOS33 | LVCMOS, $V_{CCIO}$ = 3.3 V | 0.18 | ns |
| LVCMOS25 | LVCMOS, $V_{CCIO}$ = 2.5 V | 0.00 | ns |
| LVCMOS18 | LVCMOS, $V_{CCIO}$ = 1.8 V | 0.19 | ns |
| **Output Adjusters** | | | |
| LVDS25E | LVDS, Emulated, $V_{CCIO}$ = 2.5 V | 0.00 | ns |
| subLVDSE | subLVDS, Emulated, $V_{CCIO}$ = 1.8 V | 1.32 | ns |
| LVCMOS33 | LVCMOS, $V_{CCIO}$ = 3.3 V | –0.12 | ns |
| LVCMOS25 | LVCMOS, $V_{CCIO}$ = 2.5 V | 0.00 | ns |
| LVCMOS18 | LVCMOS, $V_{CCIO}$ = 1.8 V | 1.32 | ns |

1. Timing adders are relative to LVCMOS25 and characterized but not tested on every device.
2. LVCMOS timing measured with the load specified in Switching Test Condition table.
3. All other standards tested according to the appropriate specifications.
4. Commercial timing numbers are shown.
5. Not all I/O standards are supported for all banks. See the Architecture section of this data sheet for details.

## iCE40 External Switching Characteristics – LP Devices (Continued)[1, 2]

**Over Recommended Operating Conditions**

| Parameter | Description | Device | Min. | Max. | Units |
|---|---|---|---|---|---|
| $t_{HPLL}$ | Clock to Data Hold - PIO Input Register | iCE40LP1K | –0.90 | — | ns |
| | | iCE40LP4K | –0.80 | — | ns |
| | | iCE40LP8K | –0.80 | — | ns |

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions can be extracted from the iCECube2 software.
2. General I/O timing numbers based on LVCMOS 2.5, 0pf load.
3. Supported on devices with a PLL.

# sysCLOCK PLL Timing

**Over Recommended Operating Conditions**

| Parameter | Descriptions | Conditions | Min. | Max. | Units |
|---|---|---|---|---|---|
| $f_{IN}$ | Input Clock Frequency (REFERENCECLK, EXTFEEDBACK) | | 10 | 133 | MHz |
| $f_{OUT}$ | Output Clock Frequency (PLLOUT) | | 16 | 275 | MHz |
| $f_{VCO}$ | PLL VCO Frequency | | 533 | 1066 | MHz |
| $f_{PFD}$ | Phase Detector Input Frequency | | 10 | 133 | MHz |
| **AC Characteristics** | | | | | |
| $t_{DT}$ | Output Clock Duty Cycle | $f_{OUT}$ < 175 MHz | 40 | 50 | % |
| | | 175 MHz < $f_{OUT}$ < 275 MHz | 35 | 65 | "% |
| $t_{PH}$ | Output Phase Accuracy | | — | +/–12 | deg |
| $t_{OPJIT}$[1, 5] | Output Clock Period Jitter | $f_{OUT}$ <= 100 MHz | — | 450 | ps p-p |
| | | $f_{OUT}$ > 100 MHz | — | 0.05 | UIPP |
| | Output Clock Cycle-to-cycle Jitter | $f_{OUT}$ <= 100 MHz | — | 750 | ps p-p |
| | | $f_{OUT}$ > 100 MHz | — | 0.10 | UIPP |
| | Output Clock Phase Jitter | $f_{PFD}$ <= 25 MHz | — | 275 | ps p-p |
| | | $f_{PFD}$ > 25 MHz | — | 0.05 | UIPP |
| $t_W$ | Output Clock Pulse Width | At 90% or 10% | 1.3 | — | ns |
| $t_{LOCK}$[2, 3] | PLL Lock-in Time | | — | 50 | us |
| $t_{UNLOCK}$ | PLL Unlock Time | | — | 50 | ns |
| $t_{IPJIT}$[4] | Input Clock Period Jitter | $f_{PFD} \geq$ 20 MHz | — | 1000 | ps p-p |
| | | $f_{PFD}$ < 20 MHz | — | 0.02 | UIPP |
| $t_{FDTAP}$ | Fine Delay adjustment, per Tap | | 147 | 195 | ps |
| $t_{STABLE}$[3] | LATCHINPUTVALUE LOW to PLL Stable | | — | 500 | ns |
| $t_{STABLE\_PW}$[3] | LATCHINPUTVALUE Pulse Width | | — | 100 | ns |
| $t_{RST}$ | RESET Pulse Width | | 10 | — | ns |
| $t_{RSTREC}$ | RESET Recovery Time | | 10 | — | us |
| $t_{DYNAMIC\_WD}$ | DYNAMICDELAY Pulse Width | | 100 | — | VCO Cycles |
| $t_{PDBYPASS}$ | Propagation delay with the PLL in bypass mode | iCE40LP | 1.18 | 4.68 | ns |
| | | iCE40HX | 1.73 | 4.07 | ns |

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.
2. Output clock is valid after $t_{LOCK}$ for PLL reset and dynamic delay adjustment.
3. At minimum $f_{PFD}$. As the $f_{PFD}$ increases the time will decrease to approximately 60% the value listed.
4. Maximum limit to prevent PLL unlock from occurring. Does not imply the PLL will operate within the output specifications listed in this table.
5. The jitter values will increase with loading of the PLD fabric and in the presence of SSO noise.

## SPI Master or NVCM Configuration Time[1, 2]

| Symbol | Parameter | Conditions | Typ. | Units |
|---|---|---|---|---|
| $t_{CONFIG}$ | POR/CRESET_B to Device I/O Active | iCE40LP384 - Low Frequency (Default) | 25 | ms |
| | | iCE40LP384 - Medium Frequency | 15 | ms |
| | | iCE40LP384 - High Frequency | 11 | ms |
| | | iCE40LP640 - Low Frequency (Default) | 53 | ms |
| | | iCE40LP640 - Medium Frequency | 25 | ms |
| | | iCE40LP640 - High Frequency | 13 | ms |
| | | iCE40LP/HX1K - Low Frequency (Default) | 53 | ms |
| | | iCE40LP/HX1K - Medium Frequency | 25 | ms |
| | | iCE40LP/HX1K - High Frequency | 13 | ms |
| | | iCE40LP/HX4K - Low Frequency (Default) | 230 | ms |
| | | iCE40LP/HX4K - Medium Frequency | 110 | ms |
| | | iCE40LP/HX4K - High Frequency | 70 | ms |
| | | iCE40LP/HX8K - Low Frequency (Default) | 230 | ms |
| | | iCE40LP/HX8K - Medium Frequency | 110 | ms |
| | | iCE40LP/HX8K - High Frequency | 70 | ms |

1. Assumes sysMEM Block is initialized to an all zero pattern if they are used.
2. The NVCM download time is measured with a fast ramp rate starting from the maximum voltage of POR trip point.

## sysCONFIG Port Timing Specifications[1] (Continued)

| Symbol | Parameter | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{MCLK}$ | CRESET_B high to first MCLK edge | iCE40LP384 - Low Frequency (Default) | 600 | — | — | us |
| | | iCE40LP384 - Medium Frequency | 600 | — | — | us |
| | | iCE40LP384 - High Frequency | 600 | — | — | us |
| | | iCE40LP640, iCE40LP/HX1K - Low Frequency (Default) | 800 | — | — | us |
| | | iCE40LP640, iCE40LP/HX1K - Medium Frequency | 800 | — | — | us |
| | | iCE40LP640, iCE40LP/HX1K - High Frequency | 800 | — | — | us |
| | | iCE40LP/HX1K -Low Frequency (Default) | 800 | — | — | us |
| | | iCE40LP/HX1K - Medium Frequency | 800 | — | — | us |
| | | iCE40LP/HX1K - High Frequency | 800 | — | — | us |
| | | iCE40LP/HX4K - Low Frequency (Default) | 1200 | — | — | us |
| | | iCE40LP/HX4K - Medium Frequency | 1200 | — | — | us |
| | | iCE40LP/HX4K - high frequency | 1200 | — | — | us |
| | | iCE40LP/HX8K - Low Frequency (Default) | 1200 | — | — | us |
| | | iCE40LP/HX8K - Medium Frequency | 1200 | — | — | us |
| | | iCE40LP/HX8K - High Frequency | 1200 | — | — | us |

1. Does not apply for NVCM.
2. Supported only with 1.2 V $V_{CC}$ and at 25 °C.
3. Extended range $f_{MAX}$ Write operations support up to 53 MHz only with 1.2 V $V_{CC}$ and at 25 °C.

## Signal Descriptions (Continued)

| Signal Name | I/O | Descriptions |
|---|---|---|
| VPP_FAST | — | Optional fast NVCM programming supply. $V_{PP\_FAST}$, used only for fast production programming, must be left floating or unconnected in applications, except CM36 and CM49 packages MUST have the $V_{PP\_FAST}$ ball connected to $V_{CCIO\_0}$ ball externally. |
| VPP_2V5 | — | VPP_2V5 NVCM programming and operating supply |

# iCE40 LP/HX Family Data Sheet Ordering Information

March 2017 Data Sheet DS1040

## iCE40 Part Number Description

### Ultra Low Power (LP) Devices

ICE40LPXXX – XXXXXXX

**Device Family**
iCE40 FPGA

**Series**
LP = Low Power Series

**Logic Cells**
384 = 384 Logic Cells
640 = 640 Logic Cells
1K = 1,280 Logic Cells
4K = 3,520 Logic Cells
8K = 7,680 Logic Cells

**Shipping Method**
TR = Tape and Reel
TR50 = Tape and Reel 50 units
TR1K = Tape and Reel 1,000 units

**Package**
SWG16 = 16-Ball WLCSP (0.35 mm Pitch)
CM36 = 36-Ball ucBGA (0.4 mm Pitch)
CM49 = 49-Ball ucBGA (0.4 mm Pitch)
CM81 = 81-Ball ucBGA (0.4 mm Pitch)
CB81 = 81-Ball csBGA (0.5 mm Pitch)
CM121 = 121-Ball ucBGA (0.4 mm Pitch)
CB121 = 121-Ball csBGA (0.5 mm Pitch)
CM225 = 225-Ball ucBGA (0.4 mm Pitch)
SG32 = 32-Pin QFN (0.5 mm Pitch)
QN84 = 84-Pin QFN (0.5 mm Pitch)

### High Performance (HX) Devices

ICE40HXXX – XXXXXXX

**Device Family**
iCE40 mobileFPGA

**Series**
HX = High-Performance Series

**Logic Cells**
1K = 1,280 Logic Cells
4K = 3,520 Logic Cells
8K = 7,680 Logic Cells

**Shipping Method**
TR = Tape and Reel

**Package**
CB132 = 132-Ball csBGA (0.5 mm Pitch)
CM225 = 225-Ball ucBGA (0.4 mm Pitch)
CT256 = 256-Ball caBGA (0.8 mm Pitch)
TQ144 = 144-Pin TQFP (0.5 mm Pitch)
VQ100 = 100-Pin VQFP (0.5 mm Pitch)
BG121 = 121-Ball caBGA (0.8 mm Pitch)

All parts shipped in trays unless noted.

## Ordering Information

iCE40 devices have top-side markings as shown below:

**Industrial**


Note: Markings are abbreviated for small packages.

| Part Number | LUTs | Supply Voltage | Package | Leads | Temp. |
|---|---|---|---|---|---|
| ICE40LP8K-CM121TR1K | 7680 | 1.2 V | Halogen-Free ucBGA | 121 | IND |
| ICE40LP8K-CM225 | 7680 | 1.2 V | Halogen-Free ucBGA | 225 | IND |

## High-Performance Industrial Grade Devices, Halogen Free (RoHS) Packaging

| Part Number | LUTs | Supply Voltage | Package | Leads | Temp. |
|---|---|---|---|---|---|
| ICE40HX1K-CB132 | 1280 | 1.2 V | Halogen-Free csBGA | 132 | IND |
| ICE40HX1K-VQ100 | 1280 | 1.2 V | Halogen-Free VQFP | 100 | IND |
| ICE40HX1K-TQ144 | 1280 | 1.2 V | Halogen-Free TQFP | 144 | IND |
| ICE40HX4K-BG121 | 3520 | 1.2 V | Halogen-Free caBGA | 121 | IND |
| ICE40HX4K-BG121TR | 3520 | 1.2 V | Halogen-Free caBGA | 121 | IND |
| ICE40HX4K-CB132 | 3520 | 1.2 V | Halogen-Free csBGA | 132 | IND |
| ICE40HX4K-TQ144 | 3520 | 1.2 V | Halogen-Free TQFP | 144 | IND |
| ICE40HX8K-BG121 | 7680 | 1.2 V | Halogen-Free caBGA | 121 | IND |
| ICE40HX8K-BG121TR | 7680 | 1.2 V | Halogen-Free caBGA | 121 | IND |
| ICE40HX8K-CB132 | 7680 | 1.2 V | Halogen-Free csBGA | 132 | IND |
| ICE40HX8K-CM225 | 7680 | 1.2 V | Halogen-Free ucBGA | 225 | IND |
| ICE40HX8K-CT256 | 7680 | 1.2 V | Halogen-Free caBGA | 256 | IND |

# iCE40 LP/HX Family Data Sheet Supplemental Information



## For Further Information

A variety of technical notes for the iCE40 family are available on the Lattice web site.

- TN1248, iCE40 Programming and Configuration
- TN1250, Memory Usage Guide for iCE40 Devices
- TN1251, iCE40 sysCLOCK PLL Design and Usage Guide
- TN1252, iCE40 Hardware Checklist
- TN1253, Using Differential I/O (LVDS, Sub-LVDS) in iCE40 Devices
- TN1074, PCB Layout Recommendations for BGA Packages
- iCE40 Pinout Files
- Thermal Management document
- Lattice design tools
- IBIS
- Package Diagrams Data Sheet
- Schematic Symbols

# iCE40 LP/HX Family Data Sheet Revision History

**March 2017** **Data Sheet DS1040**

| Date | Version | Section | Change Summary |
|---|---|---|---|
| March 2017 | 3.3 | Introduction | Updated Features section. Added 121-ball caBGA package for ICE40 HX4K/8K to Table 1-1, iCE40 Family Selection Guide. |
| | | Architecture | Updated PLB Blocks section. Changed “subtracters” to “subtractors” in the Carry Logic description. |
| | | | Updated Clock/Control Distribution Network section. Switched the “Clock Enable“ and the “Reset” headings in Table 2-2, Global Buffer (GBUF) Connections to Programmable Logic Blocks. |
| | | Pinout Information | Updated Pin Information Summary section. Added BG121information under iCE40HX4K and iCE40HX8K. |
| | | Ordering Information | Updated iCE40 Part Number Description section. Added Shipping Method and BG121 package under High Performance (HX) Devices. |
| | | | Updated Ordering Information section. Added part numbers for BG121 under High-Performance Industrial Grade Devices, Halogen Free (RoHS) Packaging. |
| | | Supplemental Information | Corrected reference to “Package Diagrams Data Sheet”. |
| October 2015 | 3.2 | Introduction | Updated Features section. Added footnote to 16 WLCSP Programmable I/O: Max Inputs (LVDS25) in Table 1-1, iCE40 Family Selection Guide. |
| | | DC and Switching Characteristics | Updated sysCLOCK PLL Timing section. Changed $t_{DT}$ conditions. |
| | | | Updated Programming NVCM Supply Current – LP Devices section. Changed $I_{PP\_2V5}$ and $I_{CCIO}$, $I_{CC\_SPI}$ units. |
| March 2015 | 3.1 | DC and Switching Characteristics | Updated sysIO Single-Ended DC Electrical Characteristics section. Changed LVCMOS 3.3 and LVCMOS 2. 5 $V_{OH}$ Min. (V) from 0.5 to 0.4. |
| July 2014 | 3.0 | DC and Switching Characteristics | Revised and/or added Typ. $V_{CC}$ data in the following sections.<br>— Static Supply Current – LP Devices<br>— Static Supply Current – HX Devices<br>— Programming NVCM Supply Current – LP Devices<br>— Programming NVCM Supply Current – HX Devices<br>In each section table, the footnote indicating Advanced device status was removed. |
| | | Pinout Information | Updated Pin Information Summary section. Added footnote 1 to CM49 under iCE40LP1K. |
| April 2014 | 02.9 | Ordering Information | Changed “i” to “I” in part number description and ordering part numbers. |
| | | | Added part numbers to the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging table. |