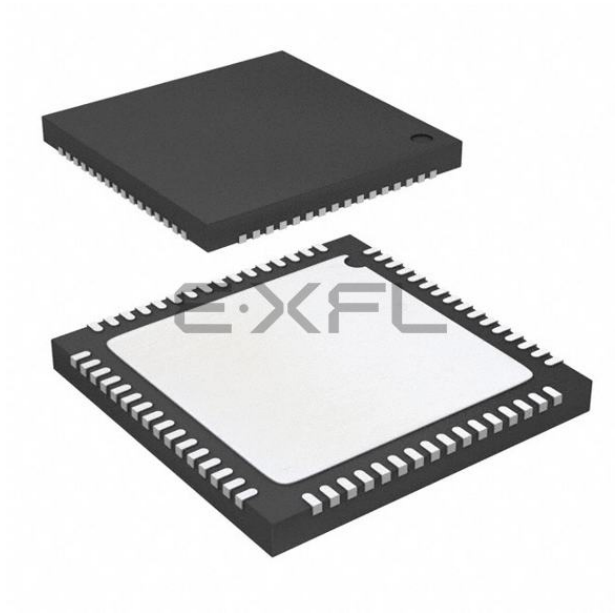

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	41.78MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	30
Program Memory Size	126KB (63K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 32
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad, CSP
Supplier Device Package	64-LFCSP-VQ (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc7124bcpz126-rl

TABLE OF CONTENTS

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ANALOG OUTPUTS					
Output Voltage Range 0		0 to DAC_{REF}		V	DAC_{REF} range: DACGND to $DACV_{DD}$
Output Voltage Range 1		0 to 2.5		V	
Output Voltage Range 2		0 to $DACV_{DD}$		V	
Output Impedance		0.5		Ω	
DAC IN OP AMP MODE					
DAC Output Buffer in Op Amp Mode					
Input Offset Voltage		±0.4		mV	
Input Offset Voltage Drift		4		µV/°C	
Input Offset Current		2		nA	
Input Bias Current		2.5		nA	
Gain		70		dB	5 kΩ load
Unity Gain Frequency		4.5		MHz	R_L = 5 kΩ, C_L = 100 pF
CMRR		78		dB	
Settling Time		12		µs	R_L = 5 kΩ, C_L = 100 pF
Output Slew Rate		3.2		V/µs	R_L = 5 kΩ, C_L = 100 pF
PSRR		75		dB	
DAC AC CHARACTERISTICS					
Voltage Output Settling Time		10		µs	
Digital-to-Analog Glitch Energy		±10		nV-sec	1 LSB change at major carry (where maximum number of bits simultaneously change in the DACxDAT register)
COMPARATOR					
Input Offset Voltage		±15		mV	
Input Bias Current		1		µA	
Input Voltage Range	AGND		AV_{DD} – 1.2	V	
Input Capacitance		8.5		pF	
Hysteresis[4, 6]	2		15	mV	Hysteresis can be turned on or off via the CMPHYST bit in the CMPCON register
Response Time		4		µs	100 mV overdrive and configured with CMPRES = 11
TEMPERATURE SENSOR					
Voltage Output at 25°C		1.415		V	ADuC7124
		1.392		V	ADuC7126
Voltage Temperature Coefficient		3.914		mV/°C	ADuC7124
		4.52		mV/°C	ADuC7126
Accuracy		±3		°C	A single point calibration is required
$θ_{JA}$ Thermal Impedance					
64-Lead LFCSP		24		°C/W	
POWER SUPPLY MONITOR (PSM)					
IOV_{DD} Trip Point Selection		2.79		V	Two selectable trip points
		3.07		V	
Power Supply Trip Point Accuracy		±2.5		%	Of the selected nominal trip point voltage
POWER-ON RESET		2.41		V	
WATCHDOG TIMER (WDT)					
Timeout Period	0		512	sec	
FLASH/EE MEMORY					
Endurance[9]	10,000			Cycles	
Data Retention[10]	20			Years	T_J = 85°C
DIGITAL INPUTS					All digital inputs excluding XCLKI and XCLKO
Logic 1 Input Current		±0.2	±1	µA	$V_{IH} = V_{DD}$ or V_{IH} = 5 V
Logic 0 Input Current		–40	–60	µA	V_{IL} = 0 V; except TDI, TDO, and RTCK
		–80	–120	µA	V_{IL} = 0 V; TDI, TDO, and RTCK
Input Capacitance		5		pF	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUTS[3]					All logic inputs excluding XCLKI
V_{INL}, Input Low Voltage			0.8	V	
V_{INH}, Input High Voltage	2.0			V	
LOGIC OUTPUTS					All digital outputs excluding XCLKO
V_{OH}, Output High Voltage	2.4			V	I_{SOURCE} = 1.6 mA
V_{OL}, Output Low Voltage[11]			0.4	V	I_{SINK} = 1.6 mA
CRYSTAL INPUTS XCLKI and XCLKO					
Logic Inputs, XCLKI Only					
V_{INL}, Input Low Voltage		0.8		V	
V_{INH}, Input High Voltage		1.6		V	
XCLKI Input Capacitance		20		pF	
XCLKO Output Capacitance		20		pF	
INTERNAL OSCILLATOR		32.768		kHz	
			±3	%	
MCU CLOCK RATE[4]					
From 32 kHz Internal Oscillator		326		kHz	CD = 7
From 32 kHz External Crystal		41.78		MHz	CD = 0
Using an External Clock	0.05		44	MHz	T_A = 85°C
	0.05		41.78	MHz	T_A = 125°C
START-UP TIME					Core clock = 41.78 MHz
At Power-On		66		ms	
From Pause/Nap Mode		2.6		µs	CD = 0
		247		µs	CD = 7
From Sleep Mode		1.58		ms	
From Stop Mode		1.7		ms	
PROGRAMMABLE LOGIC ARRAY (PLA)					
Pin Propagation Delay		12		ns	From input pin to output pin
Element Propagation Delay		2.5		ns	
POWER REQUIREMENTS[12, 13]					
Power Supply Voltage Range					
AV_{DD} to AGND and IOV_{DD} to IOGND	2.7		3.6	V	
Analog Power Supply Currents					
AV_{DD} Current		165		µA	ADC in idle mode
$DACV_{DD}$ Current[14]		0.02		µA	
Digital Power Supply Current					
IOV_{DD} Current in Active Mode					Code executing from Flash/EE
		8.1	12.5	mA	CD = 7
		11.6	17	mA	CD = 3
		33.3	50	mA	CD = 0 (41.78 MHz clock)
IOV_{DD} Current in Pause Mode		20.6	30	mA	CD = 0 (41.78 MHz clock)
IOV_{DD} Current in Sleep Mode		110		µA	T_A = 85°C
		600	680	µA	T_A = 125°C
Additional Power Supply Currents					
ADC		1.26		mA	At 1 MSPS
		0.7		mA	At 62.5 kSPS
DAC		315		µA	Per DAC

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ESD TESTS					2.5 V reference, T_A = 25°C
HBM Passed Up To			3	kV	
FICDM Passed Up To			1.5	kV	

[1] All ADC channel specifications are guaranteed during normal core operation.
[2] Apply to all ADC input channels.
[3] Measured using the factory-set default values in the ADC offset register (ADCOF) and gain coefficient register (ADCGN).
[4] Not production tested but supported by design and/or characterization data on production release.
[5] Measured using the factory-set default values in ADCOF and ADCGN with an external AD845 op amp as an input buffer stage as shown in Figure 37. Based on external ADC system components, the user may need to execute a system calibration to remove external endpoint errors and achieve these specifications (see the Calibration section).
[6] The input signal can be centered on any dc common-mode voltage (V_{CM}) as long as this value is within the ADC voltage input range specified.
[7] DAC linearity is calculated using a reduced code range of 100 to 3995.
[8] DAC gain error is calculated using a reduced code range of 100 to internal 2.5 V V_{REF}.
[9] Endurance is qualified as per JEDEC Standard 22 Method A117 and measured at −40°C, +25°C, +85°C, and +125°C.
[10] Retention lifetime equivalent at junction temperature (T_J) = 85°C as per JEDEC Standard 22 Method A117. Retention lifetime derates with junction temperature.
[11] Test carried out with a maximum of eight I/Os set to a low output level.
[12] Power supply current consumption is measured in normal, pause, and sleep modes under the following conditions: normal mode with 3.6 V supply, pause mode with 3.6 V supply, and sleep mode with 3.6 V supply.
[13] IOV_{DD} power supply current increases typically by 2 mA during a Flash/EE erase cycle.
[14] This current must be added to the AV_{DD} current.

TIMING SPECIFICATIONS

I²C Timing

Table 2. I²C Timing in Fast Mode (400 kHz)

		Slave		Master	
Parameter	Description	Min	Max	Typ	Unit
t_L	SCL low pulse width	200		1360	ns
t_H	SCL high pulse width	100		1140	ns
t_{SHD}	Start condition hold time	300			ns
t_{DSU}	Data setup time	100		740	ns
t_{DHD}	Data hold time	0		400	ns
t_{RSU}	Setup time for repeated start	100			ns
t_{PSU}	Stop condition setup time	100		800	ns
t_{BUF}	Bus-free time between a stop condition and a start condition	1.3			µs
t_R	Rise time for both SCL and SDA		300	200	ns
t_F	Fall time for both SCL and SDA		300		ns

Table 3. I²C Timing in Standard Mode (100 kHz)

		Slave		
Parameter	Description	Min	Max	Unit
t_L	SCL low pulse width	4.7		µs
t_H	SCL high pulse width	4.0		ns
t_{SHD}	Start condition hold time	4.0		µs
t_{DSU}	Data setup time	250		ns
t_{DHD}	Data hold time	0	3.45	µs
t_{RSU}	Setup time for repeated start	4.7		µs
t_{PSU}	Stop condition setup time	4.0		µs
t_{BUF}	Bus-free time between a stop condition and a start condition	4.7		µs
t_R	Rise time for both SCL and SDA		1	µs
t_F	Fall time for both SCL and SDA		300	ns

Table 6. SPI Slave Mode Timing (Phase Mode = 1)

Parameter	Description	Min	Typ	Max	Unit
$t_{\overline{CS}}$	$\overline{CS}$ to SCLK edge	200			ns
t_{SL}	SCLK low pulse width		(SPIDIV + 1) × t_{HCLK}		ns
t_{SH}	SCLK high pulse width		(SPIDIV + 1) × t_{HCLK}		ns
t_{DAV}	Data output valid after SCLK edge			25	ns
t_{DSU}	Data input setup time before SCLK edge[1]	1 × t_{UCLK}			ns
t_{DHD}	Data input hold time after SCLK edge[1]	2 × t_{UCLK}			ns
t_{DF}	Data output fall time		5	12.5	ns
t_{DR}	Data output rise time		5	12.5	ns
t_{SR}	SCLK rise time		5	12.5	ns
t_{SF}	SCLK fall time		5	12.5	ns
t_{SFS}	$\overline{CS}$ high after SCLK edge	0			ns

[1] t_{UCLK} = 23.9 ns. It corresponds to the 41.78 MHz internal clock from the PLL before the clock divider.

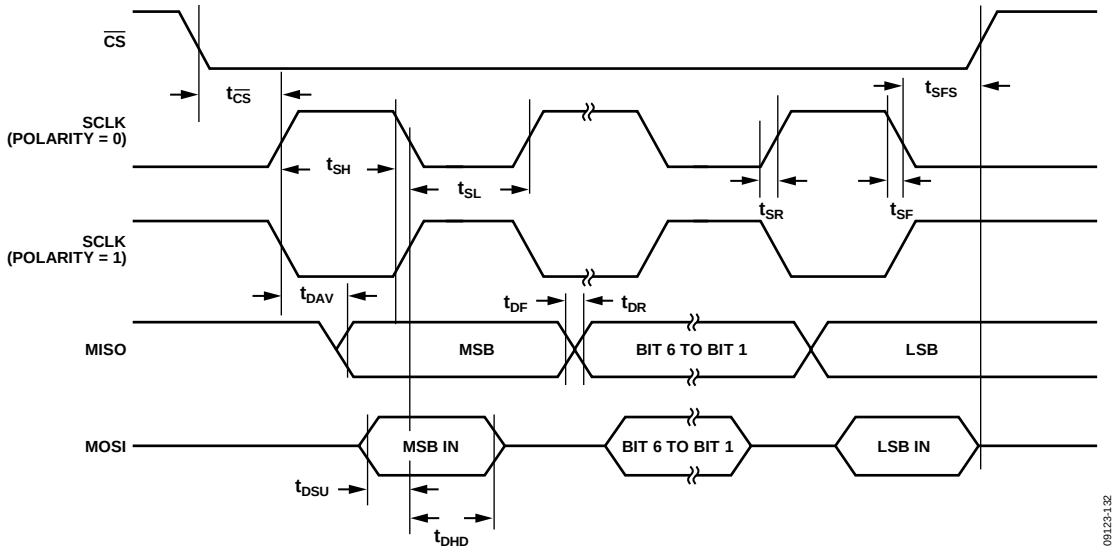

Figure 5. SPI Slave Mode Timing (Phase Mode = 1)

Pin No.	Mnemonic	Description
62	P1.1/SPM1/SOUT0/I2C0SDA/PLAI[1]	General-Purpose Input and Output Port 1.1 (P1.1). Serial Port Multiplexed (SPM1). UART0 Output (SOUT0). I2C0 (I2C0SDA). Programmable Logic Array Input Element 1 (PLAI[1]).
63	P1.0/T1/SPM0/SIN0/I2C0SCL/PLAI[0]	General-Purpose Input and Output Port 1.0 (P1.0). Timer1 Input (T1). Serial Port Multiplexed (SPM0). UART0 Input (SIN0). I2C0 (I2C0SCL). Programmable Logic Array Input Element 0 (PLAI[0]).
64	P4.2/AD10/PLAO[10]	General-Purpose Input and Output Port 4.2 (P4.2). External Memory Interface (AD10). Programmable Logic Array Output Element 10 (PLAO[10]).
65	P4.3/AD11/PLAO[11]	General-Purpose Input and Output Port 4.3 (P4.3). External Memory Interface (AD11). Programmable Logic Array Output Element 11 (PLAO[11]).
66	P4.4/AD12/PLAO[12]	General-Purpose Input and Output Port 4.4 (P4.4). External Memory Interface (AD12). Programmable Logic Array Output Element 12 (PLAO[12]).
67	P4.5/AD13/PLAO[13]/RTCK	General-Purpose Input and Output Port 4.5 (P4.5). External Memory Interface (AD13). Programmable Logic Array Output Element 13 (PLAO[13]). JTAG Return Test Clock (RTCK).
68	IOV_{DD}	3.3 V Supply for GPIO and Input of the On-Chip Voltage Regulator.
69	IOGND	Ground for GPIO. Typically connected to DGND.
70	V_{REF}	2.5 V Internal Voltage Reference. Must be connected to a 0.47 µF capacitor when using the internal reference.
71	DAC_{REF}	External Voltage Reference for the DACs. Range: DACGND to $DACV_{DD}$.
72	AV_{DD}	3.3 V Analog Power.
73, 74	AGND	Analog Ground. Ground reference point for the analog circuitry.
75	GND_{REF}	Ground Voltage Reference for the ADC. For optimal performance, the analog power supply should be separated from IOGND and DGND.
76	ADC11	Single-Ended or Differential Analog Input 11.
77	ADC0	Single-Ended or Differential Analog Input 0.
78	ADC1	Single-Ended or Differential Analog Input 1.
79	ADC2/CMP0	Single-Ended or Differential Analog Input 2 (ADC2). Comparator Positive Input (CMP0).
80	ADC3/CMP1	Single-Ended or Differential Analog Input 3 (ADC3). Comparator Negative Input (CMP1).

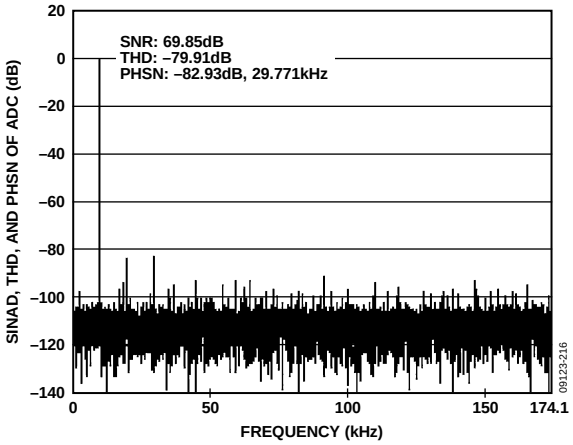

Figure 17. SINAD, THD, and PHSN of ADC,
V_{REF} = Internal 2.5 V, Single-Ended Mode
ADCCP = ADC0

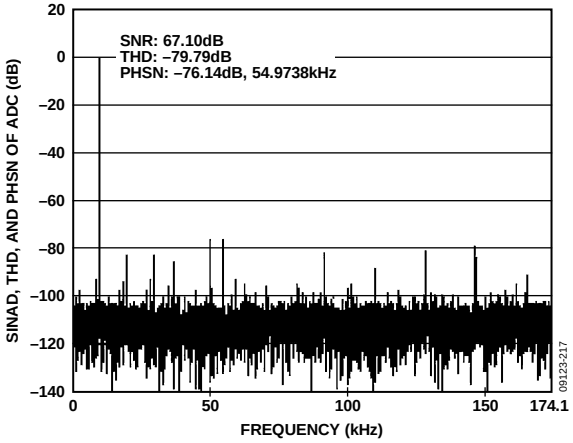

Figure 18. SINAD, THD, and PHSN of ADC,
V_{REF} = Internal 2.5 V, Single-Ended Mode
ADCCP = DAC1/ADC13, ADCCN = ADC0

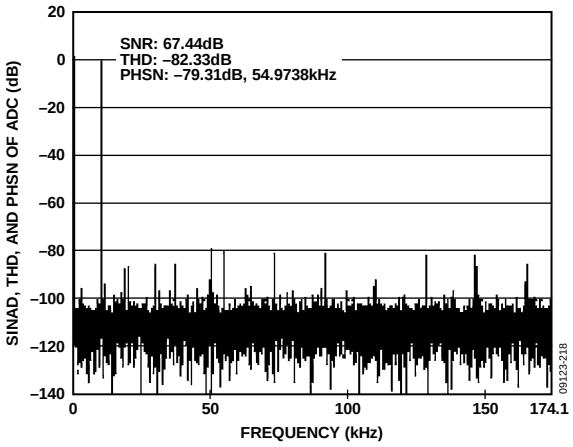

Figure 19. SINAD, THD, and PHSN of ADC,
V_{REF} = Internal 2.5 V, Single-Ended Mode
ADCCP = ADC8, ADCCN = ADC0

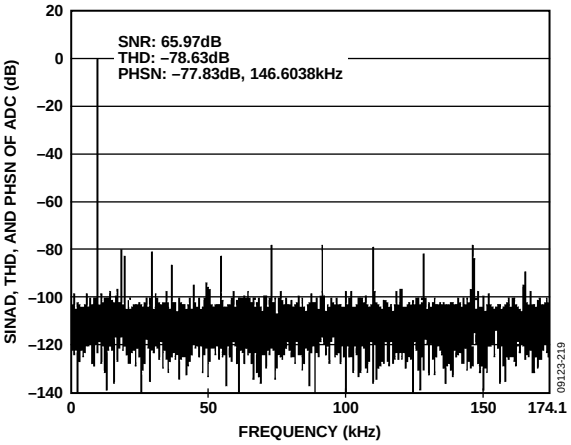

Figure 20. SINAD, THD, and PHSN of ADC,
V_{REF} = Internal 2.5 V, Single-Ended Mode
ADCCP = ADC15/DAC3, ADCCN = ADC0

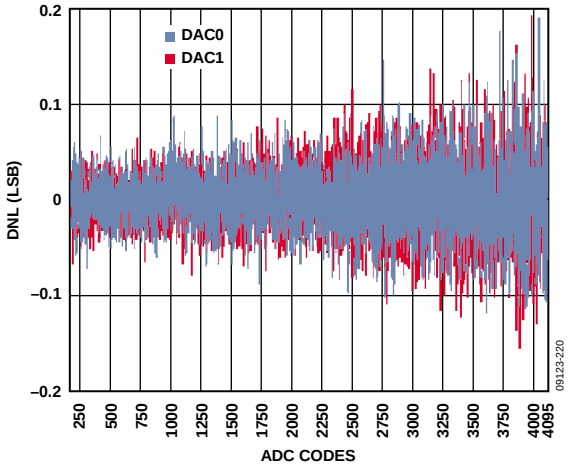

Figure 21. DAC DNL Error,
DAC0 Max Positive DNL: 0.188951, DAC1 Max Positive DNL: 0.190343
DAC0 Max Negative DNL: –0.120081, DAC1 Max Negative DNL: –0.15697

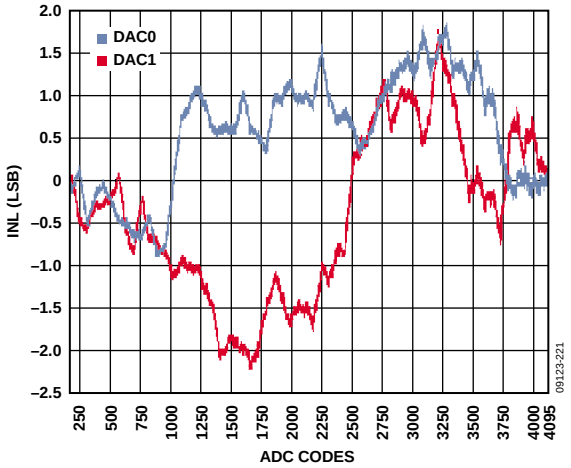

Figure 22. DAC INL Error,
DAC0 Max Positive INL: 1.84106, DAC1 Max Positive INL: 1.75312
DAC0 Max Negative INL: –0.887319, DAC1 Max Negative INL: –2.23708

ADCCN Register

Name: ADCCN

Address: 0xFFFF0508

Default Value: 0x01

Access: Read/write

ADCCN is an ADC negative channel selection register. This MMR is described in Table 32.

Table 32. ADCCN MMR Bit Designation

Bit	Value	Description
[7:5]		Reserved.
[4:0]		Negative channel selection bits.
	00000	ADC0.
	00001	ADC1.
	00010	ADC2.
	00011	ADC3.
	00100	ADC4.
	00101	ADC5.
	00110	ADC6.
	00111	ADC7.
	01000	ADC8.
	01001	ADC9.
	01010	ADC10.
	01011	ADC11.
	01100	DAC0/ADC12.
	01101	DAC1/ADC13.
	01110	DAC2/ADC14.
	01111	DAC3/ADC15.
	10000	Reserved.
	10001	AGND.
	10010	Reserved.
	10011	Reserved.
	Others	Reserved.

ADCSTA Register

Name: ADCSTA

Address: 0xFFFF050C

Default Value: 0x00

Access: Read only

ADCSTA is an ADC status register that indicates when an ADC conversion result is ready. The ADCSTA register contains only one bit, ADCReady (Bit 0), representing the status of the ADC. This bit is set at the end of an ADC conversion, generating an ADC interrupt. It is cleared automatically by reading the ADCDAT MMR. When the ADC is performing a conversion, the status of the ADC can be read externally via the ADC_{BUSY} pin. This pin is high during a conversion. When the conversion is finished, ADC_{BUSY} goes back low. This information is available on P0.5 (see the General-Purpose Input/Output section) if enabled in the ADCCON register.

ADCDAT Register

Name: ADCDAT

Address: 0xFFFF0510

Default Value: 0x00000000

Access: Read only

ADCDAT is an ADC data result register that holds the 12-bit ADC result, as shown in Figure 30.

ADCRST Register

Name: ADCRST

Address: 0xFFFF0514

Default Value: 0x00

Access: Read/write

ADCRST resets the digital interface of the ADC. Writing any value to this register resets all the ADC registers to their default values.

ADCGN Register

Name: ADCGN

Address: 0xFFFF0530

Default Value: 0x0200

Access: Read/write

ADCGN is a 10-bit gain calibration register.

ADCOF Register

Name: ADCOF

Address: 0xFFFF0534

Default Value: 0x0200

Access: Read/write

ADCOF is a 10-bit offset calibration register.

CONVERTER OPERATION

The ADC incorporates a successive approximation (SAR) architecture involving a charge-sampled input stage. This architecture can operate in three different modes: differential, pseudo differential, and single-ended.

Differential Mode

The ADuC7124/ADuC7126 each contains a successive approximation ADC based on two capacitive DACs. Figure 32 and Figure 33 show simplified schematics of the ADC in acquisition and conversion phases, respectively. The ADC comprises control logic, a SAR, and two capacitive DACs. In Figure 32 (the acquisition phase), SW3 is closed and SW1 and SW2 are in

CALIBRATION

By default, the factory-set values written to the ADC offset (ADCOF) and gain coefficient registers (ADCGN) yield optimum performance in terms of end-point errors and linearity for standalone operation of the part (see the Specifications section). If system calibration is required, it is possible to modify the default offset and gain coefficients to improve end-point errors, but note that any modification to the factory-set ADCOF and ADCGN values can degrade ADC linearity performance.

For system offset error correction, the ADC channel input stage must be tied to AGND. A continuous software ADC conversion loop must be implemented by modifying the value in ADCOF until the ADC result (ADCDAT) reads Code 0 to Code 1. If the ADCDAT value is greater than 1, ADCOF should be decremented until ADCDAT reads Code 0 to Code 1. Offset error correction is done digitally and has a resolution of 0.25 LSB and a range of ±3.125% of V_{REF}.

For system gain error correction, the ADC channel input stage must be tied to V_{REF}. A continuous software ADC conversion loop must be implemented to modify the value in ADCGN until the ADC result (ADCDAT) reads Code 4094 to Code 4095. If the ADCDAT value is less than 4094, ADCGN should be incremented until ADCDAT reads Code 4094 to Code 4095. Similar to the offset calibration, the gain calibration resolution is 0.25 LSB with a range of ±3% of V_{REF}.

TEMPERATURE SENSOR

The ADuC7124/ADuC7126 provide voltage outputs from an on-chip band gap reference that is proportional to absolute temperature. This voltage output can also be routed through the front-end ADC multiplexer (effectively, an additional ADC channel input), facilitating an internal temperature sensor channel, measuring die temperature.

An ADC temperature sensor conversion differs from a standard ADC voltage. The ADC performance specifications do not apply to the temperature sensor.

Chopping of the internal amplifier must be enabled using the TSCON register. To enable this mode, the user must set Bit 0 of TSCON. The user must also take two consecutive ADC readings and average them in this mode.

The ADCCON register must be configured to 0x37A3.

To calculate die temperature, use the following formula:

$$T - T_{REF} = (V_{ADC} - V_{TREF}) \times K$$

where:
T is the temperature result.
T_{REF} = 25°C.
For the ADuC7124, V_{TREF} = 1.415 V and for the ADuC7126, V_{TREF} = 1.392 V, which corresponds to T_{REF} = 25°C, as described in Table 1.
V_{ADC} is the average ADC result from two consecutive conversions.
K is the gain of the ADC in temperature sensor mode as determined by characterization data. K = 0.2555°C/mV for ADuC7124. K = 0.2212°C/mV for ADuC7126. This corresponds to the 1/voltage temperature coefficient specification from Table 1.

Using the default values from Table 1 and without any calibration, this equation becomes

$$T - 25°C = (V_{ADC} - 1415) \times 0.2555 \text{ for ADuC7124}$$

$$T - 25°C = (V_{ADC} - 1392) \times 0.2212 \text{ for ADuC7126}$$

where V_{ADC} is in mV.

For better accuracy, the user should perform a single point calibration at a controlled temperature value.

For the calculation with no calibration, use 25°C and 1415 mV for the ADuC7124 and 1392mV for the ADuC7126. The idea of a single point calibration is to use other known (T_{REF}, V_{TREF}) values to replace the common T = 25°C and 1415 mV for the ADuC7124 and 1392 mV for the ADuC7126 for every part.

For some users, it is not possible to obtain such a known pair.

For such cases, the ADuC7124/ADuC7126 comes with a single point calibration value loaded in the TEMPREF register. For more details on this register, see Table 35. During production testing of the ADuC7124/ADuC7126, the TEMPREF register is loaded with an offset adjustment factor. Each part has a different value in the TEMPREF register. Using this single point calibration, the same formula is still used.

$$T - T_{REF} = (V_{ADC} - V_{TREF}) \times K$$

where:
T_{REF} = 25°C but is not guaranteed.
V_{TREF} can be calculated using the TEMPREF register.

TSCON Register

Name: TSCON

Address: 0xFFFF0544

Default Value: 0x00

Access: Read/write

Table 34. TSCON MMR Bit Descriptions

Bit	Description
[7:1]	Reserved.
0	Temperature sensor chop enable bit. This bit must be set. This bit is set to 1 to enable chopping of the internal amplifier to the ADC. This bit is cleared to disable chopping. This results in incorrect temperature sensor readings. This bit is cleared by default.

Table 56. FEE0PRO and FEE0HID MMR Bit Descriptions

Bit	Description
31	Read protection. Cleared by the user to protect Block 0. Set by the user to allow reading of Block 0.
[30:0]	Write protection for Page 123 to Page 0. Each bit protects protects a group of 4 pages. Cleared by the user to protect the pages when writing to flash. Thus preventing an accidental write to specific pages in flash. Set by the user to allow writing to the pages.

Table 57. FEE1PRO and FEE1HID MMR Bit Descriptions

Bit	Description
31	Read protection. Cleared by the user to protect Block 1. Set by the user to allow reading of Block 1.
30	Write protection for Page 127 to Page 120. Cleared by the user to protect the pages when writing to flash. Thus preventing an accidental write to specific pages in flash. Set by the user to allow writing to the pages.
[29:0]	Write protection for Page 119 to Page 116 and for Page 0 to Page 3. Cleared by the user to protect the pages in writing. Set by the user to allow writing to the pages.

EXECUTION TIME FROM SRAM AND FLASH/EE

This section describes SRAM and Flash/EE access times during execution for applications where execution time is critical.

Execution from SRAM

Fetching instructions from SRAM takes one clock cycle because the access time of the SRAM is 2 ns, and a clock cycle is 24 ns minimum. However, if the instruction involves reading or writing data to memory, one extra cycle must be added if the data is in SRAM (or three cycles if the data is in Flash/EE): one cycle to execute the instruction and two cycles to get the 32-bit data from Flash/EE. A control flow instruction (a branch instruction, for example) takes one cycle to fetch but also takes two cycles to fill the pipeline with the new instructions.

Execution from Flash/EE

Because the Flash/EE width is 16 bits and access time for 16-bit words is 22 ns, execution from Flash/EE cannot be done in one cycle (as can be done from SRAM when the CD bit = 0). Also, some dead times are needed before accessing data for any value of the CD bits.

In ARM mode, where instructions are 32 bits, two cycles are needed to fetch any instruction when CD = 0. In Thumb mode, where instructions are 16 bits, one cycle is needed to fetch any instruction.

Timing is identical in both modes when executing instructions that involve using the Flash/EE for data memory. If the instruction to be executed is a control flow instruction, an extra cycle is needed to decode the new address of the program counter, and then four cycles are needed to fill the pipeline. A data processing instruction involving only the core register does not require any extra clock cycles. However, if it involves data in Flash/EE, an extra clock cycle is needed to decode the address of the data, and two cycles are needed to get the 32-bit data from Flash/EE. An extra cycle must also be added before fetching another instruction. Data transfer instructions are more complex and are summarized in Table 58.

Table 58. Execution Cycles in ARM/Thumb Mode

Instructions	Fetch Cycles	Dead Time	Data Access	Dead Time
LD[1]	2/1	1	2	1
LDH	2/1	1	1	1
LDM/PUSH	2/1	N[2]	2 × N[2]	N[1]
STR[1]	2/1	1	2 × 20 ns	1
STRH	2/1	1	20 ns	1
STRM/POP	2/1	N[1]	2 × N × 20 ns[1]	N[1]

[1] The SWAP instruction combines an LD and STR instruction with only one fetch, giving a total of eight cycles + 40 ns.
[2] N is the number of data bytes to load or store in the multiple load/store instruction (1 < N ≤ 16).

RESET AND REMAP

The ARM exception vectors are all situated at the bottom of the memory array, from Address 0x00000000 to Address 0x00000020, as shown in Figure 40.

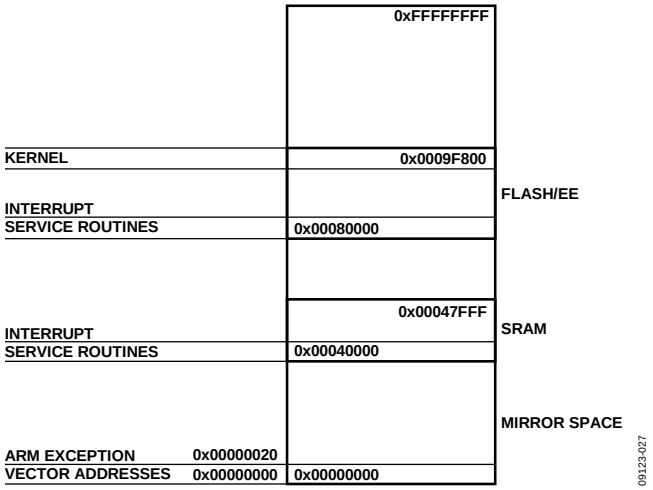

Figure 40. Remap for Exception Execution

By default, and after any reset, the Flash/EE is mirrored at the bottom of the memory array. The remap function allows the programmer to mirror the SRAM at the bottom of the memory array, which facilitates execution of exception routines from SRAM instead of from Flash/EE. This means exceptions are executed twice as fast, being executed in 32-bit ARM mode with 32-bit wide SRAM instead of 16-bit wide Flash/EE memory.

MMRs and Keys

The operating mode, clocking mode, and programmable clock divider are controlled via three MMRs, PLLCON (see Table 73), and POWCONx. PLLCON controls the operating mode of the clock system, POWCON0 controls the core clock frequency and the power-down mode, and POWCON1 controls the clock frequency to I²C and SPI.

Table 72. PLLKEYx Registers

Name	Address	Default Value	Access
PLLKEY1	0xFFFF0410	0x0000	W
PLLKEY2	0xFFFF0418	0x0000	W

PLLCON Register

Name: PLLCON

Address: 0xFFFF0414

Default Value: 0x21

Access: Read/write

Table 73. PLLCON MMR Bit Descriptions

Bit	Value	Name	Description
[7:6]			Reserved.
5		OSEL	32 kHz PLL input selection. Set by the user to select the internal 32 kHz oscillator. Set by default. Cleared by the user to select the external 32 kHz crystal.
[4:2]			Reserved.
[1:0]		MDCLK	Clocking modes.
	00		Reserved.
	01		PLL. Default configuration.
	10		Reserved.
	11		External clock on the P0.7 Pin.

To prevent accidental programming, a certain sequence must be followed to write to the PLLCON register.The PLLCON write sequence is as follows:

1. Write Code 0xAA to Register PLLKEY1.
2. Write user value to Register PLLCON.
3. Write Code 0x55 to Register PLLKEY2.

Table 74. POWKEYx Registers

Name	Address	Default Value	Access
POWKEY1	0xFFFF0404	0x0000	W
POWKEY2	0xFFFF040C	0x0000	W

POWKEY1 and POWKEY2 are used to prevent accidental programming to POWCON0.

POWCON0 Register

Name: POWCON0

Address: 0xFFFF0408

Default Value: 0x0003

Access: Read/write

Table 75. POWCON0 MMR Bit Descriptions

Bit	Value	Name	Description
7			Reserved.
[6:4]		PC	Operating modes.
	000		Active mode.
	001		Pause mode.
	010		Nap mode.
	011		Sleep mode. IRQ0 to IRQ3 and Timer2 can wake up the part.
	100		Stop mode. IRQ0 to IRQ3 can wake up the part.
	Others		Reserved.
3			Reserved.
[2:0]		CD	CPU clock divider bits.
	000		41.78 MHz.
	001		20.89 MHz.
	010		10.44 MHz.
	011		5.22 MHz.
	100		2.61 MHz.
	101		1.31 MHz.
	110		653 kHz.
	111		326 kHz.

To prevent accidental programming, a certain sequence must be followed to write to the POWCONx register. The POWCON0 write sequence is as follows:

1. Write Code 0x01 to Register POWKEY1.
2. Write a user value to Register POWCON0.
3. Write Code 0xF4 to Register POWKEY2.

Table 76. POWKEYx Registers

Name	Address	Default Value	Access
POWKEY3	0xFFFF0434	0x0000	W
POWKEY4	0xFFFF043C	0x0000	W

POWKEY3 and POWKEY4 are used to prevent accidental programming to POWCON1.

POWCON1 Register

Name: POWCON1

Address: 0xFFFF0438

Default Value: 0x124

Access: Read/write

COM1DIV0 Register

Name: COM1DIV0

Address: 0xFFFF0740

Default Value: 0x00

Access: Read/write

COM1DIV0 is a low byte divisor latch for UART1. COM1TX, COM1RX, and COM1DIV0 share the same address location. COM1TX and COM1RX can be accessed when Bit 7 in COM1CON0 register is cleared. COM1DIV0 can be accessed when Bit 7 of COM1CON0 is set.

COM0IEN0 Register

Name: COM0IEN0

Address: 0xFFFF0704

Default Value: 0x00

Access: Read/write

COM0IEN0 is the interrupt enable register for UART0.

COM1IEN0 Register

Name: COM1IEN0

Address: 0xFFFF0744

Default Value: 0x00

Access: Read/write

COM1IEN0 is the interrupt enable register for UART1.

Table 92. COMxIEN0 MMR Bit Descriptions

Bit	Name	Description
[7:4]		Reserved.
3	EDSSI	Modem status interrupt enable bit. Set by the user to enable generation of an interrupt if any of COMXSTA1[3:1] are set. Cleared by the user.
2	ELSI	Rx status interrupt enable bit. Set by the user to enable generation of an interrupt if any of COMxSTA0[3:0] are set. Cleared by the user.
1	ETBEI	Enable transmit buffer empty interrupt. Set by the user to enable interrupt when the buffer is empty during a transmission. Cleared by the user.
0	ERBFI	Enable receive buffer full interrupt. In non-FIFO mode, set by the user to enable an interrupt when buffer is full during a reception. Cleared by the user. In FIFO mode, set by the user to enable an interrupt when trigger level is reached. It also controls the character receive timeout interrupt. Cleared by the user.

COM0DIV1 Register

Name: COM0DIV1

Address: 0xFFFF0704

Default Value: 0x00

Access: Read/write

COM0DIV1 is a divisor latch (high byte) register for UART0.

COM1DIV1 Register

Name: COM1DIV1

Address: 0xFFFF0744

Default Value: 0x00

Access: Read/write

COM1DIV1 is a divisor latch (high byte) register for UART1.

COM0IID0 Register

Name: COM0IID0

Address: 0xFFFF0708

Default Value: 0x01

Access: Read only

COM0IID0 is the interrupt identification register for UART0. It also indicates if the UART is in FIFO mode.

COM1IID0 Register

Name: COM1IID0

Address: 0xFFFF0748

Default Value: 0x01

Access: Read only

COM1IID0 is the interrupt identification register for UART1. It also indicates if the UART is in FIFO mode.

COM1CON0 Register

Name: COM1CON0

Address: 0xFFFF074C

Default Value: 0x00

Access: Read/write

COM1CON0 is the line control register for UART1.

Table 95. COMxCON0 MMR Bit Descriptions

Bit	Name	Description
7	DLAB	Divisor latch access. Set by the user to enable access to the COMxDIV0 and COMxDIV1 registers. Cleared by the user to disable access to COMxDIV0 and COMxDIV1 and enable access to COMxRX and COMxTX.
6	BRK	Set break. Set by the user to force SOUTx to 0. Cleared to operate in normal mode.
5	SP	Stick parity. Set by the user to force parity to defined values: 1 if EPS = 1 and PEN = 1, 0 if EPS = 0 and PEN = 1.
4	EPS	Even parity select bit. Set for even parity. Cleared for odd parity.
3	PEN	Parity enable bit. Set by the user to transmit and check the parity bit. Cleared by the user for no parity transmission or checking.
2	Stop	Stop bit. Set by the user to transmit 1½ stop bits if the word length is five bits or two stop bits if the word length is six bits, seven bits, or eight bits. The receiver checks the first stop bit only, regardless of the number of stop bits selected. Cleared by the user to generate one stop bit in the transmitted data.
[1:0]	WLS	Word length select: 00 = five bits, 01 = six bits, 10 = seven bits, 11 = eight bits.

COM0CON1 Register

Name: COM0CON1

Address: 0xFFFF0710

Default Value: 0x00

Access: Read/write

COM0CON1 is the modem control register for UART0.

COM1CON1 Register

Name: COM1CON1

Address: 0xFFFF0750

Default Value: 0x00

Access: Read/write

COM1CON1 is the modem control register for UART1.

Table 96. COMxCON1 MMR Bit Descriptions

Bit	Name	Description
[7:5]		Reserved.
4	LOOPBACK	Loop back. Set by the user to enable loopback mode. In loopback mode, SOUTx is forced high. The modem signals are also directly connected to the status inputs (RTS to CTS and DTR to DSR). Cleared by the user to be in normal mode.
3	PEN	Parity enable bit. Set by the user to transmit and check the parity bit. Cleared by the user for no parity transmission or checking.
2	Stop	Stop bit. Set by the user to transmit 1½ stop bits if the word length is five bits or two stop bits if the word length is six bits, seven bits, or eight bits. The receiver checks the first stop bit only, regardless of the number of stop bits selected. Cleared by the user to generate one stop bit in the transmitted data.
1	RTS	Request to send. Set by the user to force the RTS output to 0. Cleared by the user to force the RTS output to 1.
0	DTR	Data terminal ready. Set by the user to force the DTR output to 0. Cleared by the user to force the DTR output to 1.

COM0STA0 Register

Name: COM0STA0

Address: 0xFFFF0714

Default Value: 0xE0

Access: Read only

COM0STA0 is the line status register for UART0.

I²C Master Status Register

Name: I2C0MSTA, I2C1MSTA

Address: 0xFFFF0804, 0xFFFF0904

Default Value: 0x0000, 0x0000

Access: Read only

Function: This 16-bit MMR is the I²C status register in master mode.

Table 103. I2CxMSTA MMR Bit Descriptions

Bit	Name	Description
[15:11]		Reserved.
10	I2CBBUSY	I²C bus busy status bit. This bit is set to 1 when a start condition is detected on the I²C bus. This bit is cleared when a stop condition is detected on the bus.
9	I2CMRxFO	Master Rx FIFO overflow. This bit is set to 1 when a byte is written to the Rx FIFO when it is already full. This bit is cleared in all other conditions.
8	I2CMTC	I²C transmission complete status bit. This bit is set to 1 when a transmission is complete between the master and the slave it was communicating with. If the I2CMCENI bit in I2CxMCON is set, an interrupt is generated when this bit is set. Clear this bit to clear the interrupt source.
7	I2CMNA	I²C master NACK data bit. This bit is set to 1 when a NACK condition is received by the master in response to a data write transfer. If the I2CNACKENI bit in I2CxMCON is set, an interrupt is generated when this bit is set. This bit is cleared in all other conditions.
6	I2CMBUSY	I²C master busy status bit. Set to 1 when the master is busy processing a transaction. Cleared if the master is ready or if another master device has control of the bus.
5	I2CAL	I²C arbitration lost status bit. This bit is set to 1 when the I²C master is unable to gain control of the I²C bus. If the I2CALENI bit in I2CxMCON is set, an interrupt is generated when this bit is set. This bit is cleared in all other conditions.
4	I2CMNA	I²C master NACK address bit. This bit is set to 1 when a NACK condition is received by the master in response to an address. If the I2CNACKENI bit in I2CxMCON is set, an interrupt is generated when this bit is set. This bit is cleared in all other conditions.
3	I2CMRXQ	I²C master receive request bit. This bit is set to 1 when data enters the Rx FIFO. If the I2CMRENI in I2CxMCON is set, an interrupt is generated. This bit is cleared in all other conditions.
2	I2CMTXQ	I²C master transmit request bit. This bit goes high if the Tx FIFO is empty or contains only one byte and the master has transmitted an address + write. If the I2CMTENI bit in I2CxMCON is set, an interrupt is generated when this bit is set. This bit is cleared in all other conditions.
[1:0]	I2CMTFSTA	I²C master Tx FIFO status bits. 00 = I²C master Tx FIFO empty. 01 = one byte in master Tx FIFO. 10 = one byte in master Tx FIFO. 11 = I²C master Tx FIFO full.

PLACLK Register

Name: PLACLK

Address: 0xFFFF0B40

Default Value: 0x00

Access: Read/write

PLACLK is the clock selection for the flip-flops of Block 0 and Block 1. Note that the maximum frequency when using the GPIO pins as the clock input for the PLA blocks is 41.78 MHz.

Table 120. PLACLK MMR Bit Descriptions

Bit	Value	Description
7		Reserved.
[6:4]		Block 1 clock source selection.
	000	GPIO clock on P0.5.
	001	GPIO clock on P0.0.
	010	GPIO clock on P0.7.
	011	HCLK.
	100	OCLK (32.768 kHz).
	101	Timer1 overflow.
	110	UCLK.
	111	Internal 32,768 oscillator.
3		Reserved.
[2:0]		Block 0 clock source selection.
	000	GPIO clock on P0.5.
	001	GPIO clock on P0.0.
	010	GPIO clock on P0.7.
	011	HCLK.
	100	OCLK (32.768 kHz).
	101	Timer1 overflow.
	Other	Reserved.

PLAIRQ Register

Name: PLAIRQ

Address: 0xFFFF0B44

Default Value: 0x00000000

Access: Read/write

PLAIRQ enables IRQ0 and/or IRQ1 and selects the source of the IRQ.

Table 121. PLAIRQ MMR Bit Descriptions

Bit	Value	Description
[15:13]		Reserved.
12		PLA IRQ1 enable bit. Set by the user to enable IRQ1 output from PLA. Cleared by the user to disable IRQ1 output from PLA.
[11:8]		PLA IRQ1 source.
	0000	PLA Element 0.
	0001	PLA Element 1.
	1111	PLA Element 15.
[7:5]		Reserved.
4		PLA IRQ0 enable bit. Set by the user to enable IRQ0 output from PLA. Cleared by the user to disable IRQ0 output from PLA.
[3:0]		PLA IRQ0 source.
	0000	PLA Element 0.
	0001	PLA Element 1.
	1111	PLA Element 15.

Table 122. Feedback Configuration

Bit	Value	PLAELM0	PLAELM1 to PLAELM7	PLAELM8	PLAELM9 to PLAELM15
[10:9]	00	Element 15	Element 0	Element 7	Element 8
	01	Element 2	Element 2	Element 10	Element 10
	10	Element 4	Element 4	Element 12	Element 12
	11	Element 6	Element 6	Element 14	Element 14
[8:7]	00	Element 1	Element 1	Element 9	Element 9
	01	Element 3	Element 3	Element 11	Element 11
	10	Element 5	Element 5	Element 13	Element 13
	11	Element 7	Element 7	Element 15	Element 15

IRQEN Register

IRQEN provides the value of the current enable mask. When a bit is set to 1, the corresponding source request is enabled to create an IRQ exception. When a bit is set to 0, the corresponding source request is disabled or masked, which does not create an IRQ exception. The IRQEN register cannot be used to disable an interrupt.

IRQEN Register

Name: IRQEN

Address: 0xFFFF0008

Default Value: 0x00000000

Access: Read/write

IRQCLR Register

IRQCLR is a write-only register that allows the IRQEN register to clear to mask an interrupt source. Each bit that is set to 1 clears the corresponding bit in the IRQEN register without affecting the remaining bits. The pair of registers, IRQEN and IRQCLR, allow independent manipulation of the enable mask without requiring an atomic read-modify-write.

This register should be used to disable an interrupt source only during the following conditions:

- In the interrupt sources interrupt service routine.
- When the peripheral is temporarily disabled by its own control register.

This register should not be used to disable an IRQ source if that IRQ source has an interrupt pending or may have an interrupt pending.

IRQCLR Register

Name: IRQCLR

Address: 0xFFFF000C

Default Value: 0x00000000

Access: Write only

FAST INTERRUPT REQUEST (FIQ)

The fast interrupt request (FIQ) is the exception signal to enter the FIQ mode of the processor. It is provided to service data transfer or communication channel tasks with low latency. The FIQ interface is identical to the IRQ interface and provides the second level interrupt (highest priority). Four 32-bit registers are dedicated to FIQ: FIQSIG, FIQEN, FIQCLR, and FIQSTA.

Bit 31 to Bit 1 of FIQSTA are logically OR'ed to create the FIQ signal to the core and to Bit 0 of both the FIQ and IRQ registers (FIQ source).

The logic for FIQEN and FIQCLR does not allow an interrupt source to be enabled in both IRQ and FIQ masks. A bit set to 1 in FIQEN clears, as a side effect, the same bit in IRQEN. Likewise, a bit set to 1 in IRQEN clears, as a side effect, the same bit in FIQEN. An interrupt source can be disabled in both the IRQEN and FIQEN masks.

FIQSIG

FIQSIG reflects the status of the different FIQ sources. If a peripheral generates an FIQ signal, the corresponding bit in the FIQSIG is set; otherwise, it is cleared. The FIQSIG bits are cleared when the interrupt in the particular peripheral is cleared. All FIQ sources can be masked in the FIQEN MMR. FIQSIG is read only.

FIQSIG Register

Name: FIQSIG

Address: 0xFFFF0104

Default Value: 0x00000000

Access: Read only

FIQEN

FIQEN provides the value of the current enable mask. When a bit is set to 1, the corresponding source request is enabled to create an FIQ exception. When a bit is set to 0, the corresponding source request is disabled or masked, which does not create an FIQ exception. The FIQEN register cannot be used to disable an interrupt.

FIQEN Register

Name: FIQEN

Address: 0xFFFF0108

Default Value: 0x00000000

Access: Read/write

FIQCLR

FIQCLR is a write-only register that allows the FIQEN register to clear to mask an interrupt source. Each bit that is set to 1 clears the corresponding bit in the FIQEN register without affecting the remaining bits. The pair of registers, FIQEN and FIQCLR, allows independent manipulation of the enable mask without requiring an atomic read-modify-write.

This register should be used to disable an interrupt source only during the following conditions:

- In the interrupt sources interrupt service routine.
- The peripheral is temporarily disabled by its own control register.

This register should not be used to disable an IRQ source if that IRQ source has an interrupt pending or may have an interrupt pending.

FIQCLR Register

Name: FIQCLR

Address: 0xFFFF010C

Default Value: 0x00000000

Access: Write only

FIQSTA

FIQSTA is a read-only register that provides the current enabled FIQ source status (effectively a logic AND of the FIQSIG and FIQEN bits). When set to 1, that source generates an active FIQ request to the ARM7TDMI core. There is no priority encoder or interrupt vector generation. This function is implemented in software in a common interrupt handler routine.

FIQSTA Register

Name: FIQSTA

Address: 0xFFFF0100

Default Value: 0x00000000

Access: Read only

Programmed Interrupts

Because the programmed interrupts are not maskable, they are controlled by another register (SWICFG) that writes into the IRQSTA and IRQSIG registers and/or the FIQSTA and FIQSIG registers at the same time.

The 32-bit register dedicated to software interrupt is SWICFG (described in Table 127). This MMR allows control of a programmed source interrupt.

Table 127. SWICFG MMR Bit Descriptions

Bit	Description
[31:3]	Reserved.
2	Programmed interrupt FIQ. Setting/clearing this bit corresponds to setting/clearing Bit 1 of FIQSTA and FIQSIG.
1	Programmed interrupt IRQ. Setting/clearing this bit corresponds to setting/clearing Bit 1 of IRQSTA and IRQSIG.
0	Reserved.

Any interrupt signal must be active for at least the minimum interrupt latency time to be detected by the interrupt controller and to be detected by the user in the IRQSTA/FIQSTA register.

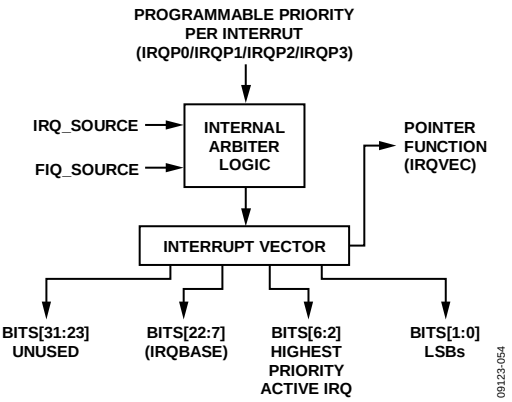

Figure 52. Interrupt Structure

VECTORED INTERRUPT CONTROLLER (VIC)

The ADuC7124/ADuC7126 incorporate an enhanced interrupt control system or (vectored interrupt controller). The vectored interrupt controller for IRQ interrupt sources is enabled by setting Bit 0 of the IRQCONN register. Similarly, Bit 1 of IRQCONN enables the vectored interrupt controller for the FIQ interrupt sources. The vectored interrupt controller provides the following enhancements to the standard IRQ/FIQ interrupts:

- Vectored interrupts—allows a user to define separate interrupt service routine addresses for every interrupt source. This is achieved by using the IRQBASE and IRQVEC registers.
- IRQ/FIQ interrupts—can be nested up to eight levels depending on the priority settings. An FIQ still has a higher priority than an IRQ. Therefore, if the VIC is enabled for both the FIQ and IRQ and prioritization is maximized, it is possible to have 16 separate interrupt levels.
- Programmable interrupt priorities—using the IRQP0 to IRQP3 registers, an interrupt source can be assigned an interrupt priority level value between 0 and 7.

VIC MMRs

IRQBASE Register

The vector base register, IRQBASE, is used to point to the start address of memory used to store 32 pointer addresses. These pointer addresses are the addresses of the individual interrupt service routines.

Name: IRQBASE

Address: 0xFFFF0014

Default Value: 0x00000000

Access: Read/write

Table 128. IRQBASE MMR Bit Descriptions

Bit	Type	Initial Value	Description
[31:16]	Read only	Reserved	Always read as 0.
[15:0]	R/W	0	Vector base address.

FIQVEC Register

The FIQ interrupt vector register, FIQVEC, points to a memory address containing a pointer to the interrupt service routine of the currently active FIQ. This register should be read only when an FIQ occurs and FIQ interrupt nesting has been enabled by setting Bit 1 of the IRQCONN register.

Name: FIQVEC

Address: 0xFFFF011C

Default Value: 0x00000000

Access: Read only

Table 136. FIQVEC MMR Bit Descriptions

Bit	Type	Initial Value	Description
[31:23]	R	0	Always read as 0.
[22:7]	R/W	0	IRQBASE register value.
[6:2]		0	Highest priority source. This is a value between 0 and 27, representing the currently active interrupt source. The interrupts are listed in Table 126. For example, if the highest currently active FIQ is Timer2, then these bits are [00100].
[1:0]		0	Reserved.

FIQSTAN Register

If IRQCONN Bit 1 is asserted and FIQVEC is read, one of the FIQSTAN[7:0] bits is asserted. The bit that asserts depends on the priority of the FIQ. If the FIQ is of Priority 0, Bit 0 asserts, if Priority 1, Bit 1 asserts, and so forth.

When a bit is set in this register all interrupts of that priority and lower are blocked.

To clear a bit in this register, all bits of a higher priority must be cleared first. It is possible to clear only one bit at a time. For example, if this register is set to 0x09, then writing 0xFF changes the register to 0x08 and writing 0xFF a second time changes the register to 0x00.

Name: FIQSTAN

Address: 0xFFFF013C

Default Value: 0x00000000

Access: Read/write

Table 137. FIQSTAN MMR Bit Descriptions

Bit	Name	Description
31:8		Reserved. These bits are reserved and should not be written to.
7:0		Setting this bit to 1 enables nesting of FIQ interrupts. Clearing this bit means no nesting or prioritization of FIQs is allowed.

External Interrupts and PLA interrupts

The ADuC7124/ADuC7126 provide up to four external interrupt sources and two PLA interrupt sources. These external interrupts can be individually configured as level or rising/falling edge triggered.

To enable the external interrupt source or the PLA interrupt source, the appropriate bit must first be set in the FIQEN or IRQEN register. To select the required edge or level to trigger on, the IRQCONE register must be appropriately configured.

To properly clear an edge-based external IRQ interrupt or an edge-based PLA interrupt, set the appropriate bit in the IRQCLRE register.

IRQCONE Register

Name: IRQCONE

Address: 0xFFFF0034

Default Value: 0x00000000

Access: Read/write

Table 138. IRQCONE MMR Bit Descriptions

Bit	Value	Name	Description
[31:12]			Reserved. These bits are reserved and should not be written to.
[11:10]	11	PLA1SRC[1:0]	PLA IRQ1 triggers on falling edge.
	10		PLA IRQ1 triggers on rising edge.
	01		PLA IRQ1 triggers on low level.
	00		PLA IRQ1 triggers on high level.
[9:8]	11	IRQ3SRC[1:0]	External IRQ3 triggers on falling edge.
	10		External IRQ3 triggers on rising edge.
	01		External IRQ3 triggers on low level.
	00		External IRQ3 triggers on high level.

Timer2 Clear Register

Name: T2CLRI

Address: 0xFFFF034C

Default Value: 0x00

Access: Write only

This 8-bit write-only MMR is written (with any value) by user code to refresh (reload) Timer2.

Timer2 Value Register

Name: T2VAL

Address: 0xFFFF0344

Default Value: 0x0000

Access: Read only

T2VAL is a 32-bit register that holds the current value of Timer2.

Timer2 Control Register

Name: T2CON

Address: 0xFFFF0348

Default Value: 0x0000

Access: Read/write

This 32-bit MMR configures the mode of operation for Timer2.

Table 144. T2CON MMR Bit Descriptions

Bit	Value	Description
[31:11]		Reserved.
10:9]		Clock source select.
	00	External 32.768 kHz watch crystal (default).
	01	External 32.768 kHz watch crystal.
	10	Internal 32.768 kHz oscillator.
	11	HCLK.
8		Count up. Set by the user for Timer2 to count up. Cleared by the user for Timer2 to count down (default).
7		Timer2 enable bit. Set by the user to enable Timer2. Cleared by the user to disable Timer2 (default).
6		Timer2 mode. Set by the user to operate in periodic mode. Cleared by the user to operate in free-running mode (default).
[5:4]		Format.
	00	Binary (default).
	01	Reserved.
	10	Hr: min: sec: hundredths (23 hours to 0 hours).
	11	Hr: min: sec: hundredths (255 hours to 0 hours).
[3:0]		Prescaler.
	0000	Source clock/1 (default).
	0100	Source clock/16.
	1000	Source clock/256.
	1111	Source clock/32,768.

POWER-ON RESET OPERATION

An internal power-on reset (POR) is implemented on the ADuC7124/ADuC7126. For LV_{DD} below 2.40 V typical, the internal POR holds the part in reset. As LV_{DD} rises above 2.41 V, an internal timer times out for typically 128 ms before the part is released from reset. The user must ensure that the power supply, IOV_{DD}, reaches a stable 2.7 V minimum level by this time. Likewise, on power-down, the internal POR holds the part in reset until LV_{DD} drops below 2.40 V. Figure 69 illustrates the operation of the internal POR in detail.

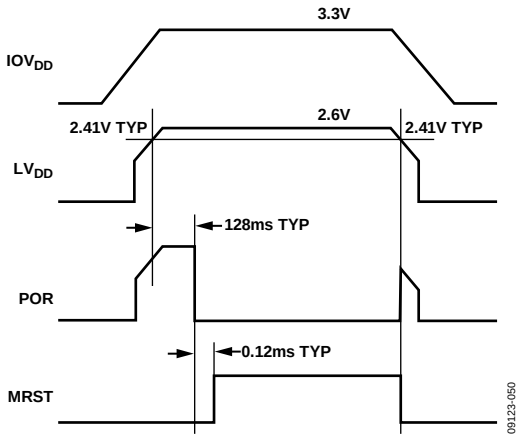

Figure 69. Internal Power-On Reset Operation