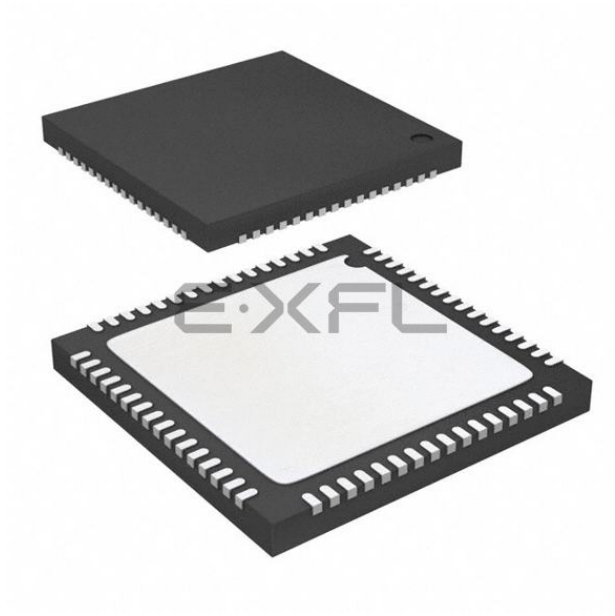

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	41.78MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	30
Program Memory Size	126KB (63K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 32
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad, CSP
Supplier Device Package	64-LFCSP-VQ (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc7124bcpz126

9/10—Revision 0: Initial Version

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ESD TESTS					2.5 V reference, T_A = 25°C
HBM Passed Up To			3	kV	
FICDM Passed Up To			1.5	kV	

[1] All ADC channel specifications are guaranteed during normal core operation.
[2] Apply to all ADC input channels.
[3] Measured using the factory-set default values in the ADC offset register (ADCOF) and gain coefficient register (ADCGN).
[4] Not production tested but supported by design and/or characterization data on production release.
[5] Measured using the factory-set default values in ADCOF and ADCGN with an external AD845 op amp as an input buffer stage as shown in Figure 37. Based on external ADC system components, the user may need to execute a system calibration to remove external endpoint errors and achieve these specifications (see the Calibration section).
[6] The input signal can be centered on any dc common-mode voltage (V_{CM}) as long as this value is within the ADC voltage input range specified.
[7] DAC linearity is calculated using a reduced code range of 100 to 3995.
[8] DAC gain error is calculated using a reduced code range of 100 to internal 2.5 V V_{REF}.
[9] Endurance is qualified as per JEDEC Standard 22 Method A117 and measured at −40°C, +25°C, +85°C, and +125°C.
[10] Retention lifetime equivalent at junction temperature (T_J) = 85°C as per JEDEC Standard 22 Method A117. Retention lifetime derates with junction temperature.
[11] Test carried out with a maximum of eight I/Os set to a low output level.
[12] Power supply current consumption is measured in normal, pause, and sleep modes under the following conditions: normal mode with 3.6 V supply, pause mode with 3.6 V supply, and sleep mode with 3.6 V supply.
[13] IOV_{DD} power supply current increases typically by 2 mA during a Flash/EE erase cycle.
[14] This current must be added to the AV_{DD} current.

TIMING SPECIFICATIONS

I²C Timing

Table 2. I²C Timing in Fast Mode (400 kHz)

		Slave		Master	
Parameter	Description	Min	Max	Typ	Unit
t_L	SCL low pulse width	200		1360	ns
t_H	SCL high pulse width	100		1140	ns
t_{SHD}	Start condition hold time	300			ns
t_{DSU}	Data setup time	100		740	ns
t_{DHD}	Data hold time	0		400	ns
t_{RSU}	Setup time for repeated start	100			ns
t_{PSU}	Stop condition setup time	100		800	ns
t_{BUF}	Bus-free time between a stop condition and a start condition	1.3			µs
t_R	Rise time for both SCL and SDA		300	200	ns
t_F	Fall time for both SCL and SDA		300		ns

Table 3. I²C Timing in Standard Mode (100 kHz)

		Slave		
Parameter	Description	Min	Max	Unit
t_L	SCL low pulse width	4.7		µs
t_H	SCL high pulse width	4.0		ns
t_{SHD}	Start condition hold time	4.0		µs
t_{DSU}	Data setup time	250		ns
t_{DHD}	Data hold time	0	3.45	µs
t_{RSU}	Setup time for repeated start	4.7		µs
t_{PSU}	Stop condition setup time	4.0		µs
t_{BUF}	Bus-free time between a stop condition and a start condition	4.7		µs
t_R	Rise time for both SCL and SDA		1	µs
t_F	Fall time for both SCL and SDA		300	ns

Table 6. SPI Slave Mode Timing (Phase Mode = 1)

Parameter	Description	Min	Typ	Max	Unit
$t_{\overline{CS}}$	$\overline{CS}$ to SCLK edge	200			ns
t_{SL}	SCLK low pulse width		(SPIDIV + 1) × t_{HCLK}		ns
t_{SH}	SCLK high pulse width		(SPIDIV + 1) × t_{HCLK}		ns
t_{DAV}	Data output valid after SCLK edge			25	ns
t_{DSU}	Data input setup time before SCLK edge[1]	1 × t_{UCLK}			ns
t_{DHD}	Data input hold time after SCLK edge[1]	2 × t_{UCLK}			ns
t_{DF}	Data output fall time		5	12.5	ns
t_{DR}	Data output rise time		5	12.5	ns
t_{SR}	SCLK rise time		5	12.5	ns
t_{SF}	SCLK fall time		5	12.5	ns
t_{SFS}	$\overline{CS}$ high after SCLK edge	0			ns

[1] t_{UCLK} = 23.9 ns. It corresponds to the 41.78 MHz internal clock from the PLL before the clock divider.

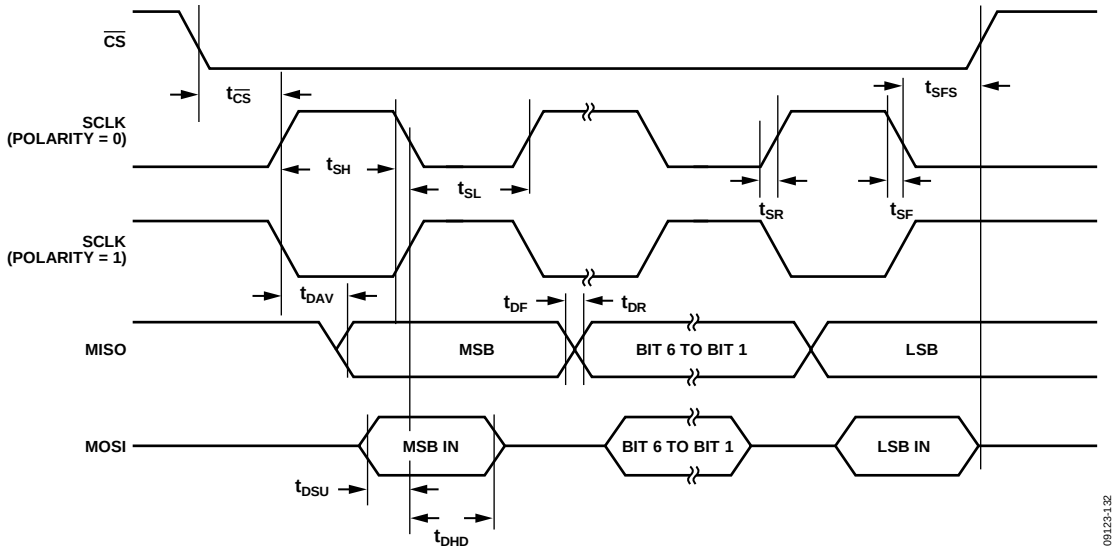

Figure 5. SPI Slave Mode Timing (Phase Mode = 1)

ABSOLUTE MAXIMUM RATINGS

AGND = GND_{REF} = DACGND = GND_{REF}, T_A = 25°C, unless otherwise noted.

Table 8.

Parameter	Rating
AV_{DD} to IOV_{DD}	−0.3 V to +0.3 V
AGND to DGND	−0.3 V to +0.3 V
IOV_{DD} to IOGND, AV_{DD} to AGND	−0.3 V to +6 V
Digital Input Voltage to IOGND	−0.3 V to +5.3 V
Digital Output Voltage to IOGND	−0.3 V to IOV_{DD} + 0.3 V
V_{REF} to AGND	−0.3 V to AV_{DD} + 0.3 V
Analog Inputs to AGND	−0.3 V to AV_{DD} + 0.3 V
Analog Outputs to AGND	−0.3 V to AV_{DD} + 0.3 V
Operating Temperature Range, Industrial	–40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance	
64-Lead LFCSP	24°C/W
80-Lead LQFP	38°C/W
Peak Solder Reflow Temperature	
SnPb Assemblies (10 sec to 30 sec)	240°C
RoHS Compliant Assemblies (20 sec to 40 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Pin No.	Mnemonic	Description
11	DAC0/ADC12	DAC0 Voltage Output (DAC0). Single-Ended or Differential Analog Input 12 (ADC12).
12	DAC1/ADC13	DAC1 Voltage Output (DAC1). Single-Ended or Differential Analog Input 13 (ADC13).
13	DAC2/ADC14	DAC2 Voltage Output (DAC2). Single-Ended or Differential Analog Input 14 (ADC14).
14	DAC3/ADC15	DAC3 Voltage Output (DAC3). Single-Ended or Differential Analog Input 15 (ADC15).
15	TMS	JTAG Test Port Input, Test Mode Select. Debug and download access.
16	TDI	JTAG Test Port Input, Test Data In. Debug and download access.
17	P0.1/PWM4/$\overline{BLE}$	General-Purpose Input and Output Port 0.1 (P0.1). PWM Phase 4 (PWM4). External Memory Byte Low Enable ($\overline{BLE}$). This pin does not work as GPIO on I²C versions of the chip.
18	XCLKO	Output from the Crystal Oscillator Inverter.
19	XCLKI	Input to the Crystal Oscillator Inverter and Input to the Internal Clock Generator Circuits.
20	BM/P0.0/CMP_{OUT}/PLAI[7]/MS0	Multifunction I/O Pin. Boot Mode Entry Pin (BM). The ADuC7126 enters UART download mode if BM is low at reset and executes code if BM is pulled high at reset through a 1 kΩ resistor.. The ADuC7126 enters I²C download mode in I²C version parts if BM is low at reset with a flash address of 0x800014 = 0xFFFFFFFF. The ADuC7126 executes code if BM is pulled high at reset or if BM is low at reset with a flash address 0x800014 ≠ 0xFFFFFFFF. General-Purpose Input and Output Port 0.0 (P0.0). Voltage Comparator Output/Programmable Logic Array Input Element 7 (CMP_{OUT}). External Memory Select 0 (MS0). By default, this pin is configured as GPIO.
21	DGND	Ground for Core Logic.
22	LV_{DD}	2.6 V Output of the On-Chip Voltage Regulator. This output must be connected to a 0.47 µF capacitor to DGND only.
23	IOV_{DD}	3.3 V Supply for GPIO and Input of the On-Chip Voltage Regulator.
24	IOGND	Ground for GPIO. Typically connected to DGND.
25	P4.6/AD14/PLAO[14]	General-Purpose Input and Output Port 4.6 (P4.6). External Memory Interface (AD14). Programmable Logic Array Output Element 14 (PLAO[14]).
26	P4.7/AD15/PLAO[15]	General-Purpose Input and Output Port 4.7 (P4.7). External Memory Interface (AD15). Programmable Logic Array Output Element 15 (PLAO[15]).
27	P0.6/T1/MRST/PLAO[3]/MS3	Multifunction Pin, Driven Low After Reset. General-Purpose Output Port 0.6 (P0.6). Timer1 Input (T1). Power-On Reset Output (MRST). Programmable Logic Array Output Element 3 (PLAO[3]). External Memory Select 3 (MS3).
28	TCK	JTAG Test Port Input, Test Clock. Debug and download access.
29	TDO	JTAG Test Port Output, Test Data Out. Debug and download access.
30	P0.2/PWM5/$\overline{BHE}$	General-Purpose Input and Output Port 0.2 (P0.2). PWM Phase 5 (PWM5). External Memory Byte High Enable ($\overline{BHE}$). This pin does not work as GPIO on I²C versions of the chip.
31	P3.0/AD0/PWM0/PLAI[8]	General-Purpose Input and Output Port 3.0 (P3.0). External Memory Interface (AD0). PWM Phase 0 (PWM0). Programmable Logic Array Input Element 8 (PLAI[8]).
32	P3.1/AD1/PWM1/PLAI[9]	General-Purpose Input and Output Port 3.1 (P3.1). External Memory Interface (AD1). PWM Phase 1 (PWM1). Programmable Logic Array Input Element 9 (PLAI[9]).

Pin No.	Mnemonic	Description
33	P3.2/AD2/PWM2/PLAI[10]	General-Purpose Input and Output Port 3.2 (P3.2). External Memory Interface (AD2). PWM Phase 2 (PWM2). Programmable Logic Array Input Element 10 (PLAI[10]).
34	P3.3/AD3/PWM3/PLAI[11]	General-Purpose Input and Output Port 3.3 (P3.3). External Memory Interface (AD3). PWM Phase 3 (PWM3). Programmable Logic Array Input Element 11 (PLAI[11]).
35	P2.4/SPM13/PWM0/MS0/SOUT1	General-Purpose Input and Output Port 2.4 (P2.4). Serial Port Multiplexed (SPM13) PWM Phase 0 (PWM0). External Memory Select 0 (MS0). UART1 Output (SOUT1).
36	P0.3/TRST/A16/ADC_{BUSY}	General-Purpose Input and Output Port 0.3 (P0.3). JTAG Test Port Input, Test Reset (TRST).JTAG Reset Input. Debug and download access. If this pin is held low, JTAG access is not possible because the JTAG interface is held in reset and P0.1/P0.2/P0.3 are configured as GPIO pins. Address Line (A16). ADC_{BUSY} Signal Output (ADC_{BUSY}).
37	P2.5/PWM1/MS1	General-Purpose Input and Output Port 2.5 (P2.5). PWM Phase 1 (PWM1). External Memory Select 1 (MS1).
38	P2.6/PWM2/MS2	General-Purpose Input and Output Port 2.6 (P2.6). PWM Phase 2 (PWM2). External Memory Select 2 (MS2).
39	P3.4/AD4/PWM4/PLAI[12]	General-Purpose Input and Output Port 3.4 (P3.4). External Memory Interface (AD4). PWM Phase 4 (PWM4). Programmable Logic Array Input 12 (PLAI[12]).
40	P3.5/AD5/PWM5/PLAI[13]	General-Purpose Input and Output Port 3.5 (P3.5). External Memory Interface (AD5). PWM Phase 5 (PWM5). Programmable Logic Array Input Element 13 (PLAI[13]).
41	$\overline{RST}$	Reset Input, Active Low.
42	IRQ0/P0.4/PWM_{TRIP}/PLAO[1]/MS1	Multifunction I/O Pin. External Interrupt Request 0, Active High (IRQ0). General-Purpose Input and Output Port 0.4 (P0.4). PWM Trip External Input (PWM_{TRIP}). Programmable Logic Array Output Element 1 (PLAO[1]). External Memory Select 1 (MS1)..
43	IRQ1/P0.5/ADC_{BUSY}/PLAO[2]/MS2	Multifunction I/O Pin. External Interrupt Request 1, Active High (IRQ1). General-Purpose Input and Output Port 0.5 (P0.5). ADC_{BUSY} Signal Output (ADC_{BUSY}). Programmable Logic Array Output Element 2 (PLAO[2]). External Memory Select 2 (MS2).
44	P2.7/PWM3/MS3	General-Purpose Input and Output Port 2.7 (P2.7). PWM Phase 3 (PWM3). External Memory Select 3 (MS3).
45	P2.0/SPM9/PLAO[5]/$CONV_{START}$/SOUT0	General-Purpose Input and Output Port 2.0 (P2.0). Serial Port Multiplexed (SPM9). Programmable Logic Array Output Element 5 (PLAO[5]). Start Conversion Input Signal for ADC ($CONV_{START}$). UART0 Output (SOUT0).
46	P0.7/SPM8/ECLK/XCLK/PLAO[4]/SIN0	General-Purpose Input and Output Port 0.7 (P0.7). Serial Port Multiplexed (SPM8). Output for External Clock Signal (ECLK). Input to the Internal Clock Generator Circuits (XCLK). Programmable Logic Array Output Element 4 (PLAO[4]). UART0 Input (SIN0).
47	IOGND	Ground for GPIO. Typically connected to DGND.

MEMORY ORGANIZATION

The ADuC7124/ADuC7126 incorporate three separate blocks of memory: 32 kB of SRAM and two 64 kB blocks of on-chip Flash/EE memory. There are 126 kB of on-chip Flash/EE memory available to the user, and the remaining 2 kB are reserved for the system kernel. These blocks are mapped as shown in Figure 24.

Note that, by default, after a reset, the Flash/EE memory is mirrored at Address 0x00000000. It is possible to remap the SRAM at Address 0x00000000 by clearing Bit 0 of the REMAP MMR. This remap function is described in more detail in the Flash/EE memory chapter.

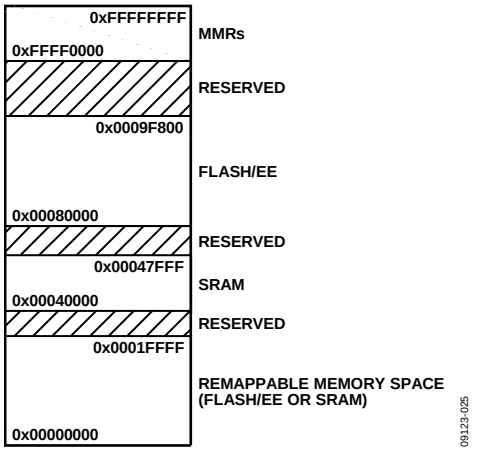

Figure 24. Physical Memory Map

MEMORY ACCESS

The ARM7 core sees memory as a linear array of a 2^{32} byte location where the different blocks of memory are mapped as outlined in Figure 24.

The ADuC7124/ADuC7126 memory organization is configured in little endian format: the least significant byte is located in the lowest byte address and the most significant byte in the highest byte address.

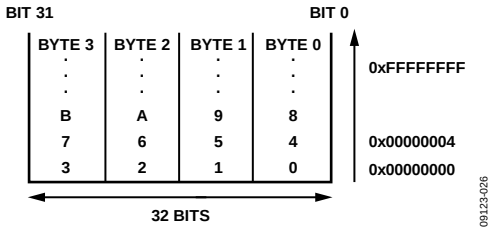

Figure 25. Little Endian Format

FLASH/EE MEMORY

The 128 kB of Flash/EE are organized as two banks of 32 k × 16 bits. Block 0 starts at Address 0x90000 and finishses at Address 0x9F700. In this block, 31 k × 16 bits is user space and 1 k × 16 bits is reserved for the factory-configured boot page. The page size of this Flash/EE memory is 512 bytes.

Block 1 starts at Address 0x80000 and finishses at Address 0x90000. In this block, all 64 kB are available as user space. The block is arranged in 32 k × 16 bits.

The 126 kB of Flash/EE are available to the user as code and nonvolatile data memory. There is no distinction between data and program because ARM code shares the same space. The real width of the Flash/EE memory is 16 bits, meaning that, in ARM mode (32-bit instruction), two accesses to the Flash/EE are necessary for each instruction fetch. Therefore, it is recommended that Thumb mode be used when executing from Flash/EE memory for optimum access speed. The maximum access speed for the Flash/EE memory is 41.78 MHz in Thumb mode and 20.89 MHz in full ARM mode (see the Execution Time from SRAM and Flash/EE section).

SRAM

The 32 kB of SRAM are available to the user, organized as 8 k × 32 bits, that is, 16 k words. ARM code can run directly from SRAM at 41.78 MHz, given that the SRAM array is configured as a 32-bit wide memory array (see the Execution Time from SRAM and Flash/EE section).

MEMORY MAPPED REGISTERS

The memory mapped register (MMR) space is mapped into the upper two pages of the memory array and accessed by indirect addressing through the ARM7 banked registers.

The MMR space provides an interface between the CPU and all on-chip peripherals. All registers except the core registers reside in the MMR area. All shaded locations shown in Figure 26 are unoccupied or reserved locations and should not be accessed by user software. Table 11 to Table 29 show the full MMR memory map.

The access time reading or writing a MMR depends on the advanced microcontroller bus architecture (AMBA) bus used to access the peripheral. The processor has two AMBA buses: the advanced high performance bus (AHB) used for system modules, and the advanced peripheral bus (APB) used for the lower performance peripheral. Access to the AHB is one cycle, and access to the APB is two cycles. All peripherals on the ADuC7124/ADuC7126 are on the APB except the Flash/EE memory and the GPIOs.

Table 11. IRQ Base Address = 0xFFFF0000

Address	Name	Byte	Access Type
0xFFFF0000	IRQSTA	4	R
0xFFFF0004	IRQSIG	4	R
0xFFFF0008	IRQEN	4	R/W
0xFFFF000C	IRQCLR	4	W
0xFFFF0010	SWICFG	4	W
0xFFFF0014	IRQBASE	4	R/W
0xFFFF001C	IRQVEC	4	R
0xFFFF0020	IRQP0	4	R/W
0xFFFF0024	IRQP1	4	R/W
0xFFFF0028	IRQP2	4	R/W
0xFFFF002C	IRQP3	4	R/W
0xFFFF0030	IRQCONN	1	R/W
0xFFFF0034	IRQCONE	4	R/W
0xFFFF0038	IRQCLRE	1	W
0xFFFF003C	IRQSTAN	1	R/W
0xFFFF0100	FIQSTA	4	R
0xFFFF0104	FIQSIG	4	R
0xFFFF0108	FIQEN	4	R/W
0xFFFF010C	FIQCLR	4	W
0xFFFF011C	FIQVEC	4	R
0xFFFF013C	FIQSTAN	1	R/W

Table 12. System Control Base Address = 0xFFFF0200

Address	Name	Byte	Access Type
0xFFFF0220	REMAP	1	R/W
0xFFFF0230	RSTSTA	1	R
0xFFFF0234	RSTCLR	1	W
0xFFFF0248	RSTKEY0	1	W
0xFFFF024C	RSTCFG	1	R/W
0xFFFF0250	RSTKEY1	1	W

Table 13. Timer Base Address = 0xFFFF0300

Address	Name	Byte	Access Type
0xFFFF0300	T0LD	2	R/W
0xFFFF0304	T0VAL	2	R
0xFFFF0308	T0CON	2	R/W
0xFFFF030C	T0CLRI	1	W
0xFFFF0320	T1LD	4	R/W
0xFFFF0324	T1VAL	4	R
0xFFFF0328	T1CON	2	R/W
0xFFFF032C	T1CLRI	1	W
0xFFFF0330	T1CAP	4	R
0xFFFF0340	T2LD	4	R/W
0xFFFF0344	T2VAL	4	R
0xFFFF0348	T2CON	2	R/W
0xFFFF034C	T2CLRI	1	W
0xFFFF0360	T3LD	2	R/W
0xFFFF0364	T3VAL	2	R
0xFFFF0368	T3CON	2	R/W
0xFFFF036C	T3CLRI	1	W

Table 22. I2C1 Base Address = 0xFFFF0900

Address	Name	Byte	Access Type	Cycle
0xFFFF0900	I2C1MCON	2	R/W	2
0xFFFF0904	I2C1MSTA	2	R	2
0xFFFF0908	I2C1MRX	1	R	2
0xFFFF090C	I2C1MTX	2	R/W	2
0xFFFF0910	I2C1MCNT0	2	R/W	2
0xFFFF0914	I2C1MCNT1	1	R	2
0xFFFF0918	I2C1ADR0	1	R/W	2
0xFFFF091C	I2C1ADR1	1	R/W	2
0xFFFF0924	I2C1DIV	2	R/W	2
0xFFFF0928	I2C1SCON	2	R/W	2
0xFFFF092C	I2C1SSTA	2	R	2
0xFFFF0930	I2C1SRX	1	R	2
0xFFFF0934	I2C1STX	1	W	2
0xFFFF0938	I2C1ALT	1	R/W	2
0xFFFF093C	I2C1ID0	1	R/W	2
0xFFFF0940	I2C1ID1	1	R/W	2
0xFFFF0944	I2C1ID2	1	R/W	2
0xFFFF0948	I2C1ID3	1	R/W	2
0xFFFF094C	I2C1FSTA	1	R/W	2

Table 23. SPI Base Address = 0xFFFF0A00

Address	Name	Byte	Access Type	Cycle
0xFFFF0A00	SPISTA	2	R	2
0xFFFF0A04	SPIRX	1	R	2
0xFFFF0A08	SPITX	1	W	2
0xFFFF0A0C	SPIDIV	1	R/W	2
0xFFFF0A10	SPICON	2	R/W	2

Table 24. PLA Base Address = 0xFFFF0B00

Address	Name	Byte	Access Type	Cycle
0xFFFF0B00	PLAELM0	2	R/W	2
0xFFFF0B04	PLAELM1	2	R/W	2
0xFFFF0B08	PLAELM2	2	R/W	2
0xFFFF0B0C	PLAELM3	2	R/W	2
0xFFFF0B10	PLAELM4	2	R/W	2
0xFFFF0B14	PLAELM5	2	R/W	2
0xFFFF0B18	PLAELM6	2	R/W	2
0xFFFF0B1C	PLAELM7	2	R/W	2
0xFFFF0B20	PLAELM8	2	R/W	2
0xFFFF0B24	PLAELM9	2	R/W	2
0xFFFF0B28	PLAELM10	2	R/W	2
0xFFFF0B2C	PLAELM11	2	R/W	2
0xFFFF0B30	PLAELM12	2	R/W	2
0xFFFF0B34	PLAELM13	2	R/W	2
0xFFFF0B38	PLAELM14	2	R/W	2
0xFFFF0B3C	PLAELM15	2	R/W	2
0xFFFF0B40	PLACLK	1	R/W	2
0xFFFF0B44	PLAIRQ	2	R/W	2
0xFFFF0B48	PLAADC	4	R/W	2
0xFFFF0B4C	PLADIN	4	R/W	2
0xFFFF0B50	PLADOUT	4	R	2
0xFFFF0B54	PLALCK	1	W	2

DACBKEY1 Register

Name: DACBKEY1

Address: 0xFFFF0650

Default Value: 0x0000

Access: Write

DACBKEY2 Register

Name: DACBKEY2

Address: 0xFFFF0658

Default Value: 0x0000

Access: Write

POWER SUPPLY MONITOR

The power supply monitor regulates the IOV_{DD} supply on the ADuC7124/ADuC7126. It indicates when the IOV_{DD} supply pin drops below one of two supply trip points. The monitor function is controlled via the PSMCON register. If enabled in the IRQEN or FIQEN register, the monitor interrupts the core using the PSMI bit in the PSMCON MMR. This bit is immediately cleared when CMP goes high.

This monitor function allows the user to save working registers to avoid possible data loss due to low supply or brown-out conditions. It also ensures that normal code execution does not resume until a safe supply level is established.

PSMCON Register

Name: PSMCON

Address: 0xFFFF0440

Default Value: 0x0008

Access: Read/write

Table 68. PSMCON MMR Bit Descriptions

Bit	Name	Description
3	CMP	Comparator bit. This is a read-only bit that directly reflects the state of the comparator. Read 1 indicates that the IOV_{DD} supply is above its selected trip point or that the PSM is in power-down mode. Read 0 indicates that the IOV_{DD} supply is below its selected trip point. This bit should be set before leaving the interrupt service routine.
2	TP	Trip point selection bits. 0 = 2.79 V, 1 = 3.07 V.
1	PSMEN	Power supply monitor enable bit. Set to 1 to enable the power supply monitor circuit. Clear to 0 to disable the power supply monitor circuit.
0	PSMI	Power supply monitor interrupt bit. This bit is set high by the MicroConverter when CMP goes low, indicating low I/O supply. The PSMI bit can be used to interrupt the processor. When CMP returns high, the PSMI bit can be cleared by writing a 1 to this location. A 0 write has no effect. There is no timeout delay; PSMI can be immediately cleared when CMP goes high.

COMPARATOR

The ADuC7124/ADuC7126 integrate a voltage comparator. The positive input is multiplexed with ADC2, and the negative input has two options: ADC3 or DAC0. The output of the comparator can be configured to generate a system interrupt, be routed directly to the programmable logic array, start an ADC conversion, or be on an external pin, CMP_{OUT}, as shown in Figure 43.

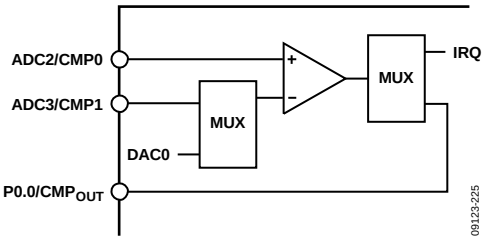

Figure 43. Comparator

Hysteresis

Figure 44 shows how the input offset voltage and hysteresis terms are defined. Input offset voltage (V_{OS}) is the difference between the center of the hysteresis range and the ground level. This can either be positive or negative. The hysteresis voltage (V_H) is ½ the width of the hysteresis range.

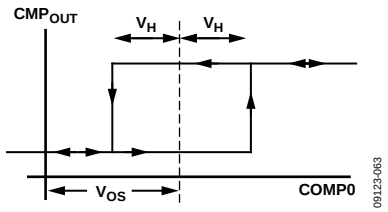

Figure 44. Comparator Hysteresis Transfer Function

Table 79. GPxCON Registers

Name	Address	Default Value	Access
GP0CON	0xFFFFF400	0x00000000	R/W
GP1CON	0xFFFFF404	0x00000000	R/W
GP2CON	0xFFFFF408	0x00000000	R/W
GP3CON	0xFFFFF40C	0x00000000	R/W
GP4CON	0xFFFFF410	0x00000000	R/W

GPxCON are the Port x control registers that select the function of each pin of Port x, as described in Table 80.

Table 80. GPxCON MMR Bit Descriptions

Bit	Description
[31:30]	Reserved.
[29:28]	Select function of Px.7 pin.
[27:26]	Reserved.
[25:24]	Select function of Px.6 pin.
[23:22]	Reserved.
[21:20]	Select function of Px.5 pin.
[19:18]	Reserved.
[17:16]	Select function of Px.4 pin.
[15:14]	Reserved.
[13:12]	Select function of Px.3 pin.
[11:10]	Reserved.
[9:8]	Select function of Px.2 pin.
[7:6]	Reserved.
[5:4]	Select function of Px.1 pin.
[3:2]	Reserved.
[1:0]	Select function of Px.0 pin.

Table 81. GPxPAR Registers

Name	Address	Default Value	Access
GP0PAR	0xFFFFF42C	0x20000000	R/W
GP1PAR	0xFFFFF43C	0x00000000	R/W
GP2PAR	0xFFFFF44C	0x000000FF	R/W
GP3PAR	0xFFFFF45C	0x00222222	R/W
GP4PAR	0xFFFFF46C	0x00000000	R/W

The GPxPAR registers program the parameters for Port 0, Port 1, Port 2, Port 3, and Port 4. Note that the GPxDAT MMR must always be written after changing the GPxPAR MMR.

Table 82. GPxPAR MMR Bit Descriptions

Bit	Description
31	Reserved.
[30:29]	Drive strength Px.7.
28	Pull-up disable Px.7.
27	Reserved.
[26:25]	Drive strength Px.6.
24	Pull-up disable Px.6.
23	Reserved.
[22:21]	Drive strength Px.5.
20	Pull-up disable Px.5.
19	Reserved.
[18:17]	Drive strength Px.4.
16	Pull-up disable Px.4.
15	Reserved.
[14:13]	Drive strength Px.3.
12	Pull-up disable Px.3.
11	Reserved.
[10:9]	Drive strength Px.2.
8	Pull-up disable Px.2.
7	Reserved.
[6:5]	Drive strength Px.1.
4	Pull-up disable Px.1.
3	Reserved.
[2:1]	Drive strength Px.0.
0	Pull-up disable Px.0.

Table 83. GPIO Drive Strength Control Bits Descriptions

Control Bits Value	Description
00	Medium drive strength.
01	Low drive strength.
1x	High drive strength.

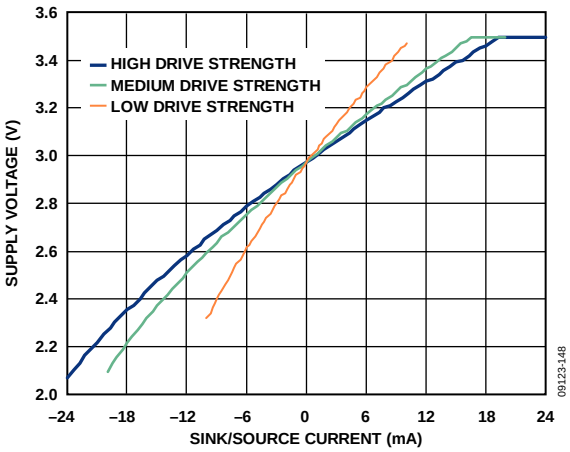

Figure 46. Programmable Strength for High Level

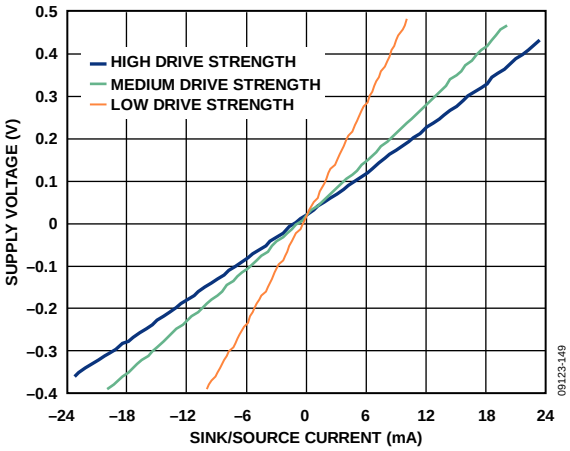

Figure 47. Programmable Strength for Low Level

SPIRX Register

Name: SPIRX

Address: 0xFFFF0A04

Default Value: 0x00

Access: Read only

Function: This 8-bit MMR is the SPI receive register.

SPITX Register

Name: SPITX

Address: 0xFFFF0A08

Default Value: 0x00

Access: Write only

Function: This 8-bit MMR is the SPI transmit register.

SPIDIV Register

Name: SPIDIV

Address: 0xFFFF0A0C

Default Value: 0x00

Access: Read/write

Function: This 8-bit MMR is the SPI baud rate selection register.

SPICON Register

Name: SPICON

Address: 0xFFFF0A10

Default Value: 0x0000

Access: Read/write

Function: This 16-bit MMR configures the SPI peripheral in both master and slave modes.

Table 101. SPICON MMR Bit Descriptions

Bit	Name	Description
[15:14]	SPIMDE	SPI IRQ mode bits. These bits configure when the Tx/Rx interrupts occur in a transfer. [00] = Tx interrupt occurs when one byte has been transferred. Rx interrupt occurs when one or more bytes have been received into the FIFO. [01] = Tx interrupt occurs when two bytes have been transferred. Rx interrupt occurs when two or more bytes have been received into the FIFO. [10] = Tx interrupt occurs when three bytes have been transferred. Rx interrupt occurs when three or more bytes have been received into the FIFO. [11] = Tx interrupt occurs when four bytes have been transferred. Rx interrupt occurs when the Rx FIFO is full or four bytes are present.
13	SPITFLH	SPI Tx FIFO flush enable bit. Set this bit to flush the Tx FIFO. This bit does not clear itself and should be toggled if a single flush is required. If this bit is left high, then either the last transmitted value or 0x00 is transmitted, depending on the SPIZEN bit. Any writes to the Tx FIFO are ignored while this bit is set. Clear this bit to disable Tx FIFO flushing.
12	SPIRFLH	SPI Rx FIFO flush enable bit. Set this bit to flush the Rx FIFO. This bit does not clear itself and should be toggled if a single flush is required. If this bit is set incoming, data is ignored and no interrupts are generated. If set and SPITMDE = 0, a read of the Rx FIFO initiates a transfer. Clear this bit to disable Rx FIFO flushing.
11	SPICONT	Continuous transfer enable. Set by the user to enable continuous transfer. In master mode, the transfer continues until no valid data is available in the SPITX register. $\overline{CS}$ is asserted and remains asserted for the duration of each 8-bit serial transfer until SPITX is empty. Cleared by the user to disable continuous transfer. Each transfer consists of a single 8-bit serial transfer. If valid data exists in the SPITX register, then a new transfer is initiated after a stall period of one serial clock cycle.
10	SPILP	Loopback enable bit. Set by the user to connect MISO to MOSI and test software. Cleared by the user to be in normal mode.

Bit	Name	Description
9	SPIOEN	Slave MISO output enable bit. Set this bit for MISO to operate as normal. Clear this bit to disable the output driver on the MISO pin. The MISO pin is open-drain when this bit is cleared.
8	SPIROW	SPIRX overflow overwrite enable. Set by the user, the valid data in the SPIRX register is overwritten by the new serial byte received. Cleared by the user, the new serial byte received is discarded.
7	SPIZEN	SPI transmits zeros when Tx FIFO is empty. Set this bit to transmit 0x00 when there is no valid data in the Tx FIFO. Clear this bit to transmit the last transmitted value when there is no valid data in the Tx FIFO.
6	SPITMDE	SPI transfer and interrupt mode. Set by the user to initiate transfer with a write to the SPITX register. Interrupt occurs only when SPITX is empty. Cleared by the user to initiate transfer with a read of the SPIRX register. Interrupt occurs only when SPIRX is full.
5	SPILF	LSB first transfer enable bit. Set by the user, the LSB is transmitted first. Cleared by the user, the MSB is transmitted first.
4	SPIWOM	SPI wire-OR'ed mode enable bit. Set to 1 enable open-drain data output. External pull-ups required on data output pins. Cleared for normal output levels.
3	SPICPO	Serial clock polarity mode bit. Set by the user, the serial clock idles high. Cleared by the user, the serial clock idles low.
2	SPICPH	Serial clock phase mode bit. Set by the user, the serial clock pulses at the beginning of each serial bit transfer. Cleared by the user, the serial clock pulses at the end of each serial bit transfer.
1	SPIMEN	Master mode enable bit. Set by the user to enable master mode. Cleared by the user to enable slave mode.
0	SPIEN	SPI enable bit. Set by the user to enable the SPI. Cleared by the user to disable the SPI.

PLACLK Register

Name: PLACLK

Address: 0xFFFF0B40

Default Value: 0x00

Access: Read/write

PLACLK is the clock selection for the flip-flops of Block 0 and Block 1. Note that the maximum frequency when using the GPIO pins as the clock input for the PLA blocks is 41.78 MHz.

Table 120. PLACLK MMR Bit Descriptions

Bit	Value	Description
7		Reserved.
[6:4]		Block 1 clock source selection.
	000	GPIO clock on P0.5.
	001	GPIO clock on P0.0.
	010	GPIO clock on P0.7.
	011	HCLK.
	100	OCLK (32.768 kHz).
	101	Timer1 overflow.
	110	UCLK.
	111	Internal 32,768 oscillator.
3		Reserved.
[2:0]		Block 0 clock source selection.
	000	GPIO clock on P0.5.
	001	GPIO clock on P0.0.
	010	GPIO clock on P0.7.
	011	HCLK.
	100	OCLK (32.768 kHz).
	101	Timer1 overflow.
	Other	Reserved.

PLAIRQ Register

Name: PLAIRQ

Address: 0xFFFF0B44

Default Value: 0x00000000

Access: Read/write

PLAIRQ enables IRQ0 and/or IRQ1 and selects the source of the IRQ.

Table 121. PLAIRQ MMR Bit Descriptions

Bit	Value	Description
[15:13]		Reserved.
12		PLA IRQ1 enable bit. Set by the user to enable IRQ1 output from PLA. Cleared by the user to disable IRQ1 output from PLA.
[11:8]		PLA IRQ1 source.
	0000	PLA Element 0.
	0001	PLA Element 1.
	1111	PLA Element 15.
[7:5]		Reserved.
4		PLA IRQ0 enable bit. Set by the user to enable IRQ0 output from PLA. Cleared by the user to disable IRQ0 output from PLA.
[3:0]		PLA IRQ0 source.
	0000	PLA Element 0.
	0001	PLA Element 1.
	1111	PLA Element 15.

Table 122. Feedback Configuration

Bit	Value	PLAELM0	PLAELM1 to PLAELM7	PLAELM8	PLAELM9 to PLAELM15
[10:9]	00	Element 15	Element 0	Element 7	Element 8
	01	Element 2	Element 2	Element 10	Element 10
	10	Element 4	Element 4	Element 12	Element 12
	11	Element 6	Element 6	Element 14	Element 14
[8:7]	00	Element 1	Element 1	Element 9	Element 9
	01	Element 3	Element 3	Element 11	Element 11
	10	Element 5	Element 5	Element 13	Element 13
	11	Element 7	Element 7	Element 15	Element 15

FIQVEC Register

The FIQ interrupt vector register, FIQVEC, points to a memory address containing a pointer to the interrupt service routine of the currently active FIQ. This register should be read only when an FIQ occurs and FIQ interrupt nesting has been enabled by setting Bit 1 of the IRQCONN register.

Name: FIQVEC

Address: 0xFFFF011C

Default Value: 0x00000000

Access: Read only

Table 136. FIQVEC MMR Bit Descriptions

Bit	Type	Initial Value	Description
[31:23]	R	0	Always read as 0.
[22:7]	R/W	0	IRQBASE register value.
[6:2]		0	Highest priority source. This is a value between 0 and 27, representing the currently active interrupt source. The interrupts are listed in Table 126. For example, if the highest currently active FIQ is Timer2, then these bits are [00100].
[1:0]		0	Reserved.

FIQSTAN Register

If IRQCONN Bit 1 is asserted and FIQVEC is read, one of the FIQSTAN[7:0] bits is asserted. The bit that asserts depends on the priority of the FIQ. If the FIQ is of Priority 0, Bit 0 asserts, if Priority 1, Bit 1 asserts, and so forth.

When a bit is set in this register all interrupts of that priority and lower are blocked.

To clear a bit in this register, all bits of a higher priority must be cleared first. It is possible to clear only one bit at a time. For example, if this register is set to 0x09, then writing 0xFF changes the register to 0x08 and writing 0xFF a second time changes the register to 0x00.

Name: FIQSTAN

Address: 0xFFFF013C

Default Value: 0x00000000

Access: Read/write

Table 137. FIQSTAN MMR Bit Descriptions

Bit	Name	Description
31:8		Reserved. These bits are reserved and should not be written to.
7:0		Setting this bit to 1 enables nesting of FIQ interrupts. Clearing this bit means no nesting or prioritization of FIQs is allowed.

External Interrupts and PLA interrupts

The ADuC7124/ADuC7126 provide up to four external interrupt sources and two PLA interrupt sources. These external interrupts can be individually configured as level or rising/falling edge triggered.

To enable the external interrupt source or the PLA interrupt source, the appropriate bit must first be set in the FIQEN or IRQEN register. To select the required edge or level to trigger on, the IRQCONE register must be appropriately configured.

To properly clear an edge-based external IRQ interrupt or an edge-based PLA interrupt, set the appropriate bit in the IRQCLRE register.

IRQCONE Register

Name: IRQCONE

Address: 0xFFFF0034

Default Value: 0x00000000

Access: Read/write

Table 138. IRQCONE MMR Bit Descriptions

Bit	Value	Name	Description
[31:12]			Reserved. These bits are reserved and should not be written to.
[11:10]	11	PLA1SRC[1:0]	PLA IRQ1 triggers on falling edge.
	10		PLA IRQ1 triggers on rising edge.
	01		PLA IRQ1 triggers on low level.
	00		PLA IRQ1 triggers on high level.
[9:8]	11	IRQ3SRC[1:0]	External IRQ3 triggers on falling edge.
	10		External IRQ3 triggers on rising edge.
	01		External IRQ3 triggers on low level.
	00		External IRQ3 triggers on high level.

Timer0 (RTOS Timer)

Timer0 is a general-purpose, 16-bit timer (count down) with a programmable prescaler. The prescaler source is the core clock frequency (HCLK) and can be scaled by a factor of 1, 16, or 256.

Timer0 can be used to start ADC conversions, as shown in the block diagram in Figure 53.

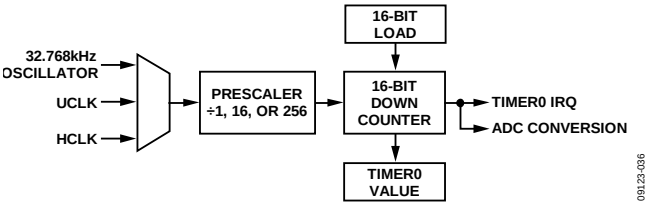

Figure 53. Timer0 Block Diagram

The Timer0 interface consists of four MMRs: T0LD, T0VAL, T0CON, and T0CLRI.

T0LD Register

Name: T0LD

Address: 0xFFFF0300

Default Value: 0x0000

Access: Read/write

T0LD is a 16-bit load register.

T0VAL Register

Name: T0VAL

Address: 0xFFFF0304

Default Value: 0xFFFF

Access: Read only

T0VAL is a 16-bit read-only register representing the current state of the counter.

T0CON Register

Name: T0CON

Address: 0xFFFF0308

Default Value: 0x0000

Access: Read/write

T0CON is the configuration MMR described in Table 141.

Timer3 (Watchdog Time)

Timer3 has two modes of operation: normal mode and watchdog mode. The watchdog timer is used to recover from an illegal software state. Once enabled, it requires periodic servicing to prevent it from forcing a processor reset.

Normal Mode

Timer3 in normal mode is identical to Timer0, except for the clock source and the count-up functionality. The clock source is 32 kHz from the PLL and can be scaled by a factor of 1, 16, or 256 (see Figure 55).

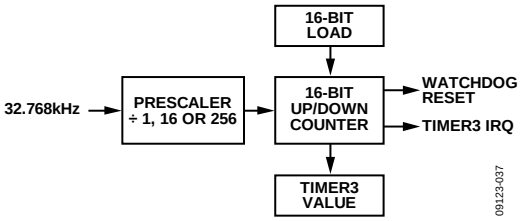

Figure 55. Timer3 Block Diagram

Watchdog Mode

Watchdog mode is entered by setting Bit 5 in the T3CON MMR. Timer3 decreases from the value present in the T3LD register until 0 is reached. T3LD is used as the timeout. The maximum timeout can be 512 sec using the prescaler/256 and full scale in T3LD. Timer3 is clocked by the internal 32 kHz crystal when operating in the watchdog mode. Note that, to enter watchdog mode successfully, Bit 5 in the T3CON MMR must be set after writing to the T3LD MMR.

If the timer reaches 0, a reset or an interrupt occurs, depending on Bit 1 in the T3CON register. To avoid reset or interrupt, any value must be written to T3CLRI before the expiration period. This reloads the counter with T3LD and begins a new timeout period.

When watchdog mode is entered, T3LD and T3CON are write-protected. These two registers cannot be modified until a reset clears the watchdog enable bit, which causes Timer3 to exit watchdog mode.

The Timer3 interface consists of four MMRs: T3LD, T3VAL, T3CON, and T3CLRI.

T3LD Register

Name: T3LD

Address: 0xFFFF0360

Default Value: 0x0000

Access: Read/write

T3LD is a 16-bit load register.

T3VAL Register

Name: T3VAL

Address: 0xFFFF0364

Default Value: 0xFFFF

Access: Read only

T3VAL is a 16-bit read-only register that represents the current state of the counter.

T3CON Register

Name: T3CON

Address: 0xFFFF0368

Default Value: 0x0000

Access: Read/write

T3CON is the configuration MMR described in Table 145.

Table 145. T3CON MMR Bit Descriptions

Bit	Value	Description
[31:9]		Reserved.
8		Count up. Set by the user for Timer3 to count up. Cleared by the user for Timer3 to count down by default.
7		Timer3 enable bit. Set by the user to enable Timer3. Cleared by the user to disable Timer3 by default.
6		Timer3 mode. Set by the user to operate in periodic mode. Cleared by the user to operate in free-running mode (default mode).
5		Watchdog mode enable bit. Set by the user to enable watchdog mode. Cleared by the user to disable watchdog mode by default.
4		Secure clear bit. Set by the user to use the secure clear option. Cleared by the user to disable the secure clear option by default.
[3:2]		Prescale.
	00	Source clock/1 by default.
	01	Source clock/16.
	10	Source clock/256.
	11	Undefined. Equivalent to 00.
1		Watchdog IRQ option bit. Set by the user to produce an IRQ instead of a reset when the watchdog reaches 0. Cleared by the user to disable the IRQ option.
0		Reserved.

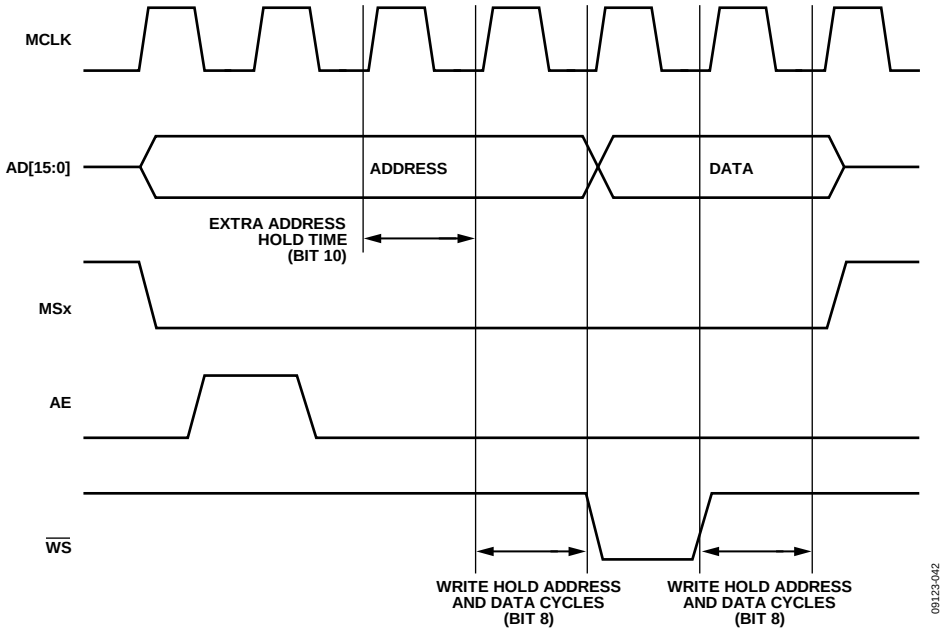

Figure 60. External Memory Write Cycle with Address and Write Hold Cycles

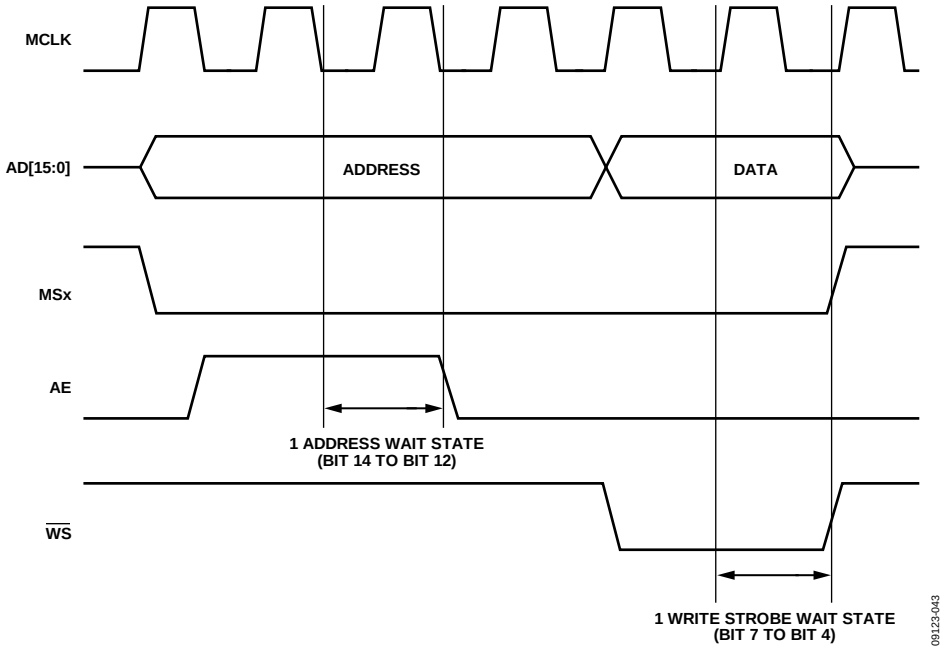

Figure 61. External Memory Write Cycle with Wait States

NOTES

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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