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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	41.78MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	40
Program Memory Size	126KB (63K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 32
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 12x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc7126bstz126-rl

ABSOLUTE MAXIMUM RATINGS

AGND = GND_{REF} = DACGND = GND_{REF}, T_A = 25°C, unless otherwise noted.

Table 8.

Parameter	Rating
AV_{DD} to IOV_{DD}	−0.3 V to +0.3 V
AGND to DGND	−0.3 V to +0.3 V
IOV_{DD} to IOGND, AV_{DD} to AGND	−0.3 V to +6 V
Digital Input Voltage to IOGND	−0.3 V to +5.3 V
Digital Output Voltage to IOGND	−0.3 V to IOV_{DD} + 0.3 V
V_{REF} to AGND	−0.3 V to AV_{DD} + 0.3 V
Analog Inputs to AGND	−0.3 V to AV_{DD} + 0.3 V
Analog Outputs to AGND	−0.3 V to AV_{DD} + 0.3 V
Operating Temperature Range, Industrial	–40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance	
64-Lead LFCSP	24°C/W
80-Lead LQFP	38°C/W
Peak Solder Reflow Temperature	
SnPb Assemblies (10 sec to 30 sec)	240°C
RoHS Compliant Assemblies (20 sec to 40 sec)	260°C

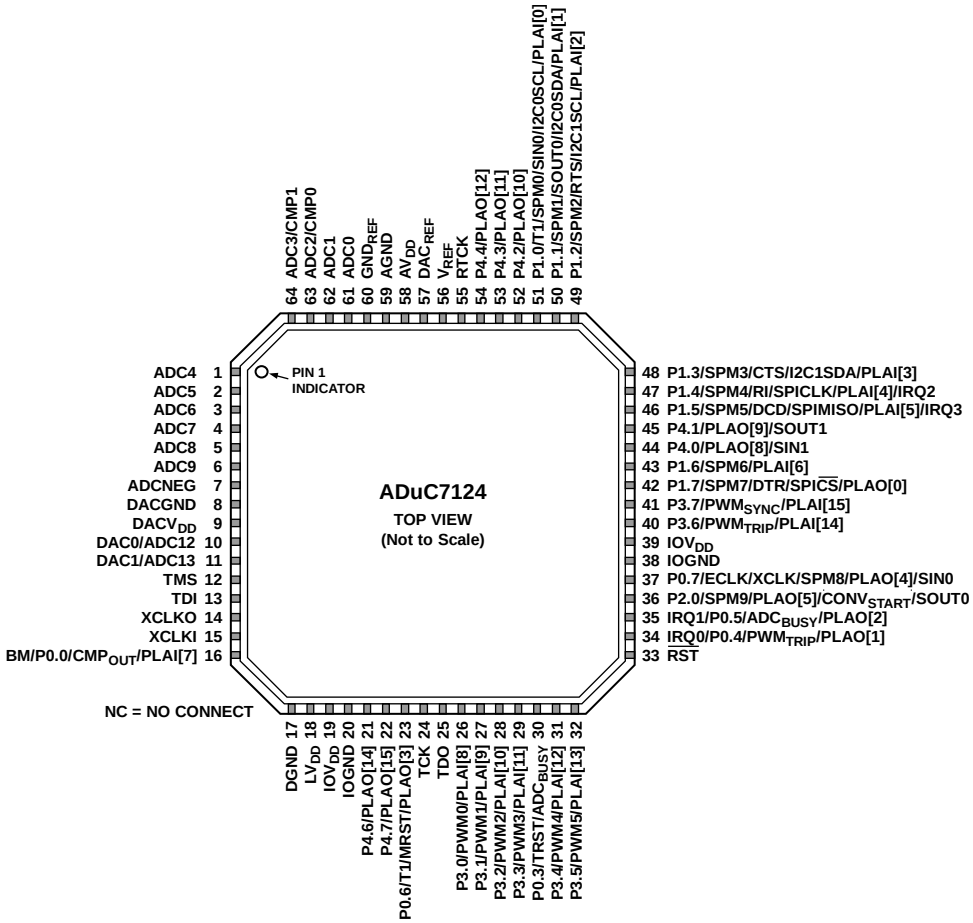
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PADDLE MUST BE SOLDERED TO THE PCB TO ENSURE PROPER HEAT DISSIPATION, NOISE, AND MECHANICAL STRENGTH BENEFITS.

09123-107

Figure 7. ADuC7124 Pin Configuration

Table 9. Pin Function Descriptions (ADuC7124 64-Lead LFCSP)

Pin No.	Mnemonic	Description
0	Exposed Paddle	Exposed Paddle. The LFCSP_VQ has an exposed paddle that must be left unconnected.
1	ADC4	Single-Ended or Differential Analog Input 4.
2	ADC5	Single-Ended or Differential Analog Input 5.
3	ADC6	Single-Ended or Differential Analog Input 6.
4	ADC7	Single-Ended or Differential Analog Input 7.
5	ADC8	Single-Ended or Differential Analog Input 8.
6	ADC9	Single-Ended or Differential Analog Input 9.
7	ADCNEG	Bias Point or Negative Analog Input of the ADC in Pseudo Differential Mode. Must be connected to the ground of the signal to convert. This bias point must be between 0 V and 1 V.
8	DACGND	Ground for the DAC. Typically connected to AGND.
9	$DACV_{DD}$	3.3 V Power Supply for the DACs. Must be connected to AV_{DD}.
10	DAC0/ADC12	DAC0 Voltage Output (DAC0). Single-Ended or Differential Analog Input 12 (ADC12).
11	DAC1/ADC13	DAC1 Voltage Output (DAC1). Single-Ended or Differential Analog Input 13 (ADC13).
12	TMS	JTAG Test Port Input, Test Mode Select. Debug and download access.
13	TDI	JTAG Test Port Input, Test Data In.

Pin No.	Mnemonic	Description
50	P1.1/SPM1/SOUT0/I2C0SDA/PLAI[1]	General-Purpose Input and Output Port 1.1 (P1.1). Serial Port Multiplexed (SPM1). UART download pin, UART0 Output (SOUT0). I2C0 (I2C0SDA). Programmable Logic Array Input Element 1 (PLAI[1]).
51	P1.0/T1/SPM0/SIN0/I2C0SCL/PLAI[0]	General-Purpose Input and Output Port 1.0 (P1.0). Timer1 Input (T1). Serial Port Multiplexed (SPM0). UART download pin, UART0 Input (SIN0). I2C0 (I2C0SCL). Programmable Logic Array Input Element 0 (PLAI[0]).
52	P4.2/PLAO[10]	General-Purpose Input and Output Port 4.2 (P4.2). Programmable Logic Array Output Element 10 (PLAO[10]).
53	P4.3/PLAO[11]	General-Purpose Input and Output Port 4.3 (P4.3). Programmable Logic Array Output Element 11 (PLAO[11]).
54	P4.4/PLAO[12]	General-Purpose Input and Output Port 4.4 (P4.4). Programmable Logic Array Output Element 12 (PLAO[12]).
55	RTCK	JTAG Test Port Output, JTAG Return Test Clock.
56	V_{REF}	2.5 V Internal Voltage Reference. Must be connected to a 0.47 µF capacitor when using the internal reference.
57	DAC_{REF}	External Voltage Reference for the DACs. Range: DACGND to $DACV_{DD}$.
58	AV_{DD}	3.3 V Analog Power.
59	AGND	Analog Ground. Ground reference point for the analog circuitry.
60	GND_{REF}	Ground Voltage Reference for the ADC. For optimal performance, the analog power supply should be separated from IOGND and DGND.
61	ADC0	Single-Ended or Differential Analog Input 0.
62	ADC1	Single-Ended or Differential Analog Input 1.
63	ADC2/CMP0	Single-Ended or Differential Analog Input 2 (ADC2). Comparator Positive Input (CMP0).
64	ADC3/CMP1	Single-Ended or Differential Analog Input 3 (ADC3). Comparator Negative Input (CMP1).

TERMINOLOGY

ADC SPECIFICATIONS

Integral Nonlinearity (INL)
The maximum deviation of any code from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point ½ LSB below the first code transition, and full scale, a point ½ LSB above the last code transition.

Differential Nonlinearity (DNL)
The difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
The deviation of the first code transition (0000…000) to (0000…001) from the ideal, that is, ½ LSB.

Gain Error
The deviation of the last code transition from the ideal AIN voltage (full scale − 1.5 LSB) after the offset error has been adjusted out.

Signal to (Noise + Distortion) Ratio
The measured ratio of signal to (noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent upon the number of quantization levels in the digitization process; the more levels there are, the smaller the quantization noise becomes.

The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

$$Signal\ to\ (Noise + Distortion) = (6.02\ N + 1.76)\ dB$$

Thus, for a 12-bit converter, this is 74 dB.

Total Harmonic Distortion
The ratio of the rms sum of the harmonics to the fundamental.

DAC SPECIFICATIONS

Relative Accuracy
Otherwise known as endpoint linearity, relative accuracy is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero error and full-scale error.

Voltage Output Settling Time
The amount of time it takes the output to settle to within a 1 LSB level for a full-scale input change.

MEMORY ORGANIZATION

The ADuC7124/ADuC7126 incorporate three separate blocks of memory: 32 kB of SRAM and two 64 kB blocks of on-chip Flash/EE memory. There are 126 kB of on-chip Flash/EE memory available to the user, and the remaining 2 kB are reserved for the system kernel. These blocks are mapped as shown in Figure 24.

Note that, by default, after a reset, the Flash/EE memory is mirrored at Address 0x00000000. It is possible to remap the SRAM at Address 0x00000000 by clearing Bit 0 of the REMAP MMR. This remap function is described in more detail in the Flash/EE memory chapter.

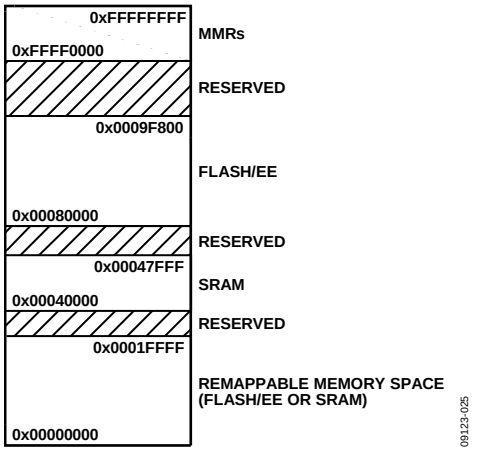


Figure 24. Physical Memory Map

MEMORY ACCESS

The ARM7 core sees memory as a linear array of a 2^{32} byte location where the different blocks of memory are mapped as outlined in Figure 24.

The ADuC7124/ADuC7126 memory organization is configured in little endian format: the least significant byte is located in the lowest byte address and the most significant byte in the highest byte address.

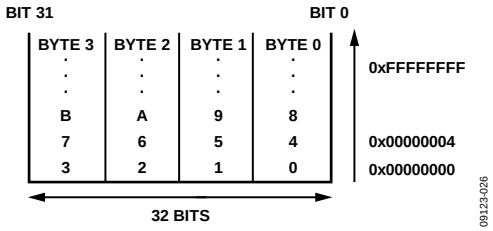


Figure 25. Little Endian Format

FLASH/EE MEMORY

The 128 kB of Flash/EE are organized as two banks of 32 k × 16 bits. Block 0 starts at Address 0x90000 and finishses at Address 0x9F700. In this block, 31 k × 16 bits is user space and 1 k × 16 bits is reserved for the factory-configured boot page. The page size of this Flash/EE memory is 512 bytes.

Block 1 starts at Address 0x80000 and finishses at Address 0x90000. In this block, all 64 kB are available as user space. The block is arranged in 32 k × 16 bits.

The 126 kB of Flash/EE are available to the user as code and nonvolatile data memory. There is no distinction between data and program because ARM code shares the same space. The real width of the Flash/EE memory is 16 bits, meaning that, in ARM mode (32-bit instruction), two accesses to the Flash/EE are necessary for each instruction fetch. Therefore, it is recommended that Thumb mode be used when executing from Flash/EE memory for optimum access speed. The maximum access speed for the Flash/EE memory is 41.78 MHz in Thumb mode and 20.89 MHz in full ARM mode (see the Execution Time from SRAM and Flash/EE section).

SRAM

The 32 kB of SRAM are available to the user, organized as 8 k × 32 bits, that is, 16 k words. ARM code can run directly from SRAM at 41.78 MHz, given that the SRAM array is configured as a 32-bit wide memory array (see the Execution Time from SRAM and Flash/EE section).

MEMORY MAPPED REGISTERS

The memory mapped register (MMR) space is mapped into the upper two pages of the memory array and accessed by indirect addressing through the ARM7 banked registers.

The MMR space provides an interface between the CPU and all on-chip peripherals. All registers except the core registers reside in the MMR area. All shaded locations shown in Figure 26 are unoccupied or reserved locations and should not be accessed by user software. Table 11 to Table 29 show the full MMR memory map.

The access time reading or writing a MMR depends on the advanced microcontroller bus architecture (AMBA) bus used to access the peripheral. The processor has two AMBA buses: the advanced high performance bus (AHB) used for system modules, and the advanced peripheral bus (APB) used for the lower performance peripheral. Access to the AHB is one cycle, and access to the APB is two cycles. All peripherals on the ADuC7124/ADuC7126 are on the APB except the Flash/EE memory and the GPIOs.

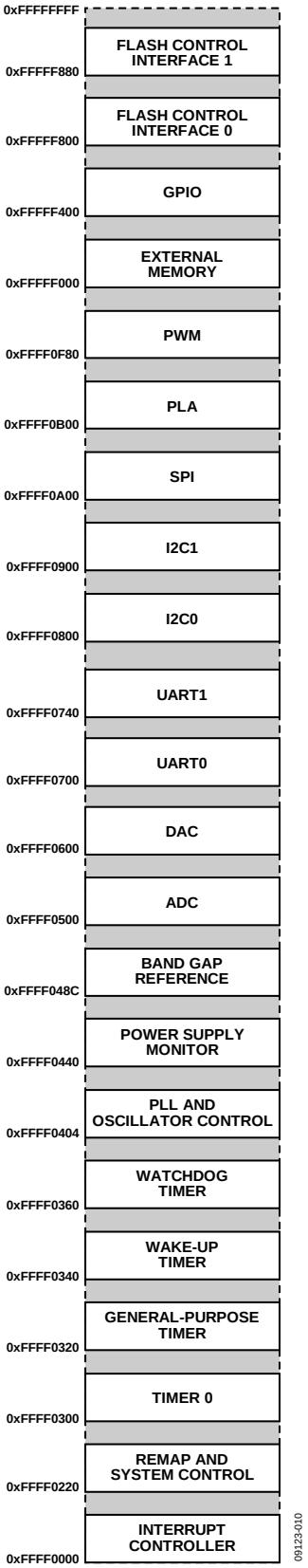


Figure 26. Memory Mapped Registers

ADCCN Register

Name: ADCCN

Address: 0xFFFF0508

Default Value: 0x01

Access: Read/write

ADCCN is an ADC negative channel selection register. This MMR is described in Table 32.

Table 32. ADCCN MMR Bit Designation

Bit	Value	Description
[7:5]		Reserved.
[4:0]		Negative channel selection bits.
	00000	ADC0.
	00001	ADC1.
	00010	ADC2.
	00011	ADC3.
	00100	ADC4.
	00101	ADC5.
	00110	ADC6.
	00111	ADC7.
	01000	ADC8.
	01001	ADC9.
	01010	ADC10.
	01011	ADC11.
	01100	DAC0/ADC12.
	01101	DAC1/ADC13.
	01110	DAC2/ADC14.
	01111	DAC3/ADC15.
	10000	Reserved.
	10001	AGND.
	10010	Reserved.
	10011	Reserved.
	Others	Reserved.

ADCSTA Register

Name: ADCSTA

Address: 0xFFFF050C

Default Value: 0x00

Access: Read only

ADCSTA is an ADC status register that indicates when an ADC conversion result is ready. The ADCSTA register contains only one bit, ADCReady (Bit 0), representing the status of the ADC. This bit is set at the end of an ADC conversion, generating an ADC interrupt. It is cleared automatically by reading the ADCDAT MMR. When the ADC is performing a conversion, the status of the ADC can be read externally via the ADC_{BUSY} pin. This pin is high during a conversion. When the conversion is finished, ADC_{BUSY} goes back low. This information is available on P0.5 (see the General-Purpose Input/Output section) if enabled in the ADCCON register.

ADCDAT Register

Name: ADCDAT

Address: 0xFFFF0510

Default Value: 0x00000000

Access: Read only

ADCDAT is an ADC data result register that holds the 12-bit ADC result, as shown in Figure 30.

ADCRST Register

Name: ADCRST

Address: 0xFFFF0514

Default Value: 0x00

Access: Read/write

ADCRST resets the digital interface of the ADC. Writing any value to this register resets all the ADC registers to their default values.

ADCGN Register

Name: ADCGN

Address: 0xFFFF0530

Default Value: 0x0200

Access: Read/write

ADCGN is a 10-bit gain calibration register.

ADCOF Register

Name: ADCOF

Address: 0xFFFF0534

Default Value: 0x0200

Access: Read/write

ADCOF is a 10-bit offset calibration register.

CONVERTER OPERATION

The ADC incorporates a successive approximation (SAR) architecture involving a charge-sampled input stage. This architecture can operate in three different modes: differential, pseudo differential, and single-ended.

Differential Mode

The ADuC7124/ADuC7126 each contains a successive approximation ADC based on two capacitive DACs. Figure 32 and Figure 33 show simplified schematics of the ADC in acquisition and conversion phases, respectively. The ADC comprises control logic, a SAR, and two capacitive DACs. In Figure 32 (the acquisition phase), SW3 is closed and SW1 and SW2 are in

Table 45. FEE1STA Register

Name	Address	Default Value	Access
FEE1STA	0xFFFFF880	0x0000	R

Table 46. FEE1MOD Register

Name	Address	Default Value	Access
FEE1MOD	0xFFFFF884	0x80	R/W

Table 47. FEE1CON Register

Name	Address	Default Value	Access
FEE1CON	0xFFFFF888	0x00	R/W

Table 48. FEE1DAT Register

Name	Address	Default Value	Access
FEE1DAT	0xFFFFF88C	0xXXXX	R/W

FEE1DAT is a 16-bit data register.

Table 49. FEE1ADR Register

Name	Address	Default Value	Access
FEE1ADR	0xFFFFF890	0x0000	R/W

FEE1ADR is a 16-bit address register.

Table 50. FEE1SGN Register

Name	Address	Default Value	Access
FEE1SGN	0xFFFFF898	0xFFFFFF	R

FEE1SGN is a 24-bit code signature.

Table 51. FEE1PRO Register

Name	Address	Default Value	Access
FEE1PRO	0xFFFFF89C	0x00000000	R/W

FEE1PRO provides protection following subsequent reset MMR. It requires a software key (see Table 57).

Table 52. FEE1HID Register

Name	Address	Default Value	Access
FEE1HID	0xFFFFF8A0	0xFFFFFFFF	R/W

FEE1HID provides immediate protection MMR. It does not require any software keys (see Table 57).

Command Sequence for Executing a Mass Erase

```
FEE0DAT = 0x3CFF;
FEE0ADR = 0xFFC3;
FEE0MOD = FEE0MOD|0x8; //Erase key enable
FEE0CON = 0x06;            //Mass erase
command
```

Table 53. FEExSTA MMR Bit Descriptions

Bit	Description
[15:6]	Reserved.
5	Reserved.
4	Reserved.
3	Flash/EE interrupt status bit. Set automatically when an interrupt occurs, that is, when a command is complete and the Flash/EE interrupt enable bit in the FEExMOD register is set. Cleared when reading the FEExSTA register.
2	Flash/EE controller busy. Set automatically when the controller is busy. Cleared automatically when the controller is not busy.
1	Command fail. Set automatically when a command completes unsuccessfully. Cleared automatically when reading the FEExSTA register.
0	Command complete. Set by MicroConverter when a command is complete. Cleared automatically when reading the FEExSTA register.

Table 56. FEE0PRO and FEE0HID MMR Bit Descriptions

Bit	Description
31	Read protection. Cleared by the user to protect Block 0. Set by the user to allow reading of Block 0.
[30:0]	Write protection for Page 123 to Page 0. Each bit protects protects a group of 4 pages. Cleared by the user to protect the pages when writing to flash. Thus preventing an accidental write to specific pages in flash. Set by the user to allow writing to the pages.

Table 57. FEE1PRO and FEE1HID MMR Bit Descriptions

Bit	Description
31	Read protection. Cleared by the user to protect Block 1. Set by the user to allow reading of Block 1.
30	Write protection for Page 127 to Page 120. Cleared by the user to protect the pages when writing to flash. Thus preventing an accidental write to specific pages in flash. Set by the user to allow writing to the pages.
[29:0]	Write protection for Page 119 to Page 116 and for Page 0 to Page 3. Cleared by the user to protect the pages in writing. Set by the user to allow writing to the pages.

EXECUTION TIME FROM SRAM AND FLASH/EE

This section describes SRAM and Flash/EE access times during execution for applications where execution time is critical.

Execution from SRAM

Fetching instructions from SRAM takes one clock cycle because the access time of the SRAM is 2 ns, and a clock cycle is 24 ns minimum. However, if the instruction involves reading or writing data to memory, one extra cycle must be added if the data is in SRAM (or three cycles if the data is in Flash/EE): one cycle to execute the instruction and two cycles to get the 32-bit data from Flash/EE. A control flow instruction (a branch instruction, for example) takes one cycle to fetch but also takes two cycles to fill the pipeline with the new instructions.

Execution from Flash/EE

Because the Flash/EE width is 16 bits and access time for 16-bit words is 22 ns, execution from Flash/EE cannot be done in one cycle (as can be done from SRAM when the CD bit = 0). Also, some dead times are needed before accessing data for any value of the CD bits.

In ARM mode, where instructions are 32 bits, two cycles are needed to fetch any instruction when CD = 0. In Thumb mode, where instructions are 16 bits, one cycle is needed to fetch any instruction.

Timing is identical in both modes when executing instructions that involve using the Flash/EE for data memory. If the instruction to be executed is a control flow instruction, an extra cycle is needed to decode the new address of the program counter, and then four cycles are needed to fill the pipeline. A data processing instruction involving only the core register does not require any extra clock cycles. However, if it involves data in Flash/EE, an extra clock cycle is needed to decode the address of the data, and two cycles are needed to get the 32-bit data from Flash/EE. An extra cycle must also be added before fetching another instruction. Data transfer instructions are more complex and are summarized in Table 58.

Table 58. Execution Cycles in ARM/Thumb Mode

Instructions	Fetch Cycles	Dead Time	Data Access	Dead Time
LD[1]	2/1	1	2	1
LDH	2/1	1	1	1
LDM/PUSH	2/1	N[2]	2 × N[2]	N[1]
STR[1]	2/1	1	2 × 20 ns	1
STRH	2/1	1	20 ns	1
STRM/POP	2/1	N[1]	2 × N × 20 ns[1]	N[1]

[1] The SWAP instruction combines an LD and STR instruction with only one fetch, giving a total of eight cycles + 40 ns.
[2] N is the number of data bytes to load or store in the multiple load/store instruction (1 < N ≤ 16).

RESET AND REMAP

The ARM exception vectors are all situated at the bottom of the memory array, from Address 0x00000000 to Address 0x00000020, as shown in Figure 40.

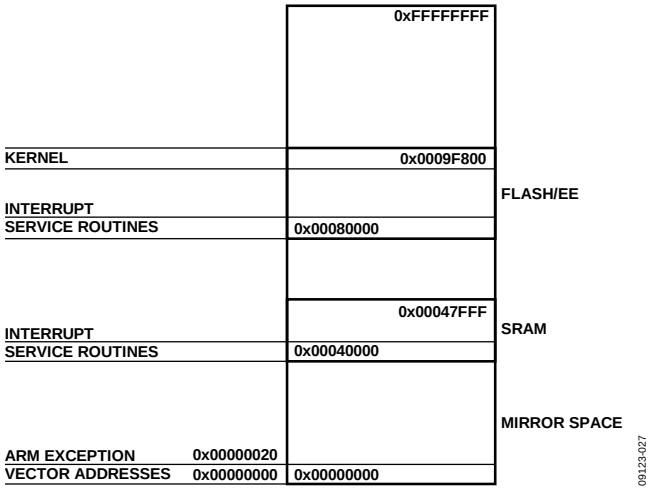


Figure 40. Remap for Exception Execution

By default, and after any reset, the Flash/EE is mirrored at the bottom of the memory array. The remap function allows the programmer to mirror the SRAM at the bottom of the memory array, which facilitates execution of exception routines from SRAM instead of from Flash/EE. This means exceptions are executed twice as fast, being executed in 32-bit ARM mode with 32-bit wide SRAM instead of 16-bit wide Flash/EE memory.

DACBKEY1 Register

Name: DACBKEY1

Address: 0xFFFF0650

Default Value: 0x0000

Access: Write

DACBKEY2 Register

Name: DACBKEY2

Address: 0xFFFF0658

Default Value: 0x0000

Access: Write

POWER SUPPLY MONITOR

The power supply monitor regulates the IOV_{DD} supply on the ADuC7124/ADuC7126. It indicates when the IOV_{DD} supply pin drops below one of two supply trip points. The monitor function is controlled via the PSMCON register. If enabled in the IRQEN or FIQEN register, the monitor interrupts the core using the PSMI bit in the PSMCON MMR. This bit is immediately cleared when CMP goes high.

This monitor function allows the user to save working registers to avoid possible data loss due to low supply or brown-out conditions. It also ensures that normal code execution does not resume until a safe supply level is established.

PSMCON Register

Name: PSMCON

Address: 0xFFFF0440

Default Value: 0x0008

Access: Read/write

Table 68. PSMCON MMR Bit Descriptions

Bit	Name	Description
3	CMP	Comparator bit. This is a read-only bit that directly reflects the state of the comparator. Read 1 indicates that the IOV_{DD} supply is above its selected trip point or that the PSM is in power-down mode. Read 0 indicates that the IOV_{DD} supply is below its selected trip point. This bit should be set before leaving the interrupt service routine.
2	TP	Trip point selection bits. 0 = 2.79 V, 1 = 3.07 V.
1	PSMEN	Power supply monitor enable bit. Set to 1 to enable the power supply monitor circuit. Clear to 0 to disable the power supply monitor circuit.
0	PSMI	Power supply monitor interrupt bit. This bit is set high by the MicroConverter when CMP goes low, indicating low I/O supply. The PSMI bit can be used to interrupt the processor. When CMP returns high, the PSMI bit can be cleared by writing a 1 to this location. A 0 write has no effect. There is no timeout delay; PSMI can be immediately cleared when CMP goes high.

COMPARATOR

The ADuC7124/ADuC7126 integrate a voltage comparator. The positive input is multiplexed with ADC2, and the negative input has two options: ADC3 or DAC0. The output of the comparator can be configured to generate a system interrupt, be routed directly to the programmable logic array, start an ADC conversion, or be on an external pin, CMP_{OUT}, as shown in Figure 43.

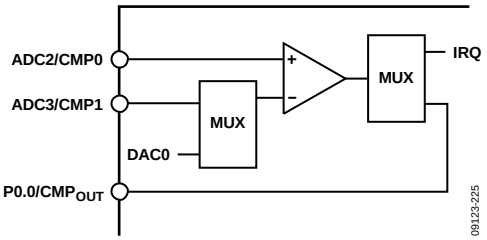


Figure 43. Comparator

Hysteresis

Figure 44 shows how the input offset voltage and hysteresis terms are defined. Input offset voltage (V_{OS}) is the difference between the center of the hysteresis range and the ground level. This can either be positive or negative. The hysteresis voltage (V_H) is ½ the width of the hysteresis range.

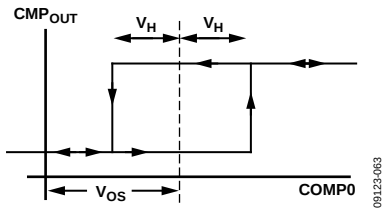


Figure 44. Comparator Hysteresis Transfer Function

COM1DIV0 Register

Name: COM1DIV0

Address: 0xFFFF0740

Default Value: 0x00

Access: Read/write

COM1DIV0 is a low byte divisor latch for UART1. COM1TX, COM1RX, and COM1DIV0 share the same address location. COM1TX and COM1RX can be accessed when Bit 7 in COM1CON0 register is cleared. COM1DIV0 can be accessed when Bit 7 of COM1CON0 is set.

COM0IEN0 Register

Name: COM0IEN0

Address: 0xFFFF0704

Default Value: 0x00

Access: Read/write

COM0IEN0 is the interrupt enable register for UART0.

COM1IEN0 Register

Name: COM1IEN0

Address: 0xFFFF0744

Default Value: 0x00

Access: Read/write

COM1IEN0 is the interrupt enable register for UART1.

Table 92. COMxIEN0 MMR Bit Descriptions

Bit	Name	Description
[7:4]		Reserved.
3	EDSSI	Modem status interrupt enable bit. Set by the user to enable generation of an interrupt if any of COMXSTA1[3:1] are set. Cleared by the user.
2	ELSI	Rx status interrupt enable bit. Set by the user to enable generation of an interrupt if any of COMxSTA0[3:0] are set. Cleared by the user.
1	ETBEI	Enable transmit buffer empty interrupt. Set by the user to enable interrupt when the buffer is empty during a transmission. Cleared by the user.
0	ERBFI	Enable receive buffer full interrupt. In non-FIFO mode, set by the user to enable an interrupt when buffer is full during a reception. Cleared by the user. In FIFO mode, set by the user to enable an interrupt when trigger level is reached. It also controls the character receive timeout interrupt. Cleared by the user.

COM0DIV1 Register

Name: COM0DIV1

Address: 0xFFFF0704

Default Value: 0x00

Access: Read/write

COM0DIV1 is a divisor latch (high byte) register for UART0.

COM1DIV1 Register

Name: COM1DIV1

Address: 0xFFFF0744

Default Value: 0x00

Access: Read/write

COM1DIV1 is a divisor latch (high byte) register for UART1.

COM0IID0 Register

Name: COM0IID0

Address: 0xFFFF0708

Default Value: 0x01

Access: Read only

COM0IID0 is the interrupt identification register for UART0. It also indicates if the UART is in FIFO mode.

COM1IID0 Register

Name: COM1IID0

Address: 0xFFFF0748

Default Value: 0x01

Access: Read only

COM1IID0 is the interrupt identification register for UART1. It also indicates if the UART is in FIFO mode.

COM1CON0 Register

Name: COM1CON0

Address: 0xFFFF074C

Default Value: 0x00

Access: Read/write

COM1CON0 is the line control register for UART1.

Table 95. COMxCON0 MMR Bit Descriptions

Bit	Name	Description
7	DLAB	Divisor latch access. Set by the user to enable access to the COMxDIV0 and COMxDIV1 registers. Cleared by the user to disable access to COMxDIV0 and COMxDIV1 and enable access to COMxRX and COMxTX.
6	BRK	Set break. Set by the user to force SOUTx to 0. Cleared to operate in normal mode.
5	SP	Stick parity. Set by the user to force parity to defined values: 1 if EPS = 1 and PEN = 1, 0 if EPS = 0 and PEN = 1.
4	EPS	Even parity select bit. Set for even parity. Cleared for odd parity.
3	PEN	Parity enable bit. Set by the user to transmit and check the parity bit. Cleared by the user for no parity transmission or checking.
2	Stop	Stop bit. Set by the user to transmit 1½ stop bits if the word length is five bits or two stop bits if the word length is six bits, seven bits, or eight bits. The receiver checks the first stop bit only, regardless of the number of stop bits selected. Cleared by the user to generate one stop bit in the transmitted data.
[1:0]	WLS	Word length select: 00 = five bits, 01 = six bits, 10 = seven bits, 11 = eight bits.

COM0CON1 Register

Name: COM0CON1

Address: 0xFFFF0710

Default Value: 0x00

Access: Read/write

COM0CON1 is the modem control register for UART0.

COM1CON1 Register

Name: COM1CON1

Address: 0xFFFF0750

Default Value: 0x00

Access: Read/write

COM1CON1 is the modem control register for UART1.

Table 96. COMxCON1 MMR Bit Descriptions

Bit	Name	Description
[7:5]		Reserved.
4	LOOPBACK	Loop back. Set by the user to enable loopback mode. In loopback mode, SOUTx is forced high. The modem signals are also directly connected to the status inputs (RTS to CTS and DTR to DSR). Cleared by the user to be in normal mode.
3	PEN	Parity enable bit. Set by the user to transmit and check the parity bit. Cleared by the user for no parity transmission or checking.
2	Stop	Stop bit. Set by the user to transmit 1½ stop bits if the word length is five bits or two stop bits if the word length is six bits, seven bits, or eight bits. The receiver checks the first stop bit only, regardless of the number of stop bits selected. Cleared by the user to generate one stop bit in the transmitted data.
1	RTS	Request to send. Set by the user to force the RTS output to 0. Cleared by the user to force the RTS output to 1.
0	DTR	Data terminal ready. Set by the user to force the DTR output to 0. Cleared by the user to force the DTR output to 1.

COM0STA0 Register

Name: COM0STA0

Address: 0xFFFF0714

Default Value: 0xE0

Access: Read only

COM0STA0 is the line status register for UART0.

I²C Master Status Register

Name: I2C0MSTA, I2C1MSTA

Address: 0xFFFF0804, 0xFFFF0904

Default Value: 0x0000, 0x0000

Access: Read only

Function: This 16-bit MMR is the I²C status register in master mode.

Table 103. I2CxMSTA MMR Bit Descriptions

Bit	Name	Description
[15:11]		Reserved.
10	I2CBBUSY	I²C bus busy status bit. This bit is set to 1 when a start condition is detected on the I²C bus. This bit is cleared when a stop condition is detected on the bus.
9	I2CMRxFO	Master Rx FIFO overflow. This bit is set to 1 when a byte is written to the Rx FIFO when it is already full. This bit is cleared in all other conditions.
8	I2CMTC	I²C transmission complete status bit. This bit is set to 1 when a transmission is complete between the master and the slave it was communicating with. If the I2CMCENI bit in I2CxMCON is set, an interrupt is generated when this bit is set. Clear this bit to clear the interrupt source.
7	I2CMNA	I²C master NACK data bit. This bit is set to 1 when a NACK condition is received by the master in response to a data write transfer. If the I2CNACKENI bit in I2CxMCON is set, an interrupt is generated when this bit is set. This bit is cleared in all other conditions.
6	I2CMBUSY	I²C master busy status bit. Set to 1 when the master is busy processing a transaction. Cleared if the master is ready or if another master device has control of the bus.
5	I2CAL	I²C arbitration lost status bit. This bit is set to 1 when the I²C master is unable to gain control of the I²C bus. If the I2CALENI bit in I2CxMCON is set, an interrupt is generated when this bit is set. This bit is cleared in all other conditions.
4	I2CMNA	I²C master NACK address bit. This bit is set to 1 when a NACK condition is received by the master in response to an address. If the I2CNACKENI bit in I2CxMCON is set, an interrupt is generated when this bit is set. This bit is cleared in all other conditions.
3	I2CMRXQ	I²C master receive request bit. This bit is set to 1 when data enters the Rx FIFO. If the I2CMRENI in I2CxMCON is set, an interrupt is generated. This bit is cleared in all other conditions.
2	I2CMTXQ	I²C master transmit request bit. This bit goes high if the Tx FIFO is empty or contains only one byte and the master has transmitted an address + write. If the I2CMTENI bit in I2CxMCON is set, an interrupt is generated when this bit is set. This bit is cleared in all other conditions.
[1:0]	I2CMTFSTA	I²C master Tx FIFO status bits. 00 = I²C master Tx FIFO empty. 01 = one byte in master Tx FIFO. 10 = one byte in master Tx FIFO. 11 = I²C master Tx FIFO full.

I²C Address 1 Register

Name: I2C0ADR1, I2C1ADR1

Address: 0xFFFF081C, 0xFFFF091C

Default Value: 0x00

Access: Read/write

Function: This 8-bit MMR is used in 10-bit addressing mode only. This register contains the least significant byte of the address.

Table 107. I2CxADR1 MMR in 10-Bit Address Mode

Bit	Name	Description
[7:0]	I2CLADR	These bits contain ADDR[7:0] in 10-bit addressing mode.

I²C Master Clock Control Register

Name: I2C0DIV, I2C1DIV

Address: 0xFFFF0824, 0xFFFF0924

Default Value: 0x1F1F

Access: Read/write

Function: This MMR controls the frequency of the I²C clock generated by the master on to the SCL pin. For further details, see the I²C section.

Table 108. I2CxDIV MMR

Bit	Name	Description
[15:8]	DIVH	These bits control the duration of the high period of SCL.
[7:0]	DIVL	These bits control the duration of the low period of SCL.

I²C Slave Registers

I²C Slave Control Register

Name: I2C0SCON, I2C1SCON

Address: 0xFFFF0828, 0xFFFF0928

Default Value: 0x0000

Access: Read/write

Function: This 16-bit MMR configures the I²C peripheral in slave mode.

Table 109. I2CxSCON MMR Bit Descriptions

Bit	Name	Description
[15:11]		Reserved.
10	I2CSTXENI	Slave transmit interrupt enable bit. Set this bit to enable an interrupt after a slave transmits a byte. Clear this interrupt source.
9	I2CSRXENI	Slave receive interrupt enable bit. Set this bit to enable an interrupt after the slave receives data. Clear this interrupt source.
8	I2CSSENI	I²C stop condition detected interrupt enable bit. Set this bit to enable an interrupt on detecting a stop condition on the I²C bus. Clear this interrupt source.
7	I2CNACKEN	I²C NACK enable bit. Set this bit to NACK the next byte in the transmission sequence. Clear this bit to let the hardware control the ACK/NACK sequence.
6	RESERVED	Reserved. A value of 0 should be written to this bit.
5	I2CSETEN	I²C early transmit interrupt enable bit. Setting this bit enables a transmit request interrupt just after the positive edge of SCL during the read bit transmission. Clear this bit to enable a transmit request interrupt just after the negative edge of SCL during the read bit transmission.
4	I2CGCCLR	I²C general call status and ID clear bit. Writing a 1 to this bit clears the general call status (I2CGC) and ID (I2CGCID[1:0]) bits in the I2CxSSTA register. Clear this bit at all other times.

I²C Slave Receive Registers

Name: I2C0SRX, I2C1SRX

Address: 0xFFFF0830, 0xFFFF0930

Default Value: 0x00

Access: Read

Function: This 8-bit MMR is the I²C slave receive register.

I²C Slave Transmit Registers

Name: I2C0STX, I2C1STX

Address: 0xFFFF0834, 0xFFFF0934

Default Value: 0x00

Access: Write

Function: This 8-bit MMR is the I²C slave transmit register.

I²C Hardware General Call Recognition Registers

Name: I2C0ALT, I2C1ALT

Address: 0xFFFF0838, 0xFFFF0938

Default Value: 0x00

Access: Read/write

Function: This 8-bit MMR is used with hardware general calls when I2CxSCON Bit 3 is set to 1. This register is used in cases where a master is unable to generate an address for a slave, and instead, the slave must generate the address for the master.

I²C Slave Device ID Registers

Name: I2C0IDx, I2C1IDx

Addresses: 0xFFFF093C = I2C1ID0
0xFFFF083C = I2C0ID0

0xFFFF0940 = I2C1ID1
0xFFFF0840 = I2C0ID1

0xFFFF0944 = I2C1ID2
0xFFFF0844 = I2C0ID2

0xFFFF0948 = I2C1ID3
0xFFFF0848 = I2C0ID3

Default Value: 0x00

Access: Read/write

Function: These 8-bit MMRs are programmed with I²C bus IDs of the slave. See the I2C Bus Addresses section for further details.

I²C Common Registers

I²C FIFO Status Register

Name: I2C0FSTA, I2C1FSTA

Address: 0xFFFF084C, 0xFFFF094C

Default Value: 0x0000

Access: Read/write

Function: These 16-bit MMRs contain the status of the Rx/Tx FIFOs in both master and slave modes.

Table 111. I2CxFSTA MMR Bit Descriptions

Bit	Name	Description
[15:10]		Reserved.
9	I2CFMTX	Set this bit to 1 to flush the master Tx FIFO.
8	I2CFSTX	Set this bit to 1 to flush the slave Tx FIFO.
[7:6]	I2CMRXSTA	I²C master receive FIFO status bits. [00] = FIFO empty. [01] = byte written to FIFO. [10] = one byte in FIFO. [11] = FIFO full.
[5:4]	I2CMTXSTA	I²C master transmit FIFO status bits. [00] = FIFO empty. [01] = byte written to FIFO. [10] = one byte in FIFO. [11] = FIFO full.
[3:2]	I2CSRXSTA	I²C slave receive FIFO status bits. [00] = FIFO empty. [01] = byte written to FIFO. [10] = one byte in FIFO. [11] = FIFO full.
[1:0]	I2CSTXSTA	I²C slave transmit FIFO status bits. [00] = FIFO empty. [01] = byte written to FIFO. [10] = one byte in FIFO. [11] = FIFO full.

PLACLK Register

Name: PLACLK

Address: 0xFFFF0B40

Default Value: 0x00

Access: Read/write

PLACLK is the clock selection for the flip-flops of Block 0 and Block 1. Note that the maximum frequency when using the GPIO pins as the clock input for the PLA blocks is 41.78 MHz.

Table 120. PLACLK MMR Bit Descriptions

Bit	Value	Description
7		Reserved.
[6:4]		Block 1 clock source selection.
	000	GPIO clock on P0.5.
	001	GPIO clock on P0.0.
	010	GPIO clock on P0.7.
	011	HCLK.
	100	OCLK (32.768 kHz).
	101	Timer1 overflow.
	110	UCLK.
	111	Internal 32,768 oscillator.
3		Reserved.
[2:0]		Block 0 clock source selection.
	000	GPIO clock on P0.5.
	001	GPIO clock on P0.0.
	010	GPIO clock on P0.7.
	011	HCLK.
	100	OCLK (32.768 kHz).
	101	Timer1 overflow.
	Other	Reserved.

PLAIRQ Register

Name: PLAIRQ

Address: 0xFFFF0B44

Default Value: 0x00000000

Access: Read/write

PLAIRQ enables IRQ0 and/or IRQ1 and selects the source of the IRQ.

Table 121. PLAIRQ MMR Bit Descriptions

Bit	Value	Description
[15:13]		Reserved.
12		PLA IRQ1 enable bit. Set by the user to enable IRQ1 output from PLA. Cleared by the user to disable IRQ1 output from PLA.
[11:8]		PLA IRQ1 source.
	0000	PLA Element 0.
	0001	PLA Element 1.
	1111	PLA Element 15.
[7:5]		Reserved.
4		PLA IRQ0 enable bit. Set by the user to enable IRQ0 output from PLA. Cleared by the user to disable IRQ0 output from PLA.
[3:0]		PLA IRQ0 source.
	0000	PLA Element 0.
	0001	PLA Element 1.
	1111	PLA Element 15.

Table 122. Feedback Configuration

Bit	Value	PLAELM0	PLAELM1 to PLAELM7	PLAELM8	PLAELM9 to PLAELM15
[10:9]	00	Element 15	Element 0	Element 7	Element 8
	01	Element 2	Element 2	Element 10	Element 10
	10	Element 4	Element 4	Element 12	Element 12
	11	Element 6	Element 6	Element 14	Element 14
[8:7]	00	Element 1	Element 1	Element 9	Element 9
	01	Element 3	Element 3	Element 11	Element 11
	10	Element 5	Element 5	Element 13	Element 13
	11	Element 7	Element 7	Element 15	Element 15

IRQEN Register

IRQEN provides the value of the current enable mask. When a bit is set to 1, the corresponding source request is enabled to create an IRQ exception. When a bit is set to 0, the corresponding source request is disabled or masked, which does not create an IRQ exception. The IRQEN register cannot be used to disable an interrupt.

IRQEN Register

Name: IRQEN

Address: 0xFFFF0008

Default Value: 0x00000000

Access: Read/write

IRQCLR Register

IRQCLR is a write-only register that allows the IRQEN register to clear to mask an interrupt source. Each bit that is set to 1 clears the corresponding bit in the IRQEN register without affecting the remaining bits. The pair of registers, IRQEN and IRQCLR, allow independent manipulation of the enable mask without requiring an atomic read-modify-write.

This register should be used to disable an interrupt source only during the following conditions:

- In the interrupt sources interrupt service routine.
- When the peripheral is temporarily disabled by its own control register.

This register should not be used to disable an IRQ source if that IRQ source has an interrupt pending or may have an interrupt pending.

IRQCLR Register

Name: IRQCLR

Address: 0xFFFF000C

Default Value: 0x00000000

Access: Write only

FAST INTERRUPT REQUEST (FIQ)

The fast interrupt request (FIQ) is the exception signal to enter the FIQ mode of the processor. It is provided to service data transfer or communication channel tasks with low latency. The FIQ interface is identical to the IRQ interface and provides the second level interrupt (highest priority). Four 32-bit registers are dedicated to FIQ: FIQSIG, FIQEN, FIQCLR, and FIQSTA.

Bit 31 to Bit 1 of FIQSTA are logically OR'ed to create the FIQ signal to the core and to Bit 0 of both the FIQ and IRQ registers (FIQ source).

The logic for FIQEN and FIQCLR does not allow an interrupt source to be enabled in both IRQ and FIQ masks. A bit set to 1 in FIQEN clears, as a side effect, the same bit in IRQEN. Likewise, a bit set to 1 in IRQEN clears, as a side effect, the same bit in FIQEN. An interrupt source can be disabled in both the IRQEN and FIQEN masks.

FIQSIG

FIQSIG reflects the status of the different FIQ sources. If a peripheral generates an FIQ signal, the corresponding bit in the FIQSIG is set; otherwise, it is cleared. The FIQSIG bits are cleared when the interrupt in the particular peripheral is cleared. All FIQ sources can be masked in the FIQEN MMR. FIQSIG is read only.

FIQSIG Register

Name: FIQSIG

Address: 0xFFFF0104

Default Value: 0x00000000

Access: Read only

FIQEN

FIQEN provides the value of the current enable mask. When a bit is set to 1, the corresponding source request is enabled to create an FIQ exception. When a bit is set to 0, the corresponding source request is disabled or masked, which does not create an FIQ exception. The FIQEN register cannot be used to disable an interrupt.

FIQEN Register

Name: FIQEN

Address: 0xFFFF0108

Default Value: 0x00000000

Access: Read/write

FIQCLR

FIQCLR is a write-only register that allows the FIQEN register to clear to mask an interrupt source. Each bit that is set to 1 clears the corresponding bit in the FIQEN register without affecting the remaining bits. The pair of registers, FIQEN and FIQCLR, allows independent manipulation of the enable mask without requiring an atomic read-modify-write.

This register should be used to disable an interrupt source only during the following conditions:

- In the interrupt sources interrupt service routine.
- The peripheral is temporarily disabled by its own control register.

This register should not be used to disable an IRQ source if that IRQ source has an interrupt pending or may have an interrupt pending.

Timer0 (RTOS Timer)

Timer0 is a general-purpose, 16-bit timer (count down) with a programmable prescaler. The prescaler source is the core clock frequency (HCLK) and can be scaled by a factor of 1, 16, or 256.

Timer0 can be used to start ADC conversions, as shown in the block diagram in Figure 53.

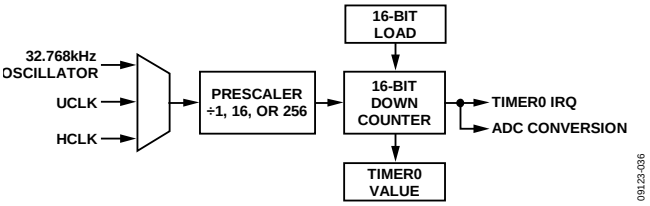


Figure 53. Timer0 Block Diagram

The Timer0 interface consists of four MMRs: T0LD, T0VAL, T0CON, and T0CLRI.

T0LD Register

Name: T0LD

Address: 0xFFFF0300

Default Value: 0x0000

Access: Read/write

T0LD is a 16-bit load register.

T0VAL Register

Name: T0VAL

Address: 0xFFFF0304

Default Value: 0xFFFF

Access: Read only

T0VAL is a 16-bit read-only register representing the current state of the counter.

T0CON Register

Name: T0CON

Address: 0xFFFF0308

Default Value: 0x0000

Access: Read/write

T0CON is the configuration MMR described in Table 141.

T3CLRI Register

Name: T3CLRI

Address: 0xFFFF036C

Default Value: 0x00

Access: Write only

T3CLRI is an 8-bit register. Writing any value to this register on successive occassions clears the Timer3 interrupt in normal mode or resets a new timeout period in watchdog mode.

Note that the user must perform successive writes to this register to ensure resetting the timeout period.

Secure Clear Bit (Watchdog Mode Only)

The secure clear bit is provided for a higher level of protection. When set, a specific sequential value must be written to T3CLRI to avoid a watchdog reset. The value is a sequence generated by the 8-bit linear feedback shift register (LFSR) polynomial = $X_8 + X_6 + X_5 + X + 1$, as shown in Figure 56.

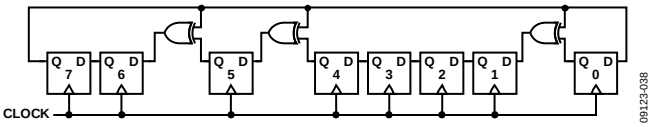


Figure 56. 8-Bit LFSR

The initial value or seed is written to T3CLRI before entering watchdog mode. After entering watchdog mode, a write to T3CLRI must match this expected value. If it matches, the LFSR is advanced to the next state when the counter reload occurs. If it fails to match the expected state, a reset is immediately generated, even if the count has not yet expired.

The value 0x00 should not be used as an initial seed due to the properties of the polynomial. The value 0x00 is always guaranteed to force an immediate reset. The value of the LFSR cannot be read; it must be tracked/generated in software.

Example of a sequence:

1. Enter initial seed, 0xAA, in T3CLRI before starting Timer3 in watchdog mode.
2. Enter 0xAA in T3CLRI; Timer3 is reloaded.
3. Enter 0x37 in T3CLRI; Timer3 is reloaded.
4. Enter 0x6E in T3CLRI; Timer3 is reloaded.
5. Enter 0x66. 0xDC was expected; the watchdog resets the chip.

EXTERNAL MEMORY INTERFACING

The ADuC7124/ADuC7126 feature an external memory interface. The external memory interface requires a larger number of pins. The XMCFG MMR must be set to 1 to use the external port.

Although 32-bit addresses are supported internally, only the lower 16 bits of the address are on external pins.

The memory interface can address up to four 128 kB of asynchronous memory (SRAM or/and EEPROM).

The pins required for interfacing to an external memory are shown in Table 146.

Table 146. External Memory Interfacing Pins

Pin	Function
AD[15:0]	Address/data bus.
A16	Extended addressing for 8-Bit memory only.
MS[3:0]	Memory select.
$\overline{WS}$	Write strobe.
$\overline{RS}$	Read strobe.
AE	Address latch enable.
$\overline{BHE}$, $\overline{BLE}$	Byte write capability.

There are four external memory regions available as described in Table 147. Associated with each region are the MS[3:0] pins. These signals allow access to the particular region of external memory. The size of each memory region can be 128 kB maximum, 64 k × 16 or 128 kB × 8. To access 128 kB with an 8-bit memory, an extra address line (A16) is provided (see the example in Figure 57). The four regions are configured independently.

Table 147. Memory Regions

Address Start	Address End	Contents
0x10000000	0x1000FFFF	External Memory 0
0x20000000	0x2000FFFF	External Memory 1
0x30000000	0x3000FFFF	External Memory 2
0x40000000	0x4000FFFF	External Memory 3

Each external memory region can be controlled through three MMRs: XMCFG, XMxCON, and XMxPAR.

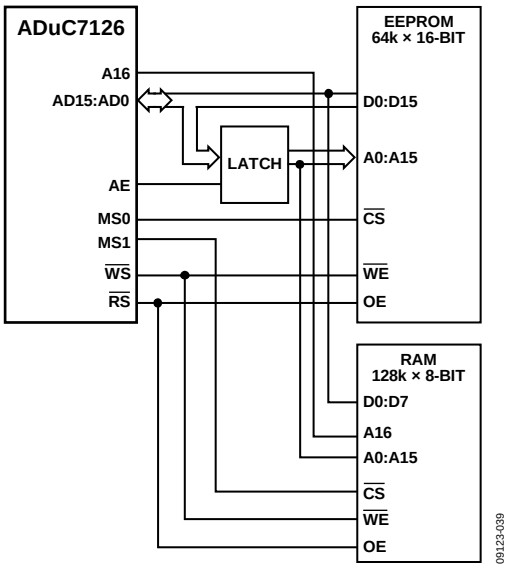


Figure 57. Interfacing to External EEPROM/RAM

XMCFG Register

Name: XMCFG

Address: 0xFFFFF000

Default Value: 0x00

Access: Read/write

XMCFG is set to 1 to enable external memory access. This must be set to 1 before any port pins can function as external memory access pins. The port pins must also be individually enabled via the GPxCON MMR.

Table 148. XMxCON Registers

Name	Address	Default Value	Access
XM0CON	0xFFFFF010	0x00	R/W
XM1CON	0xFFFFF014	0x00	R/W
XM2CON	0xFFFFF018	0x00	R/W
XM3CON	0xFFFFF01C	0x00	R/W

XMxCON are the control registers for each memory region. They allow the enabling/disabling of a memory region and control the data bus width of the memory region.

Table 149. XMxCON MMR Bit Descriptions

Bit	Description
1	Selects data bus width. Set by the user to select a 16-bit data bus. Cleared by the user to select an 8-bit data bus.
0	Enables memory region. Set by the user to enable memory region. Cleared by the user to disable the memory region.

Table 150. XMxPAR Registers

Name	Address	Default Value	Access
XM0PAR	0xFFFFF020	0x70FF	R/W
XM1PAR	0xFFFFF024	0x70FF	R/W
XM2PAR	0xFFFFF028	0x70FF	R/W
XM3PAR	0xFFFFF02C	0x70FF	R/W

XMxPAR are registers that define the protocol used for accessing the external memory for each memory region.

Table 151. XMxPAR MMR Bit Descriptions

Bit	Description
15	Enable byte write strobe. This bit is only used for two 8-bit memory blocks sharing the same memory region. Set by the user to gate the A0 output with the $\overline{WS}$ output. This allows byte write capability without using $\overline{BHE}$ and $\overline{BLE}$ signals. Cleared by user to use $\overline{BHE}$ and $\overline{BLE}$ signals.
[14:12]	Number of wait states on the address latch enable strobe.
11	Reserved.
10	Extra address hold time. Set by the user to disable extra hold time. Cleared by the user to enable one clock cycle of hold on the address in read and write.
9	Extra bus transition time on read. Set by the user to disable extra bus transition time. Cleared by the user to enable one extra clock before and after the read strobe ($\overline{RS}$).
8	Extra bus transition time on write. Set by the user to disable extra bus transition time. Cleared by the user to enable one extra clock before and after the write strobe ($\overline{WS}$).
[7:4]	Number of write wait states. Select the number of wait states added to the length of the $\overline{WS}$ pulse. 0x0 is 1 clock; 0xF is 16 clock cycles (default value).
[3:0]	Number of read wait states. Select the number of wait states added to the length of the $\overline{RS}$ pulse. 0x0 is 1 clock; 0xF is 16 clock cycles (default value).

Figure 58, Figure 59, Figure 60, and Figure 61 show the timing for a read cycle, a read cycle with address hold and bus turn cycles, a write cycle with address and write hold cycles, and a write cycle with wait sates, respectively.