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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	41.78MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	40
Program Memory Size	126KB (63K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 32
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 12x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc7126bstz126

GENERAL DESCRIPTION

The ADuC7124/ADuC7126 are fully integrated, 1 MSPS, 12-bit data acquisition system incorporating high performance multichannel ADCs, 16-bit/32-bit MCUs, and Flash/EE memory on a single chip.

The ADC consists of up to 12 single-ended inputs. An additional four inputs are available but are multiplexed with the four DAC output pins. The ADC can operate in single-ended or differential input mode. The ADC input voltage range is 0 V to VREF. A low drift band gap reference, temperature sensor, and voltage comparator complete the ADC peripheral set.

The DAC output range is programmable to one of three voltage ranges. The DAC outputs have an enhanced feature of being able to retain their output voltage during a watchdog or software reset sequence.

The devices operate from an on-chip oscillator and a PLL generating an internal high frequency clock of 41.78 MHz. This clock is routed through a programmable clock divider from which the MCU core clock operating frequency is generated. The microcontroller core is an ARM7TDMI®, 16-bit/32-bit RISC machine, which offers up to 41 MIPS of peak performance. Thirty-two kilobytes of SRAM and 126 kB of nonvolatile Flash/EE memory are provided on-chip. The ARM7TDMI core views all memory and registers as a single linear array.

The ADuC7124/ADuC7126 contain an advanced interrupt controller. The vectored interrupt controller (VIC) allows every interrupt to be assigned a priority level. It also supports nested interrupts to a maximum level of eight per IRQ and FIQ. When IRQ and FIQ interrupt sources are combined, a total of 16 nested interrupt levels are supported.

On-chip factory firmware supports in-circuit download via the UART serial interface port or the I^2C port, while nonintrusive emulation is also supported via the JTAG interface. These features are incorporated into a low cost QuickStart™ development system supporting this MicroConverter® family.

The parts contain a 16-bit PWM with six output signals.

For communication purposes, the parts contain 2× I^2C channels that can be individually configured for master or slave mode. An SPI interface supporting both master and slave modes is also provided. Thirdly, 2× UART channels are provided. Each UART contains a configurable 16-byte FIFO with receive and transmit buffers.

The parts operate from 2.7 V to 3.6 V and is specified over an industrial temperature range of −40°C to +125°C. When operating at 41.78 MHz, the power dissipation is typically 120 mW. The ADuC7124 is available in a 64-lead LFCSP package. The ADuC7126 is available in a 80-lead LQFP package.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ESD TESTS					2.5 V reference, T_A = 25°C
HBM Passed Up To			3	kV	
FICDM Passed Up To			1.5	kV	

[1] All ADC channel specifications are guaranteed during normal core operation.
[2] Apply to all ADC input channels.
[3] Measured using the factory-set default values in the ADC offset register (ADCOF) and gain coefficient register (ADCGN).
[4] Not production tested but supported by design and/or characterization data on production release.
[5] Measured using the factory-set default values in ADCOF and ADCGN with an external AD845 op amp as an input buffer stage as shown in Figure 37. Based on external ADC system components, the user may need to execute a system calibration to remove external endpoint errors and achieve these specifications (see the Calibration section).
[6] The input signal can be centered on any dc common-mode voltage (V_{CM}) as long as this value is within the ADC voltage input range specified.
[7] DAC linearity is calculated using a reduced code range of 100 to 3995.
[8] DAC gain error is calculated using a reduced code range of 100 to internal 2.5 V V_{REF}.
[9] Endurance is qualified as per JEDEC Standard 22 Method A117 and measured at −40°C, +25°C, +85°C, and +125°C.
[10] Retention lifetime equivalent at junction temperature (T_J) = 85°C as per JEDEC Standard 22 Method A117. Retention lifetime derates with junction temperature.
[11] Test carried out with a maximum of eight I/Os set to a low output level.
[12] Power supply current consumption is measured in normal, pause, and sleep modes under the following conditions: normal mode with 3.6 V supply, pause mode with 3.6 V supply, and sleep mode with 3.6 V supply.
[13] IOV_{DD} power supply current increases typically by 2 mA during a Flash/EE erase cycle.
[14] This current must be added to the AV_{DD} current.

TIMING SPECIFICATIONS

I²C Timing

Table 2. I²C Timing in Fast Mode (400 kHz)

		Slave		Master	
Parameter	Description	Min	Max	Typ	Unit
t_L	SCL low pulse width	200		1360	ns
t_H	SCL high pulse width	100		1140	ns
t_{SHD}	Start condition hold time	300			ns
t_{DSU}	Data setup time	100		740	ns
t_{DHD}	Data hold time	0		400	ns
t_{RSU}	Setup time for repeated start	100			ns
t_{PSU}	Stop condition setup time	100		800	ns
t_{BUF}	Bus-free time between a stop condition and a start condition	1.3			µs
t_R	Rise time for both SCL and SDA		300	200	ns
t_F	Fall time for both SCL and SDA		300		ns

Table 3. I²C Timing in Standard Mode (100 kHz)

		Slave		
Parameter	Description	Min	Max	Unit
t_L	SCL low pulse width	4.7		µs
t_H	SCL high pulse width	4.0		ns
t_{SHD}	Start condition hold time	4.0		µs
t_{DSU}	Data setup time	250		ns
t_{DHD}	Data hold time	0	3.45	µs
t_{RSU}	Setup time for repeated start	4.7		µs
t_{PSU}	Stop condition setup time	4.0		µs
t_{BUF}	Bus-free time between a stop condition and a start condition	4.7		µs
t_R	Rise time for both SCL and SDA		1	µs
t_F	Fall time for both SCL and SDA		300	ns

ABSOLUTE MAXIMUM RATINGS

AGND = GND_{REF} = DACGND = GND_{REF}, T_A = 25°C, unless otherwise noted.

Table 8.

Parameter	Rating
AV_{DD} to IOV_{DD}	−0.3 V to +0.3 V
AGND to DGND	−0.3 V to +0.3 V
IOV_{DD} to IOGND, AV_{DD} to AGND	−0.3 V to +6 V
Digital Input Voltage to IOGND	−0.3 V to +5.3 V
Digital Output Voltage to IOGND	−0.3 V to IOV_{DD} + 0.3 V
V_{REF} to AGND	−0.3 V to AV_{DD} + 0.3 V
Analog Inputs to AGND	−0.3 V to AV_{DD} + 0.3 V
Analog Outputs to AGND	−0.3 V to AV_{DD} + 0.3 V
Operating Temperature Range, Industrial	–40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance	
64-Lead LFCSP	24°C/W
80-Lead LQFP	38°C/W
Peak Solder Reflow Temperature	
SnPb Assemblies (10 sec to 30 sec)	240°C
RoHS Compliant Assemblies (20 sec to 40 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

MEMORY ORGANIZATION

The ADuC7124/ADuC7126 incorporate three separate blocks of memory: 32 kB of SRAM and two 64 kB blocks of on-chip Flash/EE memory. There are 126 kB of on-chip Flash/EE memory available to the user, and the remaining 2 kB are reserved for the system kernel. These blocks are mapped as shown in Figure 24.

Note that, by default, after a reset, the Flash/EE memory is mirrored at Address 0x00000000. It is possible to remap the SRAM at Address 0x00000000 by clearing Bit 0 of the REMAP MMR. This remap function is described in more detail in the Flash/EE memory chapter.

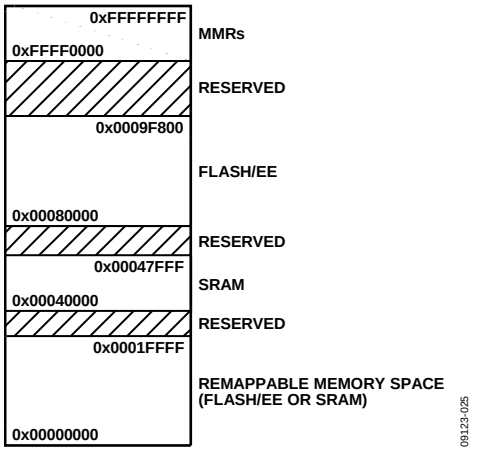

Figure 24. Physical Memory Map

MEMORY ACCESS

The ARM7 core sees memory as a linear array of a 2^{32} byte location where the different blocks of memory are mapped as outlined in Figure 24.

The ADuC7124/ADuC7126 memory organization is configured in little endian format: the least significant byte is located in the lowest byte address and the most significant byte in the highest byte address.

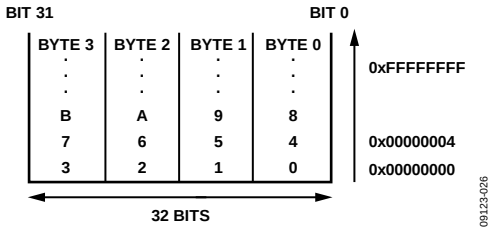

Figure 25. Little Endian Format

FLASH/EE MEMORY

The 128 kB of Flash/EE are organized as two banks of 32 k × 16 bits. Block 0 starts at Address 0x90000 and finishses at Address 0x9F700. In this block, 31 k × 16 bits is user space and 1 k × 16 bits is reserved for the factory-configured boot page. The page size of this Flash/EE memory is 512 bytes.

Block 1 starts at Address 0x80000 and finishses at Address 0x90000. In this block, all 64 kB are available as user space. The block is arranged in 32 k × 16 bits.

The 126 kB of Flash/EE are available to the user as code and nonvolatile data memory. There is no distinction between data and program because ARM code shares the same space. The real width of the Flash/EE memory is 16 bits, meaning that, in ARM mode (32-bit instruction), two accesses to the Flash/EE are necessary for each instruction fetch. Therefore, it is recommended that Thumb mode be used when executing from Flash/EE memory for optimum access speed. The maximum access speed for the Flash/EE memory is 41.78 MHz in Thumb mode and 20.89 MHz in full ARM mode (see the Execution Time from SRAM and Flash/EE section).

SRAM

The 32 kB of SRAM are available to the user, organized as 8 k × 32 bits, that is, 16 k words. ARM code can run directly from SRAM at 41.78 MHz, given that the SRAM array is configured as a 32-bit wide memory array (see the Execution Time from SRAM and Flash/EE section).

MEMORY MAPPED REGISTERS

The memory mapped register (MMR) space is mapped into the upper two pages of the memory array and accessed by indirect addressing through the ARM7 banked registers.

The MMR space provides an interface between the CPU and all on-chip peripherals. All registers except the core registers reside in the MMR area. All shaded locations shown in Figure 26 are unoccupied or reserved locations and should not be accessed by user software. Table 11 to Table 29 show the full MMR memory map.

The access time reading or writing a MMR depends on the advanced microcontroller bus architecture (AMBA) bus used to access the peripheral. The processor has two AMBA buses: the advanced high performance bus (AHB) used for system modules, and the advanced peripheral bus (APB) used for the lower performance peripheral. Access to the AHB is one cycle, and access to the APB is two cycles. All peripherals on the ADuC7124/ADuC7126 are on the APB except the Flash/EE memory and the GPIOs.

Position A. The comparator is held in a balanced condition, and the sampling capacitor arrays acquire the differential signal on the input.

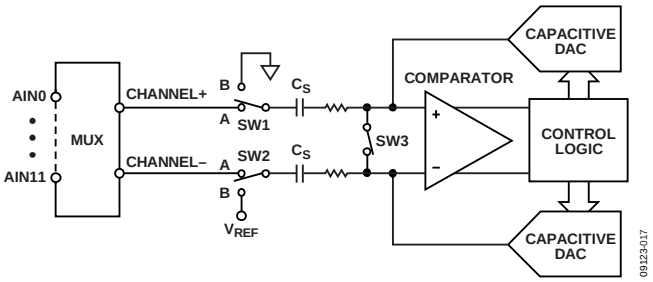

Figure 32. ADC Acquisition Phase

When the ADC starts a conversion, as shown in Figure 33, SW3 opens, and then SW1 and SW2 move to Position B. This causes the comparator to become unbalanced. Both inputs are disconnected once the conversion begins. The control logic and the charge redistribution DACs are used to add and subtract fixed amounts of charge from the sampling capacitor arrays to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. The output impedances of the sources driving the V_{IN+} and V_{IN-} pins must be matched; otherwise, the two inputs have different settling times, resulting in errors.

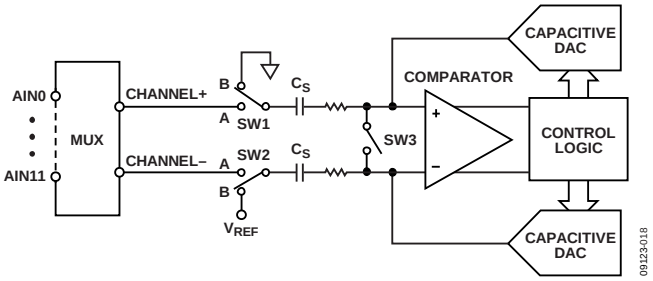

Figure 33. ADC Conversion Phase

Pseudo Differential Mode

In pseudo differential mode, Channel– is linked to the ADCNEG pin of the ADuC7124/ADuC7126. In Figure 34, ADCNEG is represented as V_{IN-}. SW2 switches between A (Channel–) and B (V_{REF}). The ADCNEG pin must be connected to ground or to a low voltage. The input signal on V_{IN+} can then vary from V_{IN-} to $V_{REF} + V_{IN-}$. Note that V_{IN-} must be chosen so that $V_{REF} + V_{IN-}$ do not exceed AV_{DD}.

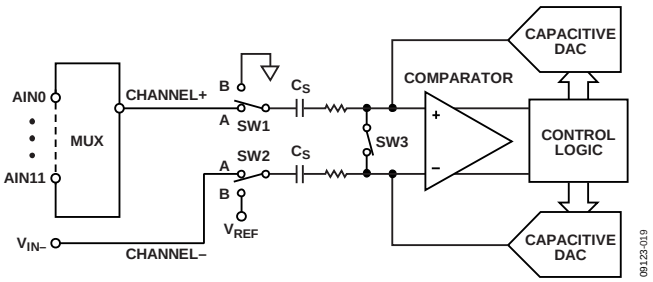

Figure 34. ADC in Pseudo Differential Mode

Single-Ended Mode

In single-ended mode, SW2 is always connected internally to ground. The V_{IN-} pin can be floating. The input signal range on V_{IN+} is 0 V to V_{REF}.

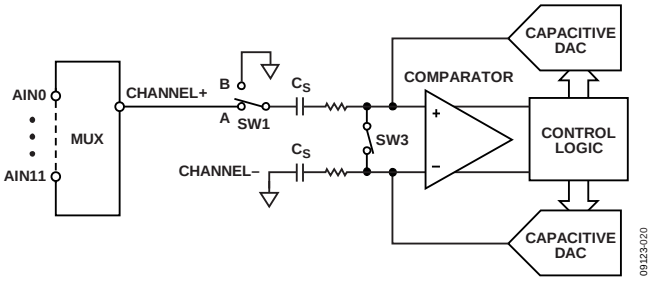

Figure 35. ADC in Single-Ended Mode

Analog Input Structure

Figure 36 shows the equivalent circuit of the analog input structure of the ADC. The four diodes provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signals never exceed the supply rails by more than 300 mV; this can cause these diodes to become forward-biased and start conducting into the substrate. These diodes can conduct up to 10 mA without causing irreversible damage to the part.

The C1 capacitors in Figure 36 are typically 4 pF and can be primarily attributed to pin capacitance. The resistors are lumped components made up of the on resistance of the switches. The value of these resistors is typically about 100 Ω. The C2 capacitors are the sampling capacitors of the ADC and typically have a capacitance of 16 pF.

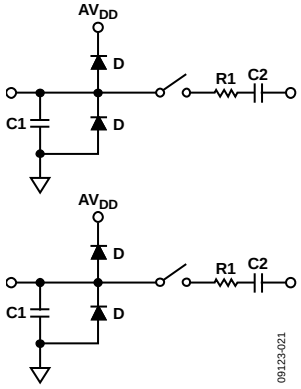

Figure 36. Equivalent Analog Input Circuit Conversion Phase: Switches Open, Track Phase: Switches Closed

for serial downloading via the I²C. A USB-to-I²C download dongle can be purchased from Analog Devices, Inc. This board connects to the USB port of a PC and to the I²C port of the ADuC7126. The part number is USB-I2C/LIN-CONV-Z.

The AN-806 Application Note describes the protocol for serial downloading via the I²C in more detail.

JTAG Access

The JTAG protocol uses the on-chip JTAG interface to facilitate code download and debug.

To access the part via the JTAG interface, the P0.0/BM pin must be set high.

When debugging, user code should not write to the P0.1, P0.2, and P0.3 pins. If user code toggles any of these pins, JTAG debug pods are not able to connect to the ADuC7124/ADuC7126. If this happens, mass erase the part using the UART/I²C downloader.

FLASH/EE MEMORY SECURITY

The 126 kB of Flash/EE memory available to the user can be read and write protected. Bit 31 of the FEE0PRO/FEE0HID MMR protects the 62 kB of Block 0 from being read through JTAG and in UART programming mode. The other 31 bits of this register protect writing to the Flash/EE memory; each bit protects four pages, that is, 2 kB. Write protection is activated for all access types. FEE1PRO and FEE1HID, similarly, protect flash Block 1. Bit 31 of the FEE1PRO/FEE1HID MMR protects the 64 kB of Block 1 from being read through JTAG. Bit 30 protects writing to the top 8 pages of Block 1. The other 30 bits of this register protect writing to the Flash/EE memory; each bit protects four pages, that is, 2 kB

Three Levels of Protection

- Protection can be set and removed by writing directly into FEExHID MMR. This protection does not remain after reset.
- Protection can be set by writing into FEExPRO MMR. It takes effect only after a save protection command (0x0C) and a reset. The FEExPRO MMR is protected by a key to avoid direct access. The key is saved once and must be entered again to modify FEExPRO. A mass erase sets the key back to 0xFFFF but also erases all the user code.
- Flash can be permanently protected by using the FEExPRO MMR and a particular key value of 0xDEADDEAD. Entering the key again to modify the FEExPRO register is not allowed.

Sequence to Write the Key

1. Write the bit in FEExPRO corresponding to the page to be protected.
2. Enable key protection by setting Bit 6 of FEExMOD (Bit 5 must equal 0).
3. Write a 32-bit key in FEExADR and FEExDAT.
4. Run the write key command 0x0C in FEExCON; wait for the read to be successful by monitoring FEExSTA.
5. Reset the part.

To remove or modify the protection, the same sequence is used with a modified value of FEExPRO. If the key chosen is the value 0xDEAD, the memory protection cannot be removed. Only a mass erase unprotects the part, but it also erases all user code.

The sequence to write the key is illustrated in the following example (this protects writing Page 4 to Page 7 of the Flash):

```
FEExPRO=0xFFFFFFFD;    //Protect Page 4 to 7
FEExMOD=0x48;          //Write key enable
FEExADR=0x1234;        //16 bit key value
FEExDAT=0x5678;        //16 bit key value
FEExCON= 0x0C;         //Write key command
```

The same sequence should be followed to protect the part permanently with FEExADR = 0xDEAD and FEExDAT = 0xDEAD.

FLASH/EE CONTROL INTERFACE

Table 37. FEE0STA Register

Name	Address	Default Value	Access
FEE0STA	0xFFFFF800	0x0000	R

Table 38. FEE0MOD Register

Name	Address	Default Value	Access
FEE0MOD	0xFFFFF804	0x80	R/W

Table 39. FEE0CON Register

Name	Address	Default Value	Access
FEE0CON	0xFFFFF808	0x00	R/W

Table 40. FEE0DAT Register

Name	Address	Default Value	Access
FEE0DAT	0xFFFFF80C	0xXXXX	R/W

FEE0DAT is a 16-bit data register.

Table 41. FEE0ADR Register

Name	Address	Default Value	Access
FEE0ADR	0xFFFFF810	0x0000	R/W

FEE0ADR is a 16-bit address register.

Table 42. FEE0SGN Register

Name	Address	Default Value	Access
FEE0SGN	0xFFFFF818	0xFFFFFF	R

FEE0SGN is a 24-bit code signature.

Table 43. FEE0PRO Register

Name	Address	Default Value	Access
FEE0PRO	0xFFFFF81C	0x00000000	R/W

FEE0PRO provides protection following subsequent reset MMR. It requires a software key (see Table 56).

Table 44. FEE0HID Register

Name	Address	Default Value	Access
FEE0HID	0xFFFFF820	0xFFFFFFFF	R/W

FEE0HID provides immediate protection MMR. It does not require any software keys (see Table 56).

Table 54. FEExMOD MMR Bit Descriptions

Bit	Description
[7:5]	Reserved.
4	Flash/EE interrupt enable. Set by the user to enable the Flash/EE interrupt. The interrupt occurs when a command is complete. Cleared by the user to disable the Flash/EE interrupt.
3	Erase/write command protection. Set by the user to enable the erase and write commands. Cleared to protect the Flash/EE memory against the erase/write command.
2	Reserved. Should always be set to 0 by the user.
[1:0]	Flash/EE wait states. Both Flash/EE blocks must have the same wait state value for any change to take effect.

Table 55. Command Codes in FEExCON

Code	Command	Description
0x00[1]	Null	Idle state.
0x01[1]	Single read	Load FEExDAT with the 16-bit data indexed by FEExADR.
0x02[1]	Single write	Write FEExDAT at the address pointed to by FEExADR. This operation takes 50 µs.
0x03[1]	Erase/write	Erase the page indexed by FEExADR and write FEExDAT at the location pointed to by FEExADR. This operation takes 20 ms.
0x04[1]	Single verify	Compare the contents of the location pointed to by FEExADR to the data in FEExDAT. The result of the comparison is returned in FEExSTA, Bit 1.
0x05[1]	Single erase	Erase the page indexed by FEExADR.
0x06[1]	Mass erase	Erase user space. The 2 kB of kernel are protected in Block 0. This operation takes 2.48 sec. To prevent accidental execution, a command sequence is required to execute this instruction.
0x07	Reserved	Reserved.
0x08	Reserved	Reserved.
0x09	Reserved	Reserved.
0x0A	Reserved	Reserved.
0x0B	Signature	Gives a signature of the 64 kB of Flash/EE in the 24-bit FEExSIGN MMR. This operation takes 32,778 clock cycles.
0x0C	Protect	This command can be run only once. The value of FEExPRO is saved and can be removed only with a mass erase (0x06) or with the key.
0x0D	Reserved	Reserved.
0x0E	Reserved	Reserved.
0x0F	Ping	No operation, interrupt generated.

[1] The FEExCON register always reads 0x07 immediately after execution of any of these commands.

Table 56. FEE0PRO and FEE0HID MMR Bit Descriptions

Bit	Description
31	Read protection. Cleared by the user to protect Block 0. Set by the user to allow reading of Block 0.
[30:0]	Write protection for Page 123 to Page 0. Each bit protects protects a group of 4 pages. Cleared by the user to protect the pages when writing to flash. Thus preventing an accidental write to specific pages in flash. Set by the user to allow writing to the pages.

Table 57. FEE1PRO and FEE1HID MMR Bit Descriptions

Bit	Description
31	Read protection. Cleared by the user to protect Block 1. Set by the user to allow reading of Block 1.
30	Write protection for Page 127 to Page 120. Cleared by the user to protect the pages when writing to flash. Thus preventing an accidental write to specific pages in flash. Set by the user to allow writing to the pages.
[29:0]	Write protection for Page 119 to Page 116 and for Page 0 to Page 3. Cleared by the user to protect the pages in writing. Set by the user to allow writing to the pages.

EXECUTION TIME FROM SRAM AND FLASH/EE

This section describes SRAM and Flash/EE access times during execution for applications where execution time is critical.

Execution from SRAM

Fetching instructions from SRAM takes one clock cycle because the access time of the SRAM is 2 ns, and a clock cycle is 24 ns minimum. However, if the instruction involves reading or writing data to memory, one extra cycle must be added if the data is in SRAM (or three cycles if the data is in Flash/EE): one cycle to execute the instruction and two cycles to get the 32-bit data from Flash/EE. A control flow instruction (a branch instruction, for example) takes one cycle to fetch but also takes two cycles to fill the pipeline with the new instructions.

Execution from Flash/EE

Because the Flash/EE width is 16 bits and access time for 16-bit words is 22 ns, execution from Flash/EE cannot be done in one cycle (as can be done from SRAM when the CD bit = 0). Also, some dead times are needed before accessing data for any value of the CD bits.

In ARM mode, where instructions are 32 bits, two cycles are needed to fetch any instruction when CD = 0. In Thumb mode, where instructions are 16 bits, one cycle is needed to fetch any instruction.

Timing is identical in both modes when executing instructions that involve using the Flash/EE for data memory. If the instruction to be executed is a control flow instruction, an extra cycle is needed to decode the new address of the program counter, and then four cycles are needed to fill the pipeline. A data processing instruction involving only the core register does not require any extra clock cycles. However, if it involves data in Flash/EE, an extra clock cycle is needed to decode the address of the data, and two cycles are needed to get the 32-bit data from Flash/EE. An extra cycle must also be added before fetching another instruction. Data transfer instructions are more complex and are summarized in Table 58.

Table 58. Execution Cycles in ARM/Thumb Mode

Instructions	Fetch Cycles	Dead Time	Data Access	Dead Time
LD[1]	2/1	1	2	1
LDH	2/1	1	1	1
LDM/PUSH	2/1	N[2]	2 × N[2]	N[1]
STR[1]	2/1	1	2 × 20 ns	1
STRH	2/1	1	20 ns	1
STRM/POP	2/1	N[1]	2 × N × 20 ns[1]	N[1]

[1] The SWAP instruction combines an LD and STR instruction with only one fetch, giving a total of eight cycles + 40 ns.
[2] N is the number of data bytes to load or store in the multiple load/store instruction (1 < N ≤ 16).

RESET AND REMAP

The ARM exception vectors are all situated at the bottom of the memory array, from Address 0x00000000 to Address 0x00000020, as shown in Figure 40.

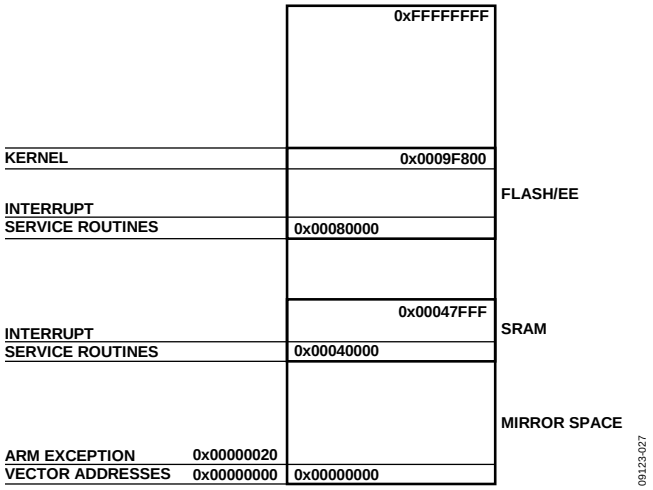

Figure 40. Remap for Exception Execution

By default, and after any reset, the Flash/EE is mirrored at the bottom of the memory array. The remap function allows the programmer to mirror the SRAM at the bottom of the memory array, which facilitates execution of exception routines from SRAM instead of from Flash/EE. This means exceptions are executed twice as fast, being executed in 32-bit ARM mode with 32-bit wide SRAM instead of 16-bit wide Flash/EE memory.

External Crystal Selection

To switch to an external crystal, the user must follow this procedure:

1. Enable the Timer2 interrupt and configure it for a timeout period of >120 µs.
2. Follow the write sequence to the PLLCON register, setting the MDCLK bits to 01 and clearing the OSEL bit.
3. Force the part into nap mode by following the correct write sequence to the POWCON0 register.
4. When the part is interrupted from nap mode by the Timer2 interrupt source, the clock source has switched to the external clock.

Example source code:

```
    T2LD = 5;
    T2CON = 0x480;
  IRQEN = 0x10;
//enable T2 interrupt
  PLLKEY1 = 0xAA;
  PLLCON = 0x01;
  PLLKEY2 = 0x55;

  POWKEY1 = 0x01;
  POWCON0 = 0x27;  // Set core into nap mode
  POWKEY2 = 0xF4;
```

In noisy environments, noise can couple to the external crystal pins, and PLL may lose lock momentarily. A PLL interrupt is provided in the interrupt controller. The core clock is immediately halted, and this interrupt is serviced only when the lock is restored.

In case of crystal loss, the watchdog timer should be used. During initialization, a test on the RSTSTA can determine if the reset came from the watchdog timer.

External Clock Selection

To switch to an external clock on P0.7, configure P0.7 in Mode 1. The external clock can be up to 41.78 MHz, providing the tolerance is 1%.

Example source code:

```
    T2LD = 5;
    T2CON = 0x480;


  IRQEN = 0x10;
//enable T2 interrupt
  PLLKEY1 = 0xAA;
  PLLCON = 0x03; //Select external clock
  PLLKEY2 = 0x55;

  POWKEY1 = 0x01;
  POWCON0 = 0x27;                          //
Set core into nap mode
  POWKEY2 = 0xF4;
```

Power Control System

A choice of operating modes is available on the ADuC7124/ ADuC7126. Table 70 describes what part is powered on in the different modes and indicates the power-up time.

Table 71 gives some typical values of the total current consumption (analog + digital supply currents) in the different modes, depending on the clock divider bits. The AC, DAC, I^2C, and SPI are turned off.

Table 70. Operating Modes

Mode	Core	Peripherals	PLL	XTAL/T2/T3	IRQ0 to IRQ3	Start-Up/Power-On Time
Active	On	On	On	On	On	66 ms at CD = 0
Pause		On	On	On	On	2.6 µs at CD = 0; 247 µs at CD = 7
Nap			On	On	On	2.6 µs at CD = 0; 247 µs at CD = 7
Sleep				On	On	1.58 ms
Stop					On	1.7 ms

Table 71. Typical Current Consumption at 25°C in mA, V_{DD} = 3.3 V

Mode	CD = 0	CD = 1	CD = 2	CD = 3	CD = 4	CD = 5	CD = 6	CD = 7
Active	33.3	23.1	15.4	11.6	9.7	8.8	8.3	8.1
Pause	20.6	12.7	8.8	6.8	5.8	5.3	5.1	4.9
Nap	4.6	4.6	4.6	4.6	4.6	4.6	4.6	4.6
Sleep	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2
Stop	0.2	0.2	0.2	0.2	0.2	0.2	0.2	0.2

Table 79. GPxCON Registers

Name	Address	Default Value	Access
GP0CON	0xFFFFF400	0x00000000	R/W
GP1CON	0xFFFFF404	0x00000000	R/W
GP2CON	0xFFFFF408	0x00000000	R/W
GP3CON	0xFFFFF40C	0x00000000	R/W
GP4CON	0xFFFFF410	0x00000000	R/W

GPxCON are the Port x control registers that select the function of each pin of Port x, as described in Table 80.

Table 80. GPxCON MMR Bit Descriptions

Bit	Description
[31:30]	Reserved.
[29:28]	Select function of Px.7 pin.
[27:26]	Reserved.
[25:24]	Select function of Px.6 pin.
[23:22]	Reserved.
[21:20]	Select function of Px.5 pin.
[19:18]	Reserved.
[17:16]	Select function of Px.4 pin.
[15:14]	Reserved.
[13:12]	Select function of Px.3 pin.
[11:10]	Reserved.
[9:8]	Select function of Px.2 pin.
[7:6]	Reserved.
[5:4]	Select function of Px.1 pin.
[3:2]	Reserved.
[1:0]	Select function of Px.0 pin.

Table 81. GPxPAR Registers

Name	Address	Default Value	Access
GP0PAR	0xFFFFF42C	0x20000000	R/W
GP1PAR	0xFFFFF43C	0x00000000	R/W
GP2PAR	0xFFFFF44C	0x000000FF	R/W
GP3PAR	0xFFFFF45C	0x00222222	R/W
GP4PAR	0xFFFFF46C	0x00000000	R/W

The GPxPAR registers program the parameters for Port 0, Port 1, Port 2, Port 3, and Port 4. Note that the GPxDAT MMR must always be written after changing the GPxPAR MMR.

Table 82. GPxPAR MMR Bit Descriptions

Bit	Description
31	Reserved.
[30:29]	Drive strength Px.7.
28	Pull-up disable Px.7.
27	Reserved.
[26:25]	Drive strength Px.6.
24	Pull-up disable Px.6.
23	Reserved.
[22:21]	Drive strength Px.5.
20	Pull-up disable Px.5.
19	Reserved.
[18:17]	Drive strength Px.4.
16	Pull-up disable Px.4.
15	Reserved.
[14:13]	Drive strength Px.3.
12	Pull-up disable Px.3.
11	Reserved.
[10:9]	Drive strength Px.2.
8	Pull-up disable Px.2.
7	Reserved.
[6:5]	Drive strength Px.1.
4	Pull-up disable Px.1.
3	Reserved.
[2:1]	Drive strength Px.0.
0	Pull-up disable Px.0.

Table 83. GPIO Drive Strength Control Bits Descriptions

Control Bits Value	Description
00	Medium drive strength.
01	Low drive strength.
1x	High drive strength.

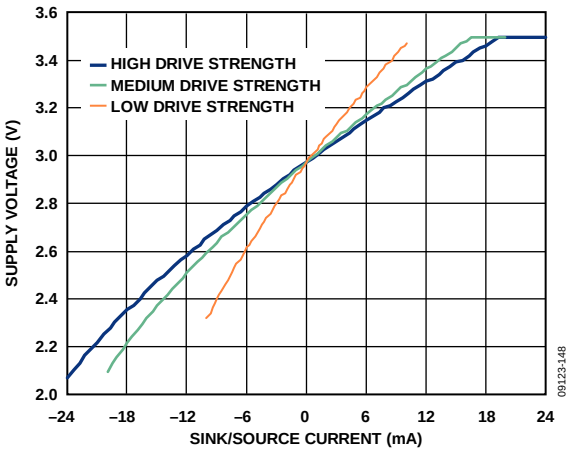

Figure 46. Programmable Strength for High Level

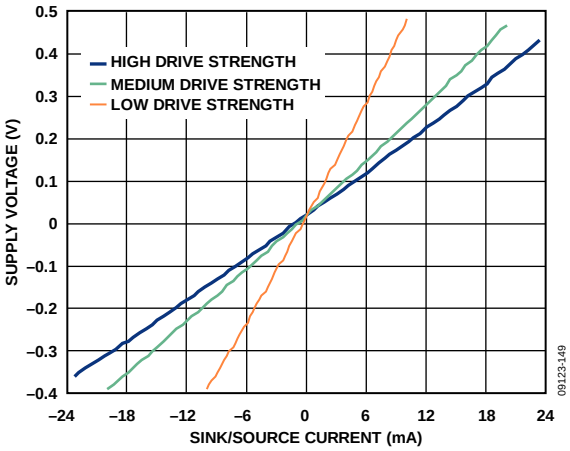

Figure 47. Programmable Strength for Low Level

COM1STA0 Register

Name: COM1STA0

Address: 0xFFFF0754

Default Value: 0xE0

Access: Read only

COM1STA0 is the line status register for UART1.

Table 97. COMxSTA0 MMR Bit Descriptions

Bit	Name	Description
11	RX_error	Set automatically if PE, FE, or BI is set. Cleared automatically when PE, FE, and BI are cleared .
10	RX_timeout	Only for FIFO mode. Set automatically if there is at least one byte in the Rx FIFO and there is no access to the Rx FIFO in the next 4-byte accessing cycle.
9	RX_triggered	Only for FIFO mode. Set automatically if the Rx FIFO number exceeds the trigger level, which is configured by the FIFO control register COMxFCR[7:5]. Cleared automatically when the Rx FIFO number is equal to or less than the trigger level.
8	TX_full	Only for FIFO mode. Set automatically if Tx FIFO is full. Cleared automatically when Tx FIFO is not full.
7	TX_half_empty	Only for FIFO mode. Set automatically if the Tx FIFO is half empty (number of bytes in Tx FIFO ≤ 8). Cleared automatically when the Tx FIFO received bytes is more than eight bytes.
6	TEMT	COMxTX empty status bit. For non-FIFO mode, both THR and TSR are empty. For FIFO mode, both Tx FIFO and TSR are empty.
5	THRE	COMxTX and transmitter shift register empty. For non-FIFO mode, transmitter hold register (THR) empty or the content of THR has been transferred to the transmitter shift register (TSR). For FIFO mode, Tx FIFO is empty, or the last character in the FIFO has been transferred to the transmitter shift register (TSR).
4	BI	Break error. Set when SINx is held low for more than the maximum word length. Cleared automatically.
3	FE	Framing error. Set when an invalid stop bit occurs. Cleared automatically.
2	PE	Parity error. Set when a parity error occurs. Cleared automatically.
1	OE	Overrun error. For non-FIFO mode, set automatically if data is overwritten before being read. Cleared automatically. For FIFO mode, set automatically if an overrun error has been detected. An overrun error occurs only after the FIFO is full and the next character has been completely received in the shift register. The new character overwrites the character in the shift register, but it is not transferred to the FIFO.
0	DR	Data ready. For non-FIFO mode, set automatically when COMxRX is full. Cleared by reading COMxRX. For FIFO mode, set automatically when there is at least one unread byte in the COMxRX.

COM0STA1 Register

Name: COM0STA1

Address: 0xFFFF0718

Default Value: 0x00

Access: Read only

COM0STA1 is a modem status register.

COM1STA1 Register

Name: COM1STA1

Address: 0xFFFF0758

Default Value: 0x00

Access: Read only

COM1STA1 is a modem status register.

Table 98. COMxSTA1 MMR Bit Descriptions

Bit	Name	Description
7	DCD	Data carrier detect.
6	RI	Ring indicator.
5	DSR	Data set ready.
4	CTS	Clear to send.
3	DDCD	Delta DCD. Set automatically if DCD changed state since last COMxSTA1 read. Cleared automatically by reading COMxSTA1.
2	TERI	Trailing edge RI. Set if RI changed from 0 to 1 since COMxSTA1 last read. Cleared automatically by reading COMxSTA1.
1	DDSR	Delta DSR. Set automatically if DSR changed state since COMxSTA1 last read. Cleared automatically by reading COMxSTA1.
0	DCTS	Delta CTS. Set automatically if CTS changed state since COMxSTA1 last read. Cleared automatically by reading COMxSTA1.

Table 113. PWMCON0 MMR Bit Descriptions

Bit	Name	Description
14	SYNC	Enables PWM synchronization. Set to 1 by the user so that all PWM counters are reset on the next clock edge after the detection of a high-to-low transition on the P3.7/PWM_{SYNC} pin. Cleared by the user to ignore transitions on the P3.7/PWM_{SYNC} pin.
13	PWM5INV	Set to 1 by the user to invert PWM5. Cleared by the user to use PWM5 in normal mode.
12	PWM3INV	Set to 1 by the user to invert PWM3. Cleared by the user to use PWM3 in normal mode.
11	PWM1INV	Set to 1 by the user to invert PWM1. Cleared by the user to use PWM1 in normal mode.
10	PWMTRIP	Set to 1 by the user to enable PWM trip interrupt. When the PWM trip input (Pin P3.6/PWM_{TRIP} or Pin P0.4/PWM_{TRIP}) is low, the PWMEN bit is cleared and an interrupt is generated. Cleared by the user to disable the PWMTRIP interrupt.
9	ENA	If HOFF = 0 and HMODE = 1; note that, if not in H-bridge mode, this bit has no effect. Set to 1 by the user to enable PWM outputs. Cleared by the user to disable PWM outputs. If HOFF = 1 and HMODE = 1, see Table 114.
[8:6]	PWMCP[2:0]	PWM clock prescaler bits. Sets the UCLK divider. [000] = UCLK/2. [001] = UCLK/4. [010] = UCLK/8. [011] = UCLK/16. [100] = UCLK/32. [101] = UCLK/64. [110] = UCLK/128. [111] = UCLK/256.
5	POINV	Set to 1 by the user to invert all PWM outputs. Cleared by the user to use PWM outputs as normal.
4	HOFF	High side off. Set to 1 by the user to force PWM0 and PWM2 outputs high. This also forces PWM1 and PWM3 low. Cleared by the user to use the PWM outputs as normal.
3	LCOMP	Load compare registers. Set to 1 by the user to load the internal compare registers with the values in PWMxCOMx on the next transition of the PWM timer from 0x00 to 0x01. Cleared by the user to use the values previously stored in the internal compare registers.
2	DIR	Direction control. Set to 1 by the user to enable PWM0 and PWM1 as the output signals while PWM2 and PWM3 are held low. Cleared by the user to enable PWM2 and PWM3 as the output signals while PWM0 and PWM1 are held low.
1	HMODE	Enables H-bridge mode.[1] Set to 1 by the user to enable H-bridge mode and Bit 1 to Bit 5 of PWMCON. Cleared by the user to operate the PWMs in standard mode.
0	PWMEN	Set to 1 by the user to enable all PWM outputs. Cleared by the user to disable all PWM outputs.

[1] In H-bridge mode, HMODE = 1. See Table 114 to determine the PWM outputs.

Table 114. PWM Output Selection, HMODE = 1

PWMCON0 MMR[1]				PWM Outputs[2]			
ENA	HOFF	POINV	DIR	PWM0	PWM1	PWM2	PWM3
0	0	X	X	1	1	1	1
X	1	X	X	1	0	1	0
1	0	0	0	0	0	HS	LS
1	0	0	1	HS	LS	0	0
1	0	1	0	HS	LS	1	1
1	0	1	1	1	1	HS	LS

[1] X = don't care.
[2] HS = high side, LS = low side.

On power-up, PWMCON0 defaults to 0x12 (HOFF = 1 and HMODE = 1). All GPIO pins associated with the PWM are configured in PWM mode by default (see Table 115).

Table 115. Compare Registers

Name	Address	Default Value	Access
PWM0COM0	0xFFFF0F84	0x0000	R/W
PWM0COM1	0xFFFF0F88	0x0000	R/W
PWM0COM2	0xFFFF0F8C	0x0000	R/W
PWM1COM0	0xFFFF0F94	0x0000	R/W
PWM1COM1	0xFFFF0F98	0x0000	R/W
PWM1COM2	0xFFFF0F9C	0x0000	R/W
PWM2COM0	0xFFFF0FA4	0x0000	R/W
PWM2COM1	0xFFFF0FA8	0x0000	R/W
PWM2COM2	0xFFFF0FAC	0x0000	R/W

The PWM trip interrupt can be cleared by writing any value to the PWMCLRI MMR. Note that, when using the PWM trip interrupt, users should make sure that the PWM interrupt has been cleared before exiting the ISR. This prevents generation of multiple interrupts.

PWM Convert Start Control

The PWM can be configured to generate an ADC convert start signal after the active low side signal goes high. There is a programmable delay between the time that the low-side signal goes high and the convert start signal is generated.

This is controlled via the PWMCON1 MMR. If the delay selected is higher than the width of the PWM pulse, the interrupt remains low.

Table 116. PWMCON1 MMR Bit Descriptions (Address = 0xFFFF0FB4; Default Value = 0x00)

Bit	Value	Name	Description
7		CSEN	Set to 1 by the user to enable the PWM to generate a convert start signal. Cleared by user to disable the PWM convert start signal.
[3:0]		CSD3 CSD2 CSD1 CSD0	Convert start delay. Delays the convert start signal by a number of clock pulses.
	0000		Four clock pulses.
	0001		Eight clock pulses.
	0010		12 clock pulses.
	0011		16 clock pulses.
	0100		20 clock pulses.
	0101		24 clock pulses.
	0110		28 clock pulses.
	0111		32 clock pulses.
	1000		36 clock pulses.
	1001		40 clock pulses.
	1010		44 clock pulses.
	1011		48 clock pulses.
	1100		52 clock pulses.
	1101		56 clock pulses.
	1110		60 clock pulses.
	1111		64 clock pulses.

When calculating the time from the convert start delay to the start of an ADC conversion, the user must take account of internal delays. The following example shows the case of a delay of four clocks. One additional clock is required to pass the convert start signal to the ADC logic. Once the ADC logic receives the convert start signal, an ADC conversion begins on the next ADC clock edge (see Figure 50).

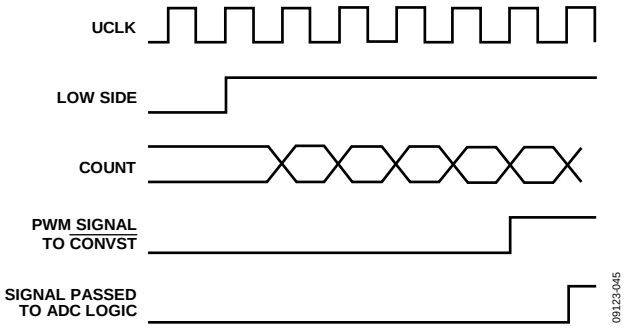

Figure 50. ADC Conversion

FIQVEC Register

The FIQ interrupt vector register, FIQVEC, points to a memory address containing a pointer to the interrupt service routine of the currently active FIQ. This register should be read only when an FIQ occurs and FIQ interrupt nesting has been enabled by setting Bit 1 of the IRQCONN register.

Name: FIQVEC

Address: 0xFFFF011C

Default Value: 0x00000000

Access: Read only

Table 136. FIQVEC MMR Bit Descriptions

Bit	Type	Initial Value	Description
[31:23]	R	0	Always read as 0.
[22:7]	R/W	0	IRQBASE register value.
[6:2]		0	Highest priority source. This is a value between 0 and 27, representing the currently active interrupt source. The interrupts are listed in Table 126. For example, if the highest currently active FIQ is Timer2, then these bits are [00100].
[1:0]		0	Reserved.

FIQSTAN Register

If IRQCONN Bit 1 is asserted and FIQVEC is read, one of the FIQSTAN[7:0] bits is asserted. The bit that asserts depends on the priority of the FIQ. If the FIQ is of Priority 0, Bit 0 asserts, if Priority 1, Bit 1 asserts, and so forth.

When a bit is set in this register all interrupts of that priority and lower are blocked.

To clear a bit in this register, all bits of a higher priority must be cleared first. It is possible to clear only one bit at a time. For example, if this register is set to 0x09, then writing 0xFF changes the register to 0x08 and writing 0xFF a second time changes the register to 0x00.

Name: FIQSTAN

Address: 0xFFFF013C

Default Value: 0x00000000

Access: Read/write

Table 137. FIQSTAN MMR Bit Descriptions

Bit	Name	Description
31:8		Reserved. These bits are reserved and should not be written to.
7:0		Setting this bit to 1 enables nesting of FIQ interrupts. Clearing this bit means no nesting or prioritization of FIQs is allowed.

External Interrupts and PLA interrupts

The ADuC7124/ADuC7126 provide up to four external interrupt sources and two PLA interrupt sources. These external interrupts can be individually configured as level or rising/falling edge triggered.

To enable the external interrupt source or the PLA interrupt source, the appropriate bit must first be set in the FIQEN or IRQEN register. To select the required edge or level to trigger on, the IRQCONE register must be appropriately configured.

To properly clear an edge-based external IRQ interrupt or an edge-based PLA interrupt, set the appropriate bit in the IRQCLRE register.

IRQCONE Register

Name: IRQCONE

Address: 0xFFFF0034

Default Value: 0x00000000

Access: Read/write

Table 138. IRQCONE MMR Bit Descriptions

Bit	Value	Name	Description
[31:12]			Reserved. These bits are reserved and should not be written to.
[11:10]	11	PLA1SRC[1:0]	PLA IRQ1 triggers on falling edge.
	10		PLA IRQ1 triggers on rising edge.
	01		PLA IRQ1 triggers on low level.
	00		PLA IRQ1 triggers on high level.
[9:8]	11	IRQ3SRC[1:0]	External IRQ3 triggers on falling edge.
	10		External IRQ3 triggers on rising edge.
	01		External IRQ3 triggers on low level.
	00		External IRQ3 triggers on high level.

Bit	Value	Name	Description
[7:6]	11	IRQ2SRC[1:0]	External IRQ2 triggers on falling edge.
	10		External IRQ2 triggers on rising edge.
	01		External IRQ2 triggers on low level.
	00		External IRQ2 triggers on high level.
[5:4]	11	PLA0SRC[1:0]	PLA IRQ0 triggers on falling edge.
	10		PLA IRQ0 triggers on rising edge.
	01		PLA IRQ0 triggers on low level.
	00		PLA IRQ0 triggers on high level.
[3:2]	11	IRQ1SRC[1:0]	External IRQ1 triggers on falling edge.
	10		External IRQ1 triggers on rising edge.
	01		External IRQ1 triggers on low level.
	00		External IRQ1 triggers on high level.
[1:0]	11	IRQ0SRC[1:0]	External IRQ0 triggers on falling edge.
	10		External IRQ0 triggers on rising edge.
	01		External IRQ0 triggers on low level.
	00		External IRQ0 triggers on high level.

IRQCLRE Register

Name: IRQCLRE

Address: 0xFFFF0038

Default Value: 0x00000000

Access: Write only

Table 139. IRQCLRE MMR Bit Descriptions

Bit	Name	Description
[31:25]		Reserved. These bits are reserved and should not be written to.
24	PLA1CLRI	A 1 must be written to this bit in the PLA IRQ1 interrupt service routine to clear an edge-triggered PLA IRQ1 interrupt.
23	IRQ3CLRI	A 1 must be written to this bit in the external IRQ3 interrupt service routine to clear an edge-triggered IRQ3 interrupt.
22	IRQ2CLRI	A 1 must be written to this bit in the external IRQ2 interrupt service routine to clear an edge-triggered IRQ2 interrupt.
21	PLA0CLRI	A 1 must be written to this bit in the PLA IRQ0 interrupt service routine to clear an edge-triggered PLA IRQ0 interrupt.
20	IRQ1CLRI	A 1 must be written to this bit in the external IRQ1 interrupt service routine to clear an edge-triggered IRQ1 interrupt.
[19:18]		Reserved. These bits are reserved and should not be written to.
17	IRQ0CLRI	A 1 must be written to this bit in the external IRQ0 interrupt service routine to clear an edge triggered IRQ0 interrupt.
[16:0]		Reserved. These bits are reserved and should not be written to.

Table 141. T0CON MMR Bit Descriptions

Bit	Value	Description
[31:8]		Reserved.
7		Timer0 enable bit. Set by the user to enable Timer0. Cleared by the user to disable Timer0 by default.
6		Timer0 mode. Set by the user to operate in periodic mode. Cleared by the user to operate in free-running mode. Default mode.
[5:4]		Clock select bits.
	00	HCLK.
	01	UCLK.
	10	32.768 kHz.
	11	Reserved.
[3:2]		Prescale.
	00	Core clock/1. Default value.
	01	Core clock/16.
	10	Core clock/256.
	11	Undefined. Equivalent to 00.
[1:0]		Reserved.

T0CLRI Register

Name: T0CLRI

Address: 0xFFFF030C

Default Value: 0xFF

Access: Write only

T0CLRI is an 8-bit register. Writing any value to this register clears the interrupt.

Timer1 (General-Purpose Timer)

Timer1 is a general-purpose, 32-bit timer (count down or count up) with a programmable prescaler. The source can be the 32 kHz external crystal, the undivided system, the core clock, or P1.1 (maximum frequency 41.78 MHz). This source can be scaled by a factor of 1, 16, 256, or 32,768.

The counter can be formatted as a standard 32-bit value or as hours: minutes: seconds: hundredths.

Timer1 has a capture register (T1CAP) that can be triggered by a selected IRQ source initial assertion. This feature can be used to determine the assertion of an event more accurately than the precision allowed by the RTOS timer when the IRQ is serviced.

Timer1 can be used to start ADC conversions.

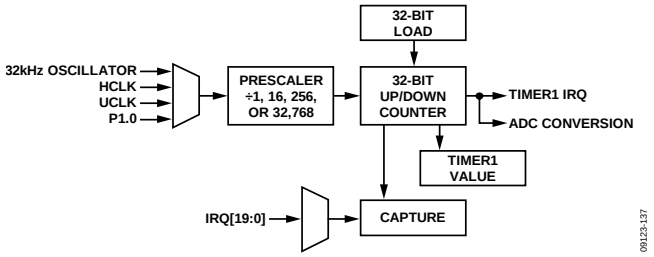

Figure 54. Timer1 Block Diagram

The Timer1 interface consists of five MMRs: T1LD, T1VAL, T1CON, T1CLRI, and T1CAP.

T1LD Register

Name: T1LD

Address: 0xFFFF0320

Default Value: 0x00000000

Access: Read/write

T1LD is a 32-bit load register.

T1VAL Register

Name: T1VAL

Address: 0xFFFF0324

Default Value: 0xFFFFFFFF

Access: Read only

T1VAL is a 32-bit read-only register that represents the current state of the counter.

T1CON Register

Name: T1CON

Address: 0xFFFF0328

Default Value: 0x0000

Access: Read/write

T1CON is the configuration MMR described in Table 142.

Table 142. T1CON MMR Bit Descriptions

Bit	Value	Description
[31:18]		Reserved.
17		Event select bit. Set by user to enable time capture of an event. Cleared by the user to disable time capture of an event.
[16:12]		Event select range, 0 to 25. These events are as described in Table 126. All events are offset by two, that is, Event 2 in Table 126 becomes Event 0 for the purposes of Timer0.
[11:9]		Clock select.
	000	Core clock (41 MHz/2^{CD}).
	001	32.768 kHz.
	010	UCLK.
	011	P1.0 raising edge triggered.
8		Count up. Set by the user for Timer1 to count up. Cleared by the user for Timer1 to count down by default.
7		Timer1 enable bit. Set by the user to enable Timer1. Cleared by the user to disable Timer1 by default.
6		Timer1 mode. Set by the user to operate in periodic mode. Cleared by the user to operate in free-running mode. Default mode.
[5:4]		Format.
	00	Binary.
	01	Reserved.
	10	Hr: min: sec: hundredths (23 hours to 0 hour).
	11	Hr: min: sec: hundredths (255 hours to 0 hour).
[3:0]		Prescale.
	0000	Source clock/1.
	0100	Source clock/16.
	1000	Source clock/256.
	1111	Source clock/32,768.

T1CLRI Register

Name: T1CLRI

Address: 0xFFFF032C

Default Value: 0xFF

Access: Write only

T1CLRI is an 8-bit register. Writing any value to this register clears the Timer1 interrupt.

T1CAP Register

Name: T1CAP

Address: 0xFFFF0330

Default Value: 0x00000000

Access: Read

T1CAP is a 32-bit register. It holds the value contained in T1VAL when a particular event occurrs. This event must be selected in T1CON.

Timer2 (Wake-Up Timer)

Timer2 is a 32-bit wake-up timer, count down or count up, with a programmable prescaler. The prescaler is clocked directly from one of four clock sources, including the core clock (default selection), the internal 32.768 kHz oscillator, the external 32.768 kHz watch crystal, or the PLL undivided clock. The selected clock source can be scaled by a factor of 1, 16, 256, or 32,768. The wake-up timer continues to run when the core clock is disabled. This gives a minimum resolution of 22 ns when the core is operating at 41.78 MHz and with a prescaler of 1. Capture of the current timer value is enabled if the Timer2 interrupt is enabled via IRQEN[4] (see Table 126).

The counter can be formatted as a plain 32-bit value or as hours: minutes: seconds: hundredths.

Timer2 reloads the value from T2LD either when Timer2 overflows or immediately when T2CLRI is written.

The Timer2 interface consists of four MMRs, shown in Table 143.

Table 143. Timer2 Interface Registers

Register	Description
T2LD	32-bit register. Holds 32-bit unsigned integers.
T2VAL	32-bit register. Holds 32-bit unsigned integers. This register is read only.
T2CLRI	8-bit register. Writing any value to this register clears the Timer2 interrupt.
T2CON	Configuration MMR.

Timer2 Load Registers

Name: T2LD

Address: 0xFFFF0340

Default Value: 0x00000

Access: Read/write

T2LD is a 32-bit register, which holds the 32-bit value that is loaded into the counter.

GROUNDING AND BOARD LAYOUT RECOMMENDATIONS

As with all high resolution data converters, special attention must be paid to grounding and PC board layout of the ADuC7124/ADuC7126-based designs to achieve optimum performance from the ADCs and DAC.

Although the part has separate pins for analog and digital ground (AGND and IOGND), the user must not tie these to two separate ground planes unless the two ground planes are connected very close to the part. This is illustrated in the simplified example shown in Figure 66a. In systems where digital and analog ground planes are connected together somewhere else (at the power supply of the system, for example), the planes cannot be reconnected near the part because a ground loop results. In these cases, tie all the ADuC7124/ADuC7126 AGND and IOGND pins to the analog ground plane, as illustrated in Figure 66b. In systems with only one ground plane, ensure that the digital and analog components are physically separated onto separate halves of the board so that digital return currents do not flow near analog circuitry (and vice versa).

The ADuC7124/ADuC7126 can then be placed between the digital and analog sections, as illustrated in Figure 66c.

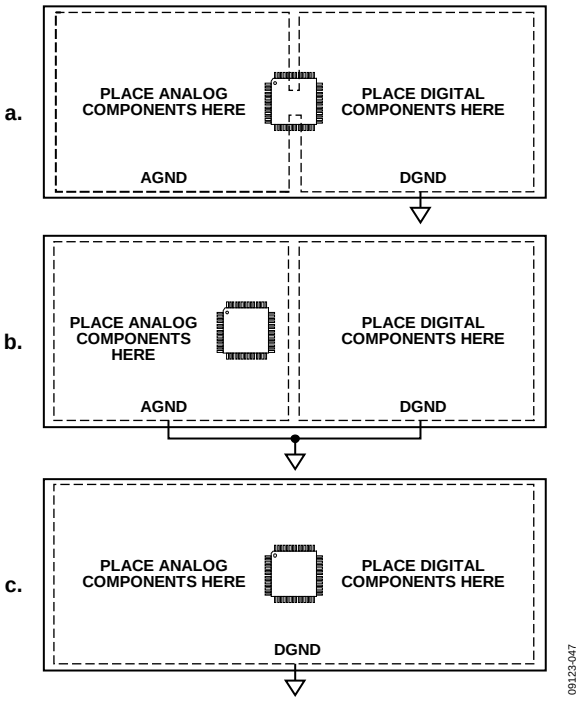

Figure 66. System Grounding Schemes

In all of these scenarios, and in more complicated real-life applications, the users should pay particular attention to the flow of current from the supplies and back to ground. Make sure the return paths for all currents are as close as possible to the paths the currents took to reach their destinations.

For example, do not power components on the analog side (as seen in Figure 66b) with IOV_{DD} because that forces return currents from IOV_{DD} to flow through AGND. Avoid digital currents flowing under analog circuitry, which can occur if a noisy digital chip is placed on the left half of the board (shown in Figure 66c). If possible, avoid large discontinuities in the ground plane(s), such as those formed by a long trace on the same layer, because they force return signals to travel a longer path. In addition, make all connections to the ground plane directly, with little or no trace separating the pin from its via to ground.

When connecting fast logic signals (rise/fall time < 5 ns) to any of the ADuC7124/ADuC7126 digital inputs, add a series resistor to each relevant line to keep rise and fall times longer than 5 ns at the input pins of the part. A value of 100 Ω or 200 Ω is usually sufficient to prevent high speed signals from coupling capacitively into the part and affecting the accuracy of ADC conversions.

CLOCK OSCILLATOR

The clock source for the ADuC7124/ADuC7126 can be generated by the internal PLL or by an external clock input. To use the internal PLL, connect a 32.768 kHz parallel resonant crystal between XCLKI and XCLKO, and connect a capacitor from each pin to ground as shown in Figure 67. The crystal allows the PLL to lock correctly to give a frequency of 41.78 MHz. If no external crystal is present, the internal oscillator is used to give a typical frequency of 32.768 kHz ± 3%.

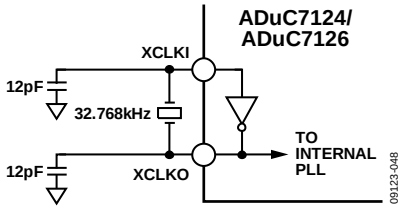

Figure 67. External Parallel Resonant Crystal Connections

To use an external source clock input instead of the PLL (see Figure 68), Bit 1 and Bit 0 of PLLCON must be modified. The external clock uses P0.7 and XCLK.

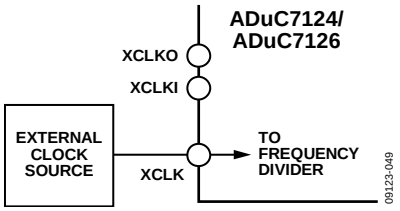

Figure 68. Connecting an External Clock Source

Using an external clock source, the ADuC7124/ADuC7126 specified operational clock speed range is 50 kHz to 41.78 MHz ± 1%, which ensures correct operation of the analog peripherals and Flash/EE.

ORDERING GUIDE

Model[1]	ADC Channels	DAC Channels	Flash/RAM	GPIO	Downloader	Temperature Range	Package Description	Package Option	Ordering Quantity
ADuC7124BCPZ126	10	2	126 kB/32 kB	30	UART	−40°C to +125°C	64-Lead LFCSP_VQ	CP-64-1	260
ADuC7124BCPZ126-RL	10	2	126 kB/32 kB	30	UART	−40°C to +125°C	64-Lead LFCSP_VQ	CP-64-1	2500
ADuC7126BSTZ126	12	4	126 kB/32 kB	40	UART	−40°C to +125°C	80-Lead LQFP	ST-80-1	119
ADuC7126BSTZ126-RL	12	4	126 kB/32 kB	40	UART	−40°C to +125°C	80-Lead LQFP	ST-80-1	1000
ADuC7126BSTZ126I	12	4	126 kB/32 kB	40	I^2C	−40°C to +125°C	80-Lead LQFP	ST-80-1	119
ADuC7126BSTZ126IRL	12	4	126 kB/32 kB	40	I^2C	−40°C to +125°C	80-Lead LQFP	ST-80-1	1000
EVAL-ADuC7124QSPZ							ADuC7124 QuickStart Development System		
EVAL-ADuC7126QSPZ							ADuC7126 QuickStart Development System		

[1] Z = RoHS Compliant Part.

NOTES