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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	41.78MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	40
Program Memory Size	126KB (63K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 32
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 12x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc7126bstz126i

REVISION HISTORY

10/14—Rev. C to Rev. D

Change $\overline{CONV}_{START}$ To $CONV_{START}$ ..... Universal
Changes to Features Section 1
Changes to Pin 17 and Pin 30 Descriptions; Table 10 19
Changes to Flash/EE Memory Section and SRAM Section 30
Changes to Table 13 32
Changes to Flash/EE Memory Section, Programming Section, and Serial Downloading (In-Circuit Programming) Section 46
Changes to Flash/EE Memory Security Section 47
Changes to Table 56 and Table 57 50
Changes to Table 69 56
Changes to Table 78 60
Changes to I^2C Section 72
Update Table 102 73
Update Table 109 76
Changes to Table 110 77
Changes to T1CAP Register 96

5/12—Rev. B to Rev. C

Changed bit to byte in General Description Section 4
Changes to Table 2 and Table 3 8
Changes to Table 4 and to Figure 2 and Figure 3 9
Changes to Table 5 and Figure 4 10
Changes to Table 6 and Figure 5 11
Changes Table 7 and Figure 6 12
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Changes to Serial Peripheral Interface Section 66
Added equation to Timers Section and added Hr: Min: Sec 1/128 Format Section 91
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1/11—Rev A to Rev B

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10/10—Rev. 0 to Rev. A

Added ADuC7126 ..... Universal
Changes to Features Section 1
Moved Figure 1 1
Changes to Figure 1 1
Changes to General Description Section 4
Changes to Voltage Output at 25°C, Voltage TC, IOV_{DD} Current in Active Mode, and IOV_{DD} Current in Pause Mode Parameters, Table 1 5
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Changes to Table 141, T1CLRI Register Section, and T1CAP Register Section 93
Changes to Table 143 94
Added External Memory Interfacting Section, Table 145, Table 146, and Figure 57 96

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUTS[3]					All logic inputs excluding XCLKI
V_{INL}, Input Low Voltage			0.8	V	
V_{INH}, Input High Voltage	2.0			V	
LOGIC OUTPUTS					All digital outputs excluding XCLKO
V_{OH}, Output High Voltage	2.4			V	I_{SOURCE} = 1.6 mA
V_{OL}, Output Low Voltage[11]			0.4	V	I_{SINK} = 1.6 mA
CRYSTAL INPUTS XCLKI and XCLKO					
Logic Inputs, XCLKI Only					
V_{INL}, Input Low Voltage		0.8		V	
V_{INH}, Input High Voltage		1.6		V	
XCLKI Input Capacitance		20		pF	
XCLKO Output Capacitance		20		pF	
INTERNAL OSCILLATOR		32.768		kHz	
			±3	%	
MCU CLOCK RATE[4]					
From 32 kHz Internal Oscillator		326		kHz	CD = 7
From 32 kHz External Crystal		41.78		MHz	CD = 0
Using an External Clock	0.05		44	MHz	T_A = 85°C
	0.05		41.78	MHz	T_A = 125°C
START-UP TIME					Core clock = 41.78 MHz
At Power-On		66		ms	
From Pause/Nap Mode		2.6		µs	CD = 0
		247		µs	CD = 7
From Sleep Mode		1.58		ms	
From Stop Mode		1.7		ms	
PROGRAMMABLE LOGIC ARRAY (PLA)					
Pin Propagation Delay		12		ns	From input pin to output pin
Element Propagation Delay		2.5		ns	
POWER REQUIREMENTS[12, 13]					
Power Supply Voltage Range					
AV_{DD} to AGND and IOV_{DD} to IOGND	2.7		3.6	V	
Analog Power Supply Currents					
AV_{DD} Current		165		µA	ADC in idle mode
$DACV_{DD}$ Current[14]		0.02		µA	
Digital Power Supply Current					
IOV_{DD} Current in Active Mode					Code executing from Flash/EE
		8.1	12.5	mA	CD = 7
		11.6	17	mA	CD = 3
		33.3	50	mA	CD = 0 (41.78 MHz clock)
IOV_{DD} Current in Pause Mode		20.6	30	mA	CD = 0 (41.78 MHz clock)
IOV_{DD} Current in Sleep Mode		110		µA	T_A = 85°C
		600	680	µA	T_A = 125°C
Additional Power Supply Currents					
ADC		1.26		mA	At 1 MSPS
		0.7		mA	At 62.5 kSPS
DAC		315		µA	Per DAC

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ESD TESTS					2.5 V reference, T_A = 25°C
HBM Passed Up To			3	kV	
FICDM Passed Up To			1.5	kV	

[1] All ADC channel specifications are guaranteed during normal core operation.
[2] Apply to all ADC input channels.
[3] Measured using the factory-set default values in the ADC offset register (ADCOF) and gain coefficient register (ADCGN).
[4] Not production tested but supported by design and/or characterization data on production release.
[5] Measured using the factory-set default values in ADCOF and ADCGN with an external AD845 op amp as an input buffer stage as shown in Figure 37. Based on external ADC system components, the user may need to execute a system calibration to remove external endpoint errors and achieve these specifications (see the Calibration section).
[6] The input signal can be centered on any dc common-mode voltage (V_{CM}) as long as this value is within the ADC voltage input range specified.
[7] DAC linearity is calculated using a reduced code range of 100 to 3995.
[8] DAC gain error is calculated using a reduced code range of 100 to internal 2.5 V V_{REF}.
[9] Endurance is qualified as per JEDEC Standard 22 Method A117 and measured at −40°C, +25°C, +85°C, and +125°C.
[10] Retention lifetime equivalent at junction temperature (T_J) = 85°C as per JEDEC Standard 22 Method A117. Retention lifetime derates with junction temperature.
[11] Test carried out with a maximum of eight I/Os set to a low output level.
[12] Power supply current consumption is measured in normal, pause, and sleep modes under the following conditions: normal mode with 3.6 V supply, pause mode with 3.6 V supply, and sleep mode with 3.6 V supply.
[13] IOV_{DD} power supply current increases typically by 2 mA during a Flash/EE erase cycle.
[14] This current must be added to the AV_{DD} current.

TIMING SPECIFICATIONS

I²C Timing

Table 2. I²C Timing in Fast Mode (400 kHz)

		Slave		Master	
Parameter	Description	Min	Max	Typ	Unit
t_L	SCL low pulse width	200		1360	ns
t_H	SCL high pulse width	100		1140	ns
t_{SHD}	Start condition hold time	300			ns
t_{DSU}	Data setup time	100		740	ns
t_{DHD}	Data hold time	0		400	ns
t_{RSU}	Setup time for repeated start	100			ns
t_{PSU}	Stop condition setup time	100		800	ns
t_{BUF}	Bus-free time between a stop condition and a start condition	1.3			µs
t_R	Rise time for both SCL and SDA		300	200	ns
t_F	Fall time for both SCL and SDA		300		ns

Table 3. I²C Timing in Standard Mode (100 kHz)

		Slave		
Parameter	Description	Min	Max	Unit
t_L	SCL low pulse width	4.7		µs
t_H	SCL high pulse width	4.0		ns
t_{SHD}	Start condition hold time	4.0		µs
t_{DSU}	Data setup time	250		ns
t_{DHD}	Data hold time	0	3.45	µs
t_{RSU}	Setup time for repeated start	4.7		µs
t_{PSU}	Stop condition setup time	4.0		µs
t_{BUF}	Bus-free time between a stop condition and a start condition	4.7		µs
t_R	Rise time for both SCL and SDA		1	µs
t_F	Fall time for both SCL and SDA		300	ns

OVERVIEW OF THE ARM7TDMI CORE

The ARM7® core is a 32-bit reduced instruction set computer (RISC). It uses a single 32-bit bus for instruction and data. The length of the data can be eight bits, 16 bits, or 32 bits. The length of the instruction word is 32 bits.

The ARM7TDMI is an ARM7 core with four additional features.

- T support for the Thumb® (16-bit) instruction set.
- D support for debug.
- M support for long multiplications.
- I includes the EmbeddedICE module to support embedded system debugging.

THUMB MODE (T)

An ARM instruction is 32 bits long. The ARM7TDMI processor supports a second instruction set that has been compressed into 16 bits, called the Thumb instruction set. Faster execution from 16-bit memory and greater code density can usually be achieved by using the Thumb instruction set instead of the ARM instruction set, which makes the ARM7TDMI core particularly suitable for embedded applications.

However, the Thumb mode has two limitations:

- Thumb code typically requires more instructions for the same job. As a result, ARM code is usually best for maximizing the performance of time-critical code.
- The Thumb instruction set does not include some of the instructions needed for exception handling, which automatically switches the core to ARM code for exception handling.

See the ARM7TDMI user guide for details on the core architecture, the programming model, and both the ARM and ARM Thumb instruction sets.

LONG MULTIPLY (M)

The ARM7TDMI instruction set includes four extra instructions that perform 32-bit by 32-bit multiplication with a 64-bit result and 32-bit by 32-bit multiplication-accumulation (MAC) with a 64-bit result. These results are achieved in fewer cycles than required on a standard ARM7 core.

EmbeddedICE (I)

EmbeddedICE provides integrated on-chip support for the core. The EmbeddedICE module contains the breakpoint and watchpoint registers that allow code to be halted for debugging purposes. These registers are controlled through the JTAG test port.

When a breakpoint or watchpoint is encountered, the processor halts and enters debug state. Once in a debug state, the processor registers can be inspected as well as the Flash/EE, SRAM, and memory mapped registers.

EXCEPTIONS

ARM supports five types of exceptions and a privileged processing mode for each type. The five types of exceptions are

- Normal interrupt or IRQ. This is provided to service general-purpose interrupt handling of internal and external events.
- Fast interrupt or FIQ. This is provided to service data transfers or communication channels with low latency. FIQ has priority over IRQ.
- Memory abort.
- Attempted execution of an undefined instruction.
- Software interrupt instruction (SWI). This can be used to make a call to an operating system.

Typically, the programmer defines an interrupt as IRQ, but for higher priority interrupt, that is, faster response time, the programmer can define an interrupt as FIQ.

ARM REGISTERS

ARM7TDMI has a total of 37 registers: 31 general-purpose registers and six status registers. Each operating mode has dedicated banked registers.

When writing user-level programs, 15 general-purpose, 32-bit registers (R0 to R14), the program counter (R15), and the current program status register (CPSR) are usable. The remaining registers are only used for system-level programming and exception handling.

When an exception occurs, some of the standard registers are replaced with registers specific to the exception mode. All exception modes have replacement banked registers for the stack pointer (R13) and the link register (R14), as represented in Figure 23. The fast interrupt mode has more registers (R8 to R12) for fast interrupt processing. This means that the interrupt processing can begin without the need to save or restore these registers, and therefore, save critical time in the interrupt handling process.

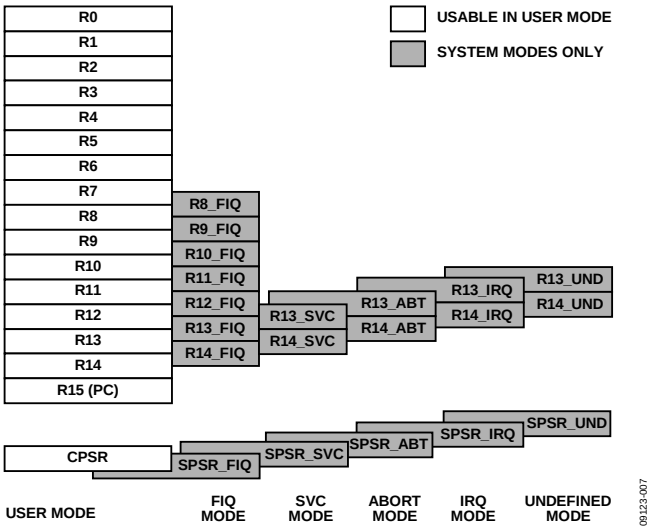

Figure 23. Register Organization

ADC CIRCUIT OVERVIEW

The analog-to-digital converter is a fast, multichannel, 12-bit ADC. It can operate from 2.7 V to 3.6 V supplies and is capable of providing a throughput of up to 1 MSPS when the clock source is 41.78 MHz. This block provides the user with a multichannel multiplexer, a differential track-and-hold, an on-chip reference, and an ADC.

The ADC consists of a 12-bit successive approximation converter based around two capacitor DACs. Depending on the input signal configuration, the ADC can operate in one of three different modes.

- Fully differential mode, for small and balanced signals
- Single-ended mode, for any single-ended signals
- Pseudo differential mode, for any single-ended signals, taking advantage of the common-mode rejection offered by the pseudo differential input

The converter accepts an analog input range of 0 V to V_{REF} when operating in single-ended or pseudo differential mode. In fully differential mode, the input signal must be balanced around a common-mode voltage (V_{CM}) in the 0 V to AV_{DD} range with a maximum amplitude of 2 × V_{REF} (see Figure 27).

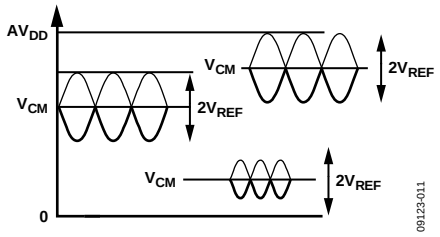

Figure 27. Examples of Balanced Signals in Fully Differential Mode

A high precision, low drift, factory calibrated, 2.5 V reference is provided on chip. An external reference can also be connected as described in the Band Gap Reference section.

Single or continuous conversion modes can be initiated in the software. An external $CONV_{START}$ pin, an output generated from the on-chip PLA, or a Timer0 or Timer1 overflow can also be used to generate a repetitive trigger for ADC conversions.

A voltage output from an on-chip band gap reference proportional to absolute temperature can also be routed through the front-end ADC multiplexer, effectively an additional ADC channel input. This facilitates an internal temperature sensor channel that measures die temperature.

TRANSFER FUNCTION

Pseudo Differential and Single-Ended Modes

In pseudo differential or single-ended mode, the input range is 0 V to V_{REF}. The output coding is straight binary in pseudo differential and single-ended modes with

1 LSB = *Full-Scale*/4096, or
2.5 V/4096 = 0.61 mV, or
610 μV when V_{REF} = 2.5 V

The ideal code transitions occur midway between successive integer LSB values (that is, ½ LSB, 3⁄2 LSB, 5⁄2 LSB, … , FS – 3/2 LSB). The ideal input/output transfer characteristic is shown in Figure 28.

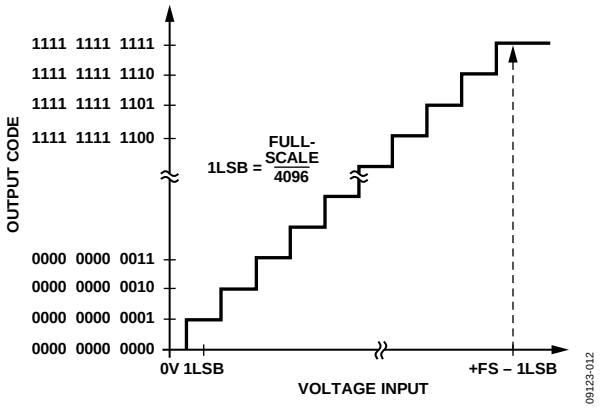

Figure 28. ADC Transfer Function in Pseudo Differential or Single-Ended Mode

Fully Differential Mode

The amplitude of the differential signal is the difference between the signals applied to the V_{IN+} and V_{IN-} pins (that is, $V_{IN+} - V_{IN-}$). V_{IN+} is selected by the ADCCP register, and V_{IN-} is selected by the ADCCN register. The maximum amplitude of the differential signal is, therefore, $-V_{REF}$ to $+V_{REF}$ p-p (that is, 2 × V_{REF}). This is regardless of the common mode (CM). The common mode is the average of the two signals, for example, (V_{IN+} + V_{IN-})/2, and is, therefore, the voltage that the two inputs are centered on. This results in the span of each input being CM ± V_{REF}/2. This voltage must be set up externally, and its range varies with V_{REF} (see the Driving the Analog Inputs section).

The output coding is twos complement in fully differential mode with 1 LSB = 2 × V_{REF}/4096, or 2 × 2.5 V/4096 = 1.22 mV when V_{REF} = 2.5 V. The output result is ±11 bits, but this is shifted by one to the right. This allows the result in ADCDAT to be declared as a signed integer when writing C code. The designed code transitions occur midway between successive integer LSB values (that is, ½ LSB, 3⁄2 LSB, 5⁄2 LSB, … , FS – 3⁄2 LSB). The ideal input/output transfer characteristic is shown in Figure 29.

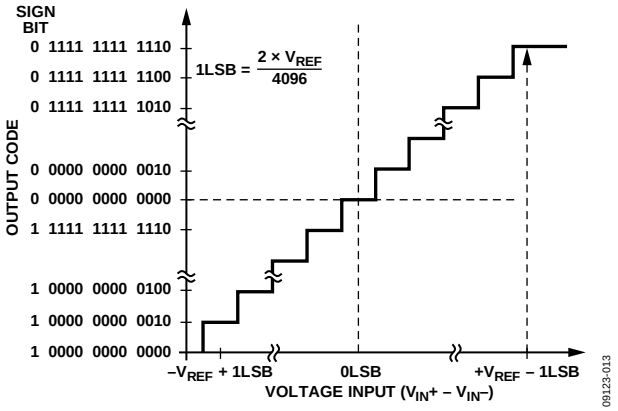

Figure 29. ADC Transfer Function in Differential Mode

NONVOLATILE FLASH/EE MEMORY

The ADuC7124/ADuC7126 incorporate Flash/EE memory technology on-chip to provide the user with nonvolatile, in-circuit reprogrammable memory space.

Like EEPROM, flash memory can be programmed in-system at a byte level, although it must first be erased. The erase is performed in page blocks. As a result, flash memory is often and more correctly referred to as Flash/EE memory.

Overall, Flash/EE memory represents a step closer to the ideal memory device that includes nonvolatility, in-circuit programmability, high density, and low cost. Incorporated in the ADuC7124/ADuC7126, Flash/EE memory technology allows the user to update program code space in-circuit, without the need to replace one-time programmable (OTP) devices at remote operating nodes.

Flash/EE Memory

The ADuC7124/ADuC7126 contain two 64 kB arrays of Flash/EE memory. In flash Block 0, the lower 62 kB is available to the user, and the upper 2 kB of this Flash/EE program memory array contain permanently embedded firmware, allowing in-circuit serial download. The 2 kB of embedded firmware also contain a power-on configuration routine that downloads factory calibrated coefficients to the various calibrated peripherals (band gap references and so on). This 2 kB embedded firmware is hidden from user code. It is not possible for the user to read, write, or erase this page. In flash Block 1, all 64 kB of Flash/EE memory are available to the user.

The 126 kB of Flash/EE memory can be programmed in-circuit, using the serial download mode or the JTAG mode provided.

Flash/EE Memory Reliability

The Flash/EE memory arrays on the parts are fully qualified for two key Flash/EE memory characteristics: Flash/EE memory cycling endurance and Flash/EE memory data retention.

Endurance quantifies the ability of the Flash/EE memory to be cycled through many program, read, and erase cycles. A single endurance cycle is composed of four independent, sequential events, defined as

1. Initial page erase sequence.
2. Read/verify sequence (single Flash/EE).
3. Byte program sequence memory.
4. Second read/verify sequence (endurance cycle).

In reliability qualification, every half word (16-bit wide) location of the three pages (top, middle, and bottom) in the Flash/EE memory is cycled 10,000 times from 0x0000 to 0xFFFF. As indicated in Table 1, the Flash/EE memory endurance qualification is carried out in accordance with JEDEC Retention Lifetime Specification A117 over the industrial temperature range of −40° to +125°C. The results allow the specification of a minimum endurance figure over a supply temperature of 10,000 cycles.

Retention quantifies the ability of the Flash/EE memory to retain its programmed data over time. Again, the parts are qualified in accordance with the formal JEDEC Retention Lifetime Specification (A117) at a specific junction temperature (T_J = 85°C). As part of this qualification procedure, the Flash/EE memory is cycled to its specified endurance limit (see the Flash/EE Memory section) before data retention is characterized. This means that the Flash/EE memory is guaranteed to retain its data for its fully specified retention lifetime every time the Flash/EE memory is reprogrammed. In addition, note that retention lifetime, based on the activation energy of 0.6 eV, derates with T_J as shown in Figure 39.

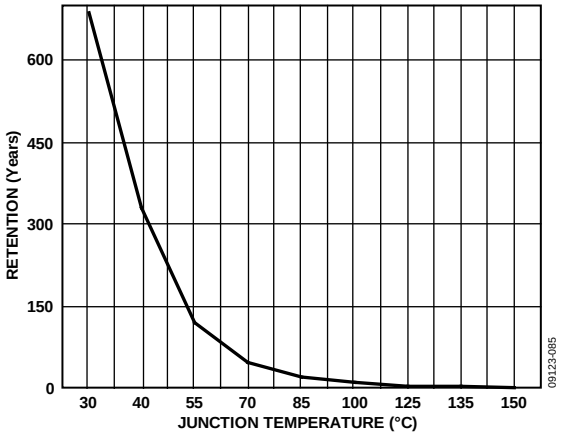

Figure 39. Flash/EE Memory Data Retention

PROGRAMMING

The 126 kB of Flash/EE memory can be programmed in-circuit, using the serial download mode or the provided JTAG mode.

Serial Downloading (In-Circuit Programming)

The ADuC7124/ADuC7126 facilitate code download via the standard UART serial port. It is only available on UART0 (P1.0 and P1.1). The parts enter serial download mode after a reset or power cycle if the BM pin is pulled low through an external 1 kΩ resistor. When in serial download mode, the user can download code to the full 126 kB of Flash/EE memory while the device is in-circuit in its target application hardware. An executable PC serial download is provided as part of the development system for serial downloading via the UART. The AN-724 application note describes the UART download protocol.

Downloading (In-Circuit Programming) via I²C

The ADuC7126BSTZ126I and ADuC7126BSTZ126IRL models facilitate code download via the the I²C port. The models enter download mode after a reset or power cycle if the BM pin is pulled low through an external 1 kΩ resistor and Flash Address 0x80014 = 0xFFFFFFFF. Once in download mode, the user can download code to the full 126 kB of Flash/EE memory while the device is in-circuit in its target application hardware. An executable PC I²C download is provided as part of the development system

Table 45. FEE1STA Register

Name	Address	Default Value	Access
FEE1STA	0xFFFFF880	0x0000	R

Table 46. FEE1MOD Register

Name	Address	Default Value	Access
FEE1MOD	0xFFFFF884	0x80	R/W

Table 47. FEE1CON Register

Name	Address	Default Value	Access
FEE1CON	0xFFFFF888	0x00	R/W

Table 48. FEE1DAT Register

Name	Address	Default Value	Access
FEE1DAT	0xFFFFF88C	0xXXXX	R/W

FEE1DAT is a 16-bit data register.

Table 49. FEE1ADR Register

Name	Address	Default Value	Access
FEE1ADR	0xFFFFF890	0x0000	R/W

FEE1ADR is a 16-bit address register.

Table 50. FEE1SGN Register

Name	Address	Default Value	Access
FEE1SGN	0xFFFFF898	0xFFFFFF	R

FEE1SGN is a 24-bit code signature.

Table 51. FEE1PRO Register

Name	Address	Default Value	Access
FEE1PRO	0xFFFFF89C	0x00000000	R/W

FEE1PRO provides protection following subsequent reset MMR. It requires a software key (see Table 57).

Table 52. FEE1HID Register

Name	Address	Default Value	Access
FEE1HID	0xFFFFF8A0	0xFFFFFFFF	R/W

FEE1HID provides immediate protection MMR. It does not require any software keys (see Table 57).

Command Sequence for Executing a Mass Erase

```
FEE0DAT = 0x3CFF;
FEE0ADR = 0xFFC3;
FEE0MOD = FEE0MOD|0x8; //Erase key enable
FEE0CON = 0x06;            //Mass erase
command
```

Table 53. FEExSTA MMR Bit Descriptions

Bit	Description
[15:6]	Reserved.
5	Reserved.
4	Reserved.
3	Flash/EE interrupt status bit. Set automatically when an interrupt occurs, that is, when a command is complete and the Flash/EE interrupt enable bit in the FEExMOD register is set. Cleared when reading the FEExSTA register.
2	Flash/EE controller busy. Set automatically when the controller is busy. Cleared automatically when the controller is not busy.
1	Command fail. Set automatically when a command completes unsuccessfully. Cleared automatically when reading the FEExSTA register.
0	Command complete. Set by MicroConverter when a command is complete. Cleared automatically when reading the FEExSTA register.

Table 77. POWCON1 MMR Bit Descriptions[1]

Bit	Value	Name	Description
[15:12]			Reserved.
11	1	PWMPO	Clearing this bit powers down the PWM. Always clear to 00.
[10:9]	00	PWMCLKDIV	
8		SPIPO	Clearing this bit powers down the SPI.
[7:6]		SPICLKDIV	SPI block driving clock divider bits.
	00		41.78 MHz.
	01		20.89 MHz.
	10		10.44 MHz.
	11		5.22 MHz.
5		I2C1PO	Clearing this bit powers down I2C1.
[4:3]		I2C1CLKDIV	I2C0 block driving clock divider bits.
	00		41.78 MHz.
	01		10.44 MHz.
	10		5.22 MHz.
	11		1.31 MHz.
2		I2C0PO	Clearing this bit powers down I2C0.
[1:0]		I2C0CLKDIV	I2C1 block driving clock divider bits.
	00		41.78 MHz.
	01		10.44 MHz.
	10		5.22 MHz.
	11		1.31 MHz.

[1] Divided clock for SPI/I2C0/I2C1 must be greater than or equal to the CPU clock as selected by POWCON0 [2:0].

The POWCON1 write sequence is as follows:

1. Write Code 0x76 to Register POWKEY3.
2. Write user value to Register POWCON1.
3. Write Code 0xB1 to Register POWKEY4.

Table 93. COMxIID0 MMR Bit Descriptions

Bit	Name	Description
[7:6]	FIFOMODE	FIFO mode flag. 0x0: non-FIFO mode. 0x1: reserved. 0x2: reserved. 0x3: FIFO mode. Set automatically if FIFOEN is set.
[5:4]	Reserved	
[3:1]	STATUS[2:0]	Interrupt status bits that work only when NINT is set. [000]: modem status interrupt. Cleared by reading COMxSTA1. Priority 4. [001]: for non-FIFO mode, transmit buffer empty interrupt. For FIFO mode, Tx FIFO is empty. Cleared by writing COMxTX or reading COMxIID0. Priority 3. [010]: non-FIFO mode. Receive buffer data ready interrupt. Cleared automatically by reading COMxRX. For FIFO mode, set trigger level reached. Cleared automatically when FIFO drops below the trigger level. Priority 2. [011]: receive line status error interrupt. Cleared by reading COMxSTA0. Priority 1. [110]: Rx FIFO timeout interrupt (FIFO mode only). Set automatically if there is at least one byte in the Rx FIFO, and there is no access to the Rx FIFO in the next four-frames accessing cycle. Cleared by reading COMxRX, setting RXRST, or when a new byte arrives in the Rx FIFO[1]. Priority 2. [Other state]: reserved.
0	NINT	Set to disable interrupt flags by STATUS[2:0]. Clear to enable interrupt.

[1] A frame time is the time allotted for one start bit, n data bits, one parity bit, and one stop bit. Here, n is the word length selected with the WLS bits in COMxCON0.
WLS[1:0] = 00: timeout threshold = time for 32 bits = (1 + 5 + 1 + 1) × 4.
WLS[1:0] = 01: timeout threshold = time for 36 bits = (1 + 6 + 1 + 1) × 4.
WLS[1:0] = 10: timeout threshold = time for 40 bits = (1 + 7 + 1 + 1) × 4.
WLS[1:0] = 11: timeout threshold = time for 44 bits = (1 + 8 + 1 + 1) × 4.

COM0FCR Register

Name: COM0FCR

Address: 0xFFFF0708

Default Value: 0x00

Access: Read/write

The FIFO control register (FCR) is a write-only register at the same address as the interrupt identification register (IIR), which is a read-only register.

COM1FCR Register

Name: COM1FCR

Address: 0xFFFF0748

Default Value: 0x00

Access: Read/write

The FIFO control register (FCR) is a write-only register at the same address as the interrupt identification register (IIR), which is a read-only register.

Table 94. COMxFCR MMR Bit Descriptions

Bit	Name	Description
[7:5]	RXFIFOTL	Receiver FIFO trigger level. RXFIFOTL sets the trigger level for the receiver FIFO. When the trigger level is reached, a receiver data-ready interrupt is generated (if the interrupt request is enabled). When the FIFO drops below the trigger level, the interrupt is cleared. 0x0: one byte. 0x1: two bytes. 0x2: four bytes. 0x3: six bytes. 0x4: eight bytes. 0x5: 10 bytes. 0x6: 12 bytes. 0x7: 14 bytes.
[4:3]	Reserved	
2	TXRST	Tx FIFO reset. Writing a 1 flushes the Tx FIFO. Does not affect shift register. Note that TXRST should be cleared manually to make Tx FIFO work after flushing.
1	RXRST	Rx FIFO reset. Writing a 1 flushes the Rx FIFO. Does not affect shift register. Note that RXRST should be cleared manually to make the Rx FIFO work after flushing.
0	FIFOEN	Transmitter and receiver FIFOs mode enable. FIFOEN must be set before other FCR bits are written to. Set for FIFO mode. The transmitter and receiver FIFOs are enabled. Cleared for non-FIFO mode; the transmitter and receiver FIFOs are disabled, and the FIFO pointers are cleared.

COM0CON0 Register

Name: COM0CON0

Address: 0xFFFF070C

Default Value: 0x00

Access: Read/write

COM0CON0 is the line control register for UART0.

COM1CON0 Register

Name: COM1CON0

Address: 0xFFFF074C

Default Value: 0x00

Access: Read/write

COM1CON0 is the line control register for UART1.

Table 95. COMxCON0 MMR Bit Descriptions

Bit	Name	Description
7	DLAB	Divisor latch access. Set by the user to enable access to the COMxDIV0 and COMxDIV1 registers. Cleared by the user to disable access to COMxDIV0 and COMxDIV1 and enable access to COMxRX and COMxTX.
6	BRK	Set break. Set by the user to force SOUTx to 0. Cleared to operate in normal mode.
5	SP	Stick parity. Set by the user to force parity to defined values: 1 if EPS = 1 and PEN = 1, 0 if EPS = 0 and PEN = 1.
4	EPS	Even parity select bit. Set for even parity. Cleared for odd parity.
3	PEN	Parity enable bit. Set by the user to transmit and check the parity bit. Cleared by the user for no parity transmission or checking.
2	Stop	Stop bit. Set by the user to transmit 1½ stop bits if the word length is five bits or two stop bits if the word length is six bits, seven bits, or eight bits. The receiver checks the first stop bit only, regardless of the number of stop bits selected. Cleared by the user to generate one stop bit in the transmitted data.
[1:0]	WLS	Word length select: 00 = five bits, 01 = six bits, 10 = seven bits, 11 = eight bits.

COM0CON1 Register

Name: COM0CON1

Address: 0xFFFF0710

Default Value: 0x00

Access: Read/write

COM0CON1 is the modem control register for UART0.

COM1CON1 Register

Name: COM1CON1

Address: 0xFFFF0750

Default Value: 0x00

Access: Read/write

COM1CON1 is the modem control register for UART1.

Table 96. COMxCON1 MMR Bit Descriptions

Bit	Name	Description
[7:5]		Reserved.
4	LOOPBACK	Loop back. Set by the user to enable loopback mode. In loopback mode, SOUTx is forced high. The modem signals are also directly connected to the status inputs (RTS to CTS and DTR to DSR). Cleared by the user to be in normal mode.
3	PEN	Parity enable bit. Set by the user to transmit and check the parity bit. Cleared by the user for no parity transmission or checking.
2	Stop	Stop bit. Set by the user to transmit 1½ stop bits if the word length is five bits or two stop bits if the word length is six bits, seven bits, or eight bits. The receiver checks the first stop bit only, regardless of the number of stop bits selected. Cleared by the user to generate one stop bit in the transmitted data.
1	RTS	Request to send. Set by the user to force the RTS output to 0. Cleared by the user to force the RTS output to 1.
0	DTR	Data terminal ready. Set by the user to force the DTR output to 0. Cleared by the user to force the DTR output to 1.

COM0STA0 Register

Name: COM0STA0

Address: 0xFFFF0714

Default Value: 0xE0

Access: Read only

COM0STA0 is the line status register for UART0.

SPI Registers

The following MMR registers control the SPI interface: SPISTA, SPIRX, SPITX, SPIDIV, and SPICON.

SPI Status Register

Name: SPISTA

Address: 0xFFFF0A00

Default Value: 0x0000

Access: Read only

Function: This 32-bit MMR contains the status of the SPI interface in both master and slave modes.

Table 100. SPISTA MMR Bit Descriptions

Bit	Name	Description
[15:12]		Reserved.
11	SPIREX	SPI Rx FIFO excess bytes present. This bit is set when there are more bytes in the Rx FIFO than indicated in the SPIMDE bits in SPICON This bit is cleared when the number of bytes in the FIFO is equal to or less than the number in SPIMDE.
[10:8]	SPIRXFSTA[2:0]	SPI Rx FIFO status bits. [000] = Rx FIFO is empty. [001] = one valid byte in the FIFO. [010] = two valid bytes in the FIFO. [011] = three valid bytes in the FIFO. [100] = four valid bytes in the FIFO.
7	SPIFOF	SPI Rx FIFO overflow status bit. Set when the Rx FIFO was already full when new data was loaded to the FIFO. This bit generates an interrupt except when SPIRFLH is set in SPICON. Cleared when the SPISTA register is read.
6	SPIRXIRQ	SPI Rx IRQ status bit. Set when a receive interrupt occurs. This bit is set when SPITMDE in SPICON is cleared and the required number of bytes has been received. Cleared when the SPISTA register is read.
5	SPITXIRQ	SPI Tx IRQ status bit. Set when a transmit interrupt occurs. This bit is set when SPITMDE in SPICON is set and the required number of bytes has been transmitted. Cleared when the SPISTA register is read.
4	SPITXUF	SPI Tx FIFO underflow. This bit is set when a transmit is initiated without any valid data in the Tx FIFO. This bit generates an interrupt except when SPITFLH is set in SPICON. Cleared when the SPISTA register is read.
[3:1]	SPITXFSTA[2:0]	SPI Tx FIFO status bits. [000] = Tx FIFO is empty. [001] = one valid byte in the FIFO. [010] = two valid bytes in the FIFO. [011] = three valid bytes in the FIFO. [100] = four valid bytes in the FIFO.
0	SPIISTA	SPI interrupt status bit. Set to 1 when an SPI-based interrupt occurs. Cleared after reading SPISTA.

Bit	Name	Description
9	SPIOEN	Slave MISO output enable bit. Set this bit for MISO to operate as normal. Clear this bit to disable the output driver on the MISO pin. The MISO pin is open-drain when this bit is cleared.
8	SPIROW	SPIRX overflow overwrite enable. Set by the user, the valid data in the SPIRX register is overwritten by the new serial byte received. Cleared by the user, the new serial byte received is discarded.
7	SPIZEN	SPI transmits zeros when Tx FIFO is empty. Set this bit to transmit 0x00 when there is no valid data in the Tx FIFO. Clear this bit to transmit the last transmitted value when there is no valid data in the Tx FIFO.
6	SPITMDE	SPI transfer and interrupt mode. Set by the user to initiate transfer with a write to the SPITX register. Interrupt occurs only when SPITX is empty. Cleared by the user to initiate transfer with a read of the SPIRX register. Interrupt occurs only when SPIRX is full.
5	SPILF	LSB first transfer enable bit. Set by the user, the LSB is transmitted first. Cleared by the user, the MSB is transmitted first.
4	SPIWOM	SPI wire-OR'ed mode enable bit. Set to 1 enable open-drain data output. External pull-ups required on data output pins. Cleared for normal output levels.
3	SPICPO	Serial clock polarity mode bit. Set by the user, the serial clock idles high. Cleared by the user, the serial clock idles low.
2	SPICPH	Serial clock phase mode bit. Set by the user, the serial clock pulses at the beginning of each serial bit transfer. Cleared by the user, the serial clock pulses at the end of each serial bit transfer.
1	SPIMEN	Master mode enable bit. Set by the user to enable master mode. Cleared by the user to enable slave mode.
0	SPIEN	SPI enable bit. Set by the user to enable the SPI. Cleared by the user to disable the SPI.

I²C Master Receive Register

Name: I2C0MRX, I2C1MRX

Address: 0xFFFF0808, 0xFFFF0908

Default Value: 0x00

Access: Read only

Function: This 8-bit MMR is the I²C master receive register.

I²C Master Transmit Register

Name: I2C0MTX, I2C1MTX

Address: 0xFFFF080C 0xFFFF090C

Default Value: 0x00, 0x00

Access: Read/write

Function: This 8-bit MMR is the I²C master transmit register.

I²C Master Read Count Register

Name: I2C0MCNT0, I2C1MCNT0

Address: 0xFFFF0810, 0xFFFF0910

Default Value: 0x0000, 0x0000

Access: Read/write

Function: This 16-bit MMR holds the required number of bytes when the master begins a read sequence from a slave device.

Table 104. I2CxMCNT0 MMR Bit Descriptions

Bit	Name	Description
[15:9]		Reserved.
8	I2CRECNT	Set this bit if more than 256 bytes are required from the slave. Clear this bit when reading 256 bytes or less.
[7:0]	I2CRCNT	These eight bits hold the number of bytes required during a slave read sequence, minus 1. If only a single byte is required, these bits should be set to 0.

I²C Master Current Read Count Register

Name: I2C0MCNT1, I2C1MCNT1

Address: 0xFFFF0814, 0xFFFF0914

Default Value: 0x00, 0x00

Access: Read only

Function: This 8-bit MMR holds the number of bytes received so far during a read sequence with a slave device.

I²C Address 0 Register

Name: I2C0ADR0, I2C1ADR0

Address: 0xFFFF0818, 0xFFFF0918

Default Value: 0x00

Access: Read/write

Function: This 8-bit MMR holds the 7-bit slave address + the read/write bit when the master begins communicating with a slave.

Table 105. I2CxADR0 MMR in 7-Bit Address Mode

Bit	Name	Description
[7:1]	I2CADR	These bits contain the 7-bit address of the required slave device.
0	R/W	Bit 0 is the read/write bit. When this bit = 1, a read sequence is requested. When this bit = 0, a write sequence is requested.

Table 106. I2CxADR0 MMR in 10-Bit Address Mode

Bit	Name	Description
[7:3]		These bits must be set to [11110b] in 10-bit address mode.
[2:1]	I2CMADR	These bits contain ADDR[9:8] in 10-bit addressing mode.
0	R/W	Read/write bit. When this bit = 1, a read sequence is requested. When this bit = 0, a write sequence is requested.

Table 113. PWMCON0 MMR Bit Descriptions

Bit	Name	Description
14	SYNC	Enables PWM synchronization. Set to 1 by the user so that all PWM counters are reset on the next clock edge after the detection of a high-to-low transition on the P3.7/PWM_{SYNC} pin. Cleared by the user to ignore transitions on the P3.7/PWM_{SYNC} pin.
13	PWM5INV	Set to 1 by the user to invert PWM5. Cleared by the user to use PWM5 in normal mode.
12	PWM3INV	Set to 1 by the user to invert PWM3. Cleared by the user to use PWM3 in normal mode.
11	PWM1INV	Set to 1 by the user to invert PWM1. Cleared by the user to use PWM1 in normal mode.
10	PWMTRIP	Set to 1 by the user to enable PWM trip interrupt. When the PWM trip input (Pin P3.6/PWM_{TRIP} or Pin P0.4/PWM_{TRIP}) is low, the PWMEN bit is cleared and an interrupt is generated. Cleared by the user to disable the PWMTRIP interrupt.
9	ENA	If HOFF = 0 and HMODE = 1; note that, if not in H-bridge mode, this bit has no effect. Set to 1 by the user to enable PWM outputs. Cleared by the user to disable PWM outputs. If HOFF = 1 and HMODE = 1, see Table 114.
[8:6]	PWMCP[2:0]	PWM clock prescaler bits. Sets the UCLK divider. [000] = UCLK/2. [001] = UCLK/4. [010] = UCLK/8. [011] = UCLK/16. [100] = UCLK/32. [101] = UCLK/64. [110] = UCLK/128. [111] = UCLK/256.
5	POINV	Set to 1 by the user to invert all PWM outputs. Cleared by the user to use PWM outputs as normal.
4	HOFF	High side off. Set to 1 by the user to force PWM0 and PWM2 outputs high. This also forces PWM1 and PWM3 low. Cleared by the user to use the PWM outputs as normal.
3	LCOMP	Load compare registers. Set to 1 by the user to load the internal compare registers with the values in PWMxCOMx on the next transition of the PWM timer from 0x00 to 0x01. Cleared by the user to use the values previously stored in the internal compare registers.
2	DIR	Direction control. Set to 1 by the user to enable PWM0 and PWM1 as the output signals while PWM2 and PWM3 are held low. Cleared by the user to enable PWM2 and PWM3 as the output signals while PWM0 and PWM1 are held low.
1	HMODE	Enables H-bridge mode.[1] Set to 1 by the user to enable H-bridge mode and Bit 1 to Bit 5 of PWMCON. Cleared by the user to operate the PWMs in standard mode.
0	PWMEN	Set to 1 by the user to enable all PWM outputs. Cleared by the user to disable all PWM outputs.

[1] In H-bridge mode, HMODE = 1. See Table 114 to determine the PWM outputs.

PLACLK Register

Name: PLACLK

Address: 0xFFFF0B40

Default Value: 0x00

Access: Read/write

PLACLK is the clock selection for the flip-flops of Block 0 and Block 1. Note that the maximum frequency when using the GPIO pins as the clock input for the PLA blocks is 41.78 MHz.

Table 120. PLACLK MMR Bit Descriptions

Bit	Value	Description
7		Reserved.
[6:4]		Block 1 clock source selection.
	000	GPIO clock on P0.5.
	001	GPIO clock on P0.0.
	010	GPIO clock on P0.7.
	011	HCLK.
	100	OCLK (32.768 kHz).
	101	Timer1 overflow.
	110	UCLK.
	111	Internal 32,768 oscillator.
3		Reserved.
[2:0]		Block 0 clock source selection.
	000	GPIO clock on P0.5.
	001	GPIO clock on P0.0.
	010	GPIO clock on P0.7.
	011	HCLK.
	100	OCLK (32.768 kHz).
	101	Timer1 overflow.
	Other	Reserved.

PLAIRQ Register

Name: PLAIRQ

Address: 0xFFFF0B44

Default Value: 0x00000000

Access: Read/write

PLAIRQ enables IRQ0 and/or IRQ1 and selects the source of the IRQ.

Table 121. PLAIRQ MMR Bit Descriptions

Bit	Value	Description
[15:13]		Reserved.
12		PLA IRQ1 enable bit. Set by the user to enable IRQ1 output from PLA. Cleared by the user to disable IRQ1 output from PLA.
[11:8]		PLA IRQ1 source.
	0000	PLA Element 0.
	0001	PLA Element 1.
	1111	PLA Element 15.
[7:5]		Reserved.
4		PLA IRQ0 enable bit. Set by the user to enable IRQ0 output from PLA. Cleared by the user to disable IRQ0 output from PLA.
[3:0]		PLA IRQ0 source.
	0000	PLA Element 0.
	0001	PLA Element 1.
	1111	PLA Element 15.

Table 122. Feedback Configuration

Bit	Value	PLAELM0	PLAELM1 to PLAELM7	PLAELM8	PLAELM9 to PLAELM15
[10:9]	00	Element 15	Element 0	Element 7	Element 8
	01	Element 2	Element 2	Element 10	Element 10
	10	Element 4	Element 4	Element 12	Element 12
	11	Element 6	Element 6	Element 14	Element 14
[8:7]	00	Element 1	Element 1	Element 9	Element 9
	01	Element 3	Element 3	Element 11	Element 11
	10	Element 5	Element 5	Element 13	Element 13
	11	Element 7	Element 7	Element 15	Element 15

PROCESSOR REFERENCE PERIPHERALS

INTERRUPT SYSTEM

There are 25 interrupt sources on the ADuC7124/ADuC7126 that are controlled by the interrupt controller. All interrupts are generated from the on-chip peripherals, except for the software interrupt (SWI), which is programmable by the user. The ARM7TDMI CPU core recognizes interrupts as one of two types: a normal interrupt request (IRQ) and a fast interrupt request (FIQ). All the interrupts can be masked separately.

The control and configuration of the interrupt system is managed through a number of interrupt-related registers. The bits in each IRQ and FIQ register represent the same interrupt source as described in Table 126.

The ADuC7124/ADuC7126 contain a vectored interrupt controller (VIC) that supports nested interrupts up to eight levels. The VIC also allows the programmer to assign priority levels to all interrupt sources. Interrupt nesting must be enabled by setting the ENIRQN bit in the IRQCONN register. A number of extra MMRs are used when the full-vectored interrupt controller is enabled.

IRQSTA/FIQSTA should be saved immediately upon entering the interrupt service routine (ISR) to ensure that all valid interrupt sources are serviced.

Table 126. IRQ/FIQ MMRs Bit Descriptions

Bit	Description	Comments
0	All interrupts OR'ed (FIQ only)	This bit is set if any FIQ is active.
1	Software interrupt	User programmable interrupt source.
2	Timer0	General-Purpose Timer 0.
3	Timer1	General-Purpose Timer 1.
4	Timer2 or wake-up timer	General-Purpose Timer 2 or wake-up timer.
5	Timer3 or watchdog timer	General-Purpose Timer 3 or watchdog timer.
6	Flash Control 0	Flash controller for Block 0 interrupt.
7	Flash Control 1	Flash controller for Block 1 interrupt.
8	ADC	ADC interrupt source bit.
9	UART0	UART0 interrupt source bit.
10	UART1	UART1 interrupt source bit.
11	PLL lock	PLL lock bit.
12	I2C0 master IRQ	I^2C master interrupt source bit.
13	I2C0 slave IRQ	I^2C slave interrupt source bit.
14	I2C1 master IRQ	I^2C master interrupt source bit.
15	I2C1 slave IRQ	I^2C slave interrupt source bit.
16	SPI	SPI interrupt source bit.
17	XIRQ0 (GPIO IRQ0)	External Interrupt 0.
18	Comparator	Voltage comparator source bit.
19	PSM	Power supply monitor.
20	XIRQ1 (GPIO IRQ1)	External Interrupt 1.
21	PLA IRQ0	PLA Block 0 IRQ bit.
22	XIRQ2 (GPIO IRQ2)	External Interrupt 2.
23	XIRQ3 (GPIO IRQ3)	External Interrupt 3.
24	PLA IRQ1	PLA Block 1 IRQ bit.
25	PWM	PWM trip interrupt source bit.

IRQ

The IRQ is the exception signal to enter the IRQ mode of the processor. It services general-purpose interrupt handling of internal and external events.

All 32 bits are logically OR'ed to create a single IRQ signal to the ARM7TDMI core. Descriptions of the four 32-bit registers dedicated to IRQ follow.

IRQSTA Register

IRQSTA is a read-only register that provides the current-enabled IRQ source status (effectively a logic AND of the IRQSIG and IRQEN bits). When set to 1, that source generates an active IRQ request to the ARM7TDMI core. There is no priority encoder or interrupt vector generation. This function is implemented in software in a common interrupt handler routine.

IRQSTA Register

Name: IRQSTA

Address: 0xFFFF0000

Default Value: 0x00000000

Access: Read only

IRQSIG Register

IRQSIG reflects the status of the various IRQ sources. If a peripheral generates an IRQ signal, the corresponding bit in the IRQSIG is set; otherwise, it is cleared. The IRQSIG bits clear when the interrupt in the particular peripheral is cleared. All IRQ sources can be masked in the IRQEN MMR. IRQSIG is read only. This register should not be used in an interrupt service routine for determining the source of an IRQ exception; IRQSTA should only be used for this purpose.

IRQSIG Register

Name: IRQSIG

Address: 0xFFFF0004

Default Value: 0x00000000

Access: Read only

IRQEN Register

IRQEN provides the value of the current enable mask. When a bit is set to 1, the corresponding source request is enabled to create an IRQ exception. When a bit is set to 0, the corresponding source request is disabled or masked, which does not create an IRQ exception. The IRQEN register cannot be used to disable an interrupt.

IRQEN Register

Name: IRQEN

Address: 0xFFFF0008

Default Value: 0x00000000

Access: Read/write

IRQCLR Register

IRQCLR is a write-only register that allows the IRQEN register to clear to mask an interrupt source. Each bit that is set to 1 clears the corresponding bit in the IRQEN register without affecting the remaining bits. The pair of registers, IRQEN and IRQCLR, allow independent manipulation of the enable mask without requiring an atomic read-modify-write.

This register should be used to disable an interrupt source only during the following conditions:

- In the interrupt sources interrupt service routine.
- When the peripheral is temporarily disabled by its own control register.

This register should not be used to disable an IRQ source if that IRQ source has an interrupt pending or may have an interrupt pending.

IRQCLR Register

Name: IRQCLR

Address: 0xFFFF000C

Default Value: 0x00000000

Access: Write only

FAST INTERRUPT REQUEST (FIQ)

The fast interrupt request (FIQ) is the exception signal to enter the FIQ mode of the processor. It is provided to service data transfer or communication channel tasks with low latency. The FIQ interface is identical to the IRQ interface and provides the second level interrupt (highest priority). Four 32-bit registers are dedicated to FIQ: FIQSIG, FIQEN, FIQCLR, and FIQSTA.

Bit 31 to Bit 1 of FIQSTA are logically OR'ed to create the FIQ signal to the core and to Bit 0 of both the FIQ and IRQ registers (FIQ source).

The logic for FIQEN and FIQCLR does not allow an interrupt source to be enabled in both IRQ and FIQ masks. A bit set to 1 in FIQEN clears, as a side effect, the same bit in IRQEN. Likewise, a bit set to 1 in IRQEN clears, as a side effect, the same bit in FIQEN. An interrupt source can be disabled in both the IRQEN and FIQEN masks.

FIQSIG

FIQSIG reflects the status of the different FIQ sources. If a peripheral generates an FIQ signal, the corresponding bit in the FIQSIG is set; otherwise, it is cleared. The FIQSIG bits are cleared when the interrupt in the particular peripheral is cleared. All FIQ sources can be masked in the FIQEN MMR. FIQSIG is read only.

FIQSIG Register

Name: FIQSIG

Address: 0xFFFF0104

Default Value: 0x00000000

Access: Read only

FIQEN

FIQEN provides the value of the current enable mask. When a bit is set to 1, the corresponding source request is enabled to create an FIQ exception. When a bit is set to 0, the corresponding source request is disabled or masked, which does not create an FIQ exception. The FIQEN register cannot be used to disable an interrupt.

FIQEN Register

Name: FIQEN

Address: 0xFFFF0108

Default Value: 0x00000000

Access: Read/write

FIQCLR

FIQCLR is a write-only register that allows the FIQEN register to clear to mask an interrupt source. Each bit that is set to 1 clears the corresponding bit in the FIQEN register without affecting the remaining bits. The pair of registers, FIQEN and FIQCLR, allows independent manipulation of the enable mask without requiring an atomic read-modify-write.

This register should be used to disable an interrupt source only during the following conditions:

- In the interrupt sources interrupt service routine.
- The peripheral is temporarily disabled by its own control register.

This register should not be used to disable an IRQ source if that IRQ source has an interrupt pending or may have an interrupt pending.

Timer2 Clear Register

Name: T2CLRI

Address: 0xFFFF034C

Default Value: 0x00

Access: Write only

This 8-bit write-only MMR is written (with any value) by user code to refresh (reload) Timer2.

Timer2 Value Register

Name: T2VAL

Address: 0xFFFF0344

Default Value: 0x0000

Access: Read only

T2VAL is a 32-bit register that holds the current value of Timer2.

Timer2 Control Register

Name: T2CON

Address: 0xFFFF0348

Default Value: 0x0000

Access: Read/write

This 32-bit MMR configures the mode of operation for Timer2.

Table 144. T2CON MMR Bit Descriptions

Bit	Value	Description
[31:11]		Reserved.
10:9]		Clock source select.
	00	External 32.768 kHz watch crystal (default).
	01	External 32.768 kHz watch crystal.
	10	Internal 32.768 kHz oscillator.
	11	HCLK.
8		Count up. Set by the user for Timer2 to count up. Cleared by the user for Timer2 to count down (default).
7		Timer2 enable bit. Set by the user to enable Timer2. Cleared by the user to disable Timer2 (default).
6		Timer2 mode. Set by the user to operate in periodic mode. Cleared by the user to operate in free-running mode (default).
[5:4]		Format.
	00	Binary (default).
	01	Reserved.
	10	Hr: min: sec: hundredths (23 hours to 0 hours).
	11	Hr: min: sec: hundredths (255 hours to 0 hours).
[3:0]		Prescaler.
	0000	Source clock/1 (default).
	0100	Source clock/16.
	1000	Source clock/256.
	1111	Source clock/32,768.

HARDWARE DESIGN CONSIDERATIONS

POWER SUPPLIES

The ADuC7124/ADuC7126 operational power supply voltage range is 2.7 V to 3.6 V. Separate analog and digital power supply pins (AV_{DD} and IOV_{DD}, respectively) allow AV_{DD} to be kept relatively free of noisy digital signals often present on the system IOV_{DD} line. In this mode, the part can also operate with split supplies; that is, it can use different voltage levels for each supply. For example, the system can be designed to operate with an IOV_{DD} voltage level of 3.3 V while the AV_{DD} level can be at 3 V or vice versa. A typical split supply configuration is shown in Figure 62.

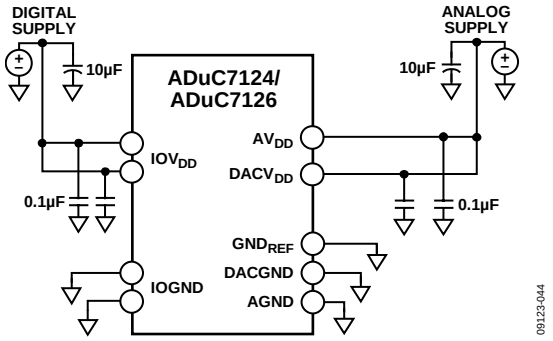

Figure 62. External Dual Supply Connections

As an alternative to providing two separate power supplies, the user can reduce noise on AV_{DD} by placing a small series resistor and/or ferrite bead between AV_{DD} and IOV_{DD} and then decoupling AV_{DD} separately to ground. An example of this configuration is shown in Figure 63. With this configuration, other analog circuitry (such as op amps, voltage reference, or any other analog circuitry) can be powered from the AV_{DD} supply line as well.

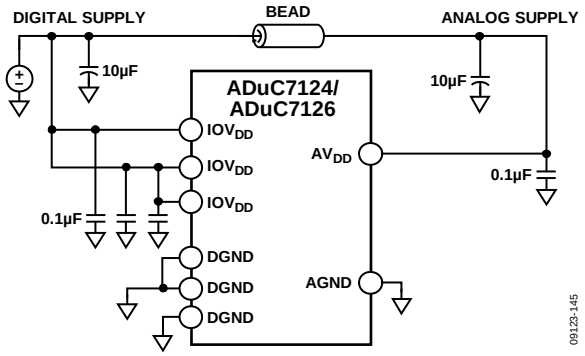

Figure 63. External Single Supply Connections

Notice that in both Figure 62 and Figure 63, a large value (10 µF) reservoir capacitor sits on IOV_{DD}, and a separate 10 µF capacitor sits on AV_{DD}. In addition, local small-value (0.1 µF) capacitors are located at each AV_{DD} and IOV_{DD} pin of the chip. As per standard design practice, be sure to include all of these capacitors and ensure that the smaller capacitors are close to each AV_{DD} pin with trace lengths as short as possible. Connect the ground terminal of each of these capacitors directly to the underlying ground plane.

Finally, note that the analog and digital ground pins on the ADuC7124/ADuC7126 must be referenced to the same system ground reference point at all times.

IOV_{DD} Supply Sensitivity

The IOV_{DD} supply is sensitive to high frequency noise because it is the supply source for the internal oscillator and PLL circuits. When the internal PLL loses lock, the clock source is removed by a gating circuit from the CPU, and the ARM7TDMI core stops executing code until the PLL regains lock. This feature ensures that no flash interface timings or ARM7TDMI timings are violated.

Typically, frequency noise greater than 50 kHz and 50 mV p-p on top of the supply causes the core to stop working.

If decoupling values recommended in the Power Supplies section do not sufficiently dampen all noise sources below 50 mV on IOV_{DD}, a filter such as the one shown in Figure 64 is recommended.

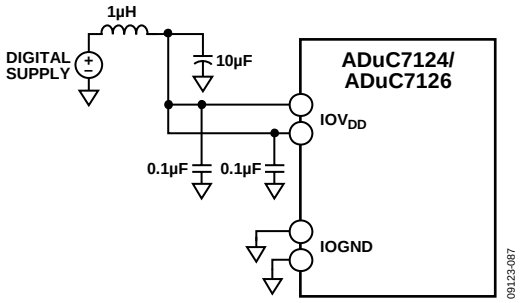

Figure 64. Recommended IOV_{DD} Supply Filter

Linear Voltage Regulator

The ADuC7124/ADuC7126 require a single 3.3 V supply, but the core logic requires a 2.6 V supply. An on-chip linear regulator generates the 2.6 V from IOV_{DD} for the core logic. The LV_{DD} pin is the 2.6 V supply for the core logic. An external compensation capacitor of 0.47 µF must be connected between LV_{DD} and DGND (as close as possible to these pins) to act as a tank of charge as shown in Figure 65.

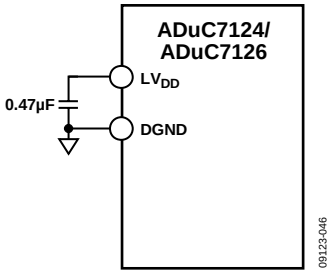

Figure 65. Voltage Regulator Connections

The LV_{DD} pin should not be used for any other chip. It is also recommended to use excellent power supply decoupling on IOV_{DD} to help improve line regulation performance of the on-chip voltage regulator.

NOTES