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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	41.78MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	40
Program Memory Size	126KB (63K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 32
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 12x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc7126bstz126irl

SPECIFICATIONS

AV_{DD} = IOV_{DD} = 2.7 V to 3.6 V, V_{REF} = 2.5 V internal reference, f_{CORE} = 41.78 MHz, T_A = −40°C to +125°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ADC CHANNEL SPECIFICATIONS					Eight acquisition clocks and $f_{ADC}/2$
ADC Power-Up Time		5		µs	
DC Accuracy[1, 2]					
Resolution	12			Bits	
Integral Nonlinearity		±0.6	±1.5	LSB	2.5 V internal reference
		±1.0		LSB	1.0 V external reference
Differential Nonlinearity[3, 4]		±0.5	+1/−0.9	LSB	2.5 V internal reference
		+0.7/−0.6		LSB	1.0 V external reference
DC Code Distribution		1		LSB	ADC input is a dc voltage
ENDPOINT ERRORS[5]					
Offset Error		±1	±2	LSB	
Offset Error Match		±1		LSB	
Gain Error		±2	±5	LSB	
Gain Error Match		±1		LSB	
DYNAMIC PERFORMANCE					f_{IN} = 10 kHz sine wave, f_{SAMPLE} = 1 MSPS
Signal-to-Noise Ratio (SNR)		69		dB	Includes distortion and noise components
Total Harmonic Distortion (THD)		−78		dB	
Peak Harmonic or Spurious Noise		−75		dB	
Channel-to-Channel Crosstalk		−90		dB	Measured on adjacent channels; input channels not being sampled have a 25 kHz sine wave connected to them
ANALOG INPUT					
Input Voltage Ranges[4]					
Differential Mode			V_{CM}[6] ± $V_{REF}/2$	V	
Single-Ended Mode			0 to V_{REF}	V	
Leakage Current		±1	±6	µA	
Input Capacitance		24		pF	During ADC acquisition
ON-CHIP VOLTAGE REFERENCE					0.47 µF from V_{REF} to AGND
Output Voltage		2.5		V	
Accuracy			±5	mV	T_A = 25°C
Reference Temperature Coefficient		±15		ppm/°C	
Power Supply Rejection Ratio		80		dB	
Output Impedance		45		Ω	T_A = 25°C
Internal V_{REF} Power-On Time		1		ms	
EXTERNAL REFERENCE INPUT					
Input Voltage Range	0.625		AV_{DD}	V	
DAC CHANNEL SPECIFICATIONS					R_L = 5 kΩ, C_L = 100 pF
DC Accuracy[7]					
Resolution		12		Bits	
Relative Accuracy		±2		LSB	
Differential Nonlinearity			±1	LSB	Guaranteed monotonic
Offset Error			10	mV	2.5 V internal reference
Gain Error[8]			1.0	%	
Gain Error Mismatch		0.1		%	% of full scale on DAC0

ABSOLUTE MAXIMUM RATINGS

AGND = GND_{REF} = DACGND = GND_{REF}, T_A = 25°C, unless otherwise noted.

Table 8.

Parameter	Rating
AV_{DD} to IOV_{DD}	−0.3 V to +0.3 V
AGND to DGND	−0.3 V to +0.3 V
IOV_{DD} to IOGND, AV_{DD} to AGND	−0.3 V to +6 V
Digital Input Voltage to IOGND	−0.3 V to +5.3 V
Digital Output Voltage to IOGND	−0.3 V to IOV_{DD} + 0.3 V
V_{REF} to AGND	−0.3 V to AV_{DD} + 0.3 V
Analog Inputs to AGND	−0.3 V to AV_{DD} + 0.3 V
Analog Outputs to AGND	−0.3 V to AV_{DD} + 0.3 V
Operating Temperature Range, Industrial	–40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance	
64-Lead LFCSP	24°C/W
80-Lead LQFP	38°C/W
Peak Solder Reflow Temperature	
SnPb Assemblies (10 sec to 30 sec)	240°C
RoHS Compliant Assemblies (20 sec to 40 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Pin No.	Mnemonic	Description
14	XCLKO	Output from the Crystal Oscillator Inverter.
15	XCLKI	Input to the Crystal Oscillator Inverter and Input to the Internal Clock Generator Circuits.
16	BM/P0.0/CMP_{OUT}/PLAI[7]	Multifunction I/O Pin. Boot mode (BM). The ADuC7124 enters download mode if BM is low at reset and executes code if BM is pulled high at reset through a 1 kΩ resistor. General-Purpose Input and Output Port 0.0 (P0.0). Voltage Comparator Output (CMP_{OUT}) Programmable Logic Array Input Element 7 (PLAI[7]).
17	DGND	Ground for Core Logic.
18	LV_{DD}	2.6 V Output of the On-Chip Voltage Regulator. This output must be connected to a 0.47 µF capacitor to DGND only.
19	IOV_{DD}	3.3 V Supply for GPIO and Input of the On-Chip Voltage Regulator.
20	IOGND	Ground for GPIO. Typically connected to DGND.
21	P4.6/PLAO[14]	General-Purpose Input and Output Port 4.6 (P4.6). Programmable Logic Array Output Element 14 (PLAO[14]).
22	P4.7/PLAO[15]	General-Purpose Input and Output Port 4.7 (P4.7). Programmable Logic Array Output Element 15 (PLAO[15]).
23	P0.6/T1/MRST/PLAO[3]	Multifunction Pin, Driven Low After Reset. General-Purpose Output Port 0.6 (P0.6). Timer1 Input (T1). Power-On Reset Output (MRST). Programmable Logic Array Output Element 3 (PLAO[3]).
24	TCK	JTAG Test Port Input, Test Clock. Debug and download access.
25	TDO	JTAG Test Port Output, Test Data Out.
26	P3.0/PWM0/PLAI[8]	General-Purpose Input and Output Port 3.0 (P3.0). PWM Phase 0 (PWM0). Programmable Logic Array Input Element 8 (PLAI[8]).
27	P3.1/PWM1/PLAI[9]	General-Purpose Input and Output Port 3.1 (P3.1). PWM Phase 1 (PWM1). Programmable Logic Array Input Element 9 (PLAI[9]).
28	P3.2/PWM2/PLAI[10]	General-Purpose Input and Output Port 3.2 (P3.2). PWM Phase 2 (PWM2). Programmable Logic Array Input Element 10 (PLAI[10]).
29	P3.3/PWM3/PLAI[11]	General-Purpose Input and Output Port 3.3 (P3.3). PWM Phase 3 (PWM3). Programmable Logic Array Input Element 11 (PLAI[11]).
30	P0.3/TRST/ADC_{BUSY}	General-Purpose Input and Output Port 0.3 (P0.3). JTAG Test Port Input, Test Reset (TRST). JTAG reset input. Debug and download access. If this pin is held low, JTAG access is not possible because the JTAG interface is held in reset and P0.1/P0.2/P0.3 are configured as GPIO pins. ADC_{BUSY} Signal Output (ADC_{BUSY}).
31	P3.4/PWM4/PLAI[12]	General-Purpose Input and Output Port 3.4 (P3.4). PWM Phase 4 (PWM4). Programmable Logic Array Input 12 (PLAI[12]).
32	P3.5/PWM5/PLAI[13]	General-Purpose Input and Output Port 3.5 (P3.5). PWM Phase 5 (PWM5). Programmable Logic Array Input Element 13 (PLAI[13]).
33	$\overline{RST}$	Reset Input, Active Low.
34	IRQ0/P0.4/PWM_{TRIP}/PLAO[1]	Multifunction I/O Pin. External Interrupt Request 0, Active High (IRQ0). General-Purpose Input and Output Port 0.4 (P0.4). PWM Trip External Input (PWM_{TRIP}). Programmable Logic Array Output Element 1 (PLAO[1]).

Pin No.	Mnemonic	Description
50	P1.1/SPM1/SOUT0/I2C0SDA/PLAI[1]	General-Purpose Input and Output Port 1.1 (P1.1). Serial Port Multiplexed (SPM1). UART download pin, UART0 Output (SOUT0). I2C0 (I2C0SDA). Programmable Logic Array Input Element 1 (PLAI[1]).
51	P1.0/T1/SPM0/SIN0/I2C0SCL/PLAI[0]	General-Purpose Input and Output Port 1.0 (P1.0). Timer1 Input (T1). Serial Port Multiplexed (SPM0). UART download pin, UART0 Input (SIN0). I2C0 (I2C0SCL). Programmable Logic Array Input Element 0 (PLAI[0]).
52	P4.2/PLAO[10]	General-Purpose Input and Output Port 4.2 (P4.2). Programmable Logic Array Output Element 10 (PLAO[10]).
53	P4.3/PLAO[11]	General-Purpose Input and Output Port 4.3 (P4.3). Programmable Logic Array Output Element 11 (PLAO[11]).
54	P4.4/PLAO[12]	General-Purpose Input and Output Port 4.4 (P4.4). Programmable Logic Array Output Element 12 (PLAO[12]).
55	RTCK	JTAG Test Port Output, JTAG Return Test Clock.
56	V_{REF}	2.5 V Internal Voltage Reference. Must be connected to a 0.47 µF capacitor when using the internal reference.
57	DAC_{REF}	External Voltage Reference for the DACs. Range: DACGND to $DACV_{DD}$.
58	AV_{DD}	3.3 V Analog Power.
59	AGND	Analog Ground. Ground reference point for the analog circuitry.
60	GND_{REF}	Ground Voltage Reference for the ADC. For optimal performance, the analog power supply should be separated from IOGND and DGND.
61	ADC0	Single-Ended or Differential Analog Input 0.
62	ADC1	Single-Ended or Differential Analog Input 1.
63	ADC2/CMP0	Single-Ended or Differential Analog Input 2 (ADC2). Comparator Positive Input (CMP0).
64	ADC3/CMP1	Single-Ended or Differential Analog Input 3 (ADC3). Comparator Negative Input (CMP1).

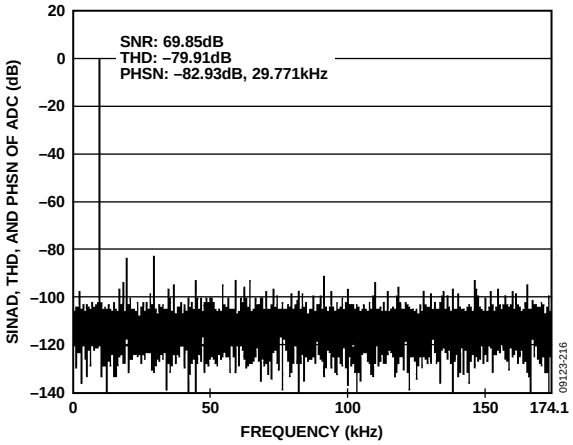

Figure 17. SINAD, THD, and PHSN of ADC,
V_{REF} = Internal 2.5 V, Single-Ended Mode
ADCCP = ADC0

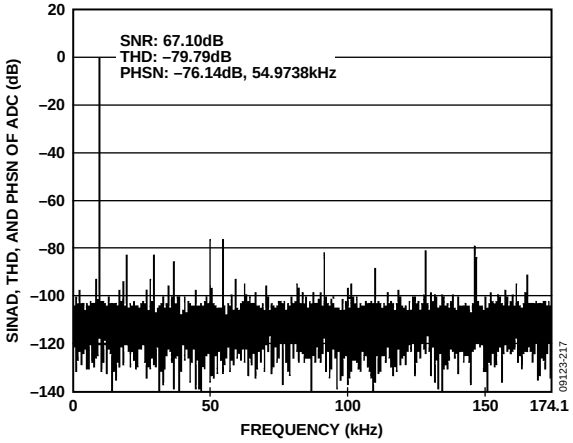

Figure 18. SINAD, THD, and PHSN of ADC,
V_{REF} = Internal 2.5 V, Single-Ended Mode
ADCCP = DAC1/ADC13, ADCCN = ADC0

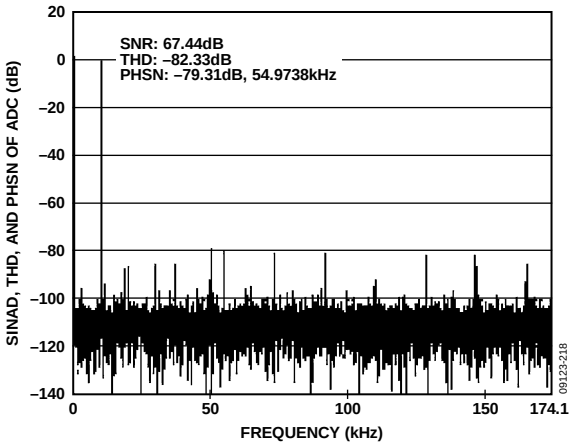

Figure 19. SINAD, THD, and PHSN of ADC,
V_{REF} = Internal 2.5 V, Single-Ended Mode
ADCCP = ADC8, ADCCN = ADC0

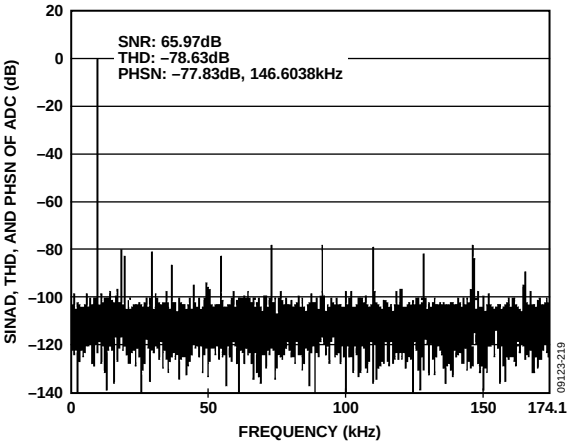

Figure 20. SINAD, THD, and PHSN of ADC,
V_{REF} = Internal 2.5 V, Single-Ended Mode
ADCCP = ADC15/DAC3, ADCCN = ADC0

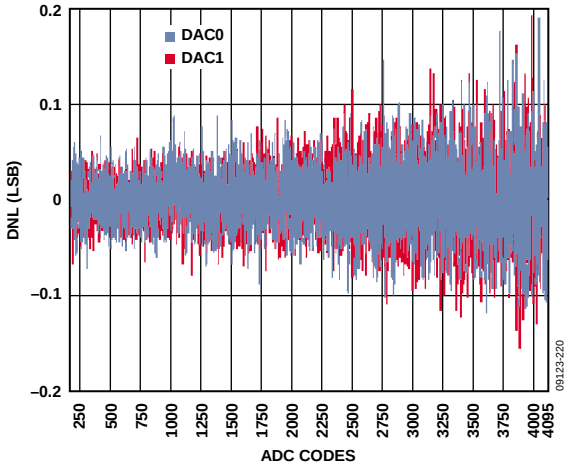

Figure 21. DAC DNL Error,
DAC0 Max Positive DNL: 0.188951, DAC1 Max Positive DNL: 0.190343
DAC0 Max Negative DNL: –0.120081, DAC1 Max Negative DNL: –0.15697

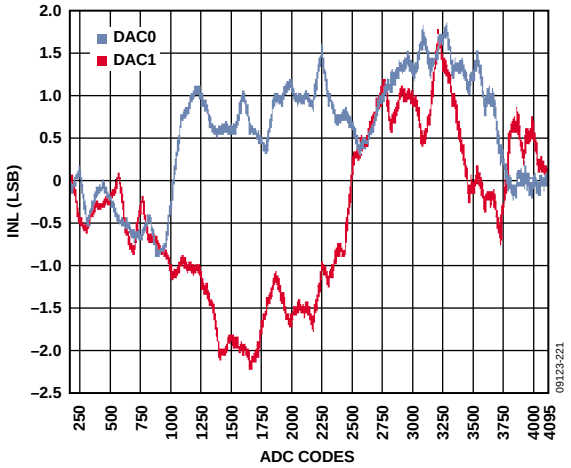

Figure 22. DAC INL Error,
DAC0 Max Positive INL: 1.84106, DAC1 Max Positive INL: 1.75312
DAC0 Max Negative INL: –0.887319, DAC1 Max Negative INL: –2.23708

More information relative to the model of the programmer and the ARM7TDMI core architecture can be found in the following materials from ARM:

- DDI0029G, *ARM7TDMI Technical Reference Manual*
- DDI-0100, *ARM Architecture Reference Manual*

INTERRUPT LATENCY

The worst-case latency for a fast interrupt request (FIQ) consists of the following:

- The longest time the request can take to pass through the synchronizer
- The time for the longest instruction to complete (the longest instruction is an LDM) that loads all the registers including the PC
- The time for the data abort entry
- The time for the FIQ entry

At the end of this time, the ARM7TDMI executes the instruction at 0x1C (FIQ interrupt vector address). The maximum total time is 50 processor cycles, which is just under 1.2 μs in a system using a continuous 41.78 MHz processor clock.

The maximum interrupt request (IRQ) latency calculation is similar but must allow for the fact that FIQ has higher priority and can delay entry into the IRQ handling routine for an arbitrary length of time. This time can be reduced to 42 cycles if the LDM command is not used. Some compilers have an option to compile without using this command. Another option is to run the part in Thumb mode where the time is reduced to 22 cycles.

The minimum latency for FIQ or IRQ interrupts is a total of five cycles, which consist of the shortest time the request can take through the synchronizer plus the time to enter the exception mode.

Note that the ARM7TDMI always runs in ARM (32-bit) mode when in privileged modes, for example, when executing interrupt service routines.

Table 11. IRQ Base Address = 0xFFFF0000

Address	Name	Byte	Access Type
0xFFFF0000	IRQSTA	4	R
0xFFFF0004	IRQSIG	4	R
0xFFFF0008	IRQEN	4	R/W
0xFFFF000C	IRQCLR	4	W
0xFFFF0010	SWICFG	4	W
0xFFFF0014	IRQBASE	4	R/W
0xFFFF001C	IRQVEC	4	R
0xFFFF0020	IRQP0	4	R/W
0xFFFF0024	IRQP1	4	R/W
0xFFFF0028	IRQP2	4	R/W
0xFFFF002C	IRQP3	4	R/W
0xFFFF0030	IRQCONN	1	R/W
0xFFFF0034	IRQCONE	4	R/W
0xFFFF0038	IRQCLRE	1	W
0xFFFF003C	IRQSTAN	1	R/W
0xFFFF0100	FIQSTA	4	R
0xFFFF0104	FIQSIG	4	R
0xFFFF0108	FIQEN	4	R/W
0xFFFF010C	FIQCLR	4	W
0xFFFF011C	FIQVEC	4	R
0xFFFF013C	FIQSTAN	1	R/W

Table 12. System Control Base Address = 0xFFFF0200

Address	Name	Byte	Access Type
0xFFFF0220	REMAP	1	R/W
0xFFFF0230	RSTSTA	1	R
0xFFFF0234	RSTCLR	1	W
0xFFFF0248	RSTKEY0	1	W
0xFFFF024C	RSTCFG	1	R/W
0xFFFF0250	RSTKEY1	1	W

Table 13. Timer Base Address = 0xFFFF0300

Address	Name	Byte	Access Type
0xFFFF0300	T0LD	2	R/W
0xFFFF0304	T0VAL	2	R
0xFFFF0308	T0CON	2	R/W
0xFFFF030C	T0CLRI	1	W
0xFFFF0320	T1LD	4	R/W
0xFFFF0324	T1VAL	4	R
0xFFFF0328	T1CON	2	R/W
0xFFFF032C	T1CLRI	1	W
0xFFFF0330	T1CAP	4	R
0xFFFF0340	T2LD	4	R/W
0xFFFF0344	T2VAL	4	R
0xFFFF0348	T2CON	2	R/W
0xFFFF034C	T2CLRI	1	W
0xFFFF0360	T3LD	2	R/W
0xFFFF0364	T3VAL	2	R
0xFFFF0368	T3CON	2	R/W
0xFFFF036C	T3CLRI	1	W

Table 22. I2C1 Base Address = 0xFFFF0900

Address	Name	Byte	Access Type	Cycle
0xFFFF0900	I2C1MCON	2	R/W	2
0xFFFF0904	I2C1MSTA	2	R	2
0xFFFF0908	I2C1MRX	1	R	2
0xFFFF090C	I2C1MTX	2	R/W	2
0xFFFF0910	I2C1MCNT0	2	R/W	2
0xFFFF0914	I2C1MCNT1	1	R	2
0xFFFF0918	I2C1ADR0	1	R/W	2
0xFFFF091C	I2C1ADR1	1	R/W	2
0xFFFF0924	I2C1DIV	2	R/W	2
0xFFFF0928	I2C1SCON	2	R/W	2
0xFFFF092C	I2C1SSTA	2	R	2
0xFFFF0930	I2C1SRX	1	R	2
0xFFFF0934	I2C1STX	1	W	2
0xFFFF0938	I2C1ALT	1	R/W	2
0xFFFF093C	I2C1ID0	1	R/W	2
0xFFFF0940	I2C1ID1	1	R/W	2
0xFFFF0944	I2C1ID2	1	R/W	2
0xFFFF0948	I2C1ID3	1	R/W	2
0xFFFF094C	I2C1FSTA	1	R/W	2

Table 23. SPI Base Address = 0xFFFF0A00

Address	Name	Byte	Access Type	Cycle
0xFFFF0A00	SPISTA	2	R	2
0xFFFF0A04	SPIRX	1	R	2
0xFFFF0A08	SPITX	1	W	2
0xFFFF0A0C	SPIDIV	1	R/W	2
0xFFFF0A10	SPICON	2	R/W	2

Table 24. PLA Base Address = 0xFFFF0B00

Address	Name	Byte	Access Type	Cycle
0xFFFF0B00	PLAELM0	2	R/W	2
0xFFFF0B04	PLAELM1	2	R/W	2
0xFFFF0B08	PLAELM2	2	R/W	2
0xFFFF0B0C	PLAELM3	2	R/W	2
0xFFFF0B10	PLAELM4	2	R/W	2
0xFFFF0B14	PLAELM5	2	R/W	2
0xFFFF0B18	PLAELM6	2	R/W	2
0xFFFF0B1C	PLAELM7	2	R/W	2
0xFFFF0B20	PLAELM8	2	R/W	2
0xFFFF0B24	PLAELM9	2	R/W	2
0xFFFF0B28	PLAELM10	2	R/W	2
0xFFFF0B2C	PLAELM11	2	R/W	2
0xFFFF0B30	PLAELM12	2	R/W	2
0xFFFF0B34	PLAELM13	2	R/W	2
0xFFFF0B38	PLAELM14	2	R/W	2
0xFFFF0B3C	PLAELM15	2	R/W	2
0xFFFF0B40	PLACLK	1	R/W	2
0xFFFF0B44	PLAIRQ	2	R/W	2
0xFFFF0B48	PLAADC	4	R/W	2
0xFFFF0B4C	PLADIN	4	R/W	2
0xFFFF0B50	PLADOUT	4	R	2
0xFFFF0B54	PLALCK	1	W	2

Table 59. REMAP MMR Bit Descriptions
(Address = 0xFFFF0220. Default Value = 0x00)

Bit	Name	Description
0	Remap	Remap bit. Set by the user to remap the SRAM to Address 0x00000000. Cleared automatically after reset to remap the Flash/EE memory to Address 0x00000000.

Remap Operation

When a reset occurs on the ADuC7124/ADuC7126, execution automatically starts in factory programmed, internal configuration code. This kernel is hidden and cannot be accessed by user code. If the part is in normal mode (BM pin is high), it executes the power-on configuration routine of the kernel and then jumps to the reset vector address, 0x00000000, to execute the reset exception routine of the user.

Because the Flash/EE is mirrored at the bottom of the memory array at reset, the reset interrupt routine must always be written in Flash/EE.

The remap is done from Flash/EE by setting Bit 0 of the REMAP register. Caution must be taken to execute this command from Flash/EE, above Address 0x00080020, and not from the bottom of the array, because this is replaced by the SRAM.

This operation is reversible. The Flash/EE can be remapped at Address 0x00000000 by clearing Bit 0 of the REMAP MMR. Caution must again be taken to execute the remap function from outside the mirrored area. Any type of reset remaps the Flash/EE memory at the bottom of the array.

Reset Operation

There are four kinds of reset: external, power-on, watchdog expiation, and software force. The RSTSTA register indicates the source of the last reset, and RSTCLR allows clearing of the RSTSTA register. These registers can be used during a reset exception service routine to identify the source of the reset. If RSTSTA is null, the reset is external.

The RSTCFG register allows different peripherals to retain their state after a watchdog or software reset.

RSTSTA Register

Name: RSTSTA

Address: 0xFFFF0230

Default Value: 0x01

Access: Read only

Table 60. RSTSTA MMR Bit Descriptions

Bit	Description
[7:3]	Reserved.
2	Software reset. Set by the user to force a software reset. Cleared by setting the corresponding bit in RSTCLR.
1	Watchdog timeout. Set automatically when a watchdog timeout occurs. Cleared by setting the corresponding bit in RSTCLR.
0	Power-on reset. Set automatically when a power-on reset occurs. Cleared by setting the corresponding bit in RSTCLR.

RSTCLR Register

Name: RSTCLR

Address: 0xFFFF0234

Default Value: 0x00

Access: Write only

Note that to clear the RSTSTA register, users must write the Value 0x07 to the RSTCLR register.

RSTCFG Register

Name: RSTCFG

Address: 0xFFFF024C

Default Value: 0x05

Access: Read/write

Table 61. RSTCFG MMR Bit Descriptions

Bit	Description
[7:3]	Reserved. Always set to 0.
2	This bit is set to 1 to configure the DAC outputs to retain their state after a watchdog or software reset. This bit is cleared for the DAC pins and registers to return to their default state.
1	Reserved. Always set to 0.
0	This bit is set to 1 to configure the GPIO pins to retain their state after a watchdog or software reset. This bit is cleared for the GPIO pins and registers to return to their default state.

The RSTCFG write sequence is as follows:

1. Write Code 0x76 to Register RSTKEY1.
2. Write user value to Register RSTCFG.
3. Write Code 0xB1 to Register RSTKEY2.

Comparator Interface

The comparator interface consists of a 16-bit MMR, CMPCON, which is described in Table 69.

CMPCON Register

Name: CMPCON

Address: 0xFFFF0444

Default Value: 0x0000

Access: Read/write

Table 69. CMPCON MMR Bit Descriptions

Bit	Value	Name	Description
[15:11]			Reserved.
10		CMPEN	Comparator enable bit. Set by the user to enable the comparator. Cleared by the user to disable the comparator.
[9:8]		CMPIN	Comparator negative input select bits.
	00		$AV_{DD}/2$.
	01		ADC3 input.
	10		DAC0 output.
	11		Reserved.
[7:6]		CMPOC	Comparator output configuration bits.
	00		Reserved.
	01		Reserved.
	10		Output on CMP_{OUT}.
	11		IRQ.
5		CMPOL	Comparator output logic state bit. When low, the comparator output is high if the positive input (CMP0) is above the negative input (CMP1). When high, the comparator output is high if the positive input is below the negative input.
[4:3]		CMPRES	Response time.
	00		5 µs response time typical for large signals (2.5 V differential). 17 µs response time typical for small signals (0.65 mV differential).
	11		4 µs typical.
	01/10		Reserved.
2		CMPHYST	Comparator hysteresis sit. Set by user to have a hysteresis of about 7.5 mV. Cleared by user to have no hysteresis.
1		CMPORI	Comparator output rising edge interrupt. Set automatically when a rising edge occurs on the monitored voltage (CMP0). Cleared by user by writing a 1 to this bit.
0		CMPOFI	Comparator output falling edge interrupt. Set automatically when a falling edge occurs on the monitored voltage (CMP0). Cleared by user by writing a 1 to this bit.

OSCILLATOR AND PLL—POWER CONTROL

Clocking System

The ADuC7124/ADuC7126 integrate a 32.768 kHz ± 3% oscillator, a clock divider, and a PLL. The PLL locks onto a multiple (1275) of the internal oscillator or an external 32.768 kHz crystal to provide a stable 41.78 MHz clock (UCLK) for the system. To allow power saving, the core can operate at this frequency or at binary submultiples of it. The actual core operating frequency, UCLK/2^{CD}, is referred to as HCLK. The default core clock is the PLL clock divided by 8 (CD = 3) or 5.22 MHz. The core clock frequency can also come from an external clock on the ECLK pin as shown in Figure 45. The core clock can be output on ECLK when using an internal oscillator or external crystal.

Note that, when the ECLK pin is used to output the core clock, the output signal is not buffered and is not suitable for use as a clock source to an external device without an external buffer.

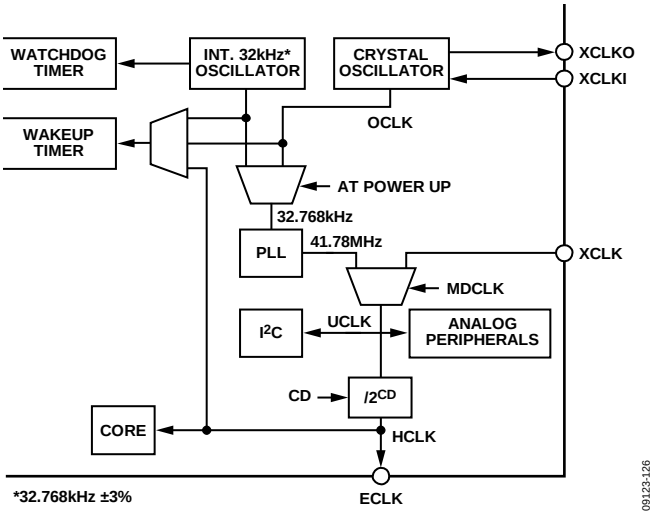

Figure 45. Clocking System

The selection of the clock source is in the PLLCON register. By default, the part uses the internal oscillator feeding the PLL.

Table 79. GPxCON Registers

Name	Address	Default Value	Access
GP0CON	0xFFFFF400	0x00000000	R/W
GP1CON	0xFFFFF404	0x00000000	R/W
GP2CON	0xFFFFF408	0x00000000	R/W
GP3CON	0xFFFFF40C	0x00000000	R/W
GP4CON	0xFFFFF410	0x00000000	R/W

GPxCON are the Port x control registers that select the function of each pin of Port x, as described in Table 80.

Table 80. GPxCON MMR Bit Descriptions

Bit	Description
[31:30]	Reserved.
[29:28]	Select function of Px.7 pin.
[27:26]	Reserved.
[25:24]	Select function of Px.6 pin.
[23:22]	Reserved.
[21:20]	Select function of Px.5 pin.
[19:18]	Reserved.
[17:16]	Select function of Px.4 pin.
[15:14]	Reserved.
[13:12]	Select function of Px.3 pin.
[11:10]	Reserved.
[9:8]	Select function of Px.2 pin.
[7:6]	Reserved.
[5:4]	Select function of Px.1 pin.
[3:2]	Reserved.
[1:0]	Select function of Px.0 pin.

Table 81. GPxPAR Registers

Name	Address	Default Value	Access
GP0PAR	0xFFFFF42C	0x20000000	R/W
GP1PAR	0xFFFFF43C	0x00000000	R/W
GP2PAR	0xFFFFF44C	0x000000FF	R/W
GP3PAR	0xFFFFF45C	0x00222222	R/W
GP4PAR	0xFFFFF46C	0x00000000	R/W

The GPxPAR registers program the parameters for Port 0, Port 1, Port 2, Port 3, and Port 4. Note that the GPxDAT MMR must always be written after changing the GPxPAR MMR.

Table 82. GPxPAR MMR Bit Descriptions

Bit	Description
31	Reserved.
[30:29]	Drive strength Px.7.
28	Pull-up disable Px.7.
27	Reserved.
[26:25]	Drive strength Px.6.
24	Pull-up disable Px.6.
23	Reserved.
[22:21]	Drive strength Px.5.
20	Pull-up disable Px.5.
19	Reserved.
[18:17]	Drive strength Px.4.
16	Pull-up disable Px.4.
15	Reserved.
[14:13]	Drive strength Px.3.
12	Pull-up disable Px.3.
11	Reserved.
[10:9]	Drive strength Px.2.
8	Pull-up disable Px.2.
7	Reserved.
[6:5]	Drive strength Px.1.
4	Pull-up disable Px.1.
3	Reserved.
[2:1]	Drive strength Px.0.
0	Pull-up disable Px.0.

Table 83. GPIO Drive Strength Control Bits Descriptions

Control Bits Value	Description
00	Medium drive strength.
01	Low drive strength.
1x	High drive strength.

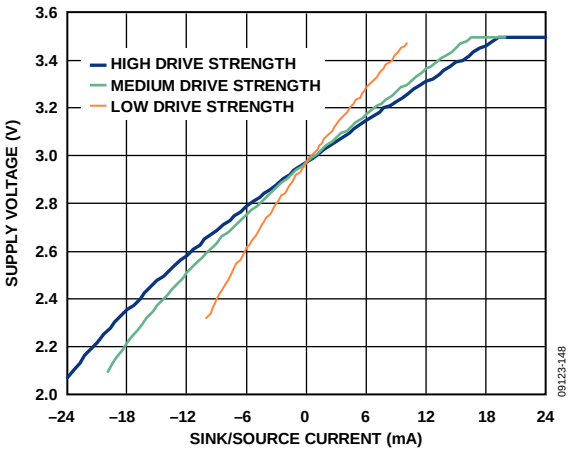

Figure 46. Programmable Strength for High Level

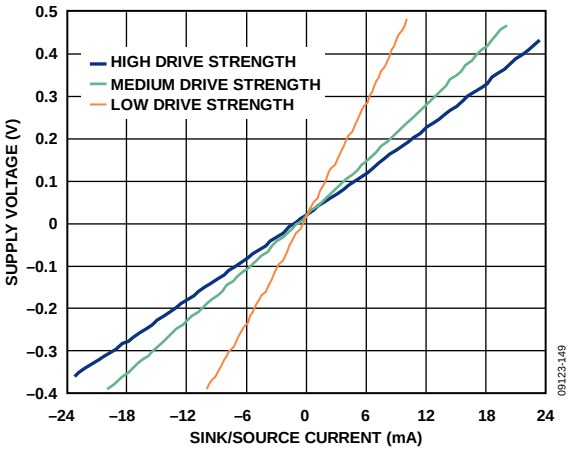

Figure 47. Programmable Strength for Low Level

COM0DIV2 Register

Name: COM0DIV2

Address: 0xFFFF072C

Default Value: 0x0000

Access: Read/write

COM0DIV2 is a 16-bit fractional baud divide register for UART0.

COM1DIV2 Register

Name: COM1DIV2

Address: 0xFFFF076C

Default Value: 0x0000

Access: Read/write

COM1DIV2 is a 16-bit fractional baud divide register for UART1.

Table 99. COMxDIV2 MMR Bit Descriptions

Bit	Name	Description
15	FBEN	Fractional baud rate generator enable bit. Set by the user to enable the fractional baud rate generator. Cleared by the user to generate the baud rate using the standard 450 UART baud rate generator.
[14:13]		Reserved.
[12:11]	FBM[1:0]	M if FBM = 0, M = 4 (see The Fractional Divider section).
[10:0]	FBN[10:0]	N (see The Fractional Divider section).

SERIAL PERIPHERAL INTERFACE

The ADuC7124/ADuC7126 integrate a complete hardware serial peripheral interface (SPI) on chip. SPI is an industry standard, synchronous serial interface that allows eight bits of data to be synchronously transmitted and simultaneously received, that is, full duplex up to a maximum bit rate of 20 Mbps.

The SPI port can be configured for master or slave operation and typically consists of four pins: MISO, MOSI, SCLK, and $\overline{CS}$.

MISO (Master In, Slave Out) Pin

The MISO pin is configured as an input line in master mode and an output line in slave mode. The MISO line on the master (data in) should be connected to the MISO line in the slave device (data out). The data is transferred as byte wide (8-bit) serial data, MSB first.

MOSI (Master Out, Slave In) Pin

The MOSI pin is configured as an output line in master mode and an input line in slave mode. The MOSI line on the master (data out) should be connected to the MOSI line in the slave device (data in). The data is transferred as byte wide (8-bit) serial data, MSB first.

SCLK (Serial Clock I/O) Pin

The master serial clock (SCLK) synchronizes the data being transmitted and received through the MOSI SCLK period. Therefore, a byte is transmitted/received after eight SCLK periods. The SCLK pin is configured as an output in master mode and as an input in slave mode.

In master mode, polarity and phase of the clock are controlled by the SPICON register, and the bit rate is defined in the SPIDIV register as follows:

$$f_{SERIAL\ CLOCK} = \frac{f_{UCLK}}{2\times(1+SPIDIV)}$$

The maximum speed of the SPI clock is independent of the clock divider bits.

In slave mode, the SPICON register must be configured with the phase and polarity of the expected input clock. The slave accepts data from an external master up to 10 Mbps.

In both master and slave modes, data is transmitted on one edge of the SCLK signal and sampled on the other. Therefore, it is important that the polarity and phase be configured the same for the master and slave devices.

$\overline{CS}$ (SPI Chip Select Input) Pin

In SPI slave mode, a transfer is initiated by the assertion of $\overline{CS}$, which is an active low input signal. The SPI port then transmits and receives 8-bit data until the transfer is concluded by deassertion of $\overline{CS}$. In slave mode, $\overline{CS}$ is always an input.

In SPI master mode, the $\overline{CS}$ is an active low output signal. It asserts itself automatically at the beginning of a transfer and deasserts itself upon completion.

Configuring External Pins for SPI functionality

The SPI pins of the ADuC7124/ADuC7126 device are P1.4 to P1.7.

P1.7 is the slave chip select pin. In slave mode, this pin is an input and must be driven low by the master. In master mode, this pin is an output and goes low at the beginning of a transfer and high at the end of a transfer.

P1.4 is the SCLK pin.

P1.5 is the master in, slave out (MISO) pin.

P1.6 is the master out, slave in (MOSI) pin.

To configure P1.4 to P1.7 for SPI mode, see the General-Purpose Input/Output section.

I²C Master Receive Register

Name: I2C0MRX, I2C1MRX

Address: 0xFFFF0808, 0xFFFF0908

Default Value: 0x00

Access: Read only

Function: This 8-bit MMR is the I²C master receive register.

I²C Master Transmit Register

Name: I2C0MTX, I2C1MTX

Address: 0xFFFF080C 0xFFFF090C

Default Value: 0x00, 0x00

Access: Read/write

Function: This 8-bit MMR is the I²C master transmit register.

I²C Master Read Count Register

Name: I2C0MCNT0, I2C1MCNT0

Address: 0xFFFF0810, 0xFFFF0910

Default Value: 0x0000, 0x0000

Access: Read/write

Function: This 16-bit MMR holds the required number of bytes when the master begins a read sequence from a slave device.

Table 104. I2CxMCNT0 MMR Bit Descriptions

Bit	Name	Description
[15:9]		Reserved.
8	I2CRECNT	Set this bit if more than 256 bytes are required from the slave. Clear this bit when reading 256 bytes or less.
[7:0]	I2CRCNT	These eight bits hold the number of bytes required during a slave read sequence, minus 1. If only a single byte is required, these bits should be set to 0.

I²C Master Current Read Count Register

Name: I2C0MCNT1, I2C1MCNT1

Address: 0xFFFF0814, 0xFFFF0914

Default Value: 0x00, 0x00

Access: Read only

Function: This 8-bit MMR holds the number of bytes received so far during a read sequence with a slave device.

I²C Address 0 Register

Name: I2C0ADR0, I2C1ADR0

Address: 0xFFFF0818, 0xFFFF0918

Default Value: 0x00

Access: Read/write

Function: This 8-bit MMR holds the 7-bit slave address + the read/write bit when the master begins communicating with a slave.

Table 105. I2CxADR0 MMR in 7-Bit Address Mode

Bit	Name	Description
[7:1]	I2CADR	These bits contain the 7-bit address of the required slave device.
0	R/W	Bit 0 is the read/write bit. When this bit = 1, a read sequence is requested. When this bit = 0, a write sequence is requested.

Table 106. I2CxADR0 MMR in 10-Bit Address Mode

Bit	Name	Description
[7:3]		These bits must be set to [11110b] in 10-bit address mode.
[2:1]	I2CMADR	These bits contain ADDR[9:8] in 10-bit addressing mode.
0	R/W	Read/write bit. When this bit = 1, a read sequence is requested. When this bit = 0, a write sequence is requested.

Bit	Name	Description
3	I2CHGCEN	I²C hardware general call enable. When this bit and Bit 2 are set, and having received a general call (Address 0x00) and a data byte, the device checks the contents of the I2CxALT against the receive register. If the contents match, the device has received a hardware general call. This is used if a device needs urgent attention from a master device without knowing which master it needs to turn to. This is a broadcast message to all master devices on the bus. The ADuC7124/ADuC7126 watch for these addresses. The device that requires attention embeds its own address into the message. All masters listen, and the one that can handle the device contacts its slave and acts appropriately. The LSB of the I2CxALT register should always be written to 1, as per the I²C January 2000 bus specification. Set this bit and I2CGCEN to enable hardware general call recognition in slave mode. Clear this bit to disable recognition of hardware general call commands.
2	I2CGCEN	I²C general call enable. Set this bit to enable the slave device to acknowledge an I²C general call, Address 0x00 (write). The device then recognizes a data bit. If it receives a 0x06 (reset and write programmable part of the slave address by hardware) as the data byte, the I²C interface resets as per the I²C January 2000 bus specification. This command can be used to reset an entire I²C system. If it receives a 0x04 (write programmable part of the slave address by hardware) as the data byte, the general call interrupt status bit sets on any general call. The user must take corrective action by reprogramming the device address. Set this bit to allow the slave ACK I²C general call commands. Clear this bit to disable recognition of general call commands.
1	ADR10EN	I²C 10-bit address mode. Set to 1 to enable 10-bit address mode. Clear to 0 to enable normal address mode.
0	I2CSEN	I²C slave enable bit. Set by the user to enable I²C slave mode. Clear this bit to disable I²C slave mode.

I²C Slave Status Registers

Name: I2C0SSTA, I2C1SSTA

Address: 0xFFFF082C, 0xFFFF092C

Default Value: 0x0000, 0x0000

Access: Read only

Function: This 16-bit MMR is the I²C status register in slave mode.

Table 110. I2CxSSTA MMR Bit Descriptions

Bit	Name	Description
15		Reserved.
14	I2CSTA	This bit is set to 1 if a start condition followed by a matching address is detected, a start byte (0x01) is received, or general calls are enabled and a general call code of (0x00) is received. This bit is cleared on receiving a stop condition.
13	I2CREPS	This bit is set to 1 if a repeated start condition is detected. This bit is cleared on receiving a stop condition. A read of the I2CxSSTA register also clears this bit.
[12:11]	I2CID[1:0]	I²C address matching register. These bits indicate which I2CxIDx register matches the received address. [00] = received address matches I2CxID0. [01] = received address matches I2CxID1. [10] = received address matches I2CxID2. [11] = received address matches I2CxID3.
10	I2CSS	I²C stop condition after start detected bit. This bit is set to 1 when a stop condition is detected after a previous start and matching address. When the I2CSSENI bit in I2CxSCON is set, an interrupt is generated. This bit is cleared by reading this register.

IRQVEC Register

The IRQ interrupt vector register, IRQVEC points to a memory address containing a pointer to the interrupt service routine of the currently active IRQ. This register should only be read when an IRQ occurs and IRQ interrupt nesting has been enabled by setting Bit 0 of the IRQCONN register.

Name: IRQVEC

Address: 0xFFFF001C

Default Value: 0x00000000

Access: Read only

Table 129. IRQVEC MMR Bit Descriptions

Bit	Type	Initial Value	Description
[31:23]	R	0	Always read as 0.
[22:7]	R/W	0	IRQBASE register value.
[6:2]	R	0	Highest priority source. This is a value between 0 and 27 representing the possible interrupt sources. For example, if the highest currently active IRQ is Timer 2, then these bits are [00100].
[1:0]	Reserved	0	Reserved bits.

Priority Registers

The IRQ interrupt vector register, IRQVEC points to a memory address containing a pointer to the interrupt service routine of the currently active IRQ. This register should only be read when an IRQ occurs and IRQ interrupt nesting has been enabled by setting Bit 0 of the IRQCONN register.

IRQP0 Register

Name: IRQP0

Address: 0xFFFF0020

Default Value: 0x00000000

Access: Read/write

Table 130. IRQP0 MMR Bit Descriptions

Bit	Name	Description
31		Reserved.
[30:28]	Flash1PI	A priority level of 0 to 7 can be set for the Flash Block 1 controller interrupt source.
27		Reserved.
[26:24]	Flash0PI	A priority level of 0 to 7 can be set for the Flash Block 0 controller interrupt source.
23		Reserved.
[22:20]	T3PI	A priority level of 0 to 7 can be set for Timer 3.
19		Reserved.
[18:16]	T2PI	A priority level of 0 to 7 can be set for Timer2.
15		Reserved.
[14:12]	T1PI	A priority level of 0 to 7 can be set for Timer1.
11		Reserved.
[10:8]	T0PI	A priority level of 0 to 7 can be set for Timer0.
7		Reserved.
[6:4]	SWINTP	A priority level of 0 to 7 can be set for the software interrupt source.
[3:0]		Interrupt 0 cannot be prioritized.

IRQP1 Register

Name: IRQP1

Address: 0xFFFF0024

Default Value: 0x00000000

Access: Read/write

Table 131. IRQP1 MMR Bit Descriptions

Bit	Name	Description
31		Reserved.
[30:28]	I2C1SPI	A priority level of 0 to 7 can be set for the I2C1 slave.
27		Reserved.
[26:24]	I2C1MPI	A priority level of 0 to 7 can be set for the I2C1 master.
23		Reserved.
[22:20]	I2C0SPI	A priority level of 0 to 7 can be set for the I2C0 slave.
19		Reserved.
[18:16]	I2C0MPI	A priority level of 0 to 7 can be set for the I^2C 0 master.
15		Reserved.
[14:12]	PLLPI	A priority level of 0 to 7 can be set for the PLL lock interrupt.
11		Reserved.
[10:8]	UART1PI	A priority level of 0 to 7 can be set for UART1.
7		Reserved.
[6:4]	UART0PI	A priority level of 0 to 7 can be set for UART0.
5		Reserved.
[2:0]	ADCPI	A priority level of 0 to 7 can be set for the ADC interrupt source.

IRQP2 Register

Name: IRQP2

Address: 0xFFFF0028

Default Value: 0x00000000

Access: Read/write

Table 132. IRQP2 MMR Bit Descriptions

Bit	Name	Description
31		Reserved.
[30:28]	IRQ3PI	A priority level of 0 to 7 can be set for IRQ3.
27		Reserved.
[26:24]	IRQ2PI	A priority level of 0 to 7 can be set for IRQ2.
23		Reserved.
[22:20]	PLA0PI	A priority level of 0 to 7 can be set for PLA IRQ0.
19		Reserved.
[18:16]	IRQ1PI	A priority level of 0 to 7 can be set for IRQ1.
15		Reserved.
[14:12]	PSMPI	A priority level of 0 to 7 can be set for the power supply monitor interrupt source.
11		Reserved.
[10:8]	COMPI	A priority level of 0 to 7 can be set for the comparator.
7		Reserved.
[6:4]	IRQ0PI	A priority level of 0 to 7 can be set for IRQ0.
3		Reserved.
[2:0]	SPIPI	A priority level of 0 to 7 can be set for SPI.

IRQP3 Register

Name: IRQP3

Address: 0xFFFF002C

Default Value: 0x00000000

Access: Read/write

Table 133. IRQP3 MMR Bit Descriptions

Bit	Name	Description
[31:7]		Reserved.
[6:4]	PWMPI	A priority level of 0 to 7 can be set for PWM.
3		Reserved.
[2:0]	PLA1PI	A priority level of 0 to 7 can be set for PLA IRQ1.

IRQCONN Register

The IRQCONN register is the IRQ and FIQ control register. It contains two active bits: the first to enable nesting and prioritization of IRQ interrupts and the other to enable nesting and prioritization of FIQ interrupts.

If these bits are cleared, FIQs and IRQs can still be used, but it is not possible to nest IRQs or FIQs, nor is it possible to set an interrupt source priority level. In this default state, an FIQ does have a higher priority than an IRQ.

Name: IRQCONN

Address: 0xFFFF0030

Default Value: 0x00000000

Access: Read/write

Table 134. IRQCONN MMR Bit Descriptions

Bit	Name	Description
31:2		Reserved. These bits are reserved and should not be written to.
1	ENFIQN	Setting this bit to 1 enables nesting of FIQ interrupts. Clearing this bit means no nesting or prioritization of FIQs is allowed.
0	ENIRQN	Setting this bit to 1 enables nesting of IRQ interrupts. Clearing this bit means no nesting or prioritization of IRQs is allowed.

IRQSTAN Register

If IRQCONN Bit 0 is asserted and IRQVEC is read, one of the IRQSTAN[7:0] bits is asserted. The bit that asserts depends on the priority of the IRQ. If the IRQ is of Priority 0, then Bit 0 asserts, if Priority 1, then Bit 1 asserts, and so on. When a bit is set in this register, all interrupts of that priority and lower are blocked.

To clear a bit in this register, all bits of a higher priority must be cleared first. It is only possible to clear one bit at a time. For example, if this register is set to 0x09, writing 0xFF changes the register to 0x08, and writing 0xFF a second time changes the register to 0x00.

Name: IRQSTAN

Address: 0xFFFF003C

Default Value: 0x00000000

Access: Read/write

Table 135. IRQSTAN MMR Bit Descriptions

Bit	Name	Description
31:8		Reserved. These bits are reserved and should not be written to.
7:0		Setting these bits to 1 enables nesting of FIQ interrupts. Clearing these bits means no nesting or prioritization of FIQs is allowed.

FIQVEC Register

The FIQ interrupt vector register, FIQVEC, points to a memory address containing a pointer to the interrupt service routine of the currently active FIQ. This register should be read only when an FIQ occurs and FIQ interrupt nesting has been enabled by setting Bit 1 of the IRQCONN register.

Name: FIQVEC

Address: 0xFFFF011C

Default Value: 0x00000000

Access: Read only

Table 136. FIQVEC MMR Bit Descriptions

Bit	Type	Initial Value	Description
[31:23]	R	0	Always read as 0.
[22:7]	R/W	0	IRQBASE register value.
[6:2]		0	Highest priority source. This is a value between 0 and 27, representing the currently active interrupt source. The interrupts are listed in Table 126. For example, if the highest currently active FIQ is Timer2, then these bits are [00100].
[1:0]		0	Reserved.

FIQSTAN Register

If IRQCONN Bit 1 is asserted and FIQVEC is read, one of the FIQSTAN[7:0] bits is asserted. The bit that asserts depends on the priority of the FIQ. If the FIQ is of Priority 0, Bit 0 asserts, if Priority 1, Bit 1 asserts, and so forth.

When a bit is set in this register all interrupts of that priority and lower are blocked.

To clear a bit in this register, all bits of a higher priority must be cleared first. It is possible to clear only one bit at a time. For example, if this register is set to 0x09, then writing 0xFF changes the register to 0x08 and writing 0xFF a second time changes the register to 0x00.

Name: FIQSTAN

Address: 0xFFFF013C

Default Value: 0x00000000

Access: Read/write

Table 137. FIQSTAN MMR Bit Descriptions

Bit	Name	Description
31:8		Reserved. These bits are reserved and should not be written to.
7:0		Setting this bit to 1 enables nesting of FIQ interrupts. Clearing this bit means no nesting or prioritization of FIQs is allowed.

External Interrupts and PLA interrupts

The ADuC7124/ADuC7126 provide up to four external interrupt sources and two PLA interrupt sources. These external interrupts can be individually configured as level or rising/falling edge triggered.

To enable the external interrupt source or the PLA interrupt source, the appropriate bit must first be set in the FIQEN or IRQEN register. To select the required edge or level to trigger on, the IRQCONE register must be appropriately configured.

To properly clear an edge-based external IRQ interrupt or an edge-based PLA interrupt, set the appropriate bit in the IRQCLRE register.

IRQCONE Register

Name: IRQCONE

Address: 0xFFFF0034

Default Value: 0x00000000

Access: Read/write

Table 138. IRQCONE MMR Bit Descriptions

Bit	Value	Name	Description
[31:12]			Reserved. These bits are reserved and should not be written to.
[11:10]	11	PLA1SRC[1:0]	PLA IRQ1 triggers on falling edge.
	10		PLA IRQ1 triggers on rising edge.
	01		PLA IRQ1 triggers on low level.
	00		PLA IRQ1 triggers on high level.
[9:8]	11	IRQ3SRC[1:0]	External IRQ3 triggers on falling edge.
	10		External IRQ3 triggers on rising edge.
	01		External IRQ3 triggers on low level.
	00		External IRQ3 triggers on high level.

HARDWARE DESIGN CONSIDERATIONS

POWER SUPPLIES

The ADuC7124/ADuC7126 operational power supply voltage range is 2.7 V to 3.6 V. Separate analog and digital power supply pins (AV_{DD} and IOV_{DD}, respectively) allow AV_{DD} to be kept relatively free of noisy digital signals often present on the system IOV_{DD} line. In this mode, the part can also operate with split supplies; that is, it can use different voltage levels for each supply. For example, the system can be designed to operate with an IOV_{DD} voltage level of 3.3 V while the AV_{DD} level can be at 3 V or vice versa. A typical split supply configuration is shown in Figure 62.

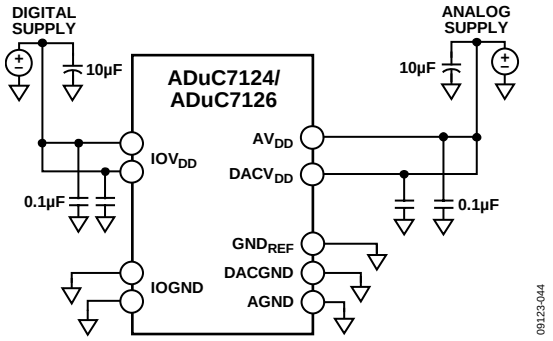

Figure 62. External Dual Supply Connections

As an alternative to providing two separate power supplies, the user can reduce noise on AV_{DD} by placing a small series resistor and/or ferrite bead between AV_{DD} and IOV_{DD} and then decoupling AV_{DD} separately to ground. An example of this configuration is shown in Figure 63. With this configuration, other analog circuitry (such as op amps, voltage reference, or any other analog circuitry) can be powered from the AV_{DD} supply line as well.

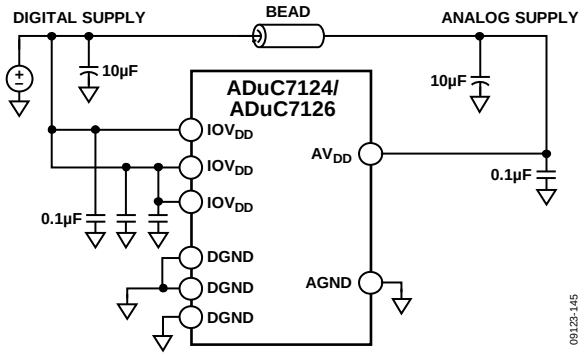

Figure 63. External Single Supply Connections

Notice that in both Figure 62 and Figure 63, a large value (10 µF) reservoir capacitor sits on IOV_{DD}, and a separate 10 µF capacitor sits on AV_{DD}. In addition, local small-value (0.1 µF) capacitors are located at each AV_{DD} and IOV_{DD} pin of the chip. As per standard design practice, be sure to include all of these capacitors and ensure that the smaller capacitors are close to each AV_{DD} pin with trace lengths as short as possible. Connect the ground terminal of each of these capacitors directly to the underlying ground plane.

Finally, note that the analog and digital ground pins on the ADuC7124/ADuC7126 must be referenced to the same system ground reference point at all times.

IOV_{DD} Supply Sensitivity

The IOV_{DD} supply is sensitive to high frequency noise because it is the supply source for the internal oscillator and PLL circuits. When the internal PLL loses lock, the clock source is removed by a gating circuit from the CPU, and the ARM7TDMI core stops executing code until the PLL regains lock. This feature ensures that no flash interface timings or ARM7TDMI timings are violated.

Typically, frequency noise greater than 50 kHz and 50 mV p-p on top of the supply causes the core to stop working.

If decoupling values recommended in the Power Supplies section do not sufficiently dampen all noise sources below 50 mV on IOV_{DD}, a filter such as the one shown in Figure 64 is recommended.

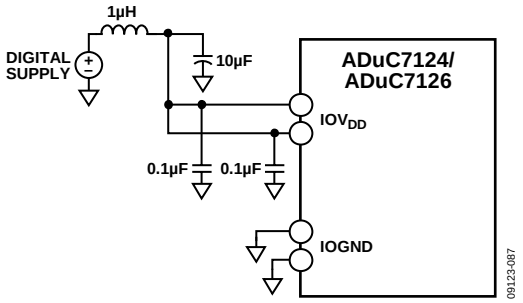

Figure 64. Recommended IOV_{DD} Supply Filter

Linear Voltage Regulator

The ADuC7124/ADuC7126 require a single 3.3 V supply, but the core logic requires a 2.6 V supply. An on-chip linear regulator generates the 2.6 V from IOV_{DD} for the core logic. The LV_{DD} pin is the 2.6 V supply for the core logic. An external compensation capacitor of 0.47 µF must be connected between LV_{DD} and DGND (as close as possible to these pins) to act as a tank of charge as shown in Figure 65.

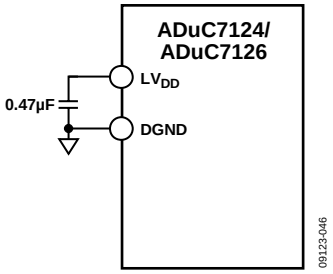

Figure 65. Voltage Regulator Connections

The LV_{DD} pin should not be used for any other chip. It is also recommended to use excellent power supply decoupling on IOV_{DD} to help improve line regulation performance of the on-chip voltage regulator.

GROUNDING AND BOARD LAYOUT RECOMMENDATIONS

As with all high resolution data converters, special attention must be paid to grounding and PC board layout of the ADuC7124/ADuC7126-based designs to achieve optimum performance from the ADCs and DAC.

Although the part has separate pins for analog and digital ground (AGND and IOGND), the user must not tie these to two separate ground planes unless the two ground planes are connected very close to the part. This is illustrated in the simplified example shown in Figure 66a. In systems where digital and analog ground planes are connected together somewhere else (at the power supply of the system, for example), the planes cannot be reconnected near the part because a ground loop results. In these cases, tie all the ADuC7124/ADuC7126 AGND and IOGND pins to the analog ground plane, as illustrated in Figure 66b. In systems with only one ground plane, ensure that the digital and analog components are physically separated onto separate halves of the board so that digital return currents do not flow near analog circuitry (and vice versa).

The ADuC7124/ADuC7126 can then be placed between the digital and analog sections, as illustrated in Figure 66c.

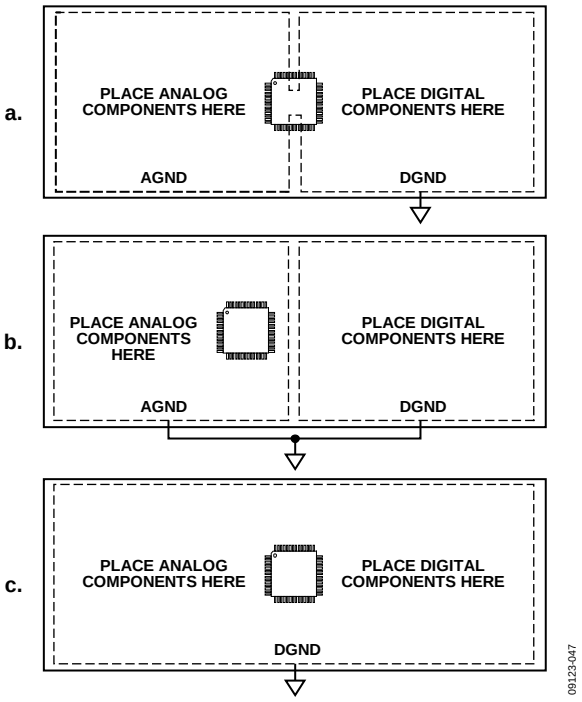

Figure 66. System Grounding Schemes

In all of these scenarios, and in more complicated real-life applications, the users should pay particular attention to the flow of current from the supplies and back to ground. Make sure the return paths for all currents are as close as possible to the paths the currents took to reach their destinations.

For example, do not power components on the analog side (as seen in Figure 66b) with IOV_{DD} because that forces return currents from IOV_{DD} to flow through AGND. Avoid digital currents flowing under analog circuitry, which can occur if a noisy digital chip is placed on the left half of the board (shown in Figure 66c). If possible, avoid large discontinuities in the ground plane(s), such as those formed by a long trace on the same layer, because they force return signals to travel a longer path. In addition, make all connections to the ground plane directly, with little or no trace separating the pin from its via to ground.

When connecting fast logic signals (rise/fall time < 5 ns) to any of the ADuC7124/ADuC7126 digital inputs, add a series resistor to each relevant line to keep rise and fall times longer than 5 ns at the input pins of the part. A value of 100 Ω or 200 Ω is usually sufficient to prevent high speed signals from coupling capacitively into the part and affecting the accuracy of ADC conversions.

CLOCK OSCILLATOR

The clock source for the ADuC7124/ADuC7126 can be generated by the internal PLL or by an external clock input. To use the internal PLL, connect a 32.768 kHz parallel resonant crystal between XCLKI and XCLKO, and connect a capacitor from each pin to ground as shown in Figure 67. The crystal allows the PLL to lock correctly to give a frequency of 41.78 MHz. If no external crystal is present, the internal oscillator is used to give a typical frequency of 32.768 kHz ± 3%.

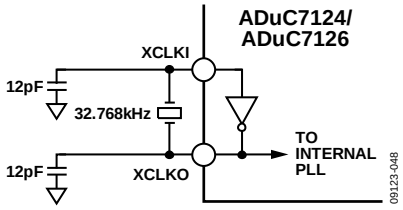

Figure 67. External Parallel Resonant Crystal Connections

To use an external source clock input instead of the PLL (see Figure 68), Bit 1 and Bit 0 of PLLCON must be modified. The external clock uses P0.7 and XCLK.

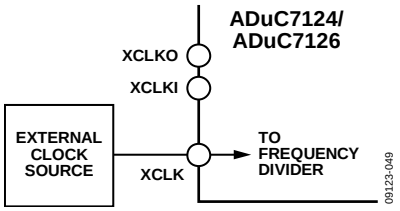

Figure 68. Connecting an External Clock Source

Using an external clock source, the ADuC7124/ADuC7126 specified operational clock speed range is 50 kHz to 41.78 MHz ± 1%, which ensures correct operation of the analog peripherals and Flash/EE.

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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