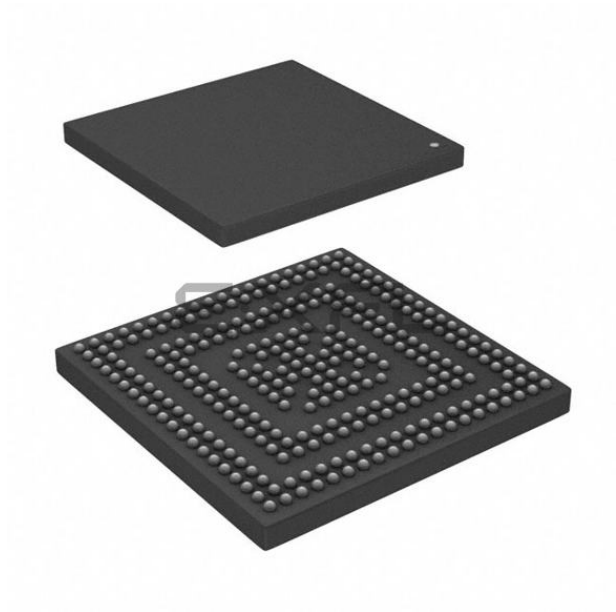
Infineon Technologies - TC1791F512F240EPABKXUMA2 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	TriCore™
Core Size	32-Bit Single-Core
Speed	240MHz
Connectivity	ASC, CANbus, FlexRay, MLI, MSC, SSC
Peripherals	DMA, POR, WDT
Number of I/O	128
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	192K x 8
RAM Size	288K x 8
Voltage - Supply (Vcc/Vdd)	1.17V ~ 3.63V
Data Converters	A/D 8x10b, 44x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	292-LFBGA
Supplier Device Package	PG-LFBGA-292-6
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tc1791f512f240epabkxuma2

2 System Overview of the TC1791

The TC1791 combines three powerful technologies within one silicon die, achieving new levels of power, speed, and economy for embedded applications:

- Reduced Instruction Set Computing (RISC) processor architecture
- Digital Signal Processing (DSP) operations and addressing modes
- On-chip memories and peripherals

DSP operations and addressing modes provide the computational power necessary to efficiently analyze complex real-world signals. The RISC load/store architecture provides high computational bandwidth with low system cost. On-chip memory and peripherals are designed to support even the most demanding high-bandwidth real-time embedded control-systems tasks.

Additional high-level features of the TC1791 include:

- Efficient memory organization: instruction and data scratch memories, caches
- Serial communication interfaces – flexible synchronous and asynchronous modes
- Peripheral Control Processor – standalone data operations and interrupt servicing
- DMA Controller – DMA operations and interrupt servicing
- General-purpose timers
- High-performance on-chip buses
- On-chip debugging and emulation facilities
- Flexible interconnections to external components
- Flexible power-management

The TC1791 is a high-performance microcontroller with TriCore CPU, program and data memories, buses, bus arbitration, an interrupt controller, a peripheral control processor and a DMA controller and several on-chip peripherals. The TC1791 is designed to meet the needs of the most demanding embedded control systems applications where the competing issues of price/performance, real-time responsiveness, computational power, data bandwidth, and power consumption are key design elements.

The TC1791 offers several versatile on-chip peripheral units such as serial controllers, timer units, and Analog-to-Digital converters. Within the TC1791, all these peripheral units are connected to the TriCore CPU/system via the Flexible Peripheral Interconnect (FPI) Bus and the Cross Bar Interconnect (SRI). Several I/O lines on the TC1791 ports are reserved for these peripheral units to communicate with the external world.

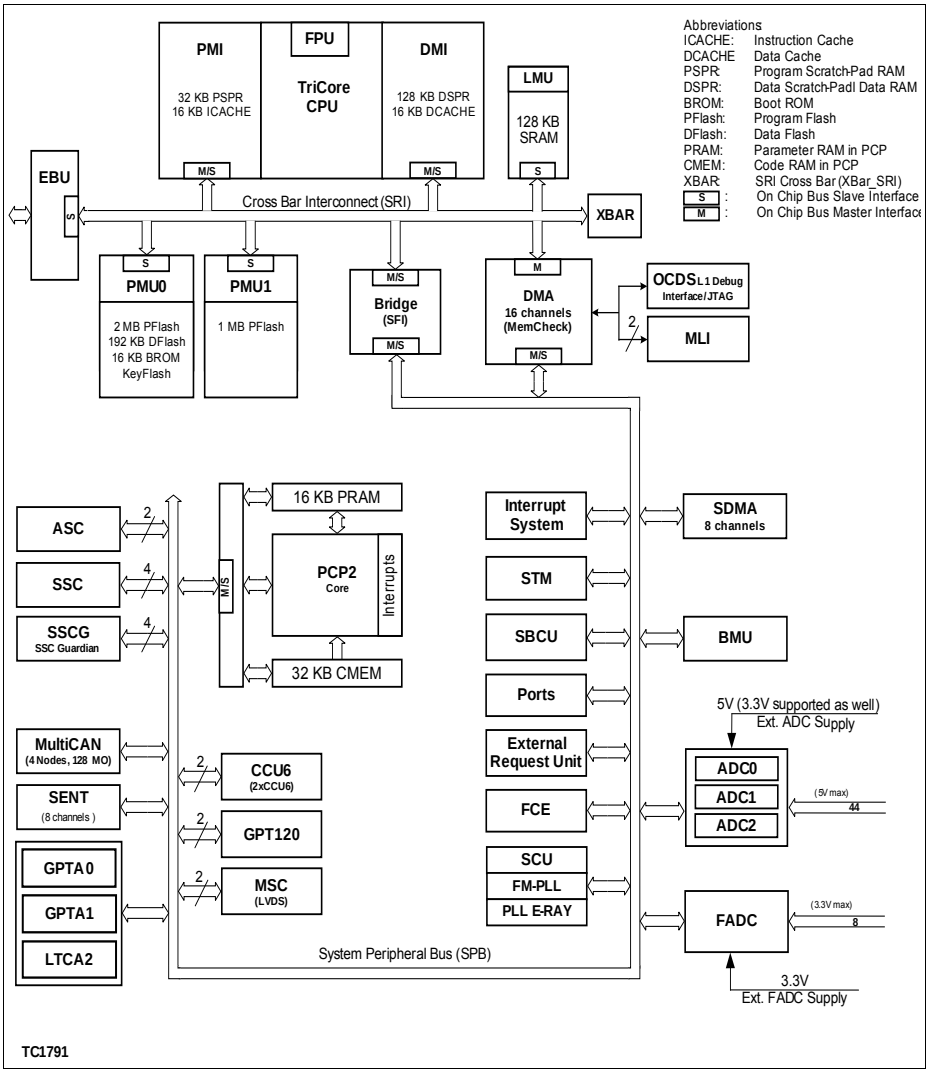

Figure 5 Block Diagram

Table 2 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
G1	P1.7	I/O	A2/ PU	**Port 1 General Purpose I/O Line 7**
	CC61INB	I		**CCU60**
	CC61INA	I		**CCU61**
	TData0	O1		**MLI0 transmit Channel Data Output**
	CC61	O2		**CCU61**
	T3OUT	O3		**GPT120**
G5	P1.9	I/O	A2/ PU	**Port 1 General Purpose I/O Line 9**
	RREADY0A	O1		**MLI0 Receive Channel ready Output A**
	SLSO11	O2		**SSC1 Slave Select Output Line 11**
	OUT65	O3		**OUT65 Line of GPTA0**
H2	P1.12	I/O	A2/ PU	**Port 1 General Purpose I/O Line 12**
	EXTCLK0	O1		**External Clock Output 0**
	OUT68	O2		**OUT68 Line of GPTA0**
	OUT68	O3		**OUT68 Line of GPTA1**
Port 2				
A6	P2.2	I/O	A1+/ PU	**Port 2 General Purpose I/O Line 2**
	SLSO02	O1		**SSC0 Slave Select Output Line 2**
	SLSO12	O2		**SSC1 Slave Select Output Line 12**
	SLSO02 AND SLSO12	O3		**SSC0 & SSC1 Slave Select Output Line 2 AND Slave Select Output Line 12**
B6	P2.3	I/O	A1+/ PU	**Port 2 General Purpose I/O Line 3**
	SLSO03	O1		**SSC0 Slave Select Output Line 3**
	SLSO13	O2		**SSC1 Slave Select Output Line 13**
	SLSO03 AND SLSO13	O3		**SSC0 & SSC1 Slave Select Output Line 3 AND Slave Select Output Line 13**

Table 2 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
U13	P4.5	I/O	A1+/ PU	**Port 4 General Purpose I/O Line 5**
	IN29	I		**IN29 Line of GPTA0**
	IN29	I		**IN29 Line of GPTA1**
	IN29	I		**IN29 Line of LTCA2**
	OUT29	O1		**OUT29 Line of GPTA0**
	OUT29	O2		**OUT29 Line of GPTA1**
	SLSO22	O3		**SSC2 Output**
W13	P4.6	I/O	A1+/ PU	**Port 4 General Purpose I/O Line 6**
	IN30	I		**IN30 Line of GPTA0**
	IN30	I		**IN30 Line of GPTA1**
	IN30	I		**IN30 Line of LTCA2**
	OUT30	O1		**OUT30 Line of GPTA0**
	OUT30	O2		**OUT30 Line of GPTA1**
	SLSO23	O3		**SSC2 Output**
Y13	P4.7	I/O	A1+/ PU	**Port 4 General Purpose I/O Line 7**
	IN31	I		**IN31 Line of GPTA0**
	IN31	I		**IN31 Line of GPTA1**
	IN31	I		**IN31Line of LTCA2**
	T6INB	I		**GPT120**
	T6INA	I		**GPT121**
	OUT31	O1		**OUT31 Line of GPTA0**
	OUT31	O2		**OUT31 Line of GPTA1**
	SLSO24	O3		**SSC2 Output**

Table 2 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
W14	P4.10	I/O	A1/ PU	**Port 4 General Purpose I/O Line 10**
	IN34	I		**IN34 Line of GPTA0**
	IN34	I		**IN34 Line of GPTA1**
	T12HRB	I		**CCU60**
	CCPOS0A	I		**CCU61**
	T2INA	I		**GPT120**
	T2INB	I		**GPT121**
	OUT34	O1		**OUT34 Line of GPTA0**
	OUT34	O2		**OUT34 Line of GPTA1**
	OUT2	O3		**OUT2 Line of LTCA2**
T15	P4.12	I/O	A1/ PU	**Port 4 General Purpose I/O Line 12**
	IN36	I		**IN36 Line of GPTA0**
	IN36	I		**IN36 Line of GPTA1**
	T13HRB	I		**CCU60**
	CCPOS1A	I		**CCU61**
	T2EUDA	I		**GPT120**
	T2EUDB	I		**GPT121**
	OUT36	O1		**OUT36 Line of GPTA0**
	OUT36	O2		**OUT36 Line of GPTA1**
	OUT4	O3		**OUT4 Line of LTCA2**

Table 2 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
B16	P5.8	I/O	F/ PU	**Port 5 General Purpose I/O Line 8**
	CC62INA	I		**CCU62**
	CC62INB	I		**CCU63**
	SON0	O1		**MSC0 Differential Driver Serial Data Output Negative**
	OUT80	O2		**OUT80 Line of GPTA0**
	CC62	O3		**CCU62**
B17	P5.9	I/O	F/ PU	**Port 5 General Purpose I/O Line 9**
	SOP0A	O1		**MSC0 Differential Driver Serial Data Output Positive A**
	OUT81	O2		**OUT81 Line of GPTA0**
	COUT60	O3		**CCU62**
A16	P5.10	I/O	F/ PU	**Port 5 General Purpose I/O Line 10**
	FCLN0	O1		**MSC0 Differential Driver Clock Output Negative**
	OUT82	O2		**OUT82 Line of GPTA0**
	COUT61	O3		**CCU62**
A17	P5.11	I/O	F/ PU	**Port 5 General Purpose I/O Line 11**
	FCLP0A	O1		**MSC0 Differential Driver Clock Output Positive A**
	OUT83	O2		**OUT83 Line of GPTA0**
	COUT62	O3		**CCU62**
D14	P5.12	I/O	F/ PU	**Port 5 General Purpose I/O Line 12**
	SON1	O1		**MSC1 Differential Driver Serial Data Output Negative**
	OUT84	O2		**OUT84 Line of GPTA0**
	OUT84	O3		**OUT84 Line of GPTA1**

Table 2 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
F2	P8.4	I/O	A1/ PU	**Port 8 General Purpose I/O Line 4**
	IN44	I		**IN44 Line of GPTA0**
	IN44	I		**IN44 Line of GPTA1**
	RCLK1A	I		**MLI1 Receive Channel Clock Input A**
	SENT4	I		**SENT Digital Input**
	CC62INB	I		**CCU60**
	CC62INA	I		**CCU61**
	OUT44	O1		**OUT44 Line of GPTA0**
	CC62	O2		**CCU61**
	T3OUT	O3		**GPT121**
F5	P8.5	I/O	A2/ PU	**Port 8 General Purpose I/O Line 5**
	IN45	I		**IN45 Line of GPTA0**
	IN45	I		**IN45 Line of GPTA1**
	SENT5	I		**SENT Digital Input**
	CTRAPA	I		**CCU60**
	CTRAPB	I		**CCU62**
	CC60INC	I		**CCU60**
	T12HRE	I		**CCU61**
	CC61INC	I		**CCU61**
	OUT45	O1		**OUT45 Line of GPTA0**
	OUT45	O2		**OUT45 Line of GPTA1**
	RREADY1A	O3		**MLI1 Receive Channel ready Output A**

Table 2 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
T19	P13.13	I/O	A2/ PU	**Port 13 General Purpose I/O Line 13**
	OUT101	O1		**OUT101 Line of GPTA0**
	OUT101	O2		**OUT101 Line of GPTA1**
	OUT93	O3		**OUT93 Line of LTCA2**
T20	P13.14	I/O	A2/ PU	**Port 13 General Purpose I/O Line 14**
	OUT102	O1		**OUT102 Line of GPTA0**
	OUT102	O2		**OUT102 Line of GPTA1**
	OUT94	O3		**OUT94 Line of LTCA2**
U19	P13.15	I/O	A2/ PU	**Port 13 General Purpose I/O Line 15**
	OUT103	O1		**OUT103 Line of GPTA0**
	OUT103	O2		**OUT103 Line of GPTA1**
	OUT95	O3		**OUT95 Line of LTCA2**
Port 14				
U20	P14.0	I/O	A2/ PU	**Port 14 General Purpose I/O Line 0**
	CC60	O1		**CCU60**
	OUT96	O2		**OUT96 Line of GPTA1**
	OUT96	O3		**OUT96 Line of LTCA2**
V20	P14.2	I/O	A2/ PU	**Port 14 General Purpose I/O Line 2**
	CC62	O1		**CCU60**
	OUT98	O2		**OUT98 Line of GPTA1**
	OUT98	O3		**OUT98 Line of LTCA2**
W18	P14.4	I/O	A2/ PU	**Port 14 General Purpose I/O Line 4**
	COUT61	O1		**CCU60**
	OUT100	O2		**OUT100 Line of GPTA1**
	OUT100	O3		**OUT100 Line of LTCA2**

Table 2 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
K5, L16	V_{DDFL3}	-	-	**Flash Power Supply (3.3V)**
J20	V_{SSOSC}	-	-	**Oscillator Ground (Main & E-Ray)**
	V_{SSOSC3}	-	-	**Oscillator Ground (Main & E-Ray)**
J19	V_{DDOSC}	-	-	**Main Oscillator Power Supply (1.3V)**
K16	V_{DDOSC3}	-	-	**Main Oscillator Power Supply (3.3V)**
K17	V_{DDPF}	-	-	**E-Ray PLL Power Supply (1.3V)**
L17	V_{DDPF3}	-	-	**E-Ray PLL Power Supply (3.3V)**
G8, G13, H7, H14, N7, N14, P8, P13, R16, T17, V19, W20	V_{DD}	-	-	**Digital Core Power Supply (1.3V)**
A2, A19, B3, B10, B18, K2, M19, M20, W11, W17	V_{DDP}	-	-	**Port Power Supply (3.3V)**
L4, L5	V_{DDSB}	-	-	**Emulation Stand-by SRAM Power Supply (1.3V) (Emulation device only)** *Note: This pin is N.C. in a productive device.*

4) Voltage overshoot to 6.5V is permissible at Power-Up and $\overline{\text{PORST}}$ low, provided the pulse duration is less than 100 µs and the cumulated sum of the pulses does not exceed 1 h.
5) Voltage overshoot to 4.0V is permissible at Power-Up and $\overline{\text{PORST}}$ low, provided the pulse duration is less than 100 µs and the cumulated sum of the pulses does not exceed 1 h.
6) This parameter is valid under the assumption the $\overline{\text{PORST}}$ signal is constantly at low level during the power-up/power-down of V_{DDP}.

5.1.5.1 Extended Range Operating Conditions

The following extended operating conditions are defined:

- $1.3V + 5\% < V_{DD} / V_{DDOSC} / V_{DDPF} / V_{DDAF} < 1.3V + 7.5\%$ (overvoltage condition):
  – limited to 10000 hour duration cumulative in lifetime, due to the reliability reduction of the chip caused by the overvoltage stress.
- $1.3V + 7.5\% < V_{DD} / V_{DDOSC} / V_{DDPF} / V_{DDAF} < 1.3V + 10\%$ (overvoltage condition):
  – limited to 1000 hours duration cumulative in lifetime, due to the reliability reduction of the chip caused by the overvoltage stress.
- $3.3V + 5\% < V_{DDP} / V_{DDOSC3} / V_{DDPF3} / V_{DDFL3} / V_{DDMF} < 3.3V + 10\%$ (overvoltage condition):
  limited to 1000 hours duration cumulative in lifetime, due to the reliability reduction of the chip caused by the overvoltage stress.

Table 18 Pin Groups for Overload / Short-Circuit Current Sum Parameter

Group	Pins
1	P2.[4:2], P6.[6:9]
2	P6.[5:4], P6.[11:10]
3	P6.[15:12]
4	P8.[5:0]
5	P8.[7:6]
6	P1.7, P1.9
7	P1.6, P1.12
8	P1.[1:0], P7.[2:0]
9	P7.[5:3]
10	P4.[6:0]
11	P4.[10:7]
12	P4.12, P4.14
13	P10.[5:0]
14	P14.8

Table 22 Standard_Pads Class_A2

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Hysteresis for A2 pads [1]	$HYSA2$ CC	0.1 x V_{DDP}	–	–	V	
Input Leakage current Class A2	I_{OZA2} CC	-6000	–	6000	nA	$V_i < V_{DDP}$ / 2 - 1 V; $V_i > V_{DDP}$ / 2 + 1 V; $V_i \geq 0$ V; $V_i \leq V_{DDP}$ V
		-3000	–	3000	nA	$V_i > V_{DDP}$ / 2 - 1 V; $V_i < V_{DDP}$ / 2 + 1 V
Ratio Vil/Vih, A2 pads	V_{ILA2} / V_{IHA2} CC	0.6	–	–		
On-Resistance of the class A2 pad, weak driver	R_{DSONW} CC	–	450	600	Ohm	$I_{OH} > -0.5$ mA; P_MOS
		–	210	340	Ohm	$I_{OL} < 0.5$ mA; N_MOS
On-Resistance of the class A2 pad, medium driver	R_{DSONM} CC	–	–	155	Ohm	$I_{OH} > -2$ mA; P_MOS
		–	–	110	Ohm	$I_{OL} < 2$ mA; N_MOS
On-Resistance of the class A2 pad, strong driver	R_{DSON2} CC	–	–	28	Ohm	$I_{OH} > -2$ mA; P_MOS
		–	–	22	Ohm	$I_{OL} < 2$ mA; N_MOS

Table 26 LVDS_Pads Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise time, pad type LVDS	t_{RL} CC	–	–	2	ns	termination 100 Ω ± 1 %; differential capacitance = 10 pF; input capacitance = 20 pF
Pad set-up time	t_{SET_LVDS} CC	–	–	13	µs	termination 100 Ω ± 1 %
Output Differential Voltage	V_{OD} CC	150	–	400	mV	termination 100 Ω ± 1 %
Output voltage high, pad class F, LVDS mode	V_{OH} CC	–	–	1525	mV	termination 100 Ω ± 1 %
Output voltage low, pad class F, LVDS mode	V_{OL} CC	875	–	–	mV	termination 100 Ω ± 1 %
Output Offset Voltage	V_{OS} CC	1075	–	1325	mV	termination 100 Ω ± 1 %

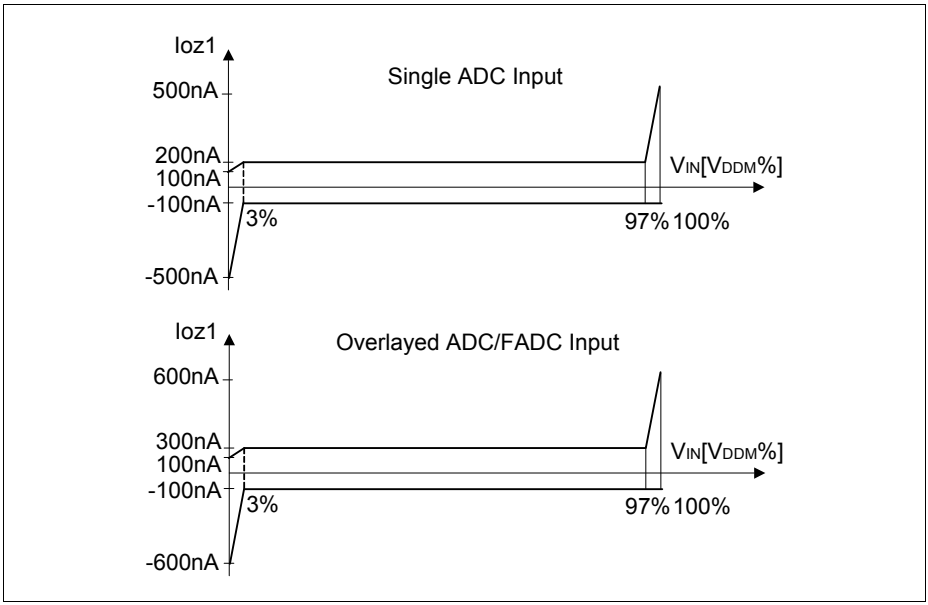

Figure 9 ADCx Analog Inputs Leakage

5.2.3 Fast Analog to Digital Converter (FADC)

FADC parameter are vaild for $V_{DD\,/\,DDAF}$ = 1.235 V to 1.365 V; V_{DDMF} = 2.97 V to 3.6 V.

Table 29 FADC Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current at VFAREF	I_{FAREF} CC	–	–	120	µA	
Input leakage current at VFAREF[1)]	I_{FOZ2} CC	-500	–	500	nA	$V_{FAREF} \leq V_{DDMF}$ V; $V_{FAREF} \geq 0$ V
Input leakage current at VFAGND	I_{FOZ3} CC	-500	–	500	nA	
DNL error	EF_{DNL} CC	-1	–	1	LSB	V_{IN} mode= differential; Gain = 1 or 2
		-2	–	2	LSB	V_{IN} mode= differential; Gain = 4 or 8[2)]
		-1	–	1	LSB	V_{IN} mode= single ended; Gain = 1 or 2
		-2	–	2	LSB	V_{IN} mode= single ended; Gain = 4 or 8[2)]
GRADient error	EF_{GRAD} CC	-5	–	5	%	V_{IN} mode= differential ; Gain≤ 4
		-5	–	5	%	V_{IN} mode= single ended ; Gain≤ 4
		-6	–	6	%	V_{IN} mode= differential ; Gain= 8
		-6	–	6	%	V_{IN} mode= single ended ; Gain= 8

Table 29 FADC Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Analog reference ground	V_{FAGND} SR	V_{SSAF} - 0.05	–	V_{SSAF} + 0.05	V	
Analog reference voltage	V_{FAREF} SR	2.97	–	3.63[5] [6]	V	

1) This value applies in power-down mode.

2) No missing codes.

3) Calibration should be preformed at each power-up. In case of a continous operation, it should be performed minimium once per week.

4) The offser error voltage drifts over the whole temperature range maximum +-3LSB.

5) Voltage overshoot to 4V is permissible, provided the pulse duration is less than 100 µs and the cumulated sum of the pulses does not exceed 1 h.

6) A running conversion may become inexact in case of violating the nomal operating conditions (voltage overshoots).

The calibration procedure should run after each power-up, when all power supply voltages and the reference voltage have stabilized.

5.3 AC Parameters

All AC parameters are defined with maximum driver strength unless otherwise noted.

5.3.1 Testing Waveforms

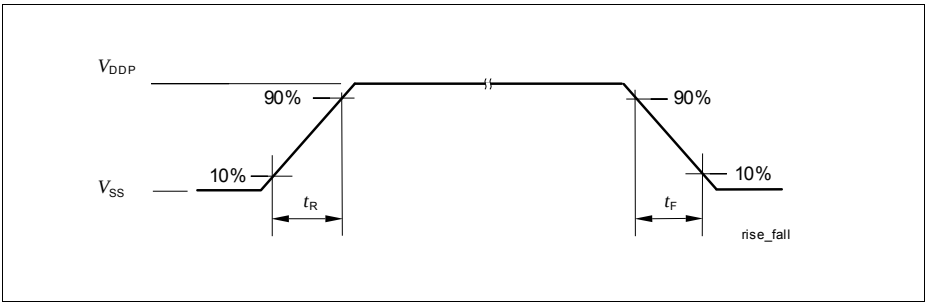

Figure 11 Rise/Fall Time Parameters

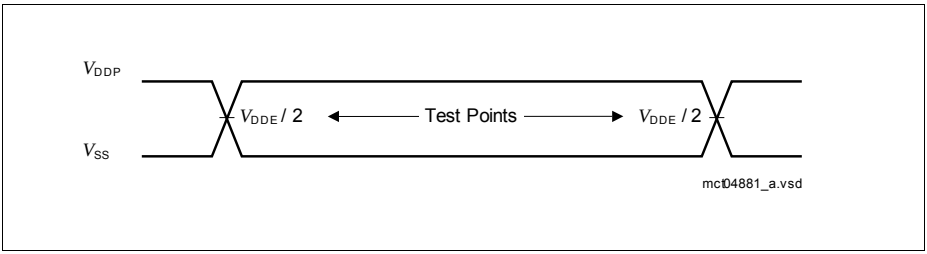

Figure 12 Testing Waveform, Output Delay

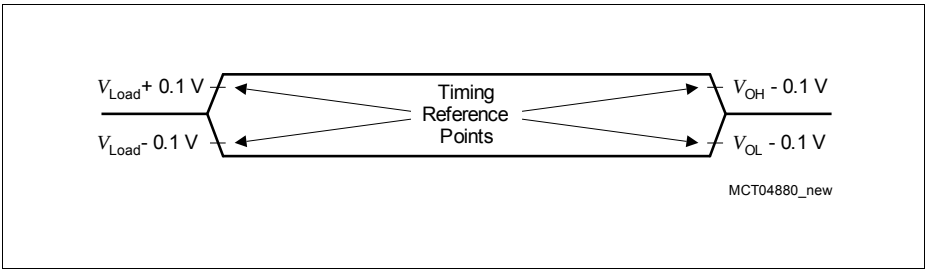

Figure 13 Testing Waveform, Output High Impedance

Table 38 MLI Receiver

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RCLK clock period	t_{20} SR	1 / f_{FPI}	–	–	ns	
RCLK high time[1)2)]	t_{21} SR	–	0.5 x t_{20}	–	ns	
RCLK low time[1)2)]	t_{22} SR	–	0.5 x t_{20}	–	ns	
RCLK rise time[3)]	t_{23} SR	–	–	4	ns	
RCLK fall time[3)]	t_{24} SR	–	–	4	ns	
RDATA/RVALID setup time before RCLK falling edge	t_{25} SR	4.2	–	–	ns	
RDATA/RVALID hold time after RCLK falling edge	t_{26} SR	2.2	–	–	ns	
RREADY output delay time	t_{27} SR	0	–	16	ns	

1) The following formula is valid: t21 + t22 = t20.

2) Min and Max values for this parameter can be derived from the typ. value by considering the other receiver timing parameters.

3) The RCLK max. input rise/fall times are best case parameters for fSYS = 90 MHz. For reduction of EMI, slower input signal rise/fall times can be used for longer RCLK clock periods.

Table 39 MLI Transmitter

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCLK clock period	t_{10} CC	2 x 1 / f_{FPI}	–	–	ns	
TCLK high time[1)2)]	t_{11} CC	0.45 x t_{10}	0.5 x t_{10}	0.55 x t_{10}	ns	
TCLK low time[1)2)]	t_{12} CC	0.45 x t_{10}	0.5 x t_{10}	0.55 x t_{10}	ns	
TCLK rise time	t_{13} CC	–	–	0.3 x t_{10}[3)]	ns	
TCLK fall time	t_{14} CC	–	–	0.3 x t_{10}[3)]	ns	

5.5.2 Package Outline

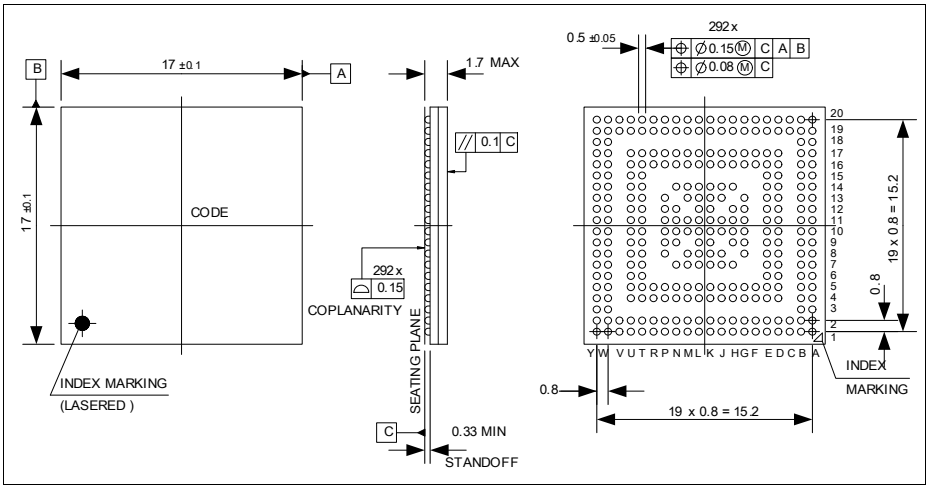

Figure 26 Package Outlines PG-LFBGA- 292-6

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: ***http://www.infineon.com/products***.

5.5.3 Quality Declarations

Table 45 Quality Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Operation Lifetime[1)]	t_{OP}	–	–	24000	hours	–[2)]
ESD susceptibility according to Human Body Model (HBM)	V_{HBM}	–	–	2000	V	Conforming to JESD22-A114-B
ESD susceptibility of the LVDS pins	V_{HBM1}	–	–	500	V	–

- removed RDSON parameters for class F pads weak driver as only medium is available
- add parameter f_{SYSD} for the SYSPLL
- update all current values of table 28 (Power Supply Parameters)
- rework the 3.3 V current part of the Power Supply Parameters for better description and usage
  - Parameters I_{DDP_FP}, I_{DDFL3E} and I_{DDFL3R} are removed and replaced in the following way
  - I_{DDP_FP} is replaced by I_{DDP} with the condition including flash programming current
  - I_{DDFL3E} is replaced by I_{DDP} with the condition including flash erase verify current
  - I_{DDFL3R} is replaced by I_{DDP} with the condition including flash read current
  - parameter I_{DDFL3R} was renamed to I_{DDFL3}

The rework of the 3.3 V current part of the Power Supply Parameters was done for simplification and clarification. Former given values could still be used if liked, the new definition results in the same resulting values or slightly better values. The flash module is supplied via I_{DDFL3} and I_{DDP}. For the different flash operating modes in worst case different allocations for the two domains resulting.

The application typical case ‘flash read’ has max I_{DDP} of 25 mA and max I_{DDFL3} of 98 mA resulting is a sum of 123 mA.

The case ‘flash programming’ has max I_{DDP} of 55 mA and max I_{DDFL3} of 29 mA resulting is a sum of 84 mA.

The case ‘flash erase verify’ has max I_{DDP} of 40 mA and max I_{DDFL3} of 98 mA resulting is a sum of 138 mA.

So for the old parameter I_{DDP} with 35 mA, the new version reads as I_{DDP} = 25+I_{DDP_PORST} = 32 mA for the same application relevant case.

The following changes where done between Version 0.7 and 1.0 of this document:

- add product options **SAK-TC1791S-512F240EP, SAK-TC1791S-384F200EP, and SAK-TC1791N-384F200EP**
- update block diagrams to cover new options
- add note to TC1791 Logic Symbol figure and pin list for E-RAY pins availability
- add identification registers for new options
- adapt Absolute Maximum Rating
- clarify pad supply levels in Pin Reliability in Overload section
- correct errors for analog inputs in tables 12 and 13
- add note at the end of Pin Reliability in Overload section
- clarify wording for valid operating conditions
- add negative limit for class S pad leakage
- change description of parameter t_{CAL} for the ADC
- update footnote 10 for the ADC
- split FADC DNL parameter into two conditions and change value for gain 4 and 8
- add footnote 5 to I_{DDP}