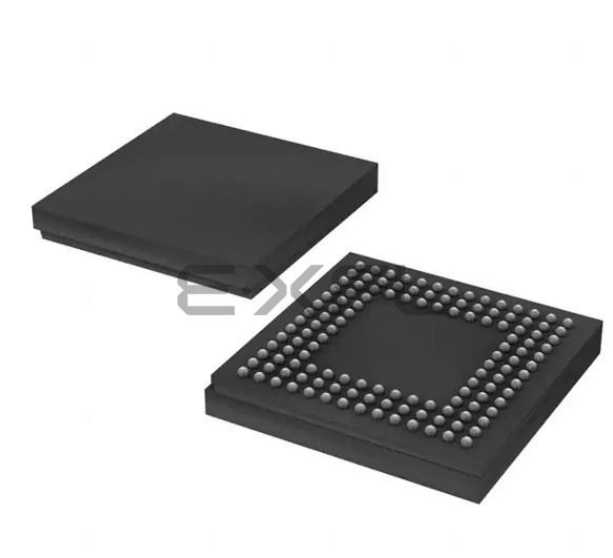

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 240 |
| Number of Logic Elements/Cells | 2160 |
| Total RAM Bits | 73728 |
| Number of I/O | 83 |
| Number of Gates | 100000 |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 132-TFBGA, CSPBGA |
| Supplier Device Package | 132-CSPBGA (8x8) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc3s100e-4cpg132c |

## Architectural Overview

The Spartan-3E family architecture consists of five fundamental programmable functional elements:

- **Configurable Logic Blocks (CLBs)** contain flexible Look-Up Tables (LUTs) that implement logic plus storage elements used as flip-flops or latches. CLBs perform a wide variety of logical functions as well as store data.
- **Input/Output Blocks (IOBs)** control the flow of data between the I/O pins and the internal logic of the device. Each IOB supports bidirectional data flow plus 3-state operation. Supports a variety of signal standards, including four high-performance differential standards. Double Data-Rate (DDR) registers are included.
- **Block RAM** provides data storage in the form of 18-Kbit dual-port blocks.
- **Multiplier Blocks** accept two 18-bit binary numbers as inputs and calculate the product.
- **Digital Clock Manager (DCM) Blocks** provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase-shifting clock signals.

These elements are organized as shown in Figure 1. A ring of IOBs surrounds a regular array of CLBs. Each device has two columns of block RAM except for the XC3S100E, which has one column. Each RAM column consists of several 18-Kbit RAM blocks. Each block RAM is associated with a dedicated multiplier. The DCMs are positioned in the center with two at the top and two at the bottom of the device. The XC3S100E has only one DCM at the top and bottom, while the XC3S1200E and XC3S1600E add two DCMs in the middle of the left and right sides.

The Spartan-3E family features a rich network of traces that interconnect all five functional elements, transmitting signals among them. Each functional element has an associated switch matrix that permits multiple connections to the routing.

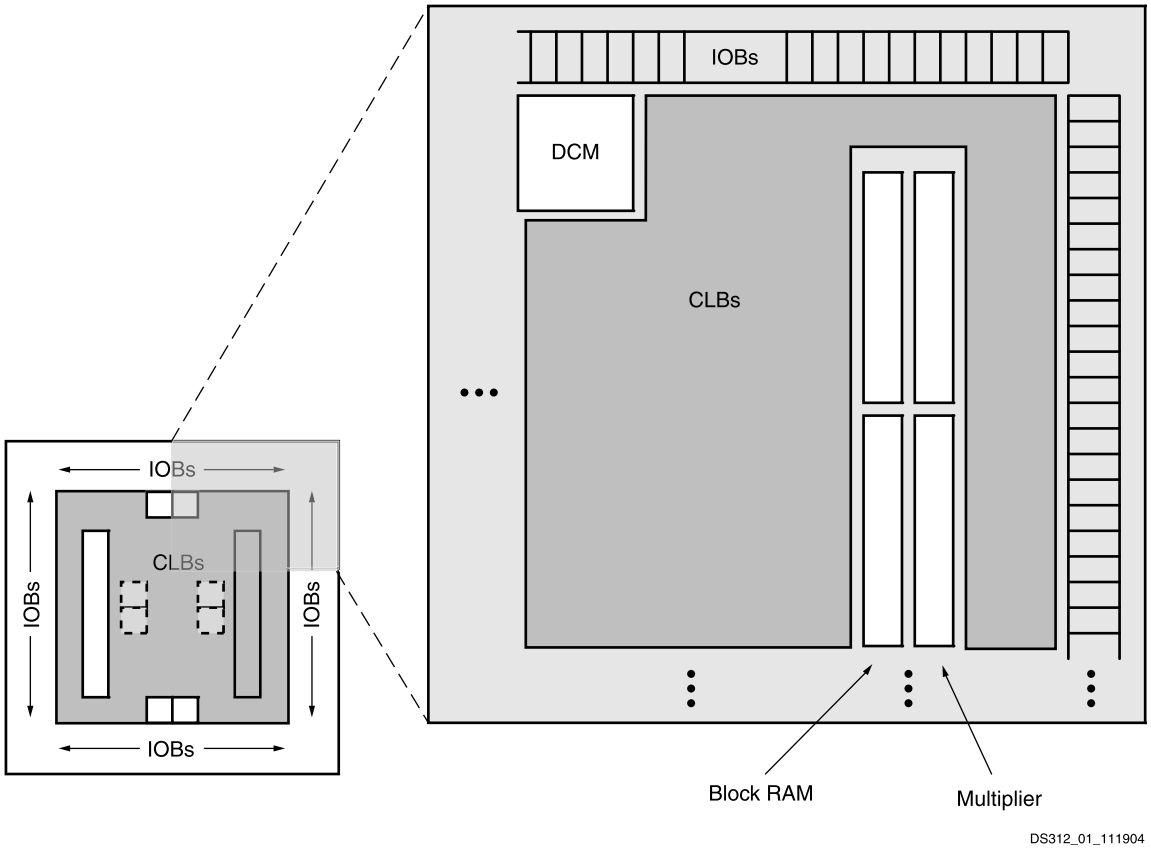


*Figure 1:* **Spartan-3E Family Architecture**

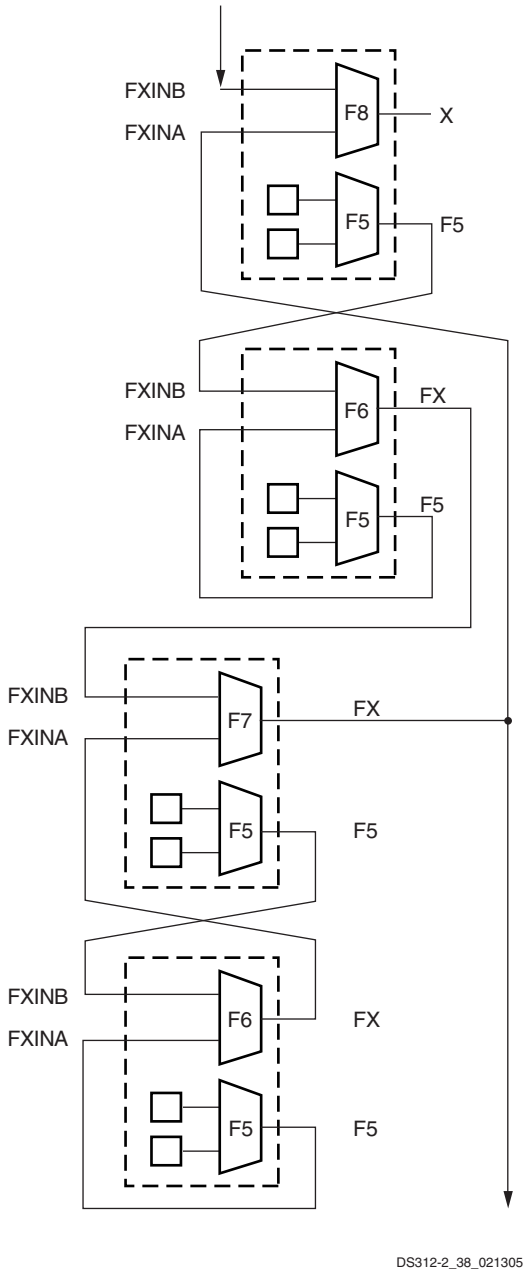


*Figure 20:* **MUXes and Dedicated Feedback in Spartan-3E CLB**

*Table 11:* **MUX Capabilities**

| MUX | Usage | Input Source | Total Number of Inputs per Function | | |
|---|---|---|---|---|---|
| | | | For Any Function | For MUX | For Limited Functions |
| F5MUX | F5MUX | LUTs | 5 | 6 (4:1 MUX) | 9 |
| FiMUX | F6MUX | F5MUX | 6 | 11 (8:1 MUX) | 19 |
| | F7MUX | F6MUX | 7 | 20 (16:1 MUX) | 39 |
| | F8MUX | F7MUX | 8 | 37 (32:1 MUX) | 79 |

## VARIABLE Phase Shift Mode

In VARIABLE phase shift mode, the FPGA application dynamically adjusts the fine phase shift value using three inputs to the PS unit (PSEN, PSCLK, and PSINCDEC), as defined in Table 36 and shown in Figure 40.

*Table 36:* **Signals for Variable Phase Mode**

| Signal | Direction | Description |
|---|---|---|
| PSEN(1) | Input | Enables the Phase Shift unit for variable phase adjustment. |
| PSCLK(1) | Input | Clock to synchronize phase shift adjustment. |
| PSINCDEC(1) | Input | When High, increments the current phase shift value. When Low, decrements the current phase shift value. This signal is synchronized to the PSCLK signal. |
| PSDONE | Output | Goes High to indicate that the present phase adjustment is complete and PS unit is ready for next phase adjustment request. This signal is synchronized to the PSCLK signal. |

**Notes:**

1. This input supports either a true or inverted polarity.

The FPGA application uses the three PS inputs on the Phase Shift unit to dynamically and incrementally increase or decrease the phase shift amount on all nine DCM clock outputs.

To adjust the current phase shift value, the PSEN enable signal must be High to enable the PS unit. Coincidently, PSINCDEC must be High to increment the current phase shift amount or Low to decrement the current amount. All VARIABLE phase shift operations are controlled by the PSCLK input, which can be the CLKIN signal or any other clock signal.

### *Design Note*

The VARIABLE phase shift feature operates differently from the Spartan-3 DCM; use the DCM_SP primitive, not the DCM primitive.

### *DCM_DELAY_STEP*

DCM_DELAY_STEP is the finest delay resolution available in the PS unit. Its value is provided at the bottom of Table 105 in Module 3. For each enabled PSCLK cycle that PSINCDEC is High, the PS unit adds one DCM_ DELAY_STEP of phase shift to all nine DCM outputs. Similarly, for each enabled PSCLK cycle that PSINCDEC is Low, the PS unit subtracts one DCM_ DELAY_STEP of phase shift from all nine DCM outputs.

Because each DCM_DELAY_STEP has a minimum and maximum value, the actual phase shift delay for the present phase increment/decrement value (VALUE) falls within the minimum and maximum values according to Equation 4 and Equation 5.

$$T_{PS}(Max) = VALUE \bullet \text{DCM\_DELAY\_STEP\_MAX} \quad Eq\ 4$$

$$T_{PS}(Min) = VALUE \bullet \text{DCM\_DELAY\_STEP\_MIN} \quad Eq\ 5$$

The maximum variable phase shift steps, MAX_STEPS, is described in Equation 6 or Equation 7, for a given CLKIN input period, $T_{CLKIN}$, in nanoseconds. To convert this to a phase shift range measured in time and not steps, use MAX_STEPS derived in Equation 6 and Equation 7 for VALUE in Equation 4 and Equation 5.

If CLKIN < 60 MHz:

$$\text{MAX\_STEPS} = \pm[INTEGER(10 \bullet (T_{CLKIN} - 3))] \quad Eq\ 6$$

If CLKIN ≥ 60 MHz:

$$\text{MAX\_STEPS} = \pm[INTEGER(15 \bullet (T_{CLKIN} - 3))] \quad Eq\ 7$$

The phase adjustment might require as many as 100 CLKIN cycles plus 3 PSCLK cycles to take effect, at which point the DCM's PSDONE output goes High for one PSCLK cycle. This pulse indicates that the PS unit completed the previous adjustment and is now ready for the next request.

Asserting the Reset (RST) input returns the phase shift to zero.

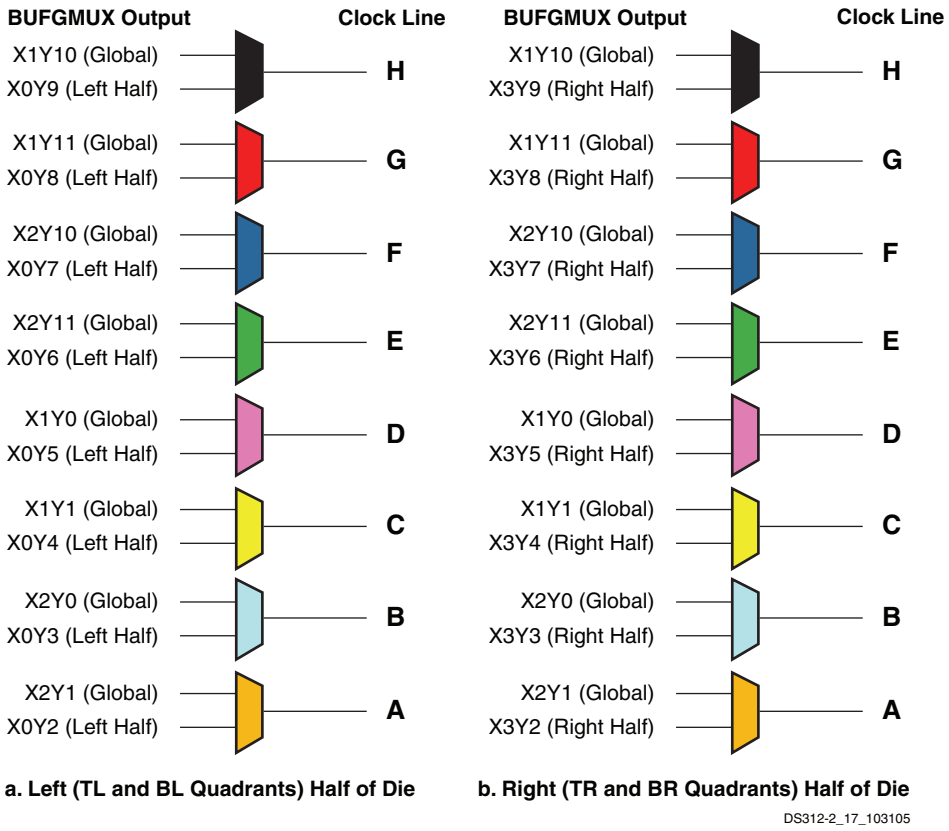


*Figure 47:* **Clock Sources for the Eight Clock Lines within a Clock Quadrant**

The outputs of the top or bottom BUFGMUX elements connect to two vertical spines, each comprising four vertical clock lines as shown in Figure 45. At the center of the die, these clock signals connect to the eight-line horizontal clock spine.

Outputs of the left and right BUFGMUX elements are routed onto the left or right horizontal spines, each comprising eight horizontal clock lines.

Each of the eight clock signals in a clock quadrant derives either from a global clock signal or a half clock signal. In other words, there are up to 24 total potential clock inputs to the FPGA, eight of which can connect to clocked elements in a single clock quadrant. Figure 47 shows how the clock lines in each quadrant are selected from associated BUFGMUX sources. For example, if quadrant clock ‘A’ in the bottom left (BL) quadrant originates from BUFGMUX_X2Y1, then the clock signal from BUFGMUX_X0Y2 is unavailable in the bottom left quadrant. However, the top left (TL) quadrant clock ‘A’ can still solely use the output from either BUFGMUX_X2Y1 or BUFGMUX_X0Y2 as the source.

To minimize the dynamic power dissipation of the clock network, the Xilinx development software automatically disables all clock segments not in use.

*Table 49:* **Pull-up or Pull-down Values for HSWAP, M[2:0], and VS[2:0]**

| HSWAP Value | I/O Pull-up Resistors during Configuration | Required Resistor Value to Define Logic Level on HSWAP, M[2:0], or VS[2:0] | |
|---|---|---|---|
| | | High | Low |
| 0 | Enabled | Pulled High via an internal pull-up resistor to the associated $V_{CCO}$ supply. No external pull-up resistor is necessary. | Pulled Low using an appropriately sized pull-down resistor to GND.<br>For a 2.5V or 3.3V interface: R ≤ 560Ω. For a 1.8V interface: R ≤ 1.1kΩ. |
| 1 | Disabled | Pulled High using a 3.3 to 4.7kΩ resistor to the associated $V_{CCO}$ supply. | Pulled Low using a 3.3 to 4.7kΩ resistor to GND. |

The logic level on HSWAP dictates how to define the logic levels on M[2:0] and VS[2:0], as shown in Table 49. If the application requires HSWAP to be High, the HSWAP pin is pulled High using an external 3.3kΩ to 4.7kΩ resistor to VCCO_0. If the application requires HSWAP to be Low during configuration, then HSWAP is either connected to GND or pulled Low using an appropriately sized external pull-down resistor to GND. When HSWAP is Low, its pin has an internal pull-up resistor to VCCO_0. The external pull-down resistor must be strong enough to define a logic Low on HSWAP for the I/O standard used during configuration. For 2.5V or 3.3V I/O, the pull-down resistor is 560Ω or lower. For 1.8V I/O, the pull-down resistor is 1.1kΩ or lower.

Once HSWAP is defined, use Table 49 to define the logic values for M[2:0] and VS[2:0].

Use the weakest external pull-up or pull-down resistor value allowed by the application. The resistor must be strong enough to define a logic Low or High during configuration. However, when driving the HSWAP, M[2:0], or VS[2:0] pins after configuration, the output driver must be strong enough to overcome the pull-up or pull-down resistor value and generate the appropriate logic levels. For example, to overcome a 560Ω pull-down resistor, a 3.3V FPGA I/O pin must use a 6 mA or stronger driver.

### Voltage Compatibility

Available SPI Flash PROMs use a single 3.3V supply voltage. All of the FPGA's SPI Flash interface signals are within I/O Bank 2. Consequently, the FPGA's VCCO_2 supply voltage must also be 3.3V to match the SPI Flash PROM.

### Power-On Precautions if 3.3V Supply is Last in Sequence

Spartan-3E FPGAs have a built-in power-on reset (POR) circuit, as shown in Figure 66, page 102. The FPGA waits for its three power supplies — $V_{CCINT}$, $V_{CCAUX}$, and $V_{CCO}$ to I/O Bank 2 (VCCO_2) — to reach their respective power-on thresholds before beginning the configuration process.

The SPI Flash PROM is powered by the same voltage supply feeding the FPGA's VCCO_2 voltage input, typically 3.3V. SPI Flash PROMs specify that they cannot be accessed until their $V_{CC}$ supply reaches its minimum data sheet voltage, followed by an additional delay. For some devices, this additional delay is as little as 10 µs as shown in Table 56. For other vendors, this delay is as much as 20 ms.

*Table 56:* **Example Minimum Power-On to Select Times for Various SPI Flash PROMs**

| Vendor | SPI Flash PROM Part Number | Data Sheet Minimum Time from $V_{CC}$ min to Select = Low | | |
|---|---|---|---|---|
| | | Symbol | Value | Units |
| STMicroelectronics | M25Pxx | $T_{VSL}$ | 10 | µs |
| Spansion | S25FLxxxA | $t_{PU}$ | 10 | ms |
| NexFlash | NX25xx | $T_{VSL}$ | 10 | µs |
| Macronix | MX25Lxxxx | $t_{VSL}$ | 10 | µs |
| Silicon Storage Technology | SST25LFxx | $T_{PU-READ}$ | 10 | µs |
| Programmable Microelectronics Corporation | Pm25LVxxx | $T_{VCS}$ | 50 | µs |
| Atmel Corporation | AT45DBxxxD | $t_{VCSL}$ | 30 | µs |
| | AT45DBxxxB | | 20 | ms |

In many systems, the 3.3V supply feeding the FPGA's VCCO_2 input is valid before the FPGA's other $V_{CCINT}$ and $V_{CCAUX}$ supplies, and consequently, there is no issue. However, if the 3.3V supply feeding the FPGA's VCCO_2 supply is last in the sequence, a potential race occurs between the FPGA and the SPI Flash PROM, as shown in Figure 55.

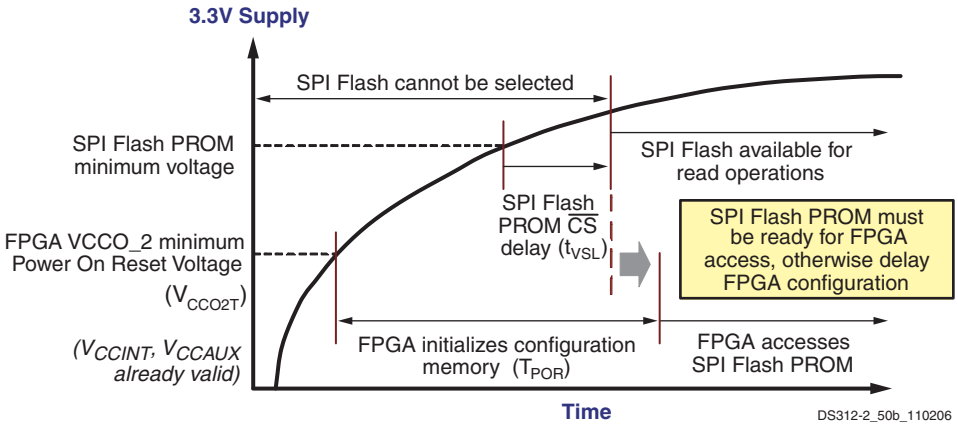


*Figure 55:* **SPI Flash PROM/FPGA Power-On Timing if 3.3V Supply is Last in Power-On Sequence**

If the FPGA's $V_{CCINT}$ and $V_{CCAUX}$ supplies are already valid, then the FPGA waits for VCCO_2 to reach its minimum threshold voltage before starting configuration. This threshold voltage is labeled as $V_{CCO2T}$ in Table 74 of Module 3 and ranges from approximately 0.4V to 1.0V, substantially lower than the SPI Flash PROM's minimum voltage. Once all three FPGA supplies reach their respective Power On Reset (POR) thresholds, the FPGA starts the configuration process and begins initializing its internal configuration memory. Initialization requires approximately 1 ms ($T_{POR}$, minimum in Table 111 of Module 3, after which the FPGA de-asserts INIT_B, selects the SPI Flash PROM, and starts sending the appropriate read command. The SPI Flash PROM must be ready for

# Powering Spartan-3E FPGAs

For additional information, refer to the “Powering Spartan-3 Generation FPGAs” chapter in UG331.

## Voltage Supplies

Like Spartan-3 FPGAs, Spartan-3E FPGAs have multiple voltage supply inputs, as shown in Table 70. There are two supply inputs for internal logic functions, $V_{CCINT}$ and $V_{CCAUX}$. Each of the four I/O banks has a separate $V_{CCO}$ supply input that powers the output buffers within the associated I/O bank. All of the $V_{CCO}$ connections to a specific I/O bank must be connected and must connect to the same voltage.

*Table 70:* **Spartan-3E Voltage Supplies**

| Supply Input | Description | Nominal Supply Voltage |
|---|---|---|
| $V_{CCINT}$ | Internal core supply voltage. Supplies all internal logic functions, such as CLBs, block RAM, and multipliers. Input to Power-On Reset (POR) circuit. | 1.2V |
| $V_{CCAUX}$ | Auxiliary supply voltage. Supplies Digital Clock Managers (DCMs), differential drivers, dedicated configuration pins, JTAG interface. Input to Power-On Reset (POR) circuit. | 2.5V |
| VCCO_0 | Supplies the output buffers in I/O Bank 0, the bank along the top edge of the FPGA. | Selectable, 3.3V, 2.5V, 1.8, 1.5V, or 1.2V |
| VCCO_1 | Supplies the output buffers in I/O Bank 1, the bank along the right edge of the FPGA. In Byte-Wide Peripheral Interface (BPI) Parallel Flash Mode, connects to the same voltage as the Flash PROM. | Selectable, 3.3V, 2.5V, 1.8, 1.5V, or 1.2V |
| VCCO_2 | Supplies the output buffers in I/O Bank 2, the bank along the bottom edge of the FPGA. Connects to the same voltage as the FPGA configuration source. Input to Power-On Reset (POR) circuit. | Selectable, 3.3V, 2.5V, 1.8, 1.5V, or 1.2V |
| VCCO_3 | Supplies the output buffers in I/O Bank 3, the bank along the left edge of the FPGA. | Selectable, 3.3V, 2.5V, 1.8, 1.5V, or 1.2V |

In a 3.3V-only application, all four $V_{CCO}$ supplies connect to 3.3V. However, Spartan-3E FPGAs provide the ability to bridge between different I/O voltages and standards by applying different voltages to the $V_{CCO}$ inputs of different banks. Refer to I/O Banking Rules for which I/O standards can be intermixed within a single I/O bank.

Each I/O bank also has an separate, optional input voltage reference supply, called $V_{REF}$. If the I/O bank includes an I/O standard that requires a voltage reference such as HSTL or SSTL, then all $V_{REF}$ pins within the I/O bank must be connected to the same voltage.

# Production Stepping

The Spartan-3E FPGA family uses production stepping to indicate improved capabilities or enhanced features.

Stepping 1 is, by definition, a functional superset of Stepping 0. Furthermore, configuration bitstreams generated for Stepping 0 are compatible with Stepping 1.

Designs operating on the Stepping 0 devices perform similarly on a Stepping 1 device.

## Differences Between Steppings

Table 71 summarizes the feature and performance differences between Stepping 0 devices and Stepping 1 devices.

*Table 71:* **Differences between Spartan-3E Production Stepping Levels**

| | Stepping 0 | Stepping 1 |
|---|---|---|
| Production status | Production from 2005 to 2007 | Production starting March 2006 |
| Speed grade and operating conditions | -4C only | -4C, -4I, -5C |
| JTAG ID code | Different revision fields. See Table 67. | |
| DCM DLL maximum input frequency | 90 MHz<br>(200 MHz for XC3S1200E) | 240 MHz (-4 speed grade)<br>275 MHz (-5 speed grade) |
| DCM DFS output frequency range(s) | Split ranges at 5 – 90 MHz and 220 – 307 MHz<br>(single range 5 – 307 MHz for XC3S1200E) | Continuous range:<br>5 – 311 MHz (-4)<br>5 – 333 MHz (-5) |
| Supports multi-FPGA daisy-chain configurations from SPI Flash | No, single FPGA only | Yes |
| JTAG configuration supported when FPGA in BPI mode with a valid image in the attached parallel NOR Flash PROM | No(1) | Yes |
| JTAG EXTEST, INTEST, SAMPLE support | Yes: XC3S100E, XC3S250E, XC3S500E<br>No(2): XC3S1200E, XC3S1600E | Yes<br>All Devices |
| Power sequencing when using HSWAP Pull-Up | Requires $V_{CCINT}$ before $V_{CCAUX}$ | Any sequence |
| PCI compliance | No | Yes |

**Notes:**

1. Workarounds exist. See Stepping 0 Limitations when Reprogramming via JTAG if FPGA Set for BPI Configuration.
2. JTAG BYPASS and JTAG configuration are supported

## Ordering a Later Stepping

-5C and -4I devices, and -4C devices (with date codes 0901 (2009) and later) always support the Stepping 1 feature set independent of the stepping code. Optionally, to order only Stepping 1 for the -4C devices, append an “S1” suffix to the standard ordering code, where ‘1’ is the stepping number, as indicated in Table 72.

*Table 72:* **Spartan-3E Optional Stepping Ordering**

| Stepping Number | Suffix Code | Status |
|---|---|---|
| 0 | None | Production |
| 1 | S1 | Production |

## Software Version Requirements

Production Spartan-3E applications must be processed using the Xilinx ISE 8.1i, Service Pack 3 or later development software, using the v1.21 or later speed files. The ISE 8.1i software implements critical bitstream generator updates.

For additional information on Spartan-3E development software and known issues, see the following Answer Record:

- Xilinx Answer #22253
  http://www.xilinx.com/support/answers/22253.htm

## Revision History

The following table shows the revision history for this document.

| Date | Version | Revision |
|---|---|---|
| 03/01/05 | 1.0 | Initial Xilinx release. |
| 03/21/05 | 1.1 | Updated Figure 45. Modified title on Table 39 and Table 45. |
| 11/23/05 | 2.0 | Updated values of On-Chip Differential Termination resistors. Updated Table 7. Updated configuration bitstream sizes for XC3S250E through XC3S1600E in Table 45, Table 51, Table 57, and Table 60. Added DLL Performance Differences Between Steppings. Added Stepping 0 Limitations when Reprogramming via JTAG if FPGA Set for BPI Configuration. Added Stepping 0 limitations when Daisy-Chaining in SPI configuration mode. Added Multiplier/Block RAM Interaction section. Updated Digital Clock Managers (DCMs) section, especially Phase Shifter (PS) portion. Corrected and enhanced the clock infrastructure diagram in Figure 45 and Table 41. Added CCLK Design Considerations section. Added Design Considerations for the HSWAP, M[2:0], and VS[2:0] Pins section. Added Spansion, Winbond, and Macronix to list of SPI Flash vendors in Table 53 and Table 56. Clarified that SPI mode configuration supports Atmel 'C'- and 'D'-series DataFlash. Updated the Programming Support section for SPI Flash PROMs. Added Power-On Precautions if PROM Supply is Last in Sequence, Compatible Flash Families, and BPI Mode Interaction with Right and Bottom Edge Global Clock Inputs sections to BPI configuration mode topic. Updated and amplified Powering Spartan-3E FPGAs section. Added Production Stepping section. |
| 03/22/06 | 3.0 | Upgraded data sheet status to Preliminary. Updated Input Delay Functions and Figure 6. Added clarification that Input-only pins also have Pull-Up and Pull-Down Resistors. Added design note about address setup and hold requirements to Block RAM. Added warning message about software differences between ISE 8.1i, Service Pack 3 and earlier software to FIXED Phase Shift Mode and VARIABLE Phase Shift Mode. Added message about using GCLK1 in DLL Clock Input Connections and Clock Inputs. Updated Figure 45. Added additional information on HSWAP behavior to Pin Behavior During Configuration. Highlighted which pins have configuration pull-up resistors unaffected by HSWAP in Table 46. Updated bitstream image sizes for the XC3S1200E and XC3S1600E in Table 45, Table 51, Table 57, and Table 60. Clarified that 'B'-series Atmel DataFlash SPI PROMs can be used in Commercial temperature range applications in Table 53 and Figure 54. Updated Figure 56. Updated Dynamically Loading Multiple Configuration Images Using MultiBoot Option section. Added design note about BPI daisy-chaining software support to BPI Daisy-Chaining section. Updated JTAG revision codes in Table 67. Added No Internal Charge Pumps or Free-Running Oscillators. Updated information on production stepping differences in Table 71. Updated Software Version Requirements. |
| 04/10/06 | 3.1 | Updated JTAG User ID information. Clarified Note 1, Figure 5. Clarified that Figure 45 shows electrical connectivity and corrected left- and right-edge DCM coordinates. Updated Table 30, Table 31, and Table 32 to show the specific clock line driven by the associated BUFGMUX primitive. Corrected the coordinate locations for the associated BUFGMUX primitives in Table 31 and Table 32. Updated Table 41 to show that the I0-input is the preferred connection to a BUFGMUX. |
| 05/19/06 | 3.2 | Made further clarifying changes to Figure 46, showing both direct inputs to BUFGMUX primitives and to DCMs. Added Atmel AT45DBxxxD-series DataFlash serial PROMs to Table 53. Added details that intermediate FPGAs in a BPI-mode, multi-FPGA configuration daisy-chain must be from either the Spartan-3E or the Virtex-5 FPGA families (see BPI Daisy-Chaining). Added Using JTAG Interface to Communicate to a Configured FPGA Design. Minor updates to Figure 66 and Figure 67. Clarified which Spartan-3E FPGA product options support the Readback feature, shown in Table 68. |
| 05/30/06 | 3.2.1 | Corrected various typos and incorrect links. |
| 10/02/06 | 3.3 | Clarified that the block RAM Readback feature is available either on the -5 speed grade or the Industrial temperature range. |
| 11/09/06 | 3.4 | Updated the description of the Input Delay Functions. The ODDR2 flip-flop with C0 or C1 Alignment is no longer supported. Updated Figure 5. Updated Table 6 for improved PCI input voltage tolerance. Replaced missing text in Clock Buffers/Multiplexers. Updated SPI Flash devices in Table 53. Updated parallel NOR Flash devices in Table 61. Direct, SPI Flash in-system Programming Support was added beginning with ISE 8.1i iMPACT software for STMicro and Atmel SPI PROMs. Updated Table 71 and Table 72 as Stepping 1 is in full production. Freshened various hyper links. Promoted Module 2 to Production status. |

## Power Supply Specifications

*Table 74:* **Supply Voltage Thresholds for Power-On Reset**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $V_{CCINTT}$ | Threshold for the $V_{CCINT}$ supply | 0.4 | 1.0 | V |
| $V_{CCAUXT}$ | Threshold for the $V_{CCAUX}$ supply | 0.8 | 2.0 | V |
| $V_{CCO2T}$ | Threshold for the $V_{CCO}$ Bank 2 supply | 0.4 | 1.0 | V |

**Notes:**

1. $V_{CCINT}$, $V_{CCAUX}$, and $V_{CCO}$ supplies to the FPGA can be applied in any order. However, the FPGA's configuration source (Platform Flash, SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source. In Step 0 devices using the HSWAP internal pull-up, $V_{CCINT}$ must be applied before $V_{CCAUX}$.
2. To ensure successful power-on, $V_{CCINT}$, $V_{CCO}$ Bank 2, and $V_{CCAUX}$ supplies must rise through their respective threshold-voltage ranges with no dips at any point.

*Table 75:* **Supply Voltage Ramp Rate**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $V_{CCINTR}$ | Ramp rate from GND to valid $V_{CCINT}$ supply level | 0.2 | 50 | ms |
| $V_{CCAUXR}$ | Ramp rate from GND to valid $V_{CCAUX}$ supply level | 0.2 | 50 | ms |
| $V_{CCO2R}$ | Ramp rate from GND to valid $V_{CCO}$ Bank 2 supply level | 0.2 | 50 | ms |

**Notes:**

1. $V_{CCINT}$, $V_{CCAUX}$, and $V_{CCO}$ supplies to the FPGA can be applied in any order. However, the FPGA's configuration source (Platform Flash, SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source. In Step 0 devices using the HSWAP internal pull-up, $V_{CCINT}$ must be applied before $V_{CCAUX}$.
2. To ensure successful power-on, $V_{CCINT}$, $V_{CCO}$ Bank 2, and $V_{CCAUX}$ supplies must rise through their respective threshold-voltage ranges with no dips at any point.

*Table 76:* **Supply Voltage Levels Necessary for Preserving RAM Contents**

| Symbol | Description | Min | Units |
|---|---|---|---|
| $V_{DRINT}$ | $V_{CCINT}$ level required to retain RAM data | 1.0 | V |
| $V_{DRAUX}$ | $V_{CCAUX}$ level required to retain RAM data | 2.0 | V |

**Notes:**

1. RAM contents include configuration data.

## General Recommended Operating Conditions

*Table 77:* **General Recommended Operating Conditions**

| Symbol | Description | | | Min | Nominal | Max | Units |
|---|---|---|---|---|---|---|---|
| $T_J$ | Junction temperature | Commercial | | 0 | – | 85 | °C |
| | | Industrial | | –40 | – | 100 | °C |
| $V_{CCINT}$ | Internal supply voltage | | | 1.140 | 1.200 | 1.260 | V |
| $V_{CCO}$ (1) | Output driver supply voltage | | | 1.100 | - | 3.465 | V |
| $V_{CCAUX}$ | Auxiliary supply voltage | | | 2.375 | 2.500 | 2.625 | V |
| $V_{IN}$ (2,3) | Input voltage extremes to avoid turning on I/O protection diodes | I/O, Input-only, and Dual-Purpose pins (4) | IP or IO_# | –0.5 | – | $V_{CCO}$ + 0.5 | V |
| | | | IO_Lxxy_# (5) | –0.5 | – | $V_{CCO}$ + 0.5 | V |
| | | Dedicated pins (6) | | –0.5 | – | $V_{CCAUX}$ + 0.5 | V |
| $T_{IN}$ | Input signal transition time (7) | | | – | – | 500 | ns |

**Notes:**

1. This $V_{CCO}$ range spans the lowest and highest operating voltages for all supported I/O standards. Table 80 lists the recommended $V_{CCO}$ range specific to each of the single-ended I/O standards, and Table 82 lists that specific to the differential standards.
2. Input voltages outside the recommended range require the $I_{IK}$ input clamp diode rating is met and no more than 100 pins exceed the range simultaneously. Refer to Table 73.
3. See XAPP459: *Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins on Spartan-3 Families*.
4. Each of the User I/O and Dual-Purpose pins is associated with one of the four banks' $V_{CCO}$ rails. Meeting the $V_{IN}$ limit ensures that the internal diode junctions that exist between these pins and their associated $V_{CCO}$ and GND rails do not turn on. The absolute maximum rating is provided in Table 73.
5. For single-ended signals that are placed on a differential-capable I/O, $V_{IN}$ of –0.2V to –0.5V is supported but can cause increased leakage between the two pins. See *Parasitic Leakage* in UG331, *Spartan-3 Generation FPGA User Guide*.
6. All Dedicated pins (PROG_B, DONE, TCK, TDI, TDO, and TMS) draw power from the $V_{CCAUX}$ rail (2.5V). Meeting the $V_{IN}$ max limit ensures that the internal diode junctions that exist between each of these pins and the $V_{CCAUX}$ and GND rails do not turn on.
7. Measured between 10% and 90% $V_{CCO}$. Follow Signal Integrity recommendations.

## Differential I/O Standards

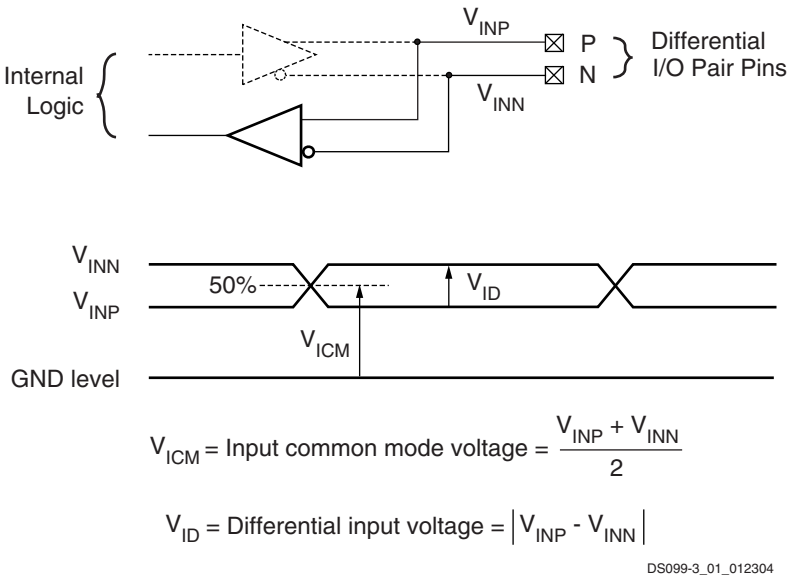


*Figure 69:* **Differential Input Voltages**

*Table 82:* **Recommended Operating Conditions for User I/Os Using Differential Signal Standards**

| IOSTANDARD Attribute | $V_{CCO}$ for Drivers[1] | | | $V_{ID}$ | | | $V_{ICM}$ | | |
|---|---|---|---|---|---|---|---|---|---|
| | Min (V) | Nom (V) | Max (V) | Min (mV) | Nom (mV) | Max (mV) | Min (V) | Nom (V) | Max (V) |
| LVDS_25 | 2.375 | 2.50 | 2.625 | 100 | 350 | 600 | 0.30 | 1.25 | 2.20 |
| BLVDS_25 | 2.375 | 2.50 | 2.625 | 100 | 350 | 600 | 0.30 | 1.25 | 2.20 |
| MINI_LVDS_25 | 2.375 | 2.50 | 2.625 | 200 | - | 600 | 0.30 | - | 2.2 |
| LVPECL_25[2] | Inputs Only | | | 100 | 800 | 1000 | 0.5 | 1.2 | 2.0 |
| RSDS_25 | 2.375 | 2.50 | 2.625 | 100 | 200 | - | 0.3 | 1.20 | 1.4 |
| DIFF_HSTL_I_18 | 1.7 | 1.8 | 1.9 | 100 | - | - | 0.8 | - | 1.1 |
| DIFF_HSTL_III_18 | 1.7 | 1.8 | 1.9 | 100 | - | - | 0.8 | - | 1.1 |
| DIFF_SSTL18_I | 1.7 | 1.8 | 1.9 | 100 | - | - | 0.7 | - | 1.1 |
| DIFF_SSTL2_I | 2.3 | 2.5 | 2.7 | 100 | - | - | 1.0 | - | 1.5 |

**Notes:**

1. The $V_{CCO}$ rails supply only differential output drivers, not input circuits.
2. $V_{REF}$ inputs are not used for any of the differential I/O standards.

*Table 99:* **CLB Distributed RAM Switching Characteristics**

| Symbol | Description | -5 | | -4 | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| **Clock-to-Output Times** | | | | | | |
| $T_{SHCKO}$ | Time from the active edge at the CLK input to data appearing on the distributed RAM output | - | 2.05 | - | 2.35 | ns |
| **Setup Times** | | | | | | |
| $T_{DS}$ | Setup time of data at the BX or BY input before the active transition at the CLK input of the distributed RAM | 0.40 | - | 0.46 | - | ns |
| $T_{AS}$ | Setup time of the F/G address inputs before the active transition at the CLK input of the distributed RAM | 0.46 | - | 0.52 | - | ns |
| $T_{WS}$ | Setup time of the write enable input before the active transition at the CLK input of the distributed RAM | 0.34 | - | 0.40 | - | ns |
| **Hold Times** | | | | | | |
| $T_{DH}$ | Hold time of the BX, BY data inputs after the active transition at the CLK input of the distributed RAM | 0.13 | - | 0.15 | - | ns |
| $T_{AH}$, $T_{WH}$ | Hold time of the F/G address inputs or the write enable input after the active transition at the CLK input of the distributed RAM | 0 | - | 0 | - | ns |
| **Clock Pulse Width** | | | | | | |
| $T_{WPH}$, $T_{WPL}$ | Minimum High or Low pulse width at CLK input | 0.88 | - | 1.01 | - | ns |

*Table 100:* **CLB Shift Register Switching Characteristics**

| Symbol | Description | -5 | | -4 | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| **Clock-to-Output Times** | | | | | | |
| $T_{REG}$ | Time from the active edge at the CLK input to data appearing on the shift register output | - | 3.62 | - | 4.16 | ns |
| **Setup Times** | | | | | | |
| $T_{SRLDS}$ | Setup time of data at the BX or BY input before the active transition at the CLK input of the shift register | 0.41 | - | 0.46 | - | ns |
| **Hold Times** | | | | | | |
| $T_{SRLDH}$ | Hold time of the BX or BY data input after the active transition at the CLK input of the shift register | 0.14 | - | 0.16 | - | ns |
| **Clock Pulse Width** | | | | | | |
| $T_{WPH}$, $T_{WPL}$ | Minimum High or Low pulse width at CLK input | 0.88 | - | 1.01 | - | ns |

## Clock Buffer/Multiplexer Switching Characteristics

*Table 101:* **Clock Distribution Switching Characteristics**

| Description | Symbol | Maximum | | Units |
|---|---|---|---|---|
| | | Speed Grade | | |
| | | -5 | -4 | |
| Global clock buffer (BUFG, BUFGMUX, BUFGCE) I input to O-output delay | $T_{GIO}$ | 1.46 | 1.46 | ns |
| Global clock multiplexer (BUFGMUX) select S-input setup to I0 and I1 inputs. Same as BUFGCE enable CE-input | $T_{GSI}$ | 0.55 | 0.63 | ns |
| Frequency of signals distributed on global buffers (all sides) | $F_{BUFG}$ | 333 | 311 | MHz |

*Table 119:* **Configuration Timing Requirements for Attached SPI Serial Flash**

| Symbol | Description | Requirement | Units |
|---|---|---|---|
| $T_{CCS}$ | SPI serial Flash PROM chip-select time | $T_{CCS} \leq T_{MCCL1} - T_{CCO}$ | ns |
| $T_{DSU}$ | SPI serial Flash PROM data input setup time | $T_{DSU} \leq T_{MCCL1} - T_{CCO}$ | ns |
| $T_{DH}$ | SPI serial Flash PROM data input hold time | $T_{DH} \leq T_{MCCH1}$ | ns |
| $T_V$ | SPI serial Flash PROM data clock-to-output time | $T_V \leq T_{MCCLn} - T_{DCC}$ | ns |
| $f_C$ or $f_R$ | Maximum SPI serial Flash PROM clock frequency (also depends on specific read command used) | $f_C \geq \frac{1}{T_{CCLKn(min)}}$ | MHz |

**Notes:**

1. These requirements are for successful FPGA configuration in SPI mode, where the FPGA provides the CCLK frequency. The post configuration timing can be different to support the specific needs of the application loaded into the FPGA and the resulting clock source.
2. Subtract additional printed circuit board routing delay as required by the application.

## Package Thermal Characteristics

The power dissipated by an FPGA application has implications on package selection and system design. The power consumed by a Spartan-3E FPGA is reported using either the XPower Estimator or the XPower Analyzer calculator integrated in the Xilinx ISE® development software. Table 130 provides the thermal characteristics for the various Spartan-3E package offerings.

The junction-to-case thermal resistance ($\theta_{JC}$) indicates the difference between the temperature measured on the package body (case) and the die junction temperature per watt of power consumption. The junction-to-board ($\theta_{JB}$) value similarly reports the difference between the board and junction temperature. The junction-to-ambient ($\theta_{JA}$) value reports the temperature difference per watt between the ambient environment and the junction temperature. The $\theta_{JA}$ value is reported at different air velocities, measured in linear feet per minute (LFM). The Still Air (0 LFM) column shows the $\theta_{JA}$ value in a system without a fan. The thermal resistance drops with increasing air flow.

*Table 130:* **Spartan-3E Package Thermal Characteristics**

| Device | Package | Junction-to-Case ($\theta_{JC}$) | Junction-to-Board ($\theta_{JB}$) | Junction-to-Ambient ($\theta_{JA}$) at Different Air Flows | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | Still Air (0 LFM) | 250 LFM | 500 LFM | 750 LFM | |
| XC3S100E | VQ100 | 13.0 | 30.9 | 49.0 | 40.7 | 37.9 | 37.0 | °C/Watt |
| XC3S250E | | 11.0 | 25.9 | 43.3 | 36.0 | 33.6 | 32.7 | °C/Watt |
| XC3S500E | | 9.8 | | 40.0 | 33.3 | 31.0 | 30.2 | °C/Watt |
| XC3S100E | CP132 | 19.3 | 42.0 | 62.1 | 55.3 | 52.8 | 51.2 | °C/Watt |
| XC3S250E | | 11.8 | 28.1 | 48.3 | 41.8 | 39.5 | 38.0 | °C/Watt |
| XC3S500E | | 8.5 | 21.3 | 41.5 | 35.2 | 32.9 | 31.5 | °C/Watt |
| XC3S100E | TQ144 | 8.2 | 31.9 | 52.1 | 40.5 | 34.6 | 32.5 | °C/Watt |
| XC3S250E | | 7.2 | 25.7 | 37.6 | 29.2 | 25.0 | 23.4 | °C/Watt |
| XC3S250E | PQ208 | 9.8 | 29.0 | 37.0 | 27.3 | 24.1 | 22.4 | °C/Watt |
| XC3S500E | | 8.5 | 26.8 | 36.1 | 26.6 | 23.6 | 21.8 | °C/Watt |
| XC3S250E | FT256 | 12.4 | 27.7 | 35.8 | 29.3 | 28.4 | 28.1 | °C/Watt |
| XC3S500E | | 9.6 | 22.2 | 31.1 | 25.0 | 24.0 | 23.6 | °C/Watt |
| XC3S1200E | | 6.5 | 16.4 | 26.2 | 20.5 | 19.3 | 18.9 | °C/Watt |
| XC3S500E | FG320 | 9.8 | 15.6 | 26.1 | 20.6 | 19.4 | 18.6 | °C/Watt |
| XC3S1200E | | 8.2 | 12.5 | 23.0 | 17.7 | 16.4 | 15.7 | °C/Watt |
| XC3S1600E | | 7.1 | 10.6 | 21.1 | 15.9 | 14.6 | 13.8 | °C/Watt |
| XC3S1200E | FG400 | 7.5 | 12.4 | 22.3 | 17.2 | 16.0 | 15.3 | °C/Watt |
| XC3S1600E | | 6.0 | 10.4 | 20.3 | 15.2 | 14.0 | 13.3 | °C/Watt |
| XC3S1600E | FG484 | 5.7 | 9.4 | 18.8 | 12.5 | 11.3 | 10.8 | °C/Watt |

## User I/Os by Bank

Table 142 indicates how the 158 available user-I/O pins are distributed between the four I/O banks on the PQ208 package.

## Footprint Migration Differences

The XC3S250E and XC3S500E FPGAs have identical footprints in the PQ208 package. Designs can migrate between the XC3S250E and XC3S500E without further consideration.

*Table 142:* **User I/Os Per Bank for the XC3S250E and XC3S500E in the PQ208 Package**

| Package Edge | I/O Bank | Maximum I/O | All Possible I/O Pins by Type | | | | |
|---|---|---|---|---|---|---|---|
| | | | I/O | INPUT | DUAL | VREF(1) | CLK(2) |
| Top | 0 | 38 | 18 | 6 | 1 | 5 | 8 |
| Right | 1 | 40 | 9 | 7 | 21 | 3 | 0(2) |
| Bottom | 2 | 40 | 8 | 6 | 24 | 2 | 0(2) |
| Left | 3 | 40 | 23 | 6 | 0 | 3 | 8 |
| **TOTAL** | | **158** | **58** | **25** | **46** | **13** | **16** |

**Notes:**

1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

# FT256: 256-ball Fine-pitch, Thin Ball Grid Array

The 256-ball fine-pitch, thin ball grid array package, FT256, supports three different Spartan-3E FPGAs, including the XC3S250E, the XC3S500E, and the XC3S1200E.

Table 143 lists all the package pins. They are sorted by bank number and then by pin name of the largest device. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The highlighted rows indicate pinout differences between the XC3S250E, the XC3S500E, and the XC3S1200E FPGAs. The XC3S250E has 18 unconnected balls, indicated as N.C. (No Connection) in Table 143 and with the black diamond character (◆) in Table 143 and Figure 83.

If the table row is highlighted in tan, then this is an instance where an unconnected pin on the XC3S250E FPGA maps to a VREF pin on the XC3S500E and XC3S1200E FPGA. If the FPGA application uses an I/O standard that requires a VREF voltage reference, connect the highlighted pin to the VREF voltage supply, even though this does not actually connect to the XC3S250E FPGA. This VREF connection on the board allows future migration to the larger devices without modifying the printed-circuit board.

All other balls have nearly identical functionality on all three devices. Table 147 summarizes the Spartan-3E footprint migration differences for the FT256 package.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx web site at:

http://www.xilinx.com/support/documentation/data_sheets/s3e_pin.zip

## Pinout Table

*Table 143:* **FT256 Package Pinout**

| Bank | XC3S250E Pin Name | XC3S500E Pin Name | XC3S1200E Pin Name | FT256 Ball | Type |
|---|---|---|---|---|---|
| 0 | IO | IO | IO | A7 | I/O |
| 0 | IO | IO | IO | A12 | I/O |
| 0 | IO | IO | IO | B4 | I/O |
| 0 | IP | IP | IO | B6 | ***250E:*** INPUT ***500E:*** INPUT ***1200E:*** I/O |
| 0 | IP | IP | IO | B10 | ***250E:*** INPUT ***500E:*** INPUT ***1200E:*** I/O |
| 0 | IO/VREF_0 | IO/VREF_0 | IO/VREF_0 | D9 | VREF |
| 0 | IO_L01N_0 | IO_L01N_0 | IO_L01N_0 | A14 | I/O |
| 0 | IO_L01P_0 | IO_L01P_0 | IO_L01P_0 | B14 | I/O |
| 0 | IO_L03N_0/VREF_0 | IO_L03N_0/VREF_0 | IO_L03N_0/VREF_0 | A13 | VREF |
| 0 | IO_L03P_0 | IO_L03P_0 | IO_L03P_0 | B13 | I/O |
| 0 | IO_L04N_0 | IO_L04N_0 | IO_L04N_0 | E11 | I/O |
| 0 | IO_L04P_0 | IO_L04P_0 | IO_L04P_0 | D11 | I/O |
| 0 | IO_L05N_0/VREF_0 | IO_L05N_0/VREF_0 | IO_L05N_0/VREF_0 | B11 | VREF |
| 0 | IO_L05P_0 | IO_L05P_0 | IO_L05P_0 | C11 | I/O |
| 0 | IO_L06N_0 | IO_L06N_0 | IO_L06N_0 | E10 | I/O |
| 0 | IO_L06P_0 | IO_L06P_0 | IO_L06P_0 | D10 | I/O |
| 0 | IO_L08N_0/GCLK5 | IO_L08N_0/GCLK5 | IO_L08N_0/GCLK5 | F9 | GCLK |
| 0 | IO_L08P_0/GCLK4 | IO_L08P_0/GCLK4 | IO_L08P_0/GCLK4 | E9 | GCLK |
| 0 | IO_L09N_0/GCLK7 | IO_L09N_0/GCLK7 | IO_L09N_0/GCLK7 | A9 | GCLK |
| 0 | IO_L09P_0/GCLK6 | IO_L09P_0/GCLK6 | IO_L09P_0/GCLK6 | A10 | GCLK |
| 0 | IO_L11N_0/GCLK11 | IO_L11N_0/GCLK11 | IO_L11N_0/GCLK11 | D8 | GCLK |
| 0 | IO_L11P_0/GCLK10 | IO_L11P_0/GCLK10 | IO_L11P_0/GCLK10 | C8 | GCLK |
| 0 | IO_L12N_0 | IO_L12N_0 | IO_L12N_0 | F8 | I/O |

*Table 143:* **FT256 Package Pinout *(Cont'd)***

| Bank | XC3S250E Pin Name | XC3S500E Pin Name | XC3S1200E Pin Name | FT256 Ball | Type |
|---|---|---|---|---|---|
| 1 | IO | IO | IP | M14 | ***250E:*** I/O ***500E:*** I/O ***1200E:*** INPUT |
| 1 | IO/VREF_1 | IP/VREF_1 | IP/VREF_1 | D16 | ***250E:*** VREF(I/O) ***500E:*** VREF(INPUT) ***1200E:*** VREF(INPUT) |
| 1 | IP/VREF_1 | IP/VREF_1 | IP/VREF_1 | H13 | VREF |
| 1 | VCCO_1 | VCCO_1 | VCCO_1 | E15 | VCCO |
| 1 | VCCO_1 | VCCO_1 | VCCO_1 | G11 | VCCO |
| 1 | VCCO_1 | VCCO_1 | VCCO_1 | K11 | VCCO |
| 1 | VCCO_1 | VCCO_1 | VCCO_1 | M15 | VCCO |
| 2 | IP | IP | IO | M7 | ***250E:*** INPUT ***500E:*** INPUT ***1200E:*** I/O |
| 2 | IP | IP | IO | T12 | ***250E:*** INPUT ***500E:*** INPUT ***1200E:*** I/O |
| 2 | IO/D5 | IO/D5 | IO/D5 | T8 | DUAL |
| 2 | IO/M1 | IO/M1 | IO/M1 | T10 | DUAL |
| 2 | IO/VREF_2 | IO/VREF_2 | IO/VREF_2 | P13 | VREF |
| 2 | IO/VREF_2 | IO/VREF_2 | IO/VREF_2 | R4 | VREF |
| 2 | IO_L01N_2/INIT_B | IO_L01N_2/INIT_B | IO_L01N_2/INIT_B | P4 | DUAL |
| 2 | IO_L01P_2/CSO_B | IO_L01P_2/CSO_B | IO_L01P_2/CSO_B | P3 | DUAL |
| 2 | IO_L03N_2/MOSI/CSI_B | IO_L03N_2/MOSI/CSI_B | IO_L03N_2/MOSI/CSI_B | N5 | DUAL |
| 2 | IO_L03P_2/DOUT/BUSY | IO_L03P_2/DOUT/BUSY | IO_L03P_2/DOUT/BUSY | P5 | DUAL |
| 2 | IO_L04N_2 | IO_L04N_2 | IO_L04N_2 | T5 | I/O |
| 2 | IO_L04P_2 | IO_L04P_2 | IO_L04P_2 | T4 | I/O |
| 2 | IO_L05N_2 | IO_L05N_2 | IO_L05N_2 | N6 | I/O |
| 2 | IO_L05P_2 | IO_L05P_2 | IO_L05P_2 | M6 | I/O |
| 2 | IO_L06N_2 | IO_L06N_2 | IO_L06N_2 | P6 | I/O |
| 2 | IO_L06P_2 | IO_L06P_2 | IO_L06P_2 | R6 | I/O |
| 2 | N.C. (◆) | IO_L07N_2 | IO_L07N_2 | P7 | ***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O |
| 2 | N.C. (◆) | IO_L07P_2 | IO_L07P_2 | N7 | ***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O |
| 2 | IO_L09N_2/D6/GCLK13 | IO_L09N_2/D6/GCLK13 | IO_L09N_2/D6/GCLK13 | L8 | DUAL/GCLK |
| 2 | IO_L09P_2/D7/GCLK12 | IO_L09P_2/D7/GCLK12 | IO_L09P_2/D7/GCLK12 | M8 | DUAL/GCLK |
| 2 | IO_L10N_2/D3/GCLK15 | IO_L10N_2/D3/GCLK15 | IO_L10N_2/D3/GCLK15 | P8 | DUAL/GCLK |
| 2 | IO_L10P_2/D4/GCLK14 | IO_L10P_2/D4/GCLK14 | IO_L10P_2/D4/GCLK14 | N8 | DUAL/GCLK |
| 2 | IO_L12N_2/D1/GCLK3 | IO_L12N_2/D1/GCLK3 | IO_L12N_2/D1/GCLK3 | N9 | DUAL/GCLK |
| 2 | IO_L12P_2/D2/GCLK2 | IO_L12P_2/D2/GCLK2 | IO_L12P_2/D2/GCLK2 | P9 | DUAL/GCLK |
| 2 | IO_L13N_2/DIN/D0 | IO_L13N_2/DIN/D0 | IO_L13N_2/DIN/D0 | M9 | DUAL |
| 2 | IO_L13P_2/M0 | IO_L13P_2/M0 | IO_L13P_2/M0 | L9 | DUAL |

## User I/Os by Bank

Table 149 and Table 150 indicate how the available user-I/O pins are distributed between the four I/O banks on the FG320 package.

*Table 149:* **User I/Os Per Bank for XC3S500E in the FG320 Package**

| Package Edge | I/O Bank | Maximum I/O | All Possible I/O Pins by Type | | | | |
|---|---|---|---|---|---|---|---|
| | | | I/O | INPUT | DUAL | VREF(1) | CLK(2) |
| Top | 0 | 58 | 29 | 14 | 1 | 6 | 8 |
| Right | 1 | 58 | 22 | 10 | 21 | 5 | 0(2) |
| Bottom | 2 | 58 | 17 | 13 | 24 | 4 | 0(2) |
| Left | 3 | 58 | 34 | 11 | 0 | 5 | 8 |
| **TOTAL** | | **232** | **102** | **48** | **46** | **20** | **16** |

**Notes:**

1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

*Table 150:* **User I/Os Per Bank for XC3S1200E and XC3S1600E in the FG320 Package**

| Package Edge | I/O Bank | Maximum I/O | All Possible I/O Pins by Type | | | | |
|---|---|---|---|---|---|---|---|
| | | | I/O | INPUT | DUAL | VREF(1) | CLK(2) |
| Top | 0 | 61 | 34 | 12 | 1 | 6 | 8 |
| Right | 1 | 63 | 25 | 12 | 21 | 5 | 0(2) |
| Bottom | 2 | 63 | 23 | 11 | 24 | 5 | 0(2) |
| Left | 3 | 63 | 38 | 12 | 0 | 5 | 8 |
| **TOTAL** | | **250** | **120** | **47** | **46** | **21** | **16** |

**Notes:**

1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

*Table 154:* **FG484 Package Pinout *(Cont'd)***

| Bank | XC3S1600E Pin Name | FG484 Ball | Type |
|---|---|---|---|
| 3 | IO_L11N_3 | H1 | I/O |
| 3 | IO_L11P_3 | J1 | I/O |
| 3 | IO_L12N_3 | J6 | I/O |
| 3 | IO_L12P_3 | J5 | I/O |
| 3 | IO_L13N_3/VREF_3 | J3 | VREF |
| 3 | IO_L13P_3 | K3 | I/O |
| 3 | IO_L14N_3 | J8 | I/O |
| 3 | IO_L14P_3 | K8 | I/O |
| 3 | IO_L15N_3 | K4 | I/O |
| 3 | IO_L15P_3 | K5 | I/O |
| 3 | IO_L16N_3 | K1 | I/O |
| 3 | IO_L16P_3 | L1 | I/O |
| 3 | IO_L17N_3 | L7 | I/O |
| 3 | IO_L17P_3 | K7 | I/O |
| 3 | IO_L18N_3/LHCLK1 | L5 | LHCLK |
| 3 | IO_L18P_3/LHCLK0 | M5 | LHCLK |
| 3 | IO_L19N_3/LHCLK3/IRDY2 | M8 | LHCLK |
| 3 | IO_L19P_3/LHCLK2 | L8 | LHCLK |
| 3 | IO_L20N_3/LHCLK5 | N1 | LHCLK |
| 3 | IO_L20P_3/LHCLK4/TRDY2 | M1 | LHCLK |
| 3 | IO_L21N_3/LHCLK7 | M4 | LHCLK |
| 3 | IO_L21P_3/LHCLK6 | M3 | LHCLK |
| 3 | IO_L22N_3 | N6 | I/O |
| 3 | IO_L22P_3 | N7 | I/O |
| 3 | IO_L23N_3 | P8 | I/O |
| 3 | IO_L23P_3 | N8 | I/O |
| 3 | IO_L24N_3/VREF_3 | N4 | VREF |
| 3 | IO_L24P_3 | N5 | I/O |
| 3 | IO_L25N_3 | P2 | I/O |
| 3 | IO_L25P_3 | P1 | I/O |
| 3 | IO_L26N_3 | R7 | I/O |
| 3 | IO_L26P_3 | P7 | I/O |
| 3 | IO_L27N_3 | P6 | I/O |
| 3 | IO_L27P_3 | P5 | I/O |
| 3 | IO_L28N_3 | R2 | I/O |
| 3 | IO_L28P_3 | R1 | I/O |
| 3 | IO_L29N_3 | R3 | I/O |
| 3 | IO_L29P_3 | R4 | I/O |
| 3 | IO_L30N_3 | T6 | I/O |
| 3 | IO_L30P_3 | R6 | I/O |
| 3 | IO_L31N_3 | U2 | I/O |
| 3 | IO_L31P_3 | U1 | I/O |
| 3 | IO_L32N_3 | T4 | I/O |
| 3 | IO_L32P_3 | T5 | I/O |

*Table 154:* **FG484 Package Pinout *(Cont'd)***

| Bank | XC3S1600E Pin Name | FG484 Ball | Type |
|---|---|---|---|
| 3 | IO_L33N_3 | W1 | I/O |
| 3 | IO_L33P_3 | V1 | I/O |
| 3 | IO_L34N_3 | U4 | I/O |
| 3 | IO_L34P_3 | U3 | I/O |
| 3 | IO_L35N_3 | V4 | I/O |
| 3 | IO_L35P_3 | V3 | I/O |
| 3 | IO_L36N_3/VREF_3 | W3 | VREF |
| 3 | IO_L36P_3 | W2 | I/O |
| 3 | IO_L37N_3 | Y2 | I/O |
| 3 | IO_L37P_3 | Y1 | I/O |
| 3 | IO_L38N_3 | AA1 | I/O |
| 3 | IO_L38P_3 | AA2 | I/O |
| 3 | IP | F2 | INPUT |
| 3 | IP | F5 | INPUT |
| 3 | IP | G3 | INPUT |
| 3 | IP | H7 | INPUT |
| 3 | IP | J7 | INPUT |
| 3 | IP | K2 | INPUT |
| 3 | IP | K6 | INPUT |
| 3 | IP | M2 | INPUT |
| 3 | IP | M6 | INPUT |
| 3 | IP | N3 | INPUT |
| 3 | IP | P3 | INPUT |
| 3 | IP | R8 | INPUT |
| 3 | IP | T1 | INPUT |
| 3 | IP | T7 | INPUT |
| 3 | IP | U5 | INPUT |
| 3 | IP | W4 | INPUT |
| 3 | IP/VREF_3 | L3 | VREF |
| 3 | IP/VREF_3 | T3 | VREF |
| 3 | VCCO_3 | E2 | VCCO |
| 3 | VCCO_3 | H6 | VCCO |
| 3 | VCCO_3 | J2 | VCCO |
| 3 | VCCO_3 | M7 | VCCO |
| 3 | VCCO_3 | N2 | VCCO |
| 3 | VCCO_3 | R5 | VCCO |
| 3 | VCCO_3 | V2 | VCCO |
| GND | GND | A1 | GND |
| GND | GND | A11 | GND |
| GND | GND | A22 | GND |
| GND | GND | B7 | GND |
| GND | GND | B16 | GND |
| GND | GND | C3 | GND |
| GND | GND | C20 | GND |