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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	240
Number of Logic Elements/Cells	2160
Total RAM Bits	73728
Number of I/O	108
Number of Gates	100000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s100e-4tqg144c

Table 14: **Carry Logic Functions *(Cont'd)***

Function	Description
CY0G	Carry generation for top half of slice. Fixed selection of: · G1 or G2 inputs to the LUT (both equal 1 when a carry is to be generated) · GAND gate for multiplication · BY input for carry initialization · Fixed 1 or 0 input for use as a simple Boolean function
CYMUXF	Carry generation or propagation mux for bottom half of slice. Dynamic selection via CYSELF of: · CYINIT carry propagation (CYSELF = 1) · CY0F carry generation (CYSELF = 0)
CYMUXG	Carry generation or propagation mux for top half of slice. Dynamic selection via CYSELF of: · CYMUXF carry propagation (CYSELG = 1) · CY0G carry generation (CYSELG = 0)
CYSELF	Carry generation or propagation select for bottom half of slice. Fixed selection of: · F-LUT output (typically XOR result) · Fixed 1 to always propagate
CYSELG	Carry generation or propagation select for top half of slice. Fixed selection of: · G-LUT output (typically XOR result) · Fixed 1 to always propagate
XORF	Sum generation for bottom half of slice. Inputs from: · F-LUT · CYINIT carry signal from previous stage Result is sent to either the combinatorial or registered output for the top of the slice.
XORG	Sum generation for top half of slice. Inputs from: · G-LUT · CYMUXF carry signal from previous stage Result is sent to either the combinatorial or registered output for the top of the slice.
FAND	Multiplier partial product for bottom half of slice. Inputs: · F-LUT F1 input · F-LUT F2 input Result is sent through CY0F to become the carry generate signal into CYMUXF
GAND	Multiplier partial product for top half of slice. Inputs: · G-LUT G1 input · G-LUT G2 input Result is sent through CY0G to become the carry generate signal into CYMUXG

The basic usage of the carry logic is to generate a half-sum in the LUT via an XOR function, which generates or propagates a carry out COUT via the carry mux CYMUXF (or CYMUXG), and then complete the sum with the dedicated XORF (or XORG) gate and the carry input CIN. This structure allows two bits of an arithmetic function in each slice. The CYMUXF (or CYMUXG) can be instantiated using the MUXCY element, and the XORF (or XORG) can be instantiated using the XORCY element.

The FAND (or GAND) gate is used for partial product multiplication and can be instantiated using the MULT_AND component. Partial products are generated by two-input AND gates and then added. The carry logic is efficient for the adder, but one of the inputs must be outside the LUT as shown in Figure 23.

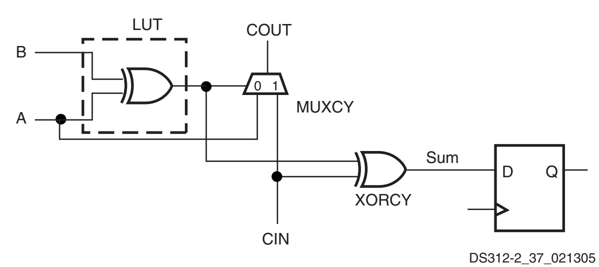

Figure 23: **Using the MUXCY and XORCY in the Carry Logic**

The FAND (or GAND) gate is used to duplicate one of the partial products, while the LUT generates both partial products and the XOR function, as shown in Figure 24.

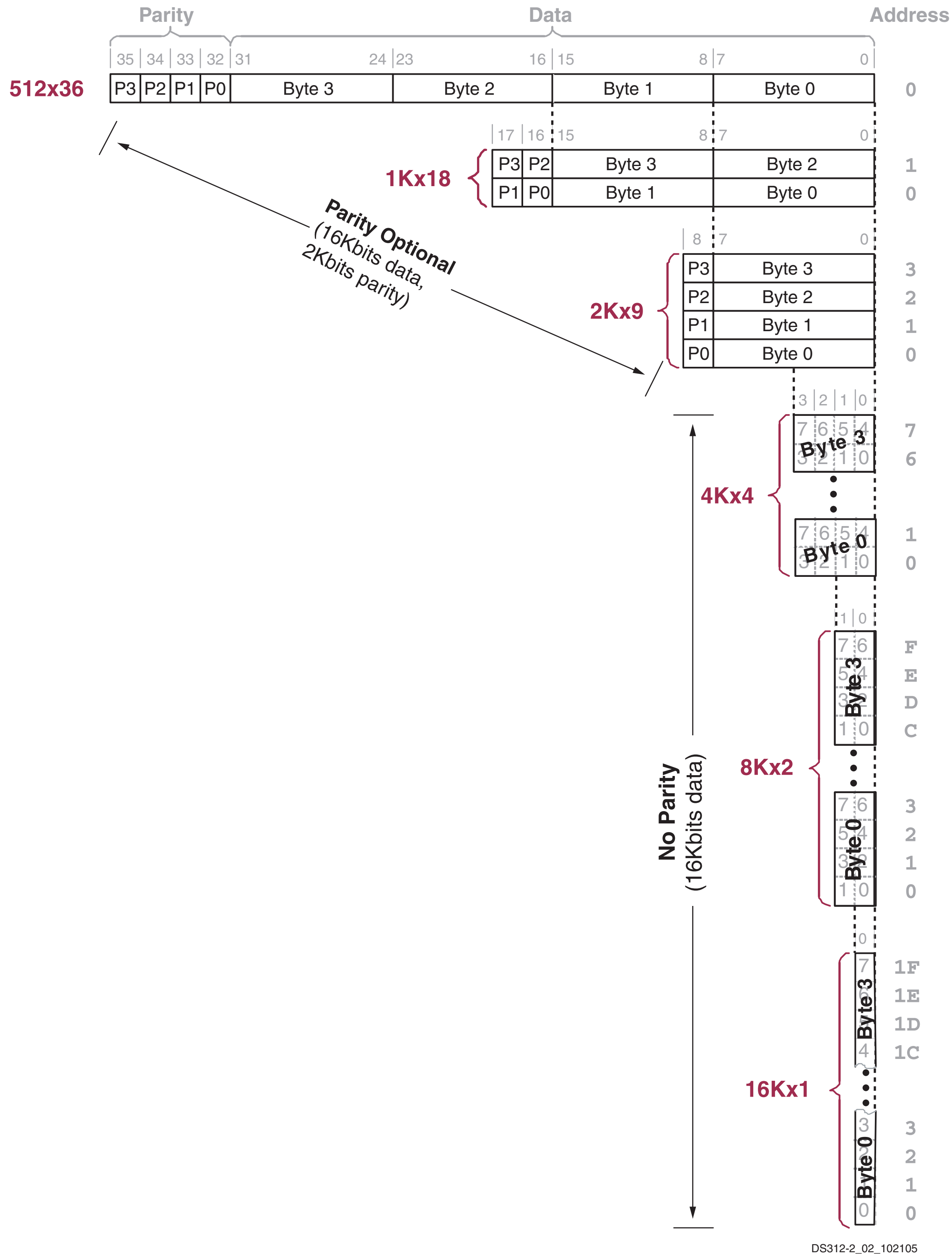

Figure 31: **Data Organization and Bus-matching Operation with Different Port Widths on Port A and Port B**

Delay-Locked Loop (DLL)

The most basic function of the DLL component is to eliminate clock skew. The main signal path of the DLL consists of an input stage, followed by a series of discrete delay elements or *steps,* which in turn leads to an output stage. This path together with logic for phase detection and control forms a system complete with feedback as shown in Figure 41. In Spartan-3E FPGAs, the DLL is implemented using a counter-based delay line.

The DLL component has two clock inputs, CLKIN and CLKFB, as well as seven clock outputs, CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV as described in Table 28. The clock outputs drive simultaneously. Signals that initialize and report the state of the DLL are discussed in Status Logic.

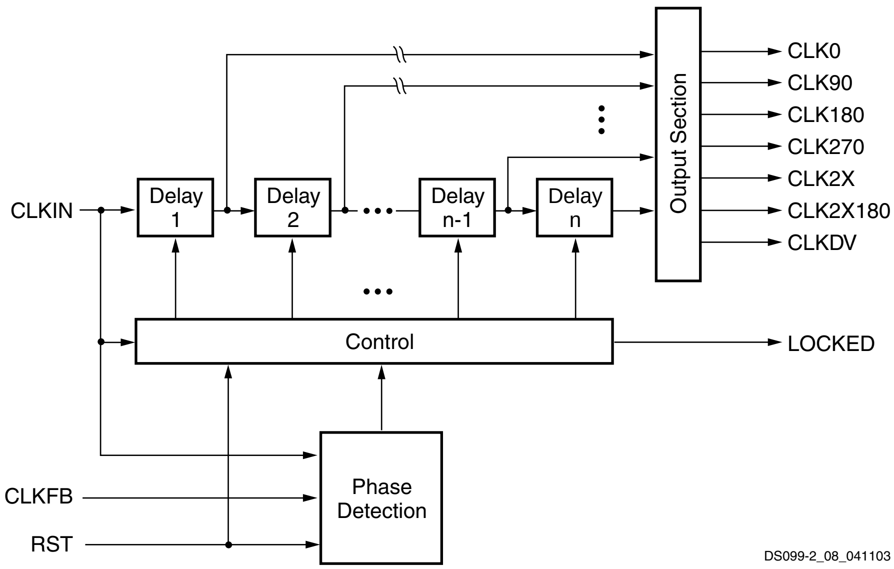

Figure 41: **Simplified Functional Diagram of DLL**

Table 28: **DLL Signals**

Signal	Direction	Description
CLKIN	Input	Receives the incoming clock signal. See Table 30, Table 31, and Table 32 for optimal external inputs to a DCM.
CLKFB	Input	Accepts either CLK0 or CLK2X as the feedback signal. (Set the CLK_FEEDBACK attribute accordingly).
CLK0	Output	Generates a clock signal with the same frequency and phase as CLKIN.
CLK90	Output	Generates a clock signal with the same frequency as CLKIN, phase-shifted by 90°.
CLK180	Output	Generates a clock signal with the same frequency as CLKIN, phase-shifted by 180°.
CLK270	Output	Generates a clock signal with the same frequency as CLKIN, phase-shifted by 270°.
CLK2X	Output	Generates a clock signal with the same phase as CLKIN, and twice the frequency.
CLK2X180	Output	Generates a clock signal with twice the frequency of CLKIN, and phase-shifted 180° with respect to CLK2X.
CLKDV	Output	Divides the CLKIN frequency by CLKDV_DIVIDE value to generate lower frequency clock signal that is phase-aligned to CLKIN.

The clock signal supplied to the CLKIN input serves as a reference waveform. The DLL seeks to align the rising-edge of feedback signal at the CLKFB input with the rising-edge of CLKIN input. When eliminating clock skew, the common approach to using the DLL is as follows: The CLK0 signal is passed through the clock distribution network that feeds all the registers it synchronizes. These registers are either internal or external to the FPGA. After passing through the clock distribution network, the clock signal returns to the DLL via a feedback line called CLKFB. The control block inside the DLL measures the phase error between CLKFB and CLKIN. This phase error is a measure of the clock skew that the clock distribution network introduces. The control block activates the appropriate number of delay steps to

SPI Serial Flash Mode

For additional information, refer to the “Master SPI Mode” chapter in UG332.

In SPI Serial Flash mode (M[2:0] = <0:0:1>), the Spartan-3E FPGA configures itself from an attached industry-standard SPI serial Flash PROM, as illustrated in Figure 53 and Figure 54. The FPGA supplies the CCLK output clock from its internal oscillator to the clock input of the attached SPI Flash PROM.

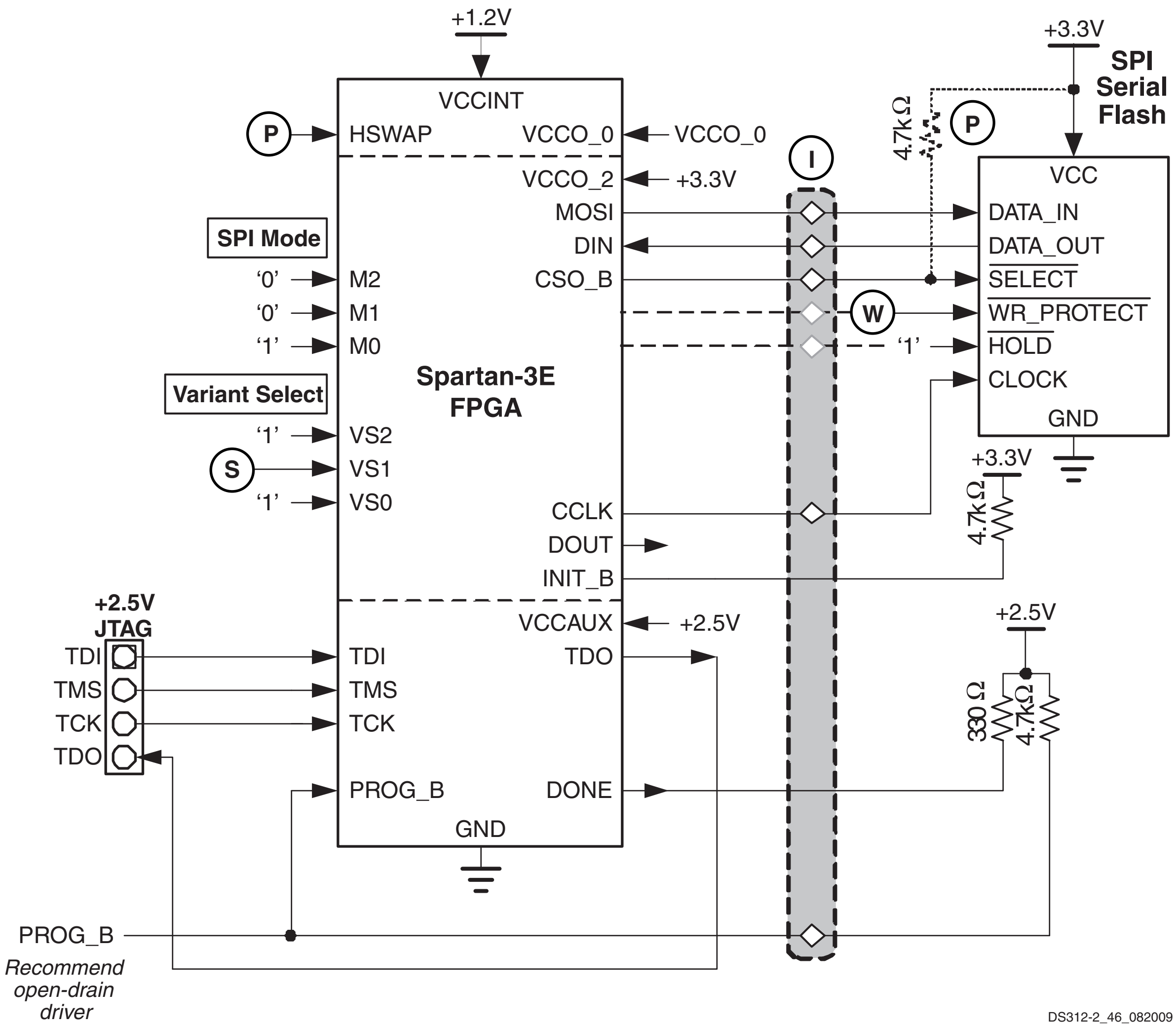

Figure 53: **SPI Flash PROM Interface for PROMs Supporting READ (0x03) and FAST_READ (0x0B) Commands**

S Although SPI is a standard four-wire interface, various available SPI Flash PROMs use different command protocols. The FPGA's variant select pins, VS[2:0], define how the FPGA communicates with the SPI Flash, including which SPI Flash command the FPGA issues to start the read operation and the number of dummy bytes inserted before the FPGA expects to receive valid data from the SPI Flash. Table 53 shows the available SPI Flash PROMs expected to operate with Spartan-3E FPGAs. Other compatible devices might work but have not been tested for suitability with Spartan-3E FPGAs. All other VS[2:0] values are reserved for future use. Consult the data sheet for the desired SPI Flash device to determine its suitability. The basic timing requirements and waveforms are provided in Serial Peripheral Interface (SPI) Configuration Timing in Module 3.

Figure 53 shows the general connection diagram for those SPI Flash PROMs that support the 0x03 READ command or the 0x0B FAST READ commands.

Figure 54 shows the connection diagram for Atmel DataFlash serial PROMs, which also use an SPI-based protocol. 'B'-series DataFlash devices are limited to FPGA applications operating over the commercial temperature range. Industrial temperature range applications must use 'C'- or 'D'-series DataFlash devices, which have a shorter DataFlash select setup time, because of the faster FPGA CCLK frequency at cold temperatures.

Table 59: **Byte-Wide Peripheral Interface (BPI) Connections *(Cont'd)***

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
HDC	Output	PROM Write Enable	Connect to PROM write-enable input (WE#). FPGA drives this signal High throughout configuration.	User I/O
LDC2 D	Output	PROM Byte Mode	This signal is not used for x8 PROMs. For PROMs with a x8/x16 data width control, connect to PROM byte-mode input (BYTE#). See Precautions Using x8/x16 Flash PROMs. FPGA drives this signal Low throughout configuration.	User I/O. Drive this pin High after configuration to use a x8/x16 PROM in x16 mode.
A[23:0]	Output	Address	Connect to PROM address inputs. High-order address lines may not be available in all packages and not all may be required. Number of address lines required depends on the size of the attached Flash PROM. FPGA address generation controlled by M0 mode pin. Addresses presented on falling CCLK edge. Only 20 address lines are available in TQ144 package.	User I/O
D[7:0]	Input	Data Input	FPGA receives byte-wide data on these pins in response the address presented on A[23:0]. Data captured by FPGA on rising edge of CCLK.	User I/O. If bitstream option ***Persist=Yes***, becomes part of SelectMap parallel peripheral interface.
CSO_B	Output	**Chip Select Output**. Active Low.	Not used in single FPGA applications. In a daisy-chain configuration, this pin connects to the CSI_B pin of the next FPGA in the chain. If HSWAP = 1 in a multi-FPGA daisy-chain application, connect this signal to a 4.7 kΩ pull-up resistor to VCCO_2. Actively drives Low when selecting a downstream device in the chain.	User I/O
BUSY	Output	**Busy Indicator**. Typically only used after configuration, if bitstream option ***Persist=Yes***.	Not used during configuration but actively drives.	User I/O. If bitstream option ***Persist=Yes***, becomes part of SelectMap parallel peripheral interface.
CCLK	Output	**Configuration Clock**. Generated by FPGA internal oscillator. Frequency controlled by ***ConfigRate*** bitstream generator option. If CCLK PCB trace is long or has multiple connections, terminate this output to maintain signal integrity. See CCLK Design Considerations.	Not used in single FPGA applications but actively drives. In a daisy-chain configuration, drives the CCLK inputs of all other FPGAs in the daisy-chain.	User I/O. If bitstream option ***Persist=Yes***, becomes part of SelectMap parallel peripheral interface.
INIT_B	Open-drain bidirectional I/O	**Initialization Indicator**. Active Low. Goes Low at start of configuration during the Initialization memory clearing process. Released at the end of memory clearing, when the mode select pins are sampled. In daisy-chain applications, this signal requires an external 4.7 kΩ pull-up resistor to VCCO_2.	Active during configuration. If CRC error detected during configuration, FPGA drives INIT_B Low.	User I/O. If unused in the application, drive INIT_B High.

Table 59: **Byte-Wide Peripheral Interface (BPI) Connections *(Cont'd)***

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
DONE	Open-drain bidirectional I/O	**FPGA Configuration Done**. Low during configuration. Goes High when FPGA successfully completes configuration. Requires external 330 Ω pull-up resistor to 2.5V.	Low indicates that the FPGA is not yet configured.	Pulled High via external pull-up. When High, indicates that the FPGA is successfully configured.
PROG_B	Input	**Program FPGA**. Active Low. When asserted Low for 500 ns or longer, forces the FPGA to restart its configuration process by clearing configuration memory and resetting the DONE and INIT_B pins once PROG_B returns High. Recommend external 4.7 kΩ pull-up resistor to 2.5V. Internal pull-up value may be weaker (see Table 78). If driving externally with a 3.3V output, use an open-drain or open-collector driver or use a current limiting series resistor.	Must be High to allow configuration to start.	Drive PROG_B Low and release to reprogram FPGA. Hold PROG_B to force FPGA I/O pins into Hi-Z, allowing direct programming access to Flash PROM pins.

Voltage Compatibility

V The FPGA's parallel Flash interface signals are within I/O Banks 1 and 2. The majority of parallel Flash PROMs use a single 3.3V supply voltage. Consequently, in most cases, the FPGA's VCCO_1 and VCCO_2 supply voltages must also be 3.3V to match the parallel Flash PROM. There are some 1.8V parallel Flash PROMs available and the FPGA interfaces with these devices if the VCCO_1 and VCCO_2 supplies are also 1.8V.

Power-On Precautions if PROM Supply is Last in Sequence

Like SPI Flash PROMs, parallel Flash PROMs typically require some amount of internal initialization time when the supply voltage reaches its minimum value.

The PROM supply voltage also connects to the FPGA's VCCO_2 supply input. In many systems, the PROM supply feeding the FPGA's VCCO_2 input is valid before the FPGA's other V_{CCINT} and V_{CCAUX} supplies, and consequently, there is no issue. However, if the PROM supply is last in the sequence, a potential race occurs between the FPGA and the parallel Flash PROM. See Power-On Precautions if 3.3V Supply is Last in Sequence for a similar description of the issue for SPI Flash PROMs.

Supported Parallel NOR Flash PROM Densities

Table 60 indicates the smallest usable parallel Flash PROM to program a single Spartan-3E FPGA. Parallel Flash density is specified in bits but addressed as bytes. The FPGA presents up to 24 address lines during configuration but not all are required for single FPGA applications. Table 60 shows the minimum required number of address lines between the FPGA and parallel Flash PROM. The actual number of address line required depends on the density of the attached parallel Flash PROM.

A multiple-FPGA daisy-chained application requires a parallel Flash PROM large enough to contain the sum of the FPGA file sizes. An application can also use a larger-density parallel Flash PROM to hold additional data beyond just FPGA configuration data. For example, the parallel Flash PROM can also contain the application code for a MicroBlaze RISC processor core implemented within the Spartan-3E FPGA. After configuration, the MicroBlaze processor can execute directly from external Flash or can copy the code to other, faster system memory before executing the code.

Table 60: **Number of Bits to Program a Spartan-3E FPGA and Smallest Parallel Flash PROM**

Spartan-3E FPGA	Uncompressed File Sizes (bits)	Smallest Usable Parallel Flash PROM	Minimum Required Address Lines
XC3S100E	581,344	1 Mbit	A[16:0]
XC3S250E	1,353,728	2 Mbit	A[17:0]
XC3S500E	2,270,208	4 Mbit	A[18:0]
XC3S1200E	3,841,184	4 Mbit	A[18:0]
XC3S1600E	5,969,696	8 Mbit	A[19:0]

Readback

FPGA configuration data can be read back using either the Slave Parallel or JTAG mode. This function is disabled if the Bitstream Generator ***Security*** option is set to either ***Level1*** or ***Level2***.

Along with the configuration data, it is possible to read back the contents of all registers and distributed RAM.

To synchronously control when register values are captured for readback, use the CAPTURE_SPARTAN3 library primitive, which applies for both Spartan-3 and Spartan-3E FPGA families.

The Readback feature is available in most Spartan-3E FPGA product options, as indicated in Table 68. The Readback feature is not available in the XC3S1200E and XC3S1600E FPGAs when using the -4 speed grade in the Commercial temperature grade. Similarly, block RAM Readback support is not available in the -4 speed grade, Commercial temperature devices. If Readback is required in an XC3S1200E or XC3S1600E FPGA, or if block RAM Readback is required on any Spartan-3E FPGA, upgrade to either the Industrial temperature grade version or the -5 speed grade.

The Xilinx iMPACT programming software uses the Readback feature for its optional Verify and Readback operations. The Xilinx ChipScope™ software presently does not use Readback but may in future updates.

Table 68: **Readback Support in Spartan-3E FPGAs**

Temperature Range	**Commercial**		**Industrial**
Speed Grade	**-4**	**-5**	**-4**
Block RAM Readback			
All Spartan-3E FPGAs	No	Yes	Yes
General Readback (registers, distributed RAM)			
XC3S100E	Yes	Yes	Yes
XC3S250E	Yes	Yes	Yes
XC3S500E	Yes	Yes	Yes
XC3S1200E	No	Yes	Yes
XC3S1600E	No	Yes	Yes

Differential I/O Standards

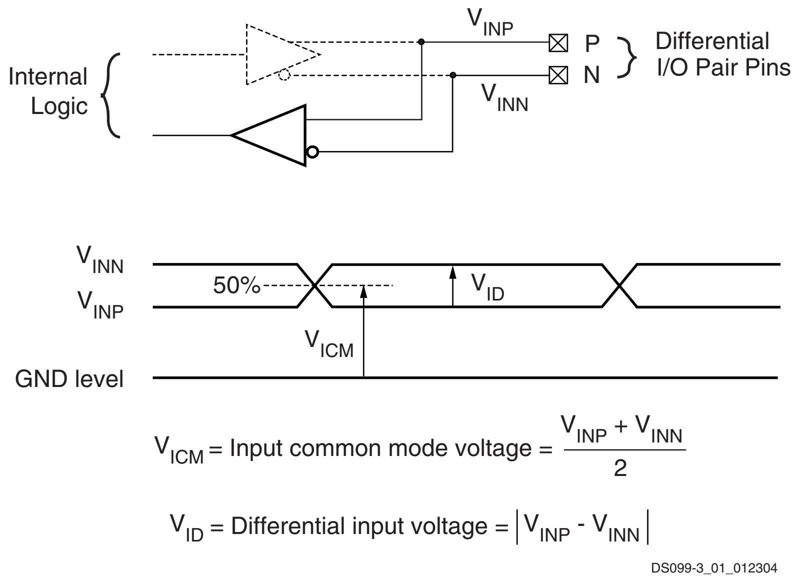

Figure 69: **Differential Input Voltages**

Table 82: **Recommended Operating Conditions for User I/Os Using Differential Signal Standards**

IOSTANDARD Attribute	V_{CCO} for Drivers(1)			V_{ID}			V_{ICM}		
	Min (V)	Nom (V)	Max (V)	Min (mV)	Nom (mV)	Max (mV)	Min (V)	Nom (V)	Max (V)
LVDS_25	2.375	2.50	2.625	100	350	600	0.30	1.25	2.20
BLVDS_25	2.375	2.50	2.625	100	350	600	0.30	1.25	2.20
MINI_LVDS_25	2.375	2.50	2.625	200	-	600	0.30	-	2.2
LVPECL_25(2)	Inputs Only			100	800	1000	0.5	1.2	2.0
RSDS_25	2.375	2.50	2.625	100	200	-	0.3	1.20	1.4
DIFF_HSTL_I_18	1.7	1.8	1.9	100	-	-	0.8	-	1.1
DIFF_HSTL_III_18	1.7	1.8	1.9	100	-	-	0.8	-	1.1
DIFF_SSTL18_I	1.7	1.8	1.9	100	-	-	0.7	-	1.1
DIFF_SSTL2_I	2.3	2.5	2.7	100	-	-	1.0	-	1.5

Notes:
1. The V_{CCO} rails supply only differential output drivers, not input circuits.
2. V_{REF} inputs are not used for any of the differential I/O standards.

Switching Characteristics

All Spartan-3E FPGAs ship in two speed grades: -4 and the higher performance -5. Switching characteristics in this document may be designated as Advance, Preliminary, or Production, as shown in Table 84. Each category is defined as follows:

Advance: These specifications are based on simulations only and are typically available soon after establishing FPGA specifications. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These specifications are based on complete early silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting preliminary delays is greatly reduced compared to Advance data.

Production: These specifications are approved once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Software Version Requirements

Production-quality systems must use FPGA designs compiled using a speed file designated as PRODUCTION status. FPGAs designs using a less mature speed file designation should only be used during system prototyping or pre-production qualification. FPGA designs with speed files designated as Advance or Preliminary should not be used in a production-quality system.

Whenever a speed file designation changes, as a device matures toward Production status, rerun the latest Xilinx ISE software on the FPGA design to ensure that the FPGA design incorporates the latest timing information and software updates.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all Spartan-3E devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.**

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Timing parameters and their representative values are selected for inclusion below either because they are important as general design requirements or they indicate fundamental device performance characteristics. The Spartan-3E speed files (v1.27), part of the Xilinx Development Software, are the original source for many but not all of the values. The speed grade designations for these files are shown in Table 84. For more complete, more precise, and worst-case data, use the values reported by the Xilinx static timing analyzer (TRACE in the Xilinx development software) and back-annotated to the simulation netlist.

Table 84: **Spartan-3E v1.27 Speed Grade Designations**

Device	Advance	Preliminary	Production
XC3S100E			-MIN, -4, -5
XC3S250E			-MIN, -4, -5
XC3S500E			-MIN, -4, -5
XC3S1200E			-MIN, -4, -5
XC3S1600E			-MIN, -4, -5

Table 85 provides the history of the Spartan-3E speed files since all devices reached Production status.

Table 85: **Spartan-3E Speed File Version History**

Version	ISE Release	Description
1.27	9.2.03i	Added XA Automotive.
1.26	8.2.02i	Added -0/-MIN speed grade, which includes minimum values.
1.25	8.2.01i	Added XA Automotive devices to speed file. Improved model for left and right DCMs.
1.23	8.2i	Updated input setup/hold values based on default IFD_DELAY_VALUE settings.
1.21	8.1.03i	All Spartan-3E FPGAs and all speed grades elevated to Production status.

Table 95: **Test Methods for Timing Measurement at I/Os *(Cont'd)***

Signal Standard (IOSTANDARD)	Inputs			Outputs		Inputs and Outputs
	V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
DIFF_HSTL_I_18	-	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{ICM}
DIFF_HSTL_III_18	-	V_{REF} – 0.5	V_{REF} + 0.5	50	1.8	V_{ICM}
DIFF_SSTL18_I	-	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{ICM}
DIFF_SSTL2_I	-	V_{REF} – 0.5	V_{REF} + 0.5	50	1.25	V_{ICM}

Notes:

1. Descriptions of the relevant symbols are as follows:
   V_{REF} – The reference voltage for setting the input switching threshold
   V_{ICM} – The common mode input voltage
   V_M – Voltage of measurement point on signal transition
   V_L – Low-level test voltage at Input pin
   V_H – High-level test voltage at Input pin
   R_T – Effective termination resistance, which takes on a value of 1MΩ when no parallel termination is required
   V_T – Termination voltage
2. The load capacitance (C_L) at the Output pin is 0 pF for all signal standards.
3. According to the PCI specification.

The capacitive load (C_L) is connected between the output and GND. *The Output timing for all standards, as published in the speed files and the data sheet, is always based on a C_L value of zero.* High-impedance probes (less than 1 pF) are used for all measurements. Any delay that the test fixture might contribute to test measurements is subtracted from those measurements to produce the final timing numbers as published in the speed files and data sheet.

Using IBIS Models to Simulate Load Conditions in Application

IBIS models permit the most accurate prediction of timing delays for a given application. The parameters found in the IBIS model (V_{REF}, R_{REF}, and V_{MEAS}) correspond directly with the parameters used in Table 95 (V_T, R_T, and V_M). Do not confuse V_{REF} (the termination voltage) from the IBIS model with V_{REF} (the input-switching threshold) from the table. A fourth parameter, C_{REF}, is always zero. The four parameters describe all relevant output test conditions. IBIS models are found in the Xilinx development software as well as at the following link:

http://www.xilinx.com/support/download/index.htm

Delays for a given application are simulated according to its specific load conditions as follows:

1. Simulate the desired signal standard with the output driver connected to the test setup shown in Figure 72. Use parameter values V_T, R_T, and V_M from Table 95. C_{REF} is zero.
2. Record the time to V_M.
3. Simulate the same signal standard with the output driver connected to the PCB trace with load. Use the appropriate IBIS model (including V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} values) or capacitive value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. Add (or subtract) the increase (or decrease) in delay to (or from) the appropriate Output standard adjustment (Table 94) to yield the worst-case delay of the PCB trace.

Table 105: **Switching Characteristics for the DLL**

Symbol	Description		Device	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Output Frequency Ranges								
CLKOUT_FREQ_CLK0	Frequency for the CLK0 and CLK180 outputs	Stepping 0	XC3S100E XC3S250E XC3S500E XC3S1600E	N/A	N/A	5	90	MHz
			XC3S1200E				200	MHz
		Stepping 1	All	5	275		240	MHz
CLKOUT_FREQ_CLK90	Frequency for the CLK90 and CLK270 outputs	Stepping 0	XC3S100E XC3S250E XC3S500E XC3S1600E	N/A	N/A	5	90	MHz
			XC3S1200E				167	MHz
		Stepping 1	All	5	200		200	MHz
CLKOUT_FREQ_2X	Frequency for the CLK2X and CLK2X180 outputs	Stepping 0	XC3S100E XC3S250E XC3S500E XC3S1600E	N/A	N/A	10	180	MHz
			XC3S1200E				311	MHz
		Stepping 1	All	10	333		311	MHz
CLKOUT_FREQ_DV	Frequency for the CLKDV output	Stepping 0	XC3S100E XC3S250E XC3S500E XC3S1600E	N/A	N/A	0.3125	60	MHz
			XC3S1200E				133	MHz
		Stepping 1	All	0.3125	183		160	MHz
Output Clock Jitter[2,3,4]								
CLKOUT_PER_JITT_0	Period jitter at the CLK0 output		All	-	±100	-	±100	ps
CLKOUT_PER_JITT_90	Period jitter at the CLK90 output			-	±150	-	±150	ps
CLKOUT_PER_JITT_180	Period jitter at the CLK180 output			-	±150	-	±150	ps
CLKOUT_PER_JITT_270	Period jitter at the CLK270 output			-	±150	-	±150	ps
CLKOUT_PER_JITT_2X	Period jitter at the CLK2X and CLK2X180 outputs			-	±[1% of CLKIN period + 150]	-	±[1% of CLKIN period + 150]	ps
CLKOUT_PER_JITT_DV1	Period jitter at the CLKDV output when performing integer division			-	±150	-	±150	ps
CLKOUT_PER_JITT_DV2	Period jitter at the CLKDV output when performing non-integer division			-	±[1% of CLKIN period + 200]	-	±[1% of CLKIN period + 200]	ps
Duty Cycle[4]								
CLKOUT_DUTY_CYCLE_DLL	Duty cycle variation for the CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV outputs, including the BUFGMUX and clock tree duty-cycle distortion		All	-	±[1% of CLKIN period + 400]	-	±[1% of CLKIN period + 400]	ps

Table 105: **Switching Characteristics for the DLL *(Cont'd)***

Symbol	Description		Device	Speed Grade -5 Min	Speed Grade -5 Max	Speed Grade -4 Min	Speed Grade -4 Max	Units
Phase Alignment(4)								
CLKIN_CLKFB_PHASE	Phase offset between the CLKIN and CLKFB inputs		All	-	±200	-	±200	ps
CLKOUT_PHASE_DLL	Phase offset between DLL outputs	CLK0 to CLK2X (not CLK2X180)	All	-	±[1% of CLKIN period + 100]	-	±[1% of CLKIN period + 100]	ps
		All others		-	±[1% of CLKIN period + 200]	-	±[1% of CLKIN period + 200]	ps
Lock Time								
LOCK_DLL(3)	When using the DLL alone: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase	5 MHz ≤ F_{CLKIN} ≤ 15 MHz	All	-	5	-	5	ms
		F_{CLKIN} > 15 MHz		-	600	-	600	µs
Delay Lines								
DCM_DELAY_STEP	Finest delay resolution		All	20	40	20	40	ps

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 77 and Table 104.
2. Indicates the maximum amount of output jitter that the DCM adds to the jitter on the CLKIN input.
3. For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
4. Some jitter and duty-cycle specifications include 1% of input clock period or 0.01 UI.
   Example: The data sheet specifies a maximum jitter of ±[1% of CLKIN period + 150]. Assume the CLKIN frequency is 100 MHz. The equivalent CLKIN period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 150 ps] = ±250 ps.

Digital Frequency Synthesizer (DFS)

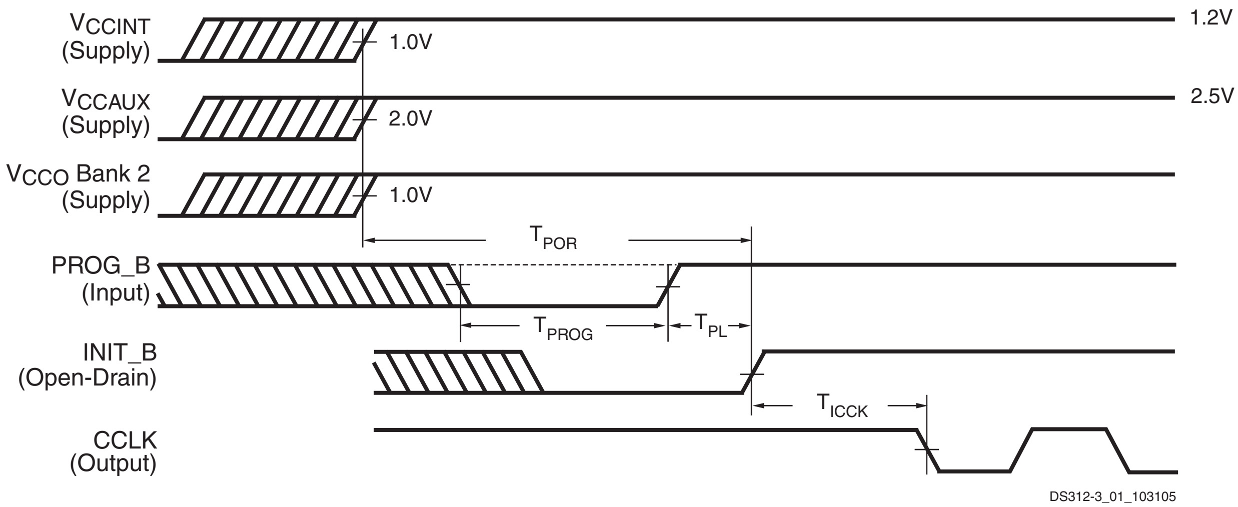
Table 106: **Recommended Operating Conditions for the DFS**

Symbol		Description		Speed Grade -5 Min	Speed Grade -5 Max	Speed Grade -4 Min	Speed Grade -4 Max	Units
Input Frequency Ranges(2)								
F_{CLKIN}	CLKIN_FREQ_FX	Frequency for the CLKIN input		0.200	333(4)	0.200	333(4)	MHz
Input Clock Jitter Tolerance(3)								
CLKIN_CYC_JITT_FX_LF		Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency	F_{CLKFX} ≤ 150 MHz	-	±300	-	±300	ps
CLKIN_CYC_JITT_FX_HF			F_{CLKFX} > 150 MHz	-	±150	-	±150	ps
CLKIN_PER_JITT_FX		Period jitter at the CLKIN input		-	±1	-	±1	ns

Notes:
1. DFS specifications apply when either of the DFS outputs (CLKFX or CLKFX180) are used.
2. If both DFS and DLL outputs are used on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 104.
3. CLKIN input jitter beyond these limits may cause the DCM to lose lock.
4. To support double the maximum effective FCLKIN limit, set the CLKIN_DIVIDE_BY_2 attribute to TRUE. This attribute divides the incoming clock frequency by two as it enters the DCM.

Configuration and JTAG Timing

General Configuration Power-On/Reconfigure Timing



Notes:
1. The V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies may be applied in any order.
2. The Low-going pulse on PROG_B is optional after power-on but necessary for reconfiguration without a power cycle.
3. The rising edge of INIT_B samples the voltage levels applied to the mode pins (M0 - M2).

Figure 73: **Waveforms for Power-On and the Beginning of Configuration**

Table 111: **Power-On Timing and the Beginning of Configuration**

Symbol	Description	Device	All Speed Grades		Units
			Min	Max	
T_{POR}[2]	The time from the application of V_{CCINT}, V_{CCAUX}, and V_{CCO} Bank 2 supply voltage ramps (whichever occurs last) to the rising transition of the INIT_B pin	XC3S100E	-	5	ms
		XC3S250E	-	5	ms
		XC3S500E	-	5	ms
		XC3S1200E	-	5	ms
		XC3S1600E	-	7	ms
T_{PROG}	The width of the low-going pulse on the PROG_B pin	All	0.5	-	µs
T_{PL}[2]	The time from the rising edge of the PROG_B pin to the rising transition on the INIT_B pin	XC3S100E	-	0.5	ms
		XC3S250E	-	0.5	ms
		XC3S500E	-	1	ms
		XC3S1200E	-	2	ms
		XC3S1600E	-	2	ms
T_{INIT}	Minimum Low pulse width on INIT_B output	All	250	-	ns
T_{ICCK}[3]	The time from the rising edge of the INIT_B pin to the generation of the configuration clock signal at the CCLK output pin	All	0.5	4.0	µs

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 77. This means power must be applied to all V_{CCINT}, V_{CCO}, and V_{CCAUX} lines.
2. Power-on reset and the clearing of configuration memory occurs during this period.
3. This specification applies only to the Master Serial, SPI, BPI-Up, and BPI-Down modes.

IEEE 1149.1/1532 JTAG Test Access Port Timing

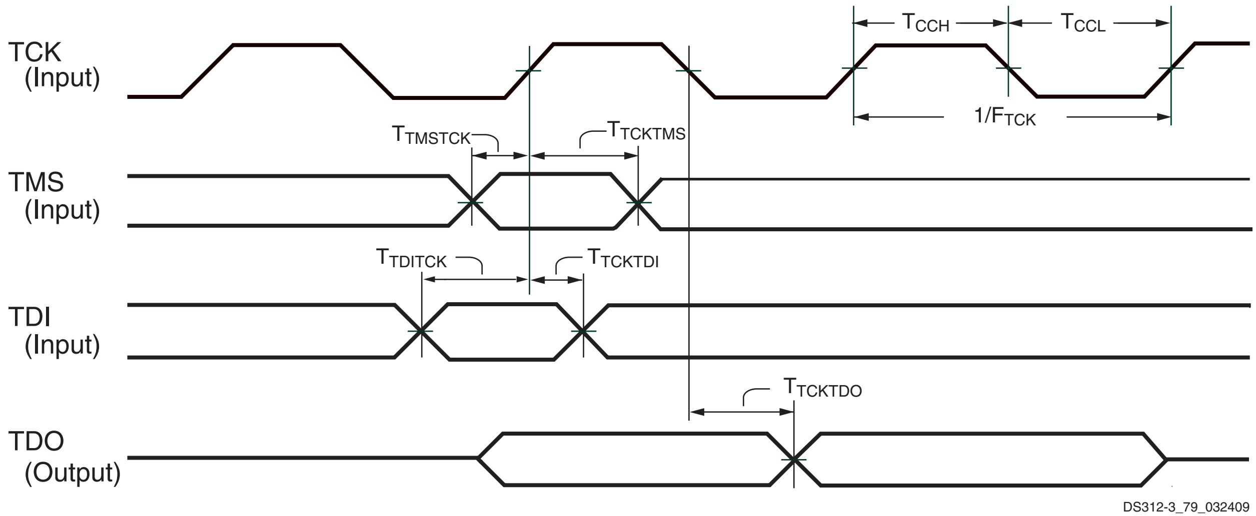


Figure 78: **JTAG Waveforms**

Table 123: **Timing for the JTAG Test Access Port**

Symbol	Description	All Speed Grades		Units
		Min	Max	
Clock-to-Output Times				
T_{TCKTDO}	The time from the falling transition on the TCK pin to data appearing at the TDO pin	1.0	11.0	ns
Setup Times				
T_{TDITCK}	The time from the setup of data at the TDI pin to the rising transition at the TCK pin	7.0	-	ns
T_{TMSTCK}	The time from the setup of a logic level at the TMS pin to the rising transition at the TCK pin	7.0	-	ns
Hold Times				
T_{TCKTDI}	The time from the rising transition at the TCK pin to the point when data is last held at the TDI pin	0	-	ns
T_{TCKTMS}	The time from the rising transition at the TCK pin to the point when a logic level is last held at the TMS pin	0	-	ns
Clock Timing				
T_{CCH}	The High pulse width at the TCK pin	5	-	ns
T_{CCL}	The Low pulse width at the TCK pin	5	-	ns
F_{TCK}	Frequency of the TCK signal	-	30	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 77.

Table 124: **Types of Pins on Spartan-3E FPGAs *(Cont'd)***

Type / Color Code	Description	Pin Name(s) in Type[(1)]
VCCAUX	Dedicated auxiliary power supply pin. The number of VCCAUX pins depends on the package used. All must be connected to +2.5V. See the Powering Spartan-3E FPGAs section in Module 2 for details.	VCCAUX
VCCINT	Dedicated internal core logic power supply pin. The number of VCCINT pins depends on the package used. All must be connected to +1.2V. See the Powering Spartan-3E FPGAs section in Module 2 for details.	VCCINT
VCCO	Along with all the other VCCO pins in the same bank, this pin supplies power to the output buffers within the I/O bank and sets the input threshold voltage for some I/O standards. See the Powering Spartan-3E FPGAs section in Module 2 for details.	VCCO_#
N.C.	This package pin is not connected in this specific device/package combination but may be connected in larger devices in the same package.	N.C.

Notes:

1. # = I/O bank number, an integer between 0 and 3.
2. IRDY/TRDY designations are for PCI designs; refer to PCI documentation for details.

Differential Pair Labeling

I/Os with Lxxy_# are part of a differential pair. 'L' indicates differential capability. The 'xx' field is a two-digit integer, unique to each bank that identifies a differential pin-pair. The 'y' field is either 'P' for the true signal or 'N' for the inverted signal in the differential pair. The '#' field is the I/O bank number.

The pin name suffix has the following significance. Figure 79 provides a specific example showing a differential input to and a differential output from Bank 1.

'L' indicates that the pin is part of a differential pair.

'xx' is a two-digit integer, unique for each bank, that identifies a differential pin-pair.

'y' is replaced by 'P' for the true signal or 'N' for the inverted. These two pins form one differential pin-pair.

'#' is an integer, 0 through 3, indicating the associated I/O bank.

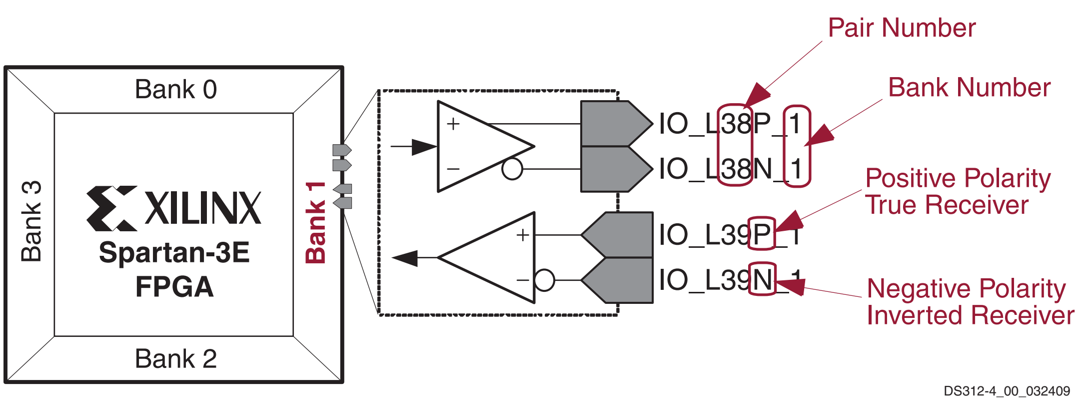


Figure 79: **Differential Pair Labeling**

Package Overview

Table 125 shows the eight low-cost, space-saving production package styles for the Spartan-3E family. Each package style is available as a standard and an environmentally friendly lead-free (Pb-free) option. The Pb-free packages include an extra 'G' in the package style name. For example, the standard "VQ100" package becomes "VQG100" when ordered as the Pb-free option. The mechanical dimensions of the standard and Pb-free packages are similar, as shown in the mechanical drawings provided in Table 127.

Not all Spartan-3E densities are available in all packages. For a specific package, however, there is a common footprint that supports all the devices available in that package. See the footprint diagrams that follow.

For additional package information, see UG112: *Device Package User Guide*.

Table 125: **Spartan-3E Family Package Options**

Package	Leads	Type	Maximum I/O	Lead Pitch (mm)	Footprint Area (mm)	Height (mm)	Mass[1] (g)
VQ100 / VQG100	100	Very-thin Quad Flat Pack (VQFP)	66	0.5	16 x 16	1.20	0.6
CP132 / CPG132	132	Chip-Scale Package (CSP)	92	0.5	8.1 x 8.1	1.10	0.1
TQ144 / TQG144	144	Thin Quad Flat Pack (TQFP)	108	0.5	22 x 22	1.60	1.4
PQ208 / PQG208	208	Plastic Quad Flat Pack (PQFP)	158	0.5	30.6 x 30.6	4.10	5.3
FT256 / FTG256	256	Fine-pitch, Thin Ball Grid Array (FBGA)	190	1.0	17 x 17	1.55	0.9
FG320 / FGG320	320	Fine-pitch Ball Grid Array (FBGA)	250	1.0	19 x 19	2.00	1.4
FG400 / FGG400	400	Fine-pitch Ball Grid Array (FBGA)	304	1.0	21 x 21	2.43	2.2
FG484 / FGG484	484	Fine-pitch Ball Grid Array (FBGA)	376	1.0	23 x 23	2.60	2.2

Notes:

1. Package mass is ±10%.

Selecting the Right Package Option

Spartan-3E FPGAs are available in both quad-flat pack (QFP) and ball grid array (BGA) packaging options. While QFP packaging offers the lowest absolute cost, the BGA packages are superior in almost every other aspect, as summarized in Table 126. Consequently, Xilinx recommends using BGA packaging whenever possible.

Table 126: **QFP and BGA Comparison**

Characteristic	Quad Flat Pack (QFP)	Ball Grid Array (BGA)
Maximum User I/O	158	376
Packing Density (Logic/Area)	Good	Better
Signal Integrity	Fair	Better
Simultaneous Switching Output (SSO) Support	Fair	Better
Thermal Dissipation	Fair	Better
Minimum Printed Circuit Board (PCB) Layers	4	4-6
Hand Assembly/Rework	Possible	Difficult

PQ208 Footprint (Right)

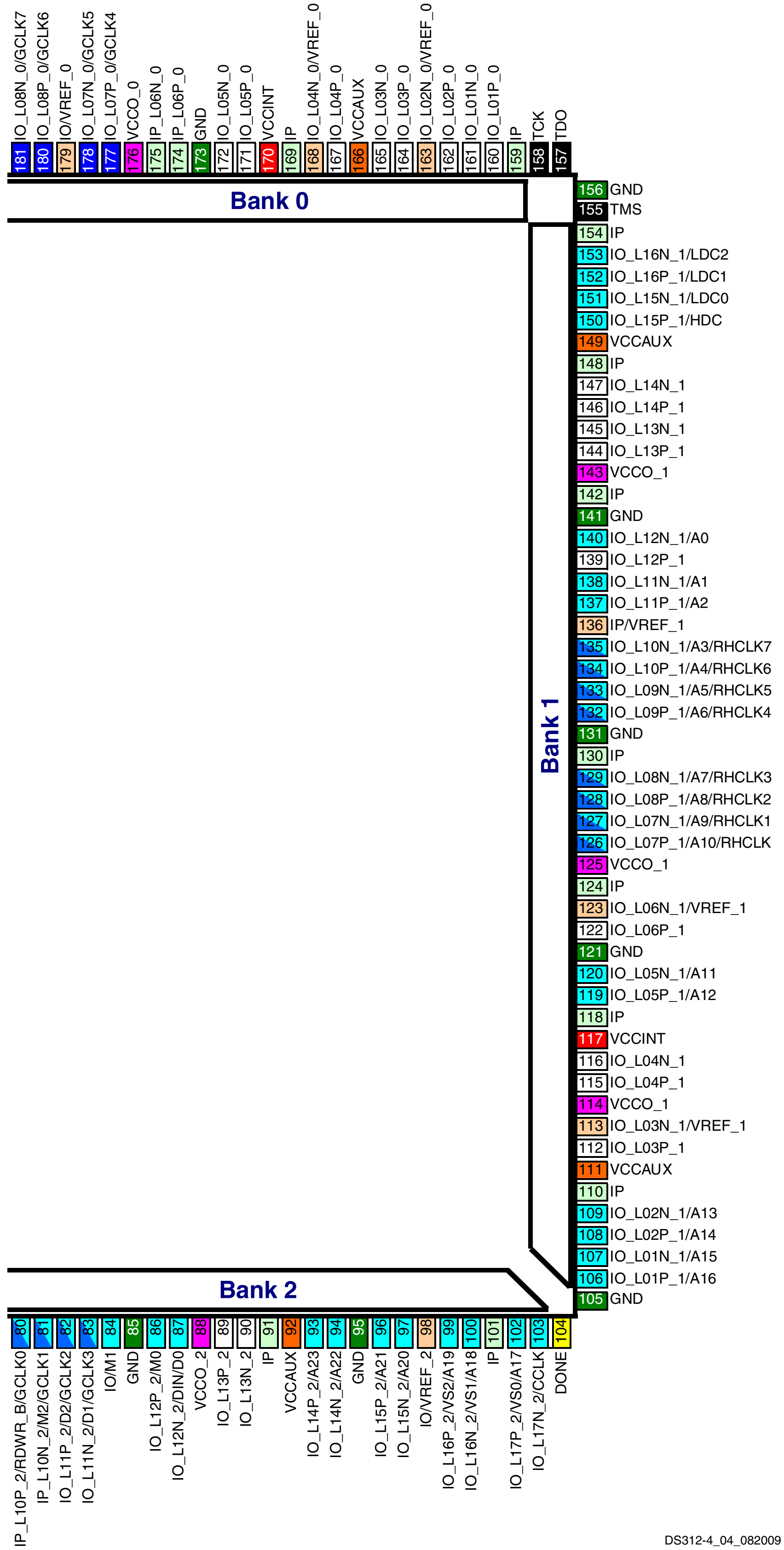


Figure 84: **PQ208 Footprint (Right)**

FT256: 256-ball Fine-pitch, Thin Ball Grid Array

The 256-ball fine-pitch, thin ball grid array package, FT256, supports three different Spartan-3E FPGAs, including the XC3S250E, the XC3S500E, and the XC3S1200E.

Table 143 lists all the package pins. They are sorted by bank number and then by pin name of the largest device. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The highlighted rows indicate pinout differences between the XC3S250E, the XC3S500E, and the XC3S1200E FPGAs. The XC3S250E has 18 unconnected balls, indicated as N.C. (No Connection) in Table 143 and with the black diamond character (◆) in Table 143 and Figure 83.

If the table row is highlighted in tan, then this is an instance where an unconnected pin on the XC3S250E FPGA maps to a VREF pin on the XC3S500E and XC3S1200E FPGA. If the FPGA application uses an I/O standard that requires a VREF voltage reference, connect the highlighted pin to the VREF voltage supply, even though this does not actually connect to the XC3S250E FPGA. This VREF connection on the board allows future migration to the larger devices without modifying the printed-circuit board.

All other balls have nearly identical functionality on all three devices. Table 147 summarizes the Spartan-3E footprint migration differences for the FT256 package.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx web site at:

http://www.xilinx.com/support/documentation/data_sheets/s3e_pin.zip

Pinout Table

Table 143: **FT256 Package Pinout**

Bank	XC3S250E Pin Name	XC3S500E Pin Name	XC3S1200E Pin Name	FT256 Ball	Type
0	IO	IO	IO	A7	I/O
0	IO	IO	IO	A12	I/O
0	IO	IO	IO	B4	I/O
0	IP	IP	IO	B6	***250E:*** INPUT ***500E:*** INPUT ***1200E:*** I/O
0	IP	IP	IO	B10	***250E:*** INPUT ***500E:*** INPUT ***1200E:*** I/O
0	IO/VREF_0	IO/VREF_0	IO/VREF_0	D9	VREF
0	IO_L01N_0	IO_L01N_0	IO_L01N_0	A14	I/O
0	IO_L01P_0	IO_L01P_0	IO_L01P_0	B14	I/O
0	IO_L03N_0/VREF_0	IO_L03N_0/VREF_0	IO_L03N_0/VREF_0	A13	VREF
0	IO_L03P_0	IO_L03P_0	IO_L03P_0	B13	I/O
0	IO_L04N_0	IO_L04N_0	IO_L04N_0	E11	I/O
0	IO_L04P_0	IO_L04P_0	IO_L04P_0	D11	I/O
0	IO_L05N_0/VREF_0	IO_L05N_0/VREF_0	IO_L05N_0/VREF_0	B11	VREF
0	IO_L05P_0	IO_L05P_0	IO_L05P_0	C11	I/O
0	IO_L06N_0	IO_L06N_0	IO_L06N_0	E10	I/O
0	IO_L06P_0	IO_L06P_0	IO_L06P_0	D10	I/O
0	IO_L08N_0/GCLK5	IO_L08N_0/GCLK5	IO_L08N_0/GCLK5	F9	GCLK
0	IO_L08P_0/GCLK4	IO_L08P_0/GCLK4	IO_L08P_0/GCLK4	E9	GCLK
0	IO_L09N_0/GCLK7	IO_L09N_0/GCLK7	IO_L09N_0/GCLK7	A9	GCLK
0	IO_L09P_0/GCLK6	IO_L09P_0/GCLK6	IO_L09P_0/GCLK6	A10	GCLK
0	IO_L11N_0/GCLK11	IO_L11N_0/GCLK11	IO_L11N_0/GCLK11	D8	GCLK
0	IO_L11P_0/GCLK10	IO_L11P_0/GCLK10	IO_L11P_0/GCLK10	C8	GCLK
0	IO_L12N_0	IO_L12N_0	IO_L12N_0	F8	I/O

User I/Os by Bank

Table 149 and Table 150 indicate how the available user-I/O pins are distributed between the four I/O banks on the FG320 package.

Table 149: **User I/Os Per Bank for XC3S500E in the FG320 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF[1]	CLK[2]
Top	0	58	29	14	1	6	8
Right	1	58	22	10	21	5	0[2]
Bottom	2	58	17	13	24	4	0[2]
Left	3	58	34	11	0	5	8
TOTAL		**232**	**102**	**48**	**46**	**20**	**16**

Notes:

1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

Table 150: **User I/Os Per Bank for XC3S1200E and XC3S1600E in the FG320 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF[1]	CLK[2]
Top	0	61	34	12	1	6	8
Right	1	63	25	12	21	5	0[2]
Bottom	2	63	23	11	24	5	0[2]
Left	3	63	38	12	0	5	8
TOTAL		**250**	**120**	**47**	**46**	**21**	**16**

Notes:

1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

Table 152: **FG400 Package Pinout *(Cont'd)***

Bank	XC3S1200E XC3S1600E Pin Name	FG400 Ball	Type
0	IP_L17P_0/GCLK8	H10	GCLK
0	IP_L20N_0	G9	INPUT
0	IP_L20P_0	G8	INPUT
0	IP_L23N_0	C8	INPUT
0	IP_L23P_0	D8	INPUT
0	IP_L26N_0	E6	INPUT
0	IP_L26P_0	E7	INPUT
0	IP_L29N_0	A4	INPUT
0	IP_L29P_0	A5	INPUT
0	VCCO_0	B4	VCCO
0	VCCO_0	B10	VCCO
0	VCCO_0	B16	VCCO
0	VCCO_0	D7	VCCO
0	VCCO_0	D13	VCCO
0	VCCO_0	F10	VCCO
1	IO_L01N_1/A15	U18	DUAL
1	IO_L01P_1/A16	U17	DUAL
1	IO_L02N_1/A13	T18	DUAL
1	IO_L02P_1/A14	T17	DUAL
1	IO_L03N_1/VREF_1	V19	VREF
1	IO_L03P_1	U19	I/O
1	IO_L04N_1	W20	I/O
1	IO_L04P_1	V20	I/O
1	IO_L05N_1	R18	I/O
1	IO_L05P_1	R17	I/O
1	IO_L06N_1	T20	I/O
1	IO_L06P_1	U20	I/O
1	IO_L07N_1	P18	I/O
1	IO_L07P_1	P17	I/O
1	IO_L08N_1/VREF_1	P20	VREF
1	IO_L08P_1	R20	I/O
1	IO_L09N_1	P16	I/O
1	IO_L09P_1	N16	I/O
1	IO_L10N_1	N19	I/O
1	IO_L10P_1	N18	I/O
1	IO_L11N_1	N15	I/O
1	IO_L11P_1	M15	I/O
1	IO_L12N_1/A11	M18	DUAL
1	IO_L12P_1/A12	M17	DUAL
1	IO_L13N_1/VREF_1	L19	VREF
1	IO_L13P_1	M19	I/O
1	IO_L14N_1/A9/RHCLK1	L16	RHCLK/ DUAL

Table 152: **FG400 Package Pinout *(Cont'd)***

Bank	XC3S1200E XC3S1600E Pin Name	FG400 Ball	Type
1	IO_L14P_1/A10/RHCLK0	M16	RHCLK/ DUAL
1	IO_L15N_1/A7/RHCLK3/ TRDY1	L14	RHCLK/ DUAL
1	IO_L15P_1/A8/RHCLK2	L15	RHCLK/ DUAL
1	IO_L16N_1/A5/RHCLK5	K14	RHCLK/ DUAL
1	IO_L16P_1/A6/RHCLK4/ IRDY1	K13	RHCLK/ DUAL
1	IO_L17N_1/A3/RHCLK7	J20	RHCLK/ DUAL
1	IO_L17P_1/A4/RHCLK6	K20	RHCLK/ DUAL
1	IO_L18N_1/A1	K16	DUAL
1	IO_L18P_1/A2	J16	DUAL
1	IO_L19N_1/A0	J13	DUAL
1	IO_L19P_1	J14	I/O
1	IO_L20N_1	J17	I/O
1	IO_L20P_1	J18	I/O
1	IO_L21N_1	H19	I/O
1	IO_L21P_1	J19	I/O
1	IO_L22N_1	H15	I/O
1	IO_L22P_1	H16	I/O
1	IO_L23N_1	H18	I/O
1	IO_L23P_1	H17	I/O
1	IO_L24N_1/VREF_1	H20	VREF
1	IO_L24P_1	G20	I/O
1	IO_L25N_1	G16	I/O
1	IO_L25P_1	F16	I/O
1	IO_L26N_1	F19	I/O
1	IO_L26P_1	F20	I/O
1	IO_L27N_1	F18	I/O
1	IO_L27P_1	F17	I/O
1	IO_L28N_1	D20	I/O
1	IO_L28P_1	E20	I/O
1	IO_L29N_1/LDC0	D18	DUAL
1	IO_L29P_1/HDC	E18	DUAL
1	IO_L30N_1/LDC2	C19	DUAL
1	IO_L30P_1/LDC1	C20	DUAL
1	IP	B20	INPUT
1	IP	G15	INPUT
1	IP	G18	INPUT
1	IP	H14	INPUT
1	IP	J15	INPUT