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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	240
Number of Logic Elements/Cells	2160
Total RAM Bits	73728
Number of I/O	66
Number of Gates	100000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s100e-4vq100i

Architectural Overview

The Spartan-3E family architecture consists of five fundamental programmable functional elements:

- **Configurable Logic Blocks (CLBs)** contain flexible Look-Up Tables (LUTs) that implement logic plus storage elements used as flip-flops or latches. CLBs perform a wide variety of logical functions as well as store data.
- **Input/Output Blocks (IOBs)** control the flow of data between the I/O pins and the internal logic of the device. Each IOB supports bidirectional data flow plus 3-state operation. Supports a variety of signal standards, including four high-performance differential standards. Double Data-Rate (DDR) registers are included.
- **Block RAM** provides data storage in the form of 18-Kbit dual-port blocks.
- **Multiplier Blocks** accept two 18-bit binary numbers as inputs and calculate the product.
- **Digital Clock Manager (DCM) Blocks** provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase-shifting clock signals.

These elements are organized as shown in Figure 1. A ring of IOBs surrounds a regular array of CLBs. Each device has two columns of block RAM except for the XC3S100E, which has one column. Each RAM column consists of several 18-Kbit RAM blocks. Each block RAM is associated with a dedicated multiplier. The DCMs are positioned in the center with two at the top and two at the bottom of the device. The XC3S100E has only one DCM at the top and bottom, while the XC3S1200E and XC3S1600E add two DCMs in the middle of the left and right sides.

The Spartan-3E family features a rich network of traces that interconnect all five functional elements, transmitting signals among them. Each functional element has an associated switch matrix that permits multiple connections to the routing.

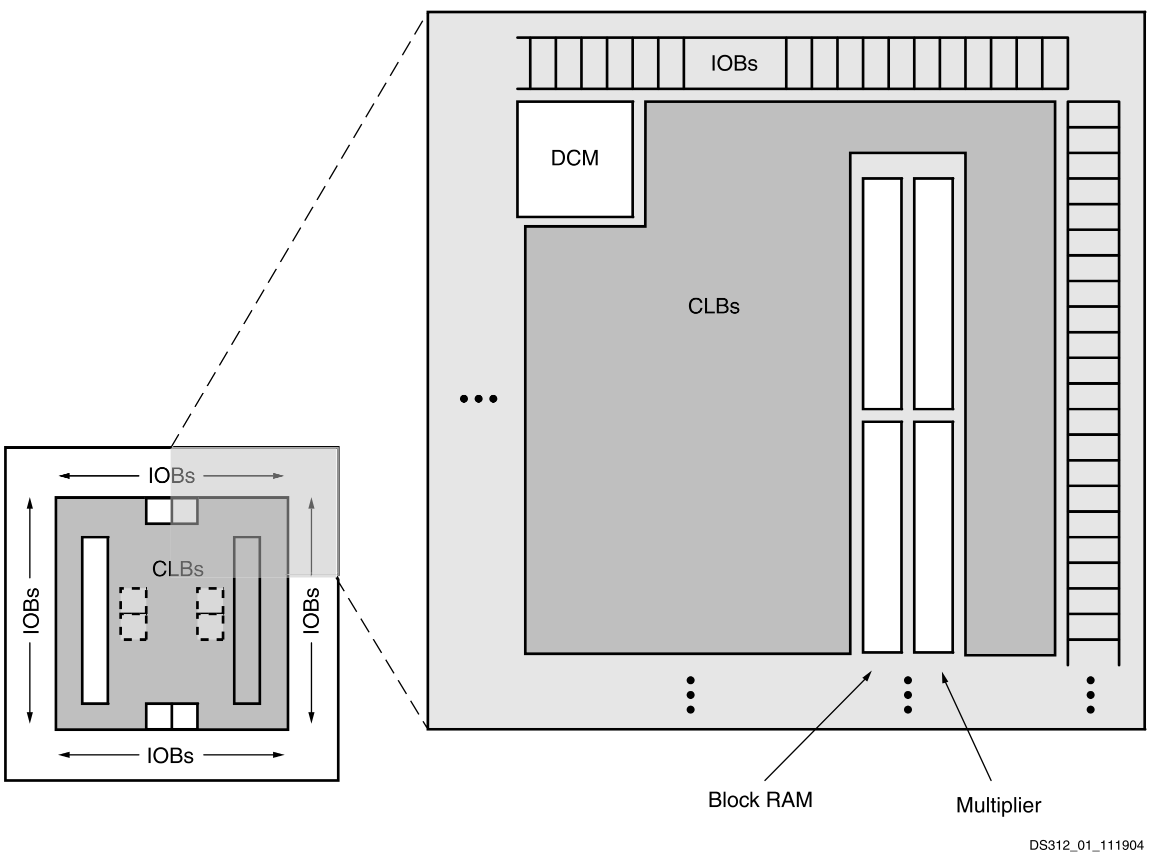


Figure 1: **Spartan-3E Family Architecture**

Double-Data-Rate Transmission

Double-Data-Rate (DDR) transmission describes the technique of synchronizing signals to both the rising and falling edges of the clock signal. Spartan-3E devices use register pairs in all three IOB paths to perform DDR operations.

The pair of storage elements on the IOB's Output path (OFF1 and OFF2), used as registers, combine with a special multiplexer to form a DDR D-type flip-flop (ODDR2). This primitive permits DDR transmission where output data bits are synchronized to both the rising and falling edges of a clock. DDR operation requires two clock signals (usually 50% duty cycle), one the inverted form of the other. These signals trigger the two registers in alternating fashion, as shown in Figure 7. The Digital Clock Manager (DCM) generates the two clock signals by mirroring an incoming signal, and then shifting it 180 degrees. This approach ensures minimal skew between the two signals. Alternatively, the inverter inside the IOB can be used to invert the clock signal, thus only using one clock line and both rising and falling edges of that clock line as the two clocks for the DDR flip-flops.

The storage-element pair on the Three-State path (TFF1 and TFF2) also can be combined with a local multiplexer to form a DDR primitive. This permits synchronizing the output enable to both the rising and falling edges of a clock. This DDR operation is realized in the same way as for the output path.

The storage-element pair on the input path (IFF1 and IFF2) allows an I/O to receive a DDR signal. An incoming DDR clock signal triggers one register, and the inverted clock signal triggers the other register. The registers take turns capturing bits of the incoming DDR data signal. The primitive to allow this functionality is called IDDR2.

Aside from high bandwidth data transfers, DDR outputs also can be used to reproduce, or *mirror*, a clock signal on the output. This approach is used to transmit clock and data signals together (source synchronously). A similar approach is used to reproduce a clock signal at multiple outputs. The advantage for both approaches is that skew across the outputs is minimal.

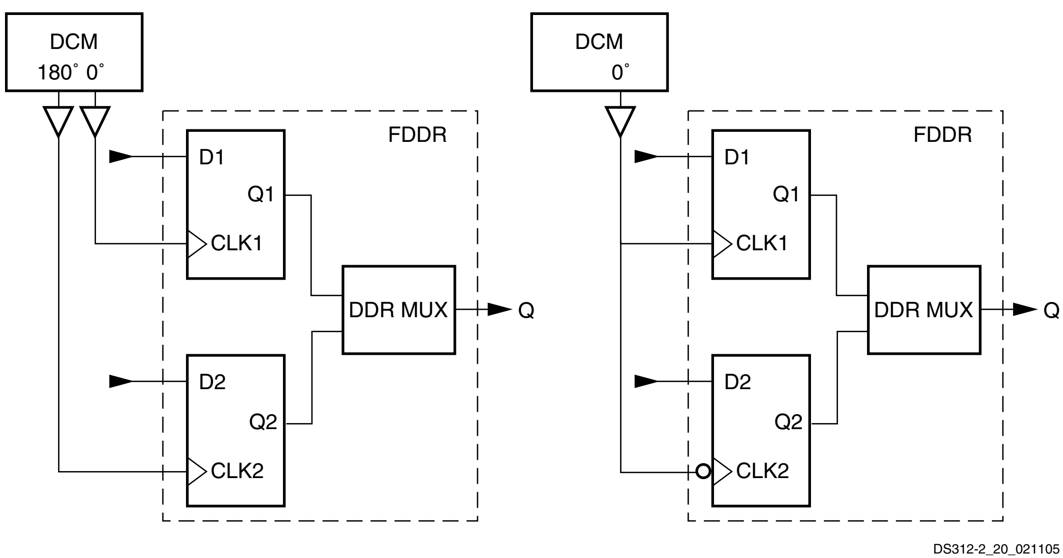


Figure 7: **Two Methods for Clocking the DDR Register**

Register Cascade Feature

In the Spartan-3E family, one of the IOBs in a differential pair can cascade its input storage elements with those in the other IOB as part of a differential pair. This is intended to make DDR operation at high speed much simpler to implement. The new DDR connections that are available are shown in Figure 5 (dashed lines), and are only available for routing between IOBs and are not accessible to the FPGA fabric. Note that this feature is only available when using the differential I/O standards LVDS, RSDS, and MINI_LVDS.

IDDR2

As a DDR input pair, the master IOB registers incoming data on the rising edge of ICLK1 (= D1) and the rising edge of ICLK2 (= D2), which is typically the same as the falling edge of ICLK1. This data is then transferred into the FPGA fabric. At some point, both signals must be brought into the same clock domain, typically ICLK1. This can be difficult at high frequencies because the available time is only one half of a clock cycle assuming a 50% duty cycle. See Figure 8 for a graphical illustration of this function.

Table 14: **Carry Logic Functions *(Cont'd)***

Function	Description
CY0G	Carry generation for top half of slice. Fixed selection of: · G1 or G2 inputs to the LUT (both equal 1 when a carry is to be generated) · GAND gate for multiplication · BY input for carry initialization · Fixed 1 or 0 input for use as a simple Boolean function
CYMUXF	Carry generation or propagation mux for bottom half of slice. Dynamic selection via CYSELF of: · CYINIT carry propagation (CYSELF = 1) · CY0F carry generation (CYSELF = 0)
CYMUXG	Carry generation or propagation mux for top half of slice. Dynamic selection via CYSELF of: · CYMUXF carry propagation (CYSELG = 1) · CY0G carry generation (CYSELG = 0)
CYSELF	Carry generation or propagation select for bottom half of slice. Fixed selection of: · F-LUT output (typically XOR result) · Fixed 1 to always propagate
CYSELG	Carry generation or propagation select for top half of slice. Fixed selection of: · G-LUT output (typically XOR result) · Fixed 1 to always propagate
XORF	Sum generation for bottom half of slice. Inputs from: · F-LUT · CYINIT carry signal from previous stage Result is sent to either the combinatorial or registered output for the top of the slice.
XORG	Sum generation for top half of slice. Inputs from: · G-LUT · CYMUXF carry signal from previous stage Result is sent to either the combinatorial or registered output for the top of the slice.
FAND	Multiplier partial product for bottom half of slice. Inputs: · F-LUT F1 input · F-LUT F2 input Result is sent through CY0F to become the carry generate signal into CYMUXF
GAND	Multiplier partial product for top half of slice. Inputs: · G-LUT G1 input · G-LUT G2 input Result is sent through CY0G to become the carry generate signal into CYMUXG

The basic usage of the carry logic is to generate a half-sum in the LUT via an XOR function, which generates or propagates a carry out COUT via the carry mux CYMUXF (or CYMUXG), and then complete the sum with the dedicated XORF (or XORG) gate and the carry input CIN. This structure allows two bits of an arithmetic function in each slice. The CYMUXF (or CYMUXG) can be instantiated using the MUXCY element, and the XORF (or XORG) can be instantiated using the XORCY element.

The FAND (or GAND) gate is used for partial product multiplication and can be instantiated using the MULT_AND component. Partial products are generated by two-input AND gates and then added. The carry logic is efficient for the adder, but one of the inputs must be outside the LUT as shown in Figure 23.

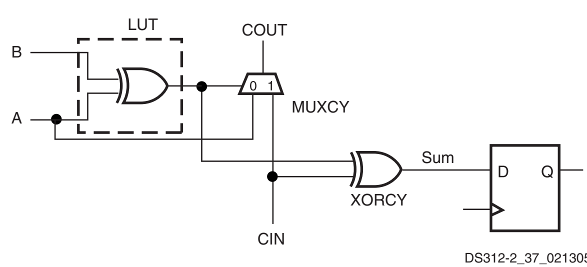


Figure 23: **Using the MUXCY and XORCY in the Carry Logic**

The FAND (or GAND) gate is used to duplicate one of the partial products, while the LUT generates both partial products and the XOR function, as shown in Figure 24.

cancel out the clock skew. When the DLL phase-aligns the CLK0 signal with the CLKIN signal, it asserts the LOCKED output, indicating a lock on to the CLKIN signal.

DLL Attributes and Related Functions

The DLL unit has a variety of associated attributes as described in Table 29. Each attribute is described in detail in the sections that follow.

Table 29: **DLL Attributes**

Attribute	Description	Values
CLK_FEEDBACK	Chooses either the CLK0 or CLK2X output to drive the CLKFB input	NONE, ***1X***, 2X
CLKIN_DIVIDE_BY_2	Halves the frequency of the CLKIN signal just as it enters the DCM	***FALSE***, TRUE
CLKDV_DIVIDE	Selects the constant used to divide the CLKIN input frequency to generate the CLKDV output frequency	1.5, ***2***, 2.5, 3, 3.5, 4, 4.5, 5, 5.5, 6.0, 6.5, 7.0, 7.5, 8, 9, 10, 11, 12, 13, 14, 15, and 16
CLKIN_PERIOD	Additional information that allows the DLL to operate with the most efficient lock time and the best jitter tolerance	Floating-point value representing the CLKIN period in nanoseconds

DLL Clock Input Connections

For best results, an external clock source enters the FPGA via a Global Clock Input (GCLK). Each specific DCM has four possible direct, optimal GCLK inputs that feed the DCM's CLKIN input, as shown in Table 30. Table 30 also provides the specific pin numbers by package for each GCLK input. The two additional DCM's on the XC3S1200E and XC3S1600E have similar optimal connections from the left-edge LHCLK and the right-edge RHCLK inputs, as described in Table 31 and Table 32.

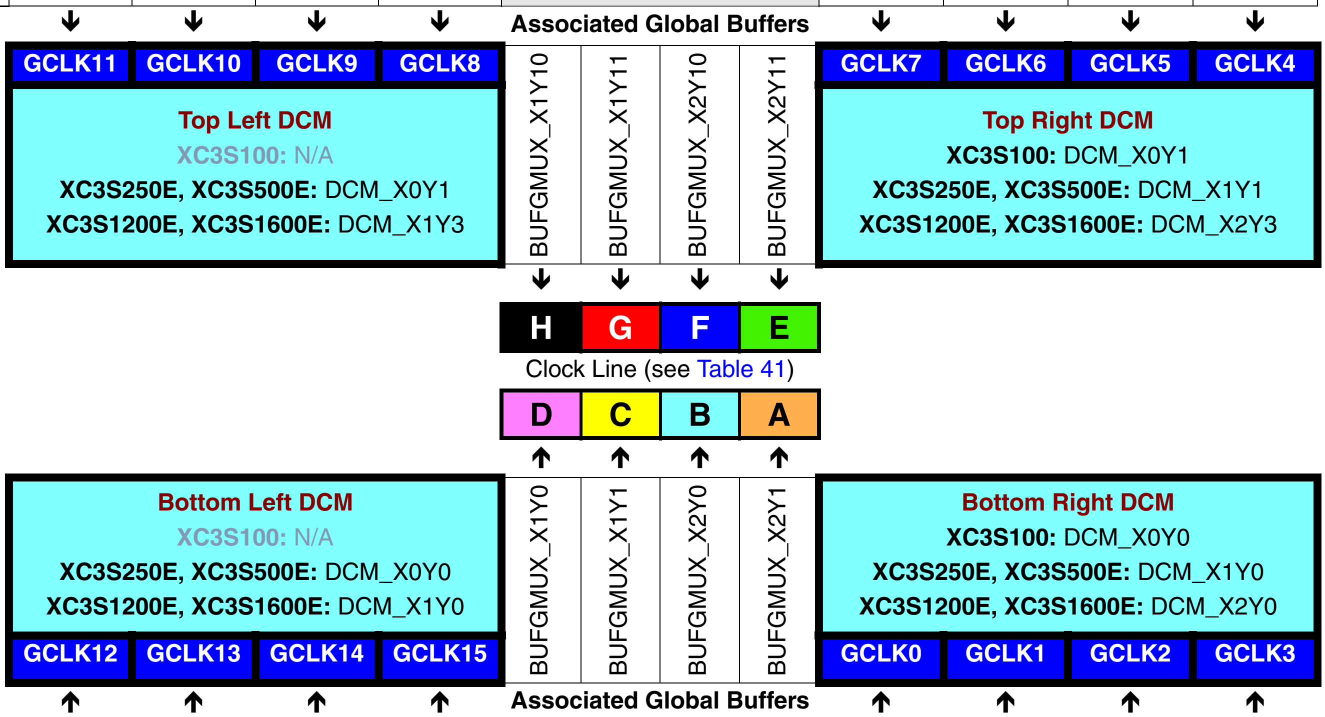
- The DCM supports differential clock inputs (for example, LVDS, LVPECL_25) via a pair of GCLK inputs that feed an internal single-ended signal to the DCM's CLKIN input.

Design Note

Avoid using global clock input GCLK1 as it is always shared with the M2 mode select pin. Global clock inputs GCLK0, GCLK2, GCLK3, GCLK12, GCLK13, GCLK14, and GCLK15 have shared functionality in some configuration modes.

Table 30: **Direct Clock Input Connections and Optional External Feedback to Associated DCMs**

Package	Differential Pair		Differential Pair		Differential Pair		Differential Pair	
	N	P	N	P	N	P	N	P
	Pin Number for Single-Ended Input				Pin Number for Single-Ended Input			
VQ100	P91	P90	P89	P88	P86	P85	P84	P83
CP132	B7	A7	C8	B8	A9	B9	C9	A10
TQ144	P131	P130	P129	P128	P126	P125	P123	P122
PQ208	P186	P185	P184	P183	P181	P180	P178	P177
FT256	D8	C8	B8	A8	A9	A10	F9	E9
FG320	D9	C9	B9	B8	A10	B10	E10	D10
FG400	A9	A10	G10	H10	E10	E11	G11	F11
FG484	B11	C11	H11	H12	C12	B12	E12	F12



Package	Differential Pair		Differential Pair		Differential Pair		Differential Pair	
	P	N	P	N	P	N	P	N
	Pin Number for Single-Ended Input				Pin Number for Single-Ended Input			
VQ100	P32	P33	P35	P36	P38	P39	P40	P41
CP132	M4	N4	M5	N5	M6	N6	P6	P7
TQ144	P50	P51	P53	P54	P56	P57	P58	P59
PQ208	P74	P75	P77	P78	P80	P81	P82	P83
FT256	M8	L8	N8	P8	T9	R9	P9	N9
FG320	N9	M9	U9	V9	U10	T10	R10	P10
FG400	W9	W10	R10	P10	P11	P12	V10	V11
FG484	V11	U11	R11	T11	R12	P12	Y12	W12

During the configuration process, CCLK is controlled by the FPGA and limited to the frequencies generated by the FPGA. After configuration, the FPGA application can use other clock signals to drive the CCLK pin and can further optimize SPI-based communication.

Refer to the individual SPI peripheral data sheet for specific interface and communication protocol requirements.

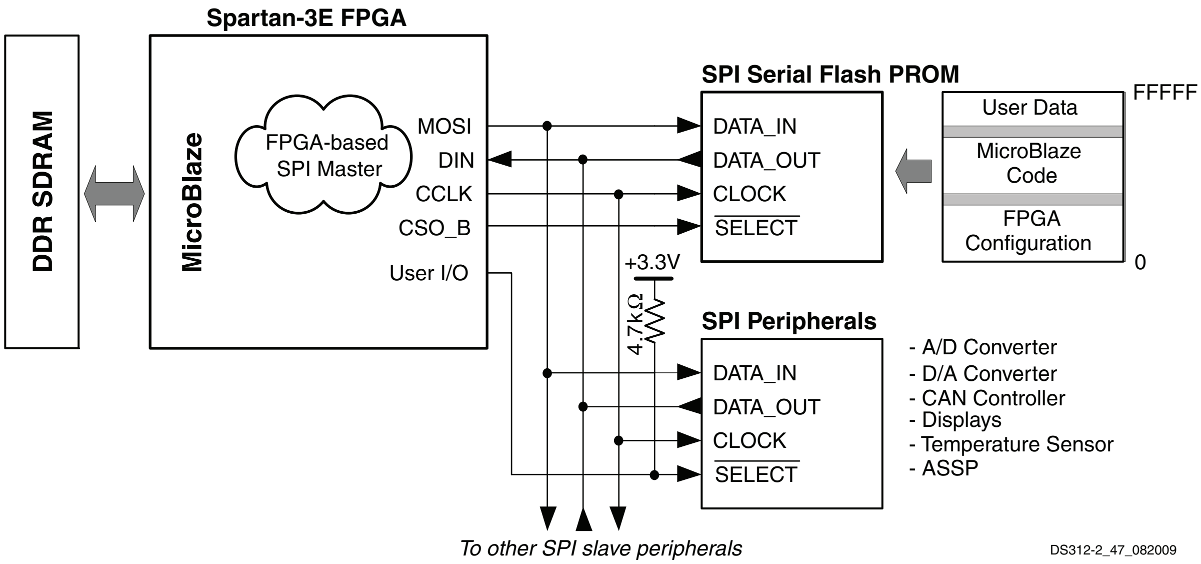


Figure 56: **Using the SPI Flash Interface After Configuration**

This addressing flexibility allows the FPGA to share the parallel Flash PROM with an external or embedded processor. Depending on the specific processor architecture, the processor boots either from the top or bottom of memory. The FPGA is flexible and boots from the opposite end of memory from the processor. Only the processor or the FPGA can boot at any given time. The FPGA can configure first, holding the processor in reset or the processor can boot first, asserting the FPGA's PROG_B pin.

The mode select pins, M[2:0], are sampled when the FPGA's INIT_B output goes High and must be at defined logic levels during this time. After configuration, when the FPGA's DONE output goes High, the mode pins are available as full-featured user-I/O pins.

(P) Similarly, the FPGA's HSWAP pin must be Low to enable pull-up resistors on all user-I/O pins or High to disable the pull-up resistors. The HSWAP control must remain at a constant logic level throughout FPGA configuration. After configuration, when the FPGA's DONE output goes High, the HSWAP pin is available as full-featured user-I/O pin and is powered by the VCCO_0 supply.

The RDWR_B and CSI_B must be Low throughout the configuration process. After configuration, these pins also become user I/O.

In a single-FPGA application, the FPGA's CSO_B and CCLK pins are not used but are actively driving during the configuration process. The BUSY pin is not used but also actively drives during configuration and is available as a user I/O after configuration.

After configuration, all of the interface pins except DONE and PROG_B are available as user I/Os. Furthermore, the bidirectional SelectMAP configuration peripheral interface (see Slave Parallel Mode) is available after configuration. To continue using SelectMAP mode, set the ***Persist*** bitstream generator option to ***Yes***. An external host can then read and verify configuration data.

The Persist option will maintain A20-A23 as configuration pins although they are not used in SelectMAP mode.

Table 59: **Byte-Wide Peripheral Interface (BPI) Connections**

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
HSWAP (P)	Input	**User I/O Pull-Up Control**. When Low during configuration, enables pull-up resistors in all I/O pins to respective I/O bank V_{CCO} input. 0: Pull-ups during configuration 1: No pull-ups	Drive at valid logic level throughout configuration.	User I/O
M[2:0] (A)	Input	**Mode Select**. Selects the FPGA configuration mode. See Design Considerations for the HSWAP, M[2:0], and VS[2:0] Pins.	M2 = 0, M1 = 1. Set M0 = 0 to start at address 0, increment addresses. Set M0 = 1 to start at address 0xFFFFFF and decrement addresses. Sampled when INIT_B goes High.	User I/O
CSI_B	Input	**Chip Select Input**. Active Low.	Must be Low throughout configuration.	User I/O. If bitstream option ***Persist=Yes***, becomes part of SelectMap parallel peripheral interface.
RDWR_B	Input	**Read/Write Control**. Active Low write enable. Read functionality typically only used after configuration, if bitstream option ***Persist=Yes***.	Must be Low throughout configuration.	User I/O. If bitstream option ***Persist=Yes***, becomes part of SelectMap parallel peripheral interface.
LDC0	Output	PROM Chip Enable	Connect to PROM chip-select input (CE#). FPGA drives this signal Low throughout configuration.	User I/O. If the FPGA does not access the PROM after configuration, drive this pin High to deselect the PROM. A[23:0], D[7:0], LDC[2:1], and HDC then become available as user I/O.
LDC1	Output	PROM Output Enable	Connect to the PROM output-enable input (OE#). The FPGA drives this signal Low throughout configuration.	User I/O

Quiescent Current Requirements

Table 79: **Quiescent Supply Current Characteristics**

Symbol	Description	Device	Typical	Commercial Maximum(1)	Industrial Maximum(1)	Units
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC3S100E	8	27	36	mA
		XC3S250E	15	78	104	mA
		XC3S500E	25	106	145	mA
		XC3S1200E	50	259	324	mA
		XC3S1600E	65	366	457	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC3S100E	0.8	1.0	1.5	mA
		XC3S250E	0.8	1.0	1.5	mA
		XC3S500E	0.8	1.0	1.5	mA
		XC3S1200E	1.5	2.0	2.5	mA
		XC3S1600E	1.5	2.0	2.5	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC3S100E	8	12	13	mA
		XC3S250E	12	22	26	mA
		XC3S500E	18	31	34	mA
		XC3S1200E	35	52	59	mA
		XC3S1600E	45	76	86	mA

Notes:

1. The maximum numbers in this table indicate the minimum current each power rail requires in order for the FPGA to power-on successfully.
2. The numbers in this table are based on the conditions set forth in Table 77.
3. Quiescent supply current is measured with all I/O drivers in a high-impedance state and with all pull-up/pull-down resistors at the I/O pads disabled. Typical values are characterized using typical devices at room temperature (T_J of 25°C at V_{CCINT} = 1.2 V, V_{CCO} = 3.3V, and V_{CCAUX} = 2.5V). The maximum limits are tested for each device at the respective maximum specified junction temperature and at maximum voltage limits with V_{CCINT} = 1.26V, V_{CCO} = 3.465V, and V_{CCAUX} = 2.625V. The FPGA is programmed with a "blank" configuration data file (i.e., a design with no functional elements instantiated). For conditions other than those described above, (e.g., a design including functional elements), measured quiescent current levels may be different than the values in the table. For more accurate estimates for a specific design, use the Xilinx® XPower tools.
4. There are two recommended ways to estimate the total power consumption (quiescent plus dynamic) for a specific design: a) The Spartan-3E XPower Estimator provides quick, approximate, typical estimates, and does not require a netlist of the design. b) XPower Analyzer uses a netlist as input to provide maximum estimates as well as more accurate typical estimates.

Table 87: **Pin-to-Pin Setup and Hold Times for the IOB Input Path (System Synchronous)**

Symbol	Description	Conditions	IFD_DELAY_VALUE=	Device	Speed Grade -5 Min	Speed Grade -4 Min	Units
Setup Times							
T_{PSDCM}	When writing to the Input Flip-Flop (IFF), the time from the setup of data at the Input pin to the active transition at a Global Clock pin. The DCM is used. No Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = 0, with DCM(3)	0	XC3S100E	2.65	2.98	ns
				XC3S250E	2.25	2.59	ns
				XC3S500E	2.25	2.59	ns
				XC3S1200E	2.25	2.58	ns
				XC3S1600E	2.25	2.59	ns
T_{PSFD}	When writing to IFF, the time from the setup of data at the Input pin to an active transition at the Global Clock pin. The DCM is not used. The Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = default software setting	2	XC3S100E	3.16	3.58	ns
			3	XC3S250E	3.44	3.91	ns
			3	XC3S500E	4.00	4.73	ns
			3	XC3S1200E	2.60	3.31	ns
			3	XC3S1600E	3.33	3.77	ns
Hold Times							
T_{PHDCM}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is used. No Input Delay is programmed.	LVCMOS25(4), IFD_DELAY_VALUE = 0, with DCM(3)	0	XC3S100E	–0.54	–0.52	ns
				XC3S250E	0.06	0.14	ns
				XC3S500E	0.07	0.14	ns
				XC3S1200E	0.07	0.15	ns
				XC3S1600E	0.06	0.14	ns
T_{PHFD}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is not used. The Input Delay is programmed.	LVCMOS25(4), IFD_DELAY_VALUE = default software setting	2	XC3S100E	–0.31	–0.24	ns
			3	XC3S250E	–0.32	–0.32	ns
			3	XC3S500E	–0.77	–0.77	ns
			3	XC3S1200E	0.13	0.16	ns
			3	XC3S1600E	–0.05	–0.03	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 95 and are based on the operating conditions set forth in Table 77 and Table 80.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, subtract the appropriate adjustment from Table 91. If this is true of the data Input, add the appropriate Input adjustment from the same table.
3. DCM output jitter is included in all measurements.
4. This hold time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, add the appropriate Input adjustment from Table 91. If this is true of the data Input, subtract the appropriate Input adjustment from the same table. When the hold time is negative, it is possible to change the data before the clock's active edge.

Table 107: **Switching Characteristics for the DFS**

Symbol	Description		Device	Speed Grade -5 Min	Speed Grade -5 Max	Speed Grade -4 Min	Speed Grade -4 Max	Units
Output Frequency Ranges								
CLKOUT_FREQ_FX_LF	Frequency for the CLKFX and CLKFX180 outputs, low frequencies	Stepping 0	XC3S100E XC3S250E XC3S500E XC3S1600E	N/A	N/A	5	90	MHz
CLKOUT_FREQ_FX_HF	Frequency for the CLKFX and CLKFX180 outputs, high frequencies					220	307	MHz
CLKOUT_FREQ_FX	Frequency for the CLKFX and CLKFX180 outputs	Stepping 0	XC3S1200E			5	307	MHz
		Stepping 1	All	5	333		311	MHz
Output Clock Jitter(2,3)								
CLKOUT_PER_JITT_FX	Period jitter at the CLKFX and CLKFX180 outputs.		All	Typ	Max	Typ	Max	
		CLKIN ≤ 20 MHz		Note 6				ps
		CLKIN > 20 MHz		±[1% of CLKFX period + 100]	±[1% of CLKFX period + 200]	±[1% of CLKFX period + 100]	±[1% of CLKFX period + 200]	ps
Duty Cycle(4,5)								
CLKOUT_DUTY_CYCLE_FX	Duty cycle precision for the CLKFX and CLKFX180 outputs, including the BUFGMUX and clock tree duty-cycle distortion		All	-	±[1% of CLKFX period + 400]	-	±[1% of CLKFX period + 400]	ps
Phase Alignment(5)								
CLKOUT_PHASE_FX	Phase offset between the DFS CLKFX output and the DLL CLK0 output when both the DFS and DLL are used		All	-	±200	-	±200	ps
CLKOUT_PHASE_FX180	Phase offset between the DFS CLKFX180 output and the DLL CLK0 output when both the DFS and DLL are used		All	-	±[1% of CLKFX period + 300]	-	±[1% of CLKFX period + 300]	ps
Lock Time								
LOCK_FX(2)	The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX and CLKFX180 signals are valid. If using both the DLL and the DFS, use the longer locking time.	5 MHz ≤ F_{CLKIN} ≤ 15 MHz	All	-	5	-	5	ms
		F_{CLKIN} > 15 MHz		-	450	-	450	µs

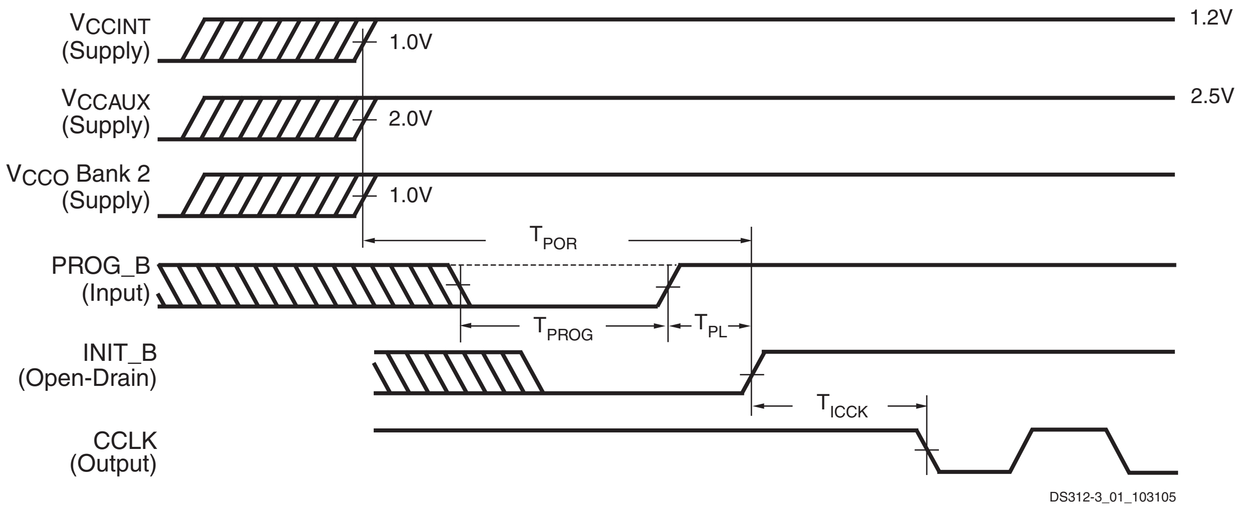
Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 77 and Table 106.
2. For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
3. Maximum output jitter is characterized within a reasonable noise environment (150 ps input period jitter, 40 SSOs and 25% CLB switching). Output jitter strongly depends on the environment, including the number of SSOs, the output drive strength, CLB utilization, CLB switching activities, switching frequency, power supply and PCB design. The actual maximum output jitter depends on the system application.
4. The CLKFX and CLKFX180 outputs always have an approximate 50% duty cycle.
5. Some duty-cycle and alignment specifications include 1% of the CLKFX output period or 0.01 UI.

   Example: The data sheet specifies a maximum jitter of ±[1% of CLKFX period + 300]. Assume the CLKFX output frequency is 100 MHz. The equivalent CLKFX period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 300 ps] = ±400 ps.
6. Use the Spartan-3A Jitter Calculator (www.xilinx.com/support/documentation/data_sheets/s3a_jitter_calc.zip) to estimate DFS output jitter. Use the Clocking Wizard to determine jitter for a specific design.

Configuration and JTAG Timing

General Configuration Power-On/Reconfigure Timing



Notes:

1. The V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies may be applied in any order.
2. The Low-going pulse on PROG_B is optional after power-on but necessary for reconfiguration without a power cycle.
3. The rising edge of INIT_B samples the voltage levels applied to the mode pins (M0 - M2).

Figure 73: **Waveforms for Power-On and the Beginning of Configuration**

Table 111: **Power-On Timing and the Beginning of Configuration**

Symbol	Description	Device	All Speed Grades		Units
			Min	Max	
T_{POR}(2)	The time from the application of V_{CCINT}, V_{CCAUX}, and V_{CCO} Bank 2 supply voltage ramps (whichever occurs last) to the rising transition of the INIT_B pin	XC3S100E	-	5	ms
		XC3S250E	-	5	ms
		XC3S500E	-	5	ms
		XC3S1200E	-	5	ms
		XC3S1600E	-	7	ms
T_{PROG}	The width of the low-going pulse on the PROG_B pin	All	0.5	-	µs
T_{PL}(2)	The time from the rising edge of the PROG_B pin to the rising transition on the INIT_B pin	XC3S100E	-	0.5	ms
		XC3S250E	-	0.5	ms
		XC3S500E	-	1	ms
		XC3S1200E	-	2	ms
		XC3S1600E	-	2	ms
T_{INIT}	Minimum Low pulse width on INIT_B output	All	250	-	ns
T_{ICCK}(3)	The time from the rising edge of the INIT_B pin to the generation of the configuration clock signal at the CCLK output pin	All	0.5	4.0	µs

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 77. This means power must be applied to all V_{CCINT}, V_{CCO}, and V_{CCAUX} lines.
2. Power-on reset and the clearing of configuration memory occurs during this period.
3. This specification applies only to the Master Serial, SPI, BPI-Up, and BPI-Down modes.

Table 117: **Timing for the Slave Parallel Configuration Mode *(Cont'd)***

Symbol	Description			All Speed Grades		Units
				Min	Max	
Clock Timing						
T_{CCH}	The High pulse width at the CCLK input pin			5	-	ns
T_{CCL}	The Low pulse width at the CCLK input pin			5	-	ns
F_{CCPAR}	Frequency of the clock signal at the CCLK input pin	No bitstream compression	Not using the BUSY pin(2)	0	50	MHz
			Using the BUSY pin	0	66	MHz
		With bitstream compression		0	20	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 77.
2. In the Slave Parallel mode, it is necessary to use the BUSY pin when the CCLK frequency exceeds this maximum specification.
3. Some Xilinx documents refer to Parallel modes as "SelectMAP" modes.

Date	Version	Revision
08/26/09	3.8	Added reference to XAPP459 in Table 73 note 2. Updated BPI timing in Figure 77, Table 119, and Table 120. Removed V_{REF} requirements for differential HSTL and differential SSTL in Table 95. Added Spread Spectrum paragraph. Revised hold times for $T_{IOICKPD}$ in Table 88 and setup times for T_{DICK} in Table 98. Added note 4 to Table 106 and note 3 to Table 107, and updated note 6 for Table 107 to add input jitter.
10/29/12	4.0	Added Notice of Disclaimer. This product is not recommended for new designs. Revised note 2 in Table 73. Revised note 2 and V_{IN} description in Table 77, and added note 5. Added note 3 to Table 78.

Notice of Disclaimer

Table 133: **CP132 Package Pinout *(Cont'd)***

Bank	XC3S100E Pin Name	XC3S250E XC3S500E Pin Name	CP132 Ball	Type
0	VCCO_0	VCCO_0	B10	VCCO
1	IO/A0	IO/A0	F12	DUAL
1	IO/VREF_1	IO/VREF_1	K13	VREF
1	IO_L01N_1/A15	IO_L01N_1/A15	N14	DUAL
1	IO_L01P_1/A16	IO_L01P_1/A16	N13	DUAL
1	IO_L02N_1/A13	IO_L02N_1/A13	M13	DUAL
1	IO_L02P_1/A14	IO_L02P_1/A14	M12	DUAL
1	IO_L03N_1/A11	IO_L03N_1/A11	L14	DUAL
1	IO_L03P_1/A12	IO_L03P_1/A12	L13	DUAL
1	IO_L04N_1/A9/RHCLK1	IO_L04N_1/A9/RHCLK1	J12	RHCLK/DUAL
1	IO_L04P_1/A10/RHCLK0	IO_L04P_1/A10/RHCLK0	K14	RHCLK/DUAL
1	IO_L05N_1/A7/RHCLK3/TRDY1	IO_L05N_1/A7/RHCLK3/TRDY1	J14	RHCLK/DUAL
1	IO_L05P_1/A8/RHCLK2	IO_L05P_1/A8/RHCLK2	J13	RHCLK/DUAL
1	IO_L06N_1/A5/RHCLK5	IO_L06N_1/A5/RHCLK5	H12	RHCLK/DUAL
1	IO_L06P_1/A6/RHCLK4/IRDY1	IO_L06P_1/A6/RHCLK4/IRDY1	H13	RHCLK/DUAL
1	IO_L07N_1/A3/RHCLK7	IO_L07N_1/A3/RHCLK7	G13	RHCLK/DUAL
1	IO_L07P_1/A4/RHCLK6	IO_L07P_1/A4/RHCLK6	G14	RHCLK/DUAL
1	IO_L08N_1/A1	IO_L08N_1/A1	F13	DUAL
1	IO_L08P_1/A2	IO_L08P_1/A2	F14	DUAL
1	IO_L09N_1/LDC0	IO_L09N_1/LDC0	D12	DUAL
1	IO_L09P_1/HDC	IO_L09P_1/HDC	D13	DUAL
1	IO_L10N_1/LDC2	IO_L10N_1/LDC2	C13	DUAL
1	IO_L10P_1/LDC1	IO_L10P_1/LDC1	C14	DUAL
1	IP/VREF_1	IP/VREF_1	G12	VREF
1	VCCO_1	VCCO_1	E13	VCCO
1	VCCO_1	VCCO_1	M14	VCCO
2	IO/D5	IO/D5	P4	DUAL
2	IO/M1	IO/M1	N7	DUAL
2	IP/VREF_2	IO/VREF_2	P11	***100E:*** VREF(INPUT) ***Others:*** VREF(I/O)
2	IO_L01N_2/INIT_B	IO_L01N_2/INIT_B	N1	DUAL
2	IO_L01P_2/CSO_B	IO_L01P_2/CSO_B	M2	DUAL
2	IO_L02N_2/MOSI/CSI_B	IO_L02N_2/MOSI/CSI_B	N2	DUAL
2	IO_L02P_2/DOUT/BUSY	IO_L02P_2/DOUT/BUSY	P1	DUAL
2	IO_L03N_2/D6/GCLK13	IO_L03N_2/D6/GCLK13	N4	DUAL/GCLK
2	IO_L03P_2/D7/GCLK12	IO_L03P_2/D7/GCLK12	M4	DUAL/GCLK
2	IO_L04N_2/D3/GCLK15	IO_L04N_2/D3/GCLK15	N5	DUAL/GCLK
2	IO_L04P_2/D4/GCLK14	IO_L04P_2/D4/GCLK14	M5	DUAL/GCLK
2	IO_L06N_2/D1/GCLK3	IO_L06N_2/D1/GCLK3	P7	DUAL/GCLK
2	IO_L06P_2/D2/GCLK2	IO_L06P_2/D2/GCLK2	P6	DUAL/GCLK
2	IO_L07N_2/DIN/D0	IO_L07N_2/DIN/D0	N8	DUAL
2	IO_L07P_2/M0	IO_L07P_2/M0	P8	DUAL
2	N.C. (◆)	IO_L08N_2/A22	M9	***100E:*** N.C. ***Others:*** DUAL

FT256: 256-ball Fine-pitch, Thin Ball Grid Array

The 256-ball fine-pitch, thin ball grid array package, FT256, supports three different Spartan-3E FPGAs, including the XC3S250E, the XC3S500E, and the XC3S1200E.

Table 143 lists all the package pins. They are sorted by bank number and then by pin name of the largest device. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The highlighted rows indicate pinout differences between the XC3S250E, the XC3S500E, and the XC3S1200E FPGAs. The XC3S250E has 18 unconnected balls, indicated as N.C. (No Connection) in Table 143 and with the black diamond character (◆) in Table 143 and Figure 83.

If the table row is highlighted in tan, then this is an instance where an unconnected pin on the XC3S250E FPGA maps to a VREF pin on the XC3S500E and XC3S1200E FPGA. If the FPGA application uses an I/O standard that requires a VREF voltage reference, connect the highlighted pin to the VREF voltage supply, even though this does not actually connect to the XC3S250E FPGA. This VREF connection on the board allows future migration to the larger devices without modifying the printed-circuit board.

All other balls have nearly identical functionality on all three devices. Table 147 summarizes the Spartan-3E footprint migration differences for the FT256 package.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx web site at:

http://www.xilinx.com/support/documentation/data_sheets/s3e_pin.zip

Pinout Table

Table 143: **FT256 Package Pinout**

Bank	XC3S250E Pin Name	XC3S500E Pin Name	XC3S1200E Pin Name	FT256 Ball	Type
0	IO	IO	IO	A7	I/O
0	IO	IO	IO	A12	I/O
0	IO	IO	IO	B4	I/O
0	IP	IP	IO	B6	***250E:*** INPUT ***500E:*** INPUT ***1200E:*** I/O
0	IP	IP	IO	B10	***250E:*** INPUT ***500E:*** INPUT ***1200E:*** I/O
0	IO/VREF_0	IO/VREF_0	IO/VREF_0	D9	VREF
0	IO_L01N_0	IO_L01N_0	IO_L01N_0	A14	I/O
0	IO_L01P_0	IO_L01P_0	IO_L01P_0	B14	I/O
0	IO_L03N_0/VREF_0	IO_L03N_0/VREF_0	IO_L03N_0/VREF_0	A13	VREF
0	IO_L03P_0	IO_L03P_0	IO_L03P_0	B13	I/O
0	IO_L04N_0	IO_L04N_0	IO_L04N_0	E11	I/O
0	IO_L04P_0	IO_L04P_0	IO_L04P_0	D11	I/O
0	IO_L05N_0/VREF_0	IO_L05N_0/VREF_0	IO_L05N_0/VREF_0	B11	VREF
0	IO_L05P_0	IO_L05P_0	IO_L05P_0	C11	I/O
0	IO_L06N_0	IO_L06N_0	IO_L06N_0	E10	I/O
0	IO_L06P_0	IO_L06P_0	IO_L06P_0	D10	I/O
0	IO_L08N_0/GCLK5	IO_L08N_0/GCLK5	IO_L08N_0/GCLK5	F9	GCLK
0	IO_L08P_0/GCLK4	IO_L08P_0/GCLK4	IO_L08P_0/GCLK4	E9	GCLK
0	IO_L09N_0/GCLK7	IO_L09N_0/GCLK7	IO_L09N_0/GCLK7	A9	GCLK
0	IO_L09P_0/GCLK6	IO_L09P_0/GCLK6	IO_L09P_0/GCLK6	A10	GCLK
0	IO_L11N_0/GCLK11	IO_L11N_0/GCLK11	IO_L11N_0/GCLK11	D8	GCLK
0	IO_L11P_0/GCLK10	IO_L11P_0/GCLK10	IO_L11P_0/GCLK10	C8	GCLK
0	IO_L12N_0	IO_L12N_0	IO_L12N_0	F8	I/O

Table 143: **FT256 Package Pinout *(Cont'd)***

Bank	XC3S250E Pin Name	XC3S500E Pin Name	XC3S1200E Pin Name	FT256 Ball	Type
1	N.C. (◆)	IO_L05P_1	IO_L05P_1	L12	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O
1	IO_L06N_1	IO_L06N_1	IO_L06N_1	L15	I/O
1	IO_L06P_1	IO_L06P_1	IO_L06P_1	L14	I/O
1	IO_L07N_1/A11	IO_L07N_1/A11	IO_L07N_1/A11	K12	DUAL
1	IO_L07P_1/A12	IO_L07P_1/A12	IO_L07P_1/A12	K13	DUAL
1	IO_L08N_1/VREF_1	IO_L08N_1/VREF_1	IO_L08N_1/VREF_1	K14	VREF
1	IO_L08P_1	IO_L08P_1	IO_L08P_1	K15	I/O
1	IO_L09N_1/A9/RHCLK1	IO_L09N_1/A9/RHCLK1	IO_L09N_1/A9/RHCLK1	J16	RHCLK/DUAL
1	IO_L09P_1/A10/RHCLK0	IO_L09P_1/A10/RHCLK0	IO_L09P_1/A10/RHCLK0	K16	RHCLK/DUAL
1	IO_L10N_1/A7/RHCLK3/ TRDY1	IO_L10N_1/A7/RHCLK3/ TRDY1	IO_L10N_1/A7/RHCLK3/ TRDY1	J13	RHCLK/DUAL
1	IO_L10P_1/A8/RHCLK2	IO_L10P_1/A8/RHCLK2	IO_L10P_1/A8/RHCLK2	J14	RHCLK/DUAL
1	IO_L11N_1/A5/RHCLK5	IO_L11N_1/A5/RHCLK5	IO_L11N_1/A5/RHCLK5	H14	RHCLK/DUAL
1	IO_L11P_1/A6/RHCLK4/ IRDY1	IO_L11P_1/A6/RHCLK4/ IRDY1	IO_L11P_1/A6/RHCLK4/ IRDY1	H15	RHCLK/DUAL
1	IO_L12N_1/A3/RHCLK7	IO_L12N_1/A3/RHCLK7	IO_L12N_1/A3/RHCLK7	H11	RHCLK/DUAL
1	IO_L12P_1/A4/RHCLK6	IO_L12P_1/A4/RHCLK6	IO_L12P_1/A4/RHCLK6	H12	RHCLK/DUAL
1	IO_L13N_1/A1	IO_L13N_1/A1	IO_L13N_1/A1	G16	DUAL
1	IO_L13P_1/A2	IO_L13P_1/A2	IO_L13P_1/A2	G15	DUAL
1	IO_L14N_1/A0	IO_L14N_1/A0	IO_L14N_1/A0	G14	DUAL
1	IO_L14P_1	IO_L14P_1	IO_L14P_1	G13	I/O
1	IO_L15N_1	IO_L15N_1	IO_L15N_1	F15	I/O
1	IO_L15P_1	IO_L15P_1	IO_L15P_1	F14	I/O
1	IO_L16N_1	IO_L16N_1	IO_L16N_1	F12	I/O
1	IO_L16P_1	IO_L16P_1	IO_L16P_1	F13	I/O
1	N.C. (◆)	IO_L17N_1	IO_L17N_1	E16	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O
1	N.C. (◆).	IO_L17P_1	IO_L17P_1	E13	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O
1	IO_L18N_1/LDC0	IO_L18N_1/LDC0	IO_L18N_1/LDC0	D14	DUAL
1	IO_L18P_1/HDC	IO_L18P_1/HDC	IO_L18P_1/HDC	D15	DUAL
1	IO_L19N_1/LDC2	IO_L19N_1/LDC2	IO_L19N_1/LDC2	C15	DUAL
1	IO_L19P_1/LDC1	IO_L19P_1/LDC1	IO_L19P_1/LDC1	C16	DUAL
1	IP	IP	IP	B16	INPUT
1	IP	IP	IP	E14	INPUT
1	IP	IP	IP	G12	INPUT
1	IP	IP	IP	H16	INPUT
1	IP	IP	IP	J11	INPUT
1	IP	IP	IP	J12	INPUT
1	IP	IP	IP	M13	INPUT

FG320: 320-ball Fine-pitch Ball Grid Array

The 320-ball fine-pitch ball grid array package, FG320, supports three different Spartan-3E FPGAs, including the XC3S500E, the XC3S1200E, and the XC3S1600E, as shown in Table 148 and Figure 86.

The FG320 package is an 18 x 18 array of solder balls minus the four center balls.

Table 148 lists all the package pins. They are sorted by bank number and then by pin name of the largest device. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The highlighted rows indicate pinout differences between the XC3S500E, the XC3S1200E, and the XC3S1600E FPGAs. The XC3S500E has 18 unconnected balls, indicated as N.C. (No Connection) in Table 148 and with the black diamond character (◆) in Table 148 and Figure 86.

If the table row is highlighted in tan, then this is an instance where an unconnected pin on the XC3S500E FPGA maps to a VREF pin on the XC3S1200E and XC3S1600E FPGA. If the FPGA application uses an I/O standard that requires a VREF voltage reference, connect the highlighted pin to the VREF voltage supply, even though this does not actually connect to the XC3S500E FPGA. This VREF connection on the board allows future migration to the larger devices without modifying the printed-circuit board.

All other balls have nearly identical functionality on all three devices. Table 147 summarizes the Spartan-3E footprint migration differences for the FG320 package.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx web site at:

http://www.xilinx.com/support/documentation/data_sheets/s3e_pin.zip

Pinout Table

Table 148: **FG320 Package Pinout**

Bank	XC3S500E Pin Name	XC3S1200E Pin Name	XC3S1600E Pin Name	FG320 Ball	Type
0	IP	IO	IO	A7	**500E:** INPUT **1200E:** I/O **1600E:** I/O
0	IO	IO	IO	A8	I/O
0	IO	IO	IO	A11	I/O
0	N.C. (◆)	IO	IO	A12	**500E:** N.C. **1200E:** I/O **1600E:** I/O
0	IO	IO	IO	C4	I/O
0	IP	IO	IO	D13	**500E:** INPUT **1200E:** I/O **1600E:** I/O
0	IO	IO	IO	E13	I/O
0	IO	IO	IO	G9	I/O
0	IO/VREF_0	IO/VREF_0	IO/VREF_0	B11	VREF
0	IO_L01N_0	IO_L01N_0	IO_L01N_0	A16	I/O
0	IO_L01P_0	IO_L01P_0	IO_L01P_0	B16	I/O
0	IO_L03N_0/VREF_0	IO_L03N_0/VREF_0	IO_L03N_0/VREF_0	C14	VREF
0	IO_L03P_0	IO_L03P_0	IO_L03P_0	D14	I/O
0	IO_L04N_0	IO_L04N_0	IO_L04N_0	A14	I/O
0	IO_L04P_0	IO_L04P_0	IO_L04P_0	B14	I/O
0	IO_L05N_0/VREF_0	IO_L05N_0/VREF_0	IO_L05N_0/VREF_0	B13	VREF
0	IO_L05P_0	IO_L05P_0	IO_L05P_0	A13	I/O
0	IO_L06N_0	IO_L06N_0	IO_L06N_0	E12	I/O
0	IO_L06P_0	IO_L06P_0	IO_L06P_0	F12	I/O
0	IO_L08N_0	IO_L08N_0	IO_L08N_0	F11	I/O

FG320 Footprint

Bank 0

Bank 1

Bank 2

Bank 3

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	GND	TDI	INPUT	I/O L24P_0	INPUT L22P_0	I/O L20N_0	INPUT ←→	I/O	VCCO_0	I/O L12N_0 GCLK7	I/O	I/O ◆	I/O L05P_0	I/O L04N_0	INPUT L02N_0	I/O L01N_0	TCK	GND
B	PROG_B	GND	I/O L25N_0 HSWAP	I/O L24N_0	INPUT L22N_0	I/O L20P_0	VCCAUX	INPUT L13P_0 GCLK8	INPUT L13N_0 GCLK9	I/O L12P_0 GCLK6	I/O VREF_0	VCCAUX	I/O L05N_0 VREF_0	I/O L04P_0	INPUT L02P_0	I/O L01P_0	GND	INPUT
C	I/O L01P_3	I/O L01N_3	I/O L25P_0	I/O	I/O L23P_0	VCCO_0	I/O L18P_0	INPUT L16P_0	I/O L14P_0 GCLK10	GND	I/O L09P_0	INPUT L07P_0	VCCO_0	I/O L03N_0 VREF_0	INPUT	TDO	I/O L24N_1 LDC2	I/O L24P_1 LDC1
D	I/O L02P_3	I/O L02N_3 VREF_3	INPUT	I/O ◆	I/O L23N_0 VREF_0	I/O L21P_0 ◆	I/O L18N_0 VREF_0	INPUT L16N_0	I/O L14N_0 GCLK11	I/O L11P_0 GCLK4	I/O L09N_0	INPUT L07N_0	INPUT ←→	I/O L03P_0	TMS	I/O L23N_1 LDC0	I/O L23P_1 HDC	INPUT VREF_1
E	I/O L03N_3	I/O L03P_3	I/O L04N_3 ◆	I/O L04P_3 ◆	VCCINT	I/O L21N_0 ◆	I/O L19N_0 VREF_0	I/O L17P_0	I/O L15P_0	I/O L11N_0 GCLK5	I/O L08P_0	I/O L06N_0	I/O	VCCINT	I/O L22P_1 ◆	I/O L22N_1 ◆	INPUT ←→	INPUT
F	I/O L05P_3	I/O L05N_3	VCCO_3	INPUT ←→	INPUT	VCCINT	I/O L19P_0	I/O L17N_0	I/O L15N_0	INPUT L10P_0	I/O L08N_0	I/O L06P_0	VCCINT	I/O L21N_1	I/O L21P_1	VCCO_1	I/O L19N_1	I/O L19P_1
G	INPUT	VCCAUX	I/O L06P_3	I/O L06N_3 VREF_3	I/O L07N_3	I/O L07P_3	GND	VCCO_0	I/O	INPUT L10N_0	VCCO_0	GND	I/O L20N_1	I/O L20P_1	I/O L18P_1	I/O L18N_1	VCCAUX	INPUT
H	I/O L10N_3	I/O L10P_3	I/O L09N_3	I/O L09P_3	I/O L08N_3	I/O L08P_3	VCCO_3	GND	GND	GND	GND	VCCO_1	INPUT	I/O L17P_1	I/O L17N_1	I/O L16P_1	I/O L16N_1 A0	INPUT VREF_1
J	I/O L12P_3 LHCLK2	I/O L12N_3 LHCLK3 IRDY2	GND	I/O L11N_3 LHCLK1	I/O L11P_3 LHCLK0	INPUT VREF_3	INPUT	GND			GND	I/O L15P_1 A2	I/O L15N_1 A1	I/O L14N_1 A3 RHCLK7	I/O L14P_1 A4 RHCLK6	I/O L13N_1 A5 RHCLK5	I/O L13P_1 A6 RHCLK4 IRDY1	VCCO_1
K	VCCO_3	INPUT	I/O L13P_3 LHCLK4 TRDY2	I/O L13N_3 LHCLK5	I/O L14N_3 LHCLK7	I/O L14P_3 LHCLK6	INPUT	GND			GND	I/O L11N_1 A9 RHCLK1	I/O L11P_1 A10 RHCLK0	I/O L12N_1 A7 RHCLK3 TRDY1	I/O L12P_1 A8 RHCLK2	GND	INPUT	INPUT
L	I/O L15P_3	I/O L15N_3	I/O L16P_3	I/O L16N_3	I/O L17N_3 VREF_3	I/O L17P_3	VCCO_3	GND	GND	GND	GND	VCCO_1	INPUT	INPUT	I/O L09N_1 A11	I/O L09P_1 A12	I/O L10N_1 VREF_1	I/O L10P_1
M	INPUT	VCCAUX	I/O L18N_3	I/O L18P_3	I/O L19P_3	I/O L19N_3	GND	VCCO_2	I/O L12N_2 D6 GCLK13	I/O L16P_2 M0	VCCO_2	GND	I/O L05N_1 VREF_1	I/O L05P_1	I/O L07P_1	I/O L07N_1	VCCAUX	I/O L08N_1
N	INPUT	INPUT	VCCO_3	I/O L20P_3	I/O L20N_3	VCCINT	I/O L07P_2	I/O L09N_2	I/O L12P_2 D7 GCLK12	I/O L16N_2 DIN D0	I/O L18N_2	I/O L21P_2 ◆	VCCINT	I/O L04N_1 ◆	I/O L04P_1 ◆	VCCO_1	INPUT	I/O L08P_1
P	I/O L21N_3	I/O L21P_3	I/O L22P_3 ◆	I/O L22N_3 ◆	VCCINT	I/O L05N_2	I/O L07N_2	I/O L09P_2	I/O	I/O L15N_2 D1 GCLK3	I/O L18P_2	I/O L21N_2 ◆	I/O L22P_2 A23	VCCINT	INPUT ←→	I/O ◆	I/O L06P_1	I/O L06N_1
R	INPUT	I/O L23N_3	I/O L23P_3	INPUT VREF_3 ←→	I/O L04P_2	I/O L05P_2	INPUT L08N_2	I/O L10P_2	I/O D5	I/O L15P_2 D2 GCLK2	I/O	I/O L20N_2	I/O L22N_2 A22	I/O L24N_2 A20	I/O L03P_1	I/O L03N_1 VREF_1	INPUT	I/O L02P_1 A14
T	I/O L24N_3	I/O L24P_3	I/O L01N_2 INIT_B	I/O L03N_2 MOSI CSI_B	I/O L04N_2	VCCO_2	INPUT L08P_2	I/O L10N_2	GND	INPUT L14N_2 M2 GCLK1	INPUT L17P_2	I/O L20P_2	VCCO_2	I/O L24P_2 A21	I/O VREF_2	I/O L26P_2 VS0 A17	I/O L01N_1 A15	I/O L02N_1 A13
U	INPUT	GND	I/O L01P_2 CSO_B	I/O L03P_2 DOUT BUSY	I/O VREF_2	INPUT ←→	VCCAUX	INPUT L11P_2	I/O L13P_2 D4 GCLK14	INPUT L14P_2 RDWR_B GCLK0	INPUT L17N_2	VCCAUX	INPUT ←→	INPUT L23N_2	I/O L25N_2 VS1 A18	I/O L26N_2 CCLK	GND	I/O L01P_1 A16
V	GND	INPUT	INPUT L02N_2	INPUT L02P_2	I/O L06P_2 ◆	I/O L06N_2 VREF_2 ◆	I/O ◆	INPUT L11N_2 VREF_2	I/O L13N_2 D3 GCLK15	VCCO_2	I/O M1	I/O L19P_2	I/O L19N_2 VREF_2	INPUT L23P_2	I/O L25P_2 VS2 A19	INPUT	DONE	GND

DS312-4_06_022106

Figure 86: **FG320 Package Footprint (top view)**

102-120	**I/O:** Unrestricted, general-purpose user I/O	46	**DUAL:** Configuration pin, then possible user-I/O	20-21	**VREF:** User I/O or input voltage reference for bank
47-48	**INPUT:** Unrestricted, general-purpose input pin	16	**CLK:** User I/O, input, or global buffer input	20	**VCCO:** Output voltage supply for bank
2	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	8	**VCCINT:** Internal core supply voltage (+1.2V)
18	**N.C.:** Not connected. Only the XC3S500E has these pins (◆).	28	**GND:** Ground	8	**VCCAUX:** Auxiliary supply voltage (+2.5V)

FG400: 400-ball Fine-pitch Ball Grid Array

The 400-ball fine-pitch ball grid array, FG400, supports two different Spartan-3E FPGAs, including the XC3S1200E and the XC3S1600E. Both devices share a common footprint for this package as shown in Table 152 and Figure 87.

Table 152 lists all the FG400 package pins. They are sorted by bank number and then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at:

http://www.xilinx.com/support/documentation/data_sheets/s3e_pin.zip

Pinout Table

Table 152: **FG400 Package Pinout**

Bank	XC3S1200E XC3S1600E Pin Name	FG400 Ball	Type
0	IO	A3	I/O
0	IO	A8	I/O
0	IO	A12	I/O
0	IO	C7	I/O
0	IO	C10	I/O
0	IO	E8	I/O
0	IO	E13	I/O
0	IO	E16	I/O
0	IO	F13	I/O
0	IO	F14	I/O
0	IO	G7	I/O
0	IO/VREF_0	C11	VREF
0	IO_L01N_0	B17	I/O
0	IO_L01P_0	C17	I/O
0	IO_L03N_0/VREF_0	A18	VREF
0	IO_L03P_0	A19	I/O
0	IO_L04N_0	A17	I/O
0	IO_L04P_0	A16	I/O
0	IO_L06N_0	A15	I/O
0	IO_L06P_0	B15	I/O
0	IO_L07N_0	C14	I/O
0	IO_L07P_0	D14	I/O
0	IO_L09N_0/VREF_0	A13	VREF
0	IO_L09P_0	A14	I/O
0	IO_L10N_0	B13	I/O
0	IO_L10P_0	C13	I/O
0	IO_L12N_0	C12	I/O

Table 152: **FG400 Package Pinout *(Cont'd)***

Bank	XC3S1200E XC3S1600E Pin Name	FG400 Ball	Type
0	IO_L12P_0	D12	I/O
0	IO_L13N_0	E12	I/O
0	IO_L13P_0	F12	I/O
0	IO_L15N_0/GCLK5	G11	GCLK
0	IO_L15P_0/GCLK4	F11	GCLK
0	IO_L16N_0/GCLK7	E10	GCLK
0	IO_L16P_0/GCLK6	E11	GCLK
0	IO_L18N_0/GCLK11	A9	GCLK
0	IO_L18P_0/GCLK10	A10	GCLK
0	IO_L19N_0	F9	I/O
0	IO_L19P_0	E9	I/O
0	IO_L21N_0	C9	I/O
0	IO_L21P_0	D9	I/O
0	IO_L22N_0/VREF_0	B8	VREF
0	IO_L22P_0	B9	I/O
0	IO_L24N_0/VREF_0	F7	VREF
0	IO_L24P_0	F8	I/O
0	IO_L25N_0	A6	I/O
0	IO_L25P_0	A7	I/O
0	IO_L27N_0	B5	I/O
0	IO_L27P_0	B6	I/O
0	IO_L28N_0	D6	I/O
0	IO_L28P_0	C6	I/O
0	IO_L30N_0/VREF_0	C5	VREF
0	IO_L30P_0	D5	I/O
0	IO_L31N_0	A2	I/O
0	IO_L31P_0	B2	I/O
0	IO_L32N_0/HSWAP	D4	DUAL
0	IO_L32P_0	C4	I/O
0	IP	B18	INPUT
0	IP	E5	INPUT
0	IP_L02N_0	C16	INPUT
0	IP_L02P_0	D16	INPUT
0	IP_L05N_0	D15	INPUT
0	IP_L05P_0	C15	INPUT
0	IP_L08N_0	E14	INPUT
0	IP_L08P_0	E15	INPUT
0	IP_L11N_0	G14	INPUT
0	IP_L11P_0	G13	INPUT
0	IP_L14N_0	B11	INPUT
0	IP_L14P_0	B12	INPUT
0	IP_L17N_0/GCLK9	G10	GCLK

Table 154: **FG484 Package Pinout *(Cont'd)***

Bank	XC3S1600E Pin Name	FG484 Ball	Type
2	IO_L19N_2/D6/GCLK13	U11	DUAL/ GCLK
2	IO_L19P_2/D7/GCLK12	V11	DUAL/ GCLK
2	IO_L20N_2/D3/GCLK15	T11	DUAL/ GCLK
2	IO_L20P_2/D4/GCLK14	R11	DUAL/ GCLK
2	IO_L22N_2/D1/GCLK3	W12	DUAL/ GCLK
2	IO_L22P_2/D2/GCLK2	Y12	DUAL/ GCLK
2	IO_L23N_2/DIN/D0	U12	DUAL
2	IO_L23P_2/M0	V12	DUAL
2	IO_L25N_2	Y13	I/O
2	IO_L25P_2	W13	I/O
2	IO_L26N_2/VREF_2	U14	VREF
2	IO_L26P_2	U13	I/O
2	IO_L27N_2	T14	I/O
2	IO_L27P_2	R14	I/O
2	IO_L28N_2	Y14	I/O
2	IO_L28P_2	AA14	I/O
2	IO_L29N_2	W14	I/O
2	IO_L29P_2	V14	I/O
2	IO_L30N_2	AB15	I/O
2	IO_L30P_2	AA15	I/O
2	IO_L32N_2	W15	I/O
2	IO_L32P_2	Y15	I/O
2	IO_L33N_2	U16	I/O
2	IO_L33P_2	V16	I/O
2	IO_L35N_2/A22	AB17	DUAL
2	IO_L35P_2/A23	AA17	DUAL
2	IO_L36N_2	W17	I/O
2	IO_L36P_2	Y17	I/O
2	IO_L38N_2/A20	Y18	DUAL
2	IO_L38P_2/A21	W18	DUAL
2	IO_L39N_2/VS1/A18	AA20	DUAL
2	IO_L39P_2/VS2/A19	AB20	DUAL
2	IO_L40N_2/CCLK	W19	DUAL
2	IO_L40P_2/VS0/A17	Y19	DUAL
2	IP	V17	INPUT
2	IP	AB2	INPUT
2	IP_L02N_2	AA4	INPUT
2	IP_L02P_2	Y4	INPUT
2	IP_L05N_2	Y6	INPUT
2	IP_L05P_2	AA6	INPUT
2	IP_L08N_2	AB7	INPUT
2	IP_L08P_2	AB6	INPUT
2	IP_L15N_2	Y10	INPUT
2	IP_L15P_2	W10	INPUT
2	IP_L18N_2/VREF_2	AA11	VREF
2	IP_L18P_2	Y11	INPUT
2	IP_L21N_2/M2/GCLK1	P12	DUAL/ GCLK
2	IP_L21P_2/RDWR_B/ GCLK0	R12	DUAL/ GCLK
2	IP_L24N_2	R13	INPUT
2	IP_L24P_2	T13	INPUT
2	IP_L31N_2/VREF_2	T15	VREF
2	IP_L31P_2	U15	INPUT
2	IP_L34N_2	Y16	INPUT
2	IP_L34P_2	W16	INPUT
2	IP_L37N_2	AA19	INPUT
2	IP_L37P_2	AB19	INPUT
2	VCCO_2	T12	VCCO
2	VCCO_2	U9	VCCO
2	VCCO_2	V15	VCCO
2	VCCO_2	AA5	VCCO
2	VCCO_2	AA9	VCCO
2	VCCO_2	AA13	VCCO
2	VCCO_2	AA18	VCCO
3	IO_L01N_3	C1	I/O
3	IO_L01P_3	C2	I/O
3	IO_L02N_3/VREF_3	D2	VREF
3	IO_L02P_3	D3	I/O
3	IO_L03N_3	E3	I/O
3	IO_L03P_3	E4	I/O
3	IO_L04N_3	E1	I/O
3	IO_L04P_3	D1	I/O
3	IO_L05N_3	F4	I/O
3	IO_L05P_3	F3	I/O
3	IO_L06N_3	G5	I/O
3	IO_L06P_3	G4	I/O
3	IO_L07N_3	F1	I/O
3	IO_L07P_3	G1	I/O
3	IO_L08N_3/VREF_3	G6	VREF
3	IO_L08P_3	G7	I/O
3	IO_L09N_3	H4	I/O
3	IO_L09P_3	H5	I/O
3	IO_L10N_3	H2	I/O
3	IO_L10P_3	H3	I/O