AMD Xilinx - XC3S100E-4VQG100C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	240
Number of Logic Elements/Cells	2160
Total RAM Bits	73728
Number of I/O	66
Number of Gates	100000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s100e-4vqg100c

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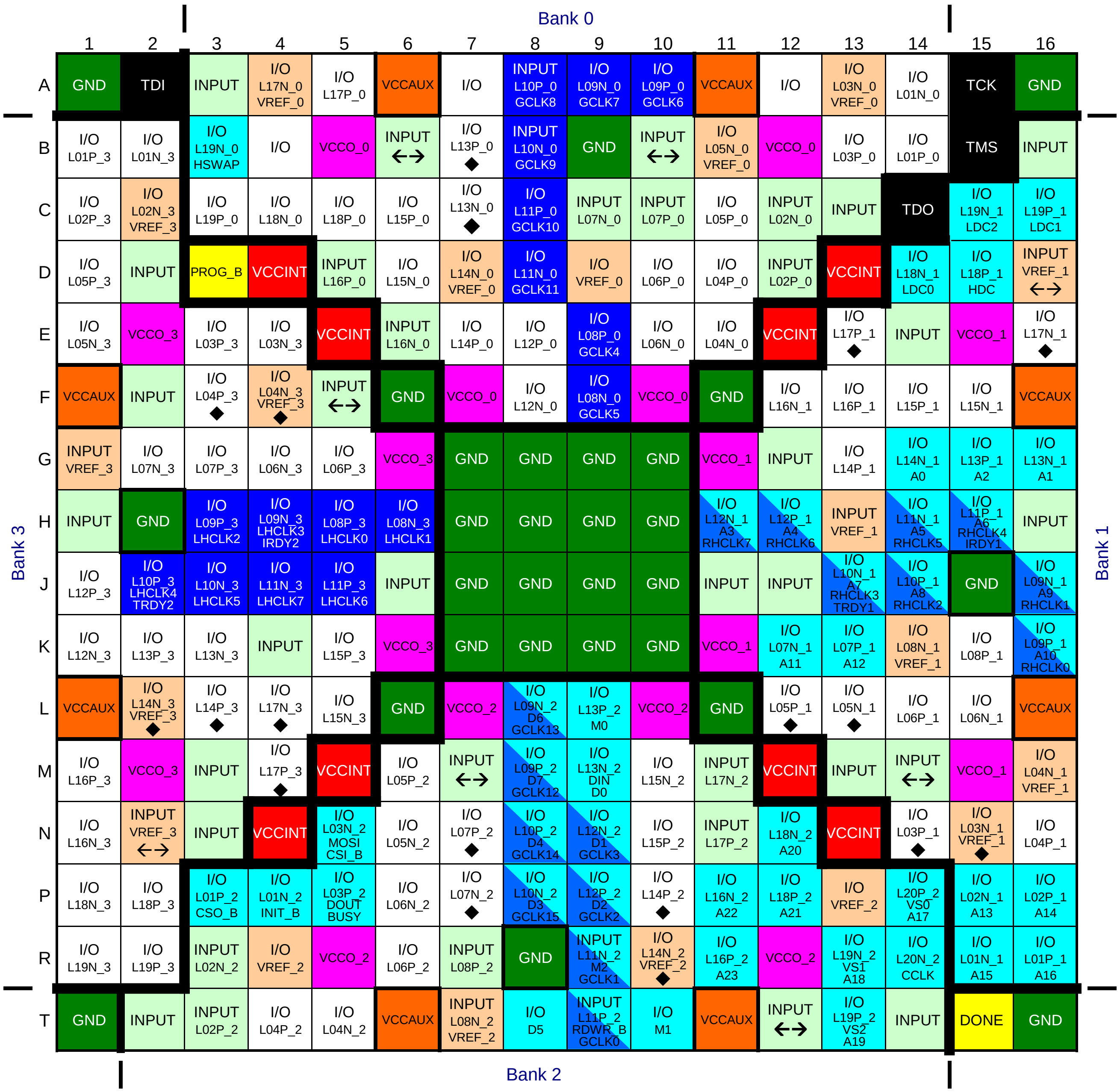
FT256 Footprint



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	GND	TDI	INPUT	I/O L17N_0 VREF_0	I/O L17P_0	VCCAUX	I/O	INPUT L10P_0 GCLK8	I/O L09N_0 GCLK7	I/O L09P_0 GCLK6	VCCAUX	I/O	I/O L03N_0 VREF_0	I/O L01N_0	TCK	GND
B	I/O L01P_3	I/O L01N_3	I/O L19N_0 HSWAP	I/O	VCCO_0	INPUT ←→	I/O L13P_0 ◆	INPUT L10N_0 GCLK9	GND	INPUT ←→	I/O L05N_0 VREF_0	VCCO_0	I/O L03P_0	I/O L01P_0	TMS	INPUT
C	I/O L02P_3	I/O L02N_3 VREF_3	I/O L19P_0	I/O L18N_0	I/O L18P_0	I/O L15P_0	I/O L13N_0 ◆	I/O L11P_0 GCLK10	INPUT L07N_0	INPUT L07P_0	I/O L05P_0	INPUT L02N_0	INPUT	TDO	I/O L19N_1 LDC2	I/O L19P_1 LDC1
D	I/O L05P_3	INPUT	PROG_B	VCCINT	INPUT L16P_0	I/O L15N_0	I/O L14N_0 VREF_0	I/O L11N_0 GCLK11	I/O VREF_0	I/O L06P_0	I/O L04P_0	INPUT L02P_0	VCCINT	I/O L18N_1 LDC0	I/O L18P_1 HDC	INPUT VREF_1 ←→
E	I/O L05N_3	VCCO_3	I/O L03P_3	I/O L03N_3	VCCINT	INPUT L16N_0	I/O L14P_0	I/O L12P_0	I/O L08P_0 GCLK4	I/O L06N_0	I/O L04N_0	VCCINT	I/O L17P_1 ◆	INPUT	VCCO_1	I/O L17N_1 ◆
F	VCCAUX	INPUT	I/O L04P_3 ◆	I/O L04N_3 VREF_3 ◆	INPUT ←→	GND	VCCO_0	I/O L12N_0	I/O L08N_0 GCLK5	VCCO_0	GND	I/O L16N_1	I/O L16P_1	I/O L15P_1	I/O L15N_1	VCCAUX
G	INPUT VREF_3	I/O L07N_3	I/O L07P_3	I/O L06N_3	I/O L06P_3	VCCO_3	GND	GND	GND	GND	VCCO_1	INPUT	I/O L14P_1	I/O L14N_1 A0	I/O L13P_1 A2	I/O L13N_1 A1
H	INPUT	GND	I/O L09P_3 LHCLK2	I/O L09N_3 LHCLK3 IRDY2	I/O L08P_3 LHCLK0	I/O L08N_3 LHCLK1	GND	GND	GND	GND	I/O L12N_1 A3 RHCLK7	I/O L12P_1 A4 RHCLK6	INPUT VREF_1	I/O L11N_1 A5 RHCLK5	I/O L11P_1 A6 RHCLK4 IRDY1	INPUT
J	I/O L12P_3	I/O L10P_3 LHCLK4 TRDY2	I/O L10N_3 LHCLK5	I/O L11N_3 LHCLK7	I/O L11P_3 LHCLK6	INPUT	GND	GND	GND	GND	INPUT	INPUT	I/O L10N_1 A7 RHCLK3 TRDY1	I/O L10P_1 A8 RHCLK2	GND	I/O L09N_1 A9 RHCLK1
K	I/O L12N_3	I/O L13P_3	I/O L13N_3	INPUT	I/O L15P_3	VCCO_3	GND	GND	GND	GND	VCCO_1	I/O L07N_1 A11	I/O L07P_1 A12	I/O L08N_1 VREF_1	I/O L08P_1	I/O L09P_1 A10 RHCLK0
L	VCCAUX	I/O L14N_3 VREF_3 ◆	I/O L14P_3 ◆	I/O L17N_3 ◆	I/O L15N_3	GND	VCCO_2	I/O L09N_2 D6 GCLK13	I/O L13P_2 M0	VCCO_2	GND	I/O L05P_1 ◆	I/O L05N_1 ◆	I/O L06P_1	I/O L06N_1	VCCAUX
M	I/O L16P_3	VCCO_3	INPUT	I/O L17P_3 ◆	VCCINT	I/O L05P_2	INPUT ←→	I/O L09P_2 D7 GCLK12	I/O L13N_2 DIN D0	I/O L15N_2	INPUT L17N_2	VCCINT	INPUT	INPUT ←→	VCCO_1	I/O L04N_1 VREF_1
N	I/O L16N_3	INPUT VREF_3 ←→	INPUT	VCCINT	I/O L03N_2 MOSI CSI_B	I/O L05N_2	I/O L07P_2 ◆	I/O L10P_2 D4 GCLK14	I/O L12N_2 D1 GCLK3	I/O L15P_2	INPUT L17P_2	I/O L18N_2 A20	VCCINT	I/O L03P_1 ◆	I/O L03N_1 VREF_1 ◆	I/O L04P_1
P	I/O L18N_3	I/O L18P_3	I/O L01P_2 CSO_B	I/O L01N_2 INIT_B	I/O L03P_2 DOUT BUSY	I/O L06N_2	I/O L07N_2 ◆	I/O L10N_2 D3 GCLK15	I/O L12P_2 D2 GCLK2	I/O L14P_2 ◆	I/O L16N_2 A22	I/O L18P_2 A21	I/O VREF_2	I/O L20P_2 VS0 A17	I/O L02N_1 A13	I/O L02P_1 A14
R	I/O L19N_3	I/O L19P_3	INPUT L02N_2	I/O VREF_2	VCCO_2	I/O L06P_2	INPUT L08P_2	GND	INPUT L11N_2 M2 GCLK1	I/O L14N_2 VREF_2 ◆	I/O L16P_2 A23	VCCO_2	I/O L19N_2 VS1 A18	I/O L20N_2 CCLK	I/O L01N_1 A15	I/O L01P_1 A16
T	GND	INPUT	INPUT L02P_2	I/O L04P_2	I/O L04N_2	VCCAUX	INPUT L08N_2 VREF_2	I/O D5	INPUT L11P_2 RDWR_B GCLK0	I/O M1	VCCAUX	INPUT ←→	I/O L19P_2 VS2 A19	INPUT	DONE	GND

DS312-4_05_101805

Figure 85: FT256 Package Footprint (top view)

2	CONFIG: Dedicated configuration pins
4	JTAG: Dedicated JTAG port pins
8	VCCINT: Internal core supply voltage (+1.2V)
28	GND: Ground
16	VCCO: Output voltage supply for bank
8	VCCAUX: Auxiliary supply voltage (+2.5V)
6 Å Æ	Migration Difference: For flexible package migration, use these pins as inputs.
18 (‹)	Unconnected pins on XC3S250E