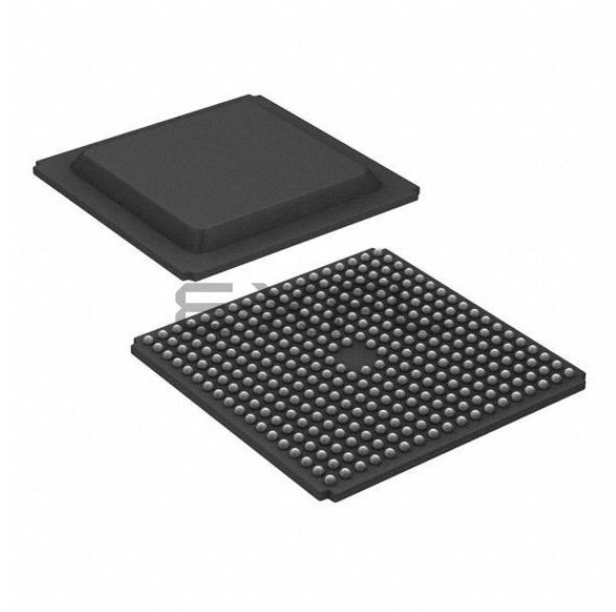

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	2168
Number of Logic Elements/Cells	19512
Total RAM Bits	516096
Number of I/O	250
Number of Gates	1200000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	320-BGA
Supplier Device Package	320-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s1200e-4fg320c

Design Documentation Available

The functionality of the Spartan®-3E FPGA family is now described and updated in the following documents. The topics covered in each guide are listed below.

- UG331: *Spartan-3 Generation FPGA User Guide*
  - Clocking Resources
  - Digital Clock Managers (DCMs)
  - Block RAM
  - Configurable Logic Blocks (CLBs)
    - Distributed RAM
    - SRL16 Shift Registers
    - Carry and Arithmetic Logic
  - I/O Resources
  - Embedded Multiplier Blocks
  - Programmable Interconnect
  - ISE® Design Tools
  - IP Cores
  - Embedded Processing and Control Solutions
  - Pin Types and Package Overview
  - Package Drawings
  - Powering FPGAs
  - Power Management
- UG332: *Spartan-3 Generation Configuration User Guide*
  - Configuration Overview
    - Configuration Pins and Behavior
    - Bitstream Sizes
  - Detailed Descriptions by Mode
    - Master Serial Mode using Xilinx® Platform Flash PROM
    - Master SPI Mode using Commodity SPI Serial Flash PROM
    - Master BPI Mode using Commodity Parallel NOR Flash PROM
    - Slave Parallel (SelectMAP) using a Processor
    - Slave Serial using a Processor
    - JTAG Mode
  - ISE iMPACT Programming Examples
  - MultiBoot Reconfiguration

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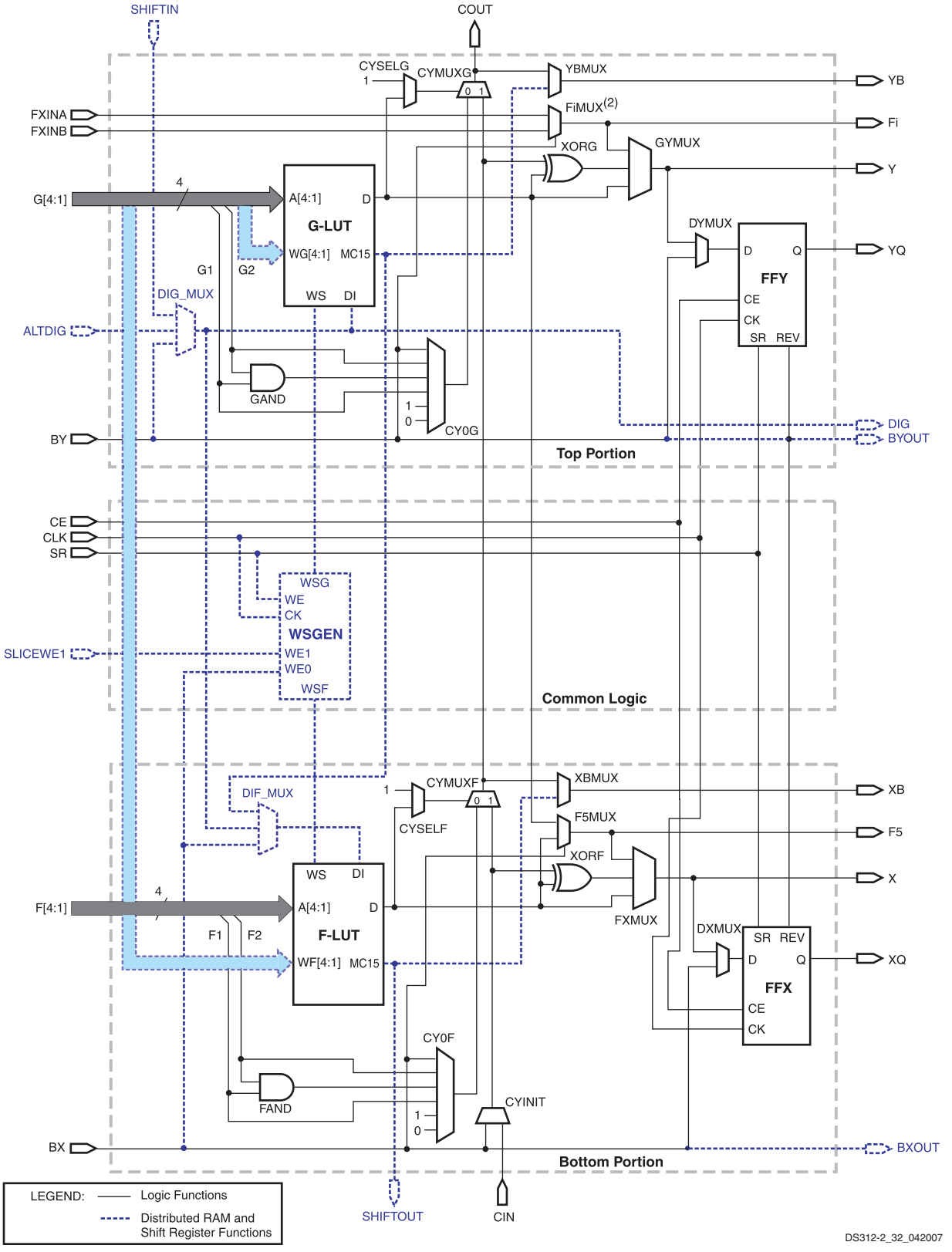
Spartan-3E FPGA Starter Kit

For specific hardware examples, please see the Spartan-3E FPGA Starter Kit board web page, which has links to various design examples and the user guide.

- Spartan-3E FPGA Starter Kit Board page
  http://www.xilinx.com/s3estarter
- UG230: *Spartan-3E FPGA Starter Kit User Guide*



Notes:

1. Options to invert signal polarity as well as other options that enable lines for various functions are not shown.
2. The index i can be 6, 7, or 8, depending on the slice. The upper SLICEL has an F8MUX, and the upper SLICEM has an F7MUX. The lower SLICEL and SLICEM both have an F6MUX.

Figure 15: **Simplified Diagram of the Left-Hand SLICEM**

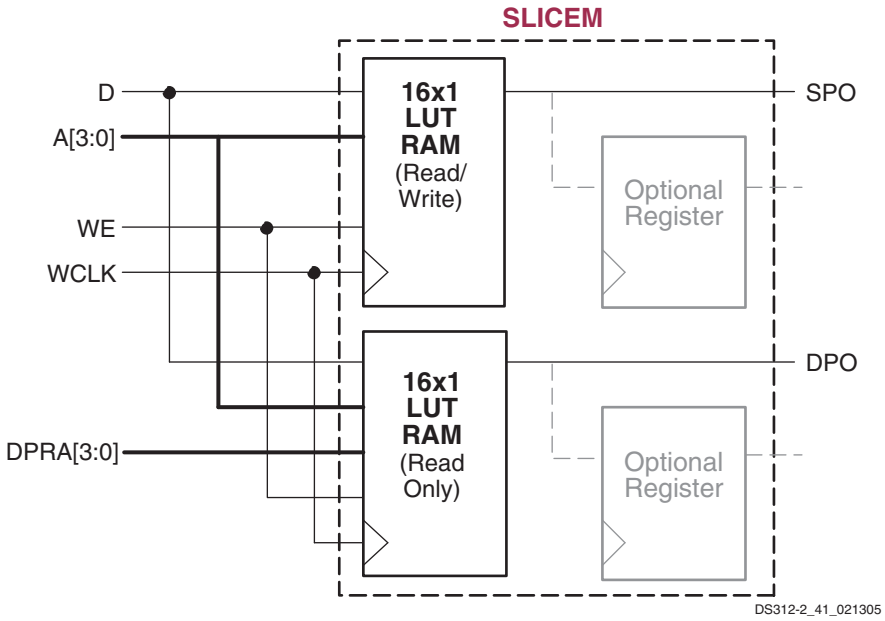


Figure 26: **RAM16X1D Dual-Port Usage**

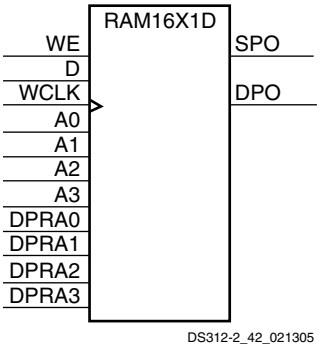


Figure 27: **Dual-Port RAM Component**

Table 18: **Dual-Port RAM Function**

Inputs			Outputs	
WE (mode)	**WCLK**	**D**	**SPO**	**DPO**
0 (read)	X	X	data_a	data_d
1 (read)	0	X	data_a	data_d
1 (read)	1	X	data_a	data_d
1 (write)	↑	D	D	data_d
1 (read)	↓	X	data_a	data_d

Notes:

1. data_a = word addressed by bits A3-A0.
2. data_d = word addressed by bits DPRA3-DPRA0.

Table 19: **Distributed RAM Signals**

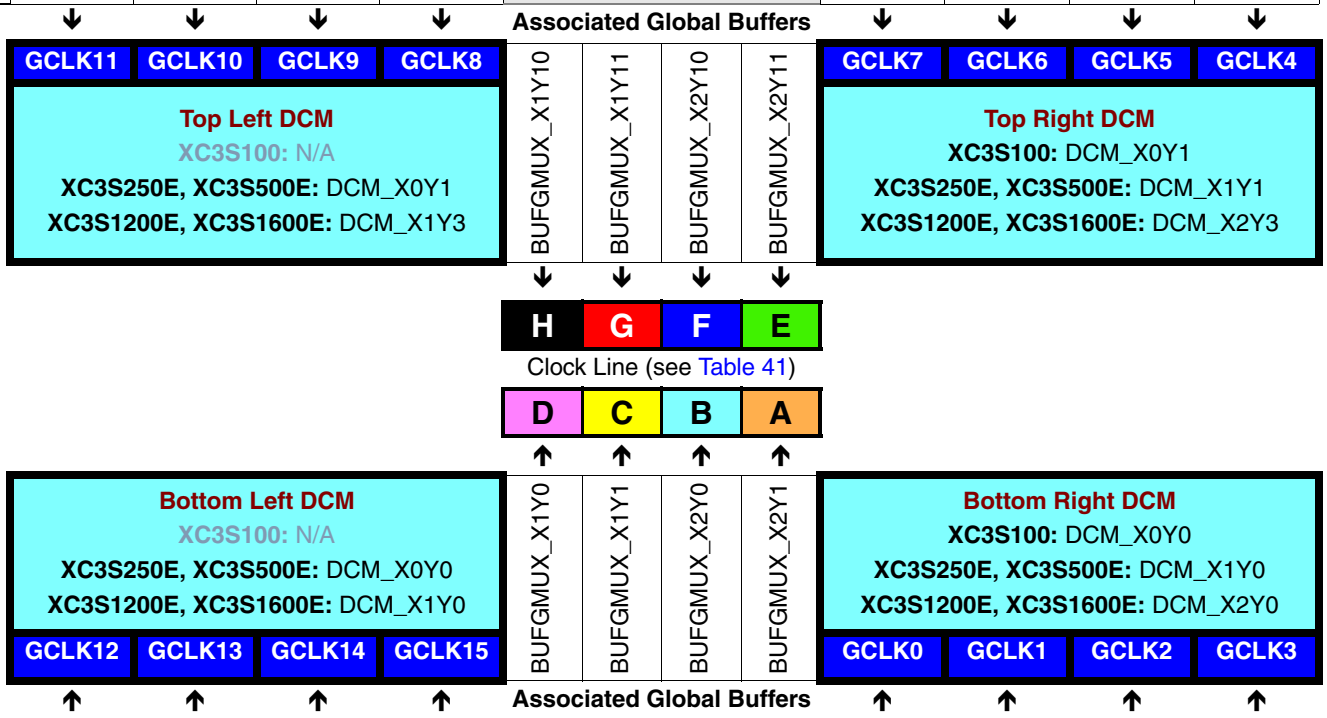
Signal	Description
WCLK	The clock is used for synchronous writes. The data and the address input pins have setup times referenced to the WCLK pin. Active on the positive edge by default with built-in programmable polarity.
WE	The enable pin affects the write functionality of the port. An inactive Write Enable prevents any writing to memory cells. An active Write Enable causes the clock edge to write the data input signal to the memory location pointed to by the address inputs. Active High by default with built-in programmable polarity.
A0, A1, A2, A3 (A4, A5)	The address inputs select the memory cells for read or write. The width of the port determines the required address inputs.
D	The data input provides the new data value to be written into the RAM.
O, SPO, and DPO	The data output O on single-port RAM or the SPO and DPO outputs on dual-port RAM reflects the contents of the memory cells referenced by the address inputs. Following an active write clock edge, the data out (O or SPO) reflects the newly written data.

The INIT attribute can be used to preload the memory with data during FPGA configuration. The default initial contents for RAM is all zeros. If the WE is held Low, the element can be considered a ROM. The ROM function is possible even in the SLICEL.

The global write enable signal, GWE, is asserted automatically at the end of device configuration to enable all writable elements. The GWE signal guarantees that the

Table 30: **Direct Clock Input Connections and Optional External Feedback to Associated DCMs**

Package	Differential Pair		Differential Pair			Differential Pair		Differential Pair	
	N	P	N	P		N	P	N	P
	Pin Number for Single-Ended Input					Pin Number for Single-Ended Input			
VQ100	P91	P90	P89	P88		P86	P85	P84	P83
CP132	B7	A7	C8	B8		A9	B9	C9	A10
TQ144	P131	P130	P129	P128		P126	P125	P123	P122
PQ208	P186	P185	P184	P183		P181	P180	P178	P177
FT256	D8	C8	B8	A8		A9	A10	F9	E9
FG320	D9	C9	B9	B8		A10	B10	E10	D10
FG400	A9	A10	G10	H10		E10	E11	G11	F11
FG484	B11	C11	H11	H12		C12	B12	E12	F12



Package	Differential Pair		Differential Pair			Differential Pair		Differential Pair	
	P	N	P	N		P	N	P	N
	Pin Number for Single-Ended Input					Pin Number for Single-Ended Input			
VQ100	P32	P33	P35	P36		P38	P39	P40	P41
CP132	M4	N4	M5	N5		M6	N6	P6	P7
TQ144	P50	P51	P53	P54		P56	P57	P58	P59
PQ208	P74	P75	P77	P78		P80	P81	P82	P83
FT256	M8	L8	N8	P8		T9	R9	P9	N9
FG320	N9	M9	U9	V9		U10	T10	R10	P10
FG400	W9	W10	R10	P10		P11	P12	V10	V11
FG484	V11	U11	R11	T11		R12	P12	Y12	W12

DLL Clock Output and Feedback Connections

As many as four of the nine DCM clock outputs can simultaneously drive four of the BUFGMUX buffers on the same die edge. All DCM clock outputs can simultaneously drive general routing resources, including interconnect leading to OBUF buffers.

The feedback loop is essential for DLL operation. Either the CLK0 or CLK2X outputs feed back to the CLKFB input via a BUFGMUX global buffer to eliminate the clock distribution delay. The specific BUFGMUX buffer used to feed back the CLK0 or CLK2X signal is ideally one of the BUFGMUX buffers associated with a specific DCM, as shown in Table 30, Table 31, and Table 32.

The feedback path also phase-aligns the other seven DLL outputs: CLK0, CLK90, CLK180, CLK270, CLKDV, CLK2X, or CLK2X180. The CLK_FEEDBACK attribute value must agree with the physical feedback connection. Use “1X” for CLK0 feedback and “2X” for CLK2X feedback. If the DFS unit is used stand-alone, without the DLL, then no feedback is required and set the CLK_FEEDBACK attribute to “NONE”.

Two basic cases determine how to connect the DLL clock outputs and feedback connections: on-chip synchronization and off-chip synchronization, which are illustrated in Figure 42a through Figure 42d.

In the on-chip synchronization case in Figure 42a and Figure 42b, it is possible to connect any of the DLL’s seven output clock signals through general routing resources to the FPGA’s internal registers. Either a Global Clock Buffer (BUFG) or a BUFGMUX affords access to the global clock network. As shown in Figure 42a, the feedback loop is created by routing CLK0 (or CLK2X) in Figure 42b to a global clock net, which in turn drives the CLKFB input.

In the off-chip synchronization case in Figure 42c and Figure 42d, CLK0 (or CLK2X) plus any of the DLL’s other output clock signals exit the FPGA using output buffers (OBUF) to drive an external clock network plus registers on the board. As shown in Figure 42c, the feedback loop is formed by feeding CLK0 (or CLK2X) in Figure 42d back into the FPGA, then to the DCM’s CLKFB input via a Global Buffer Input, specified in Table 30.

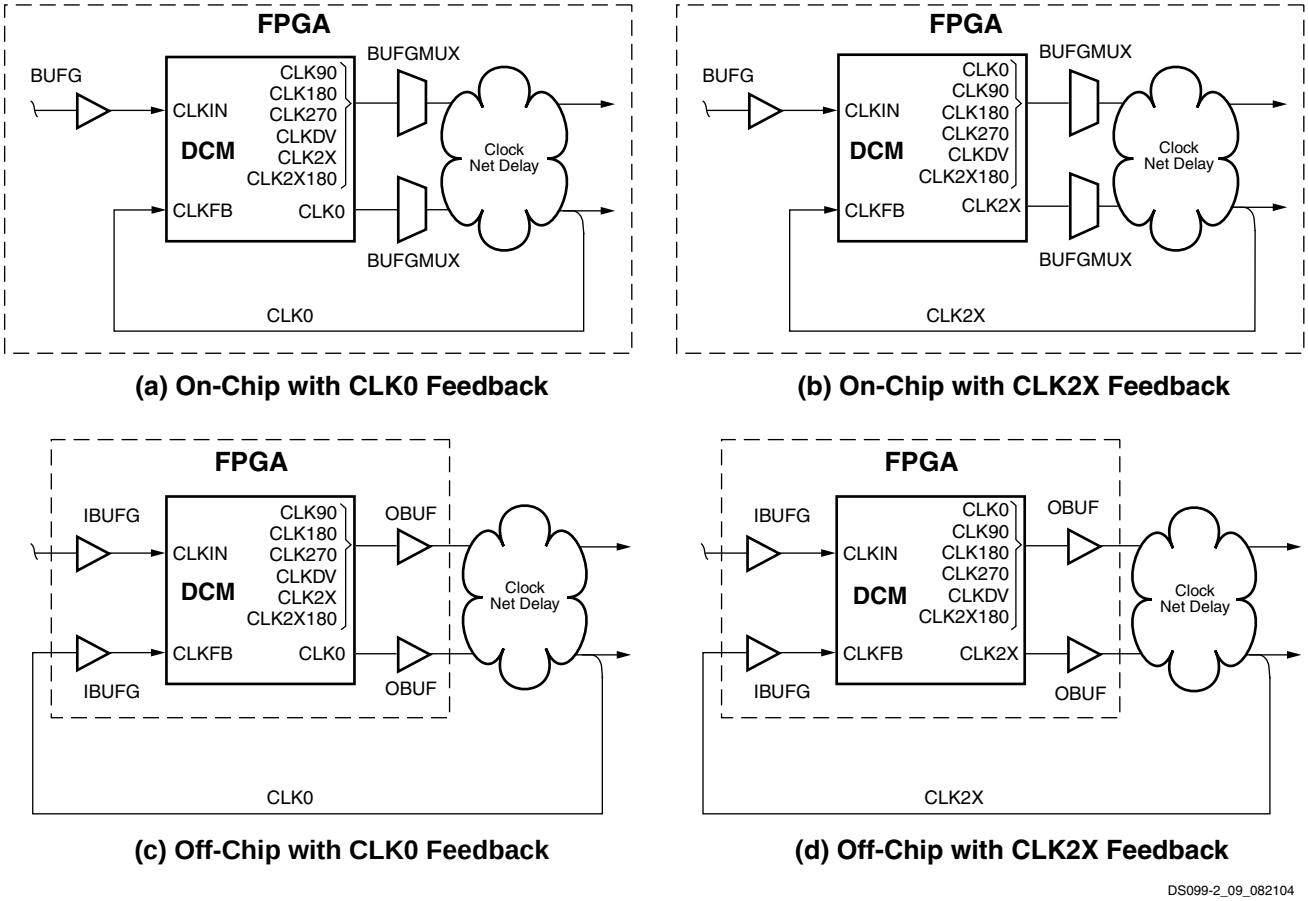


Figure 42: **Input Clock, Output Clock, and Feedback Connections for the DLL**

Direct Connections

Direct connect lines route signals to neighboring tiles: vertically, horizontally, and diagonally. These lines most often drive a signal from a “source” tile to a double, hex, or long line and conversely from the longer interconnect back to a direct line accessing a “destination” tile.

Global Controls (STARTUP_SPARTAN3E)

In addition to the general-purpose interconnect, Spartan-3E FPGAs have two global logic control signals, as described in Table 43. These signals are available to the FPGA application via the STARTUP_SPARTAN3E primitive.

Table 43: **Spartan-3E Global Logic Control Signals**

Global Control Input	Description
GSR	**Global Set/Reset:** When High, asynchronously places all registers and flip-flops in their initial state (see Initialization, page 31). Asserted automatically during the FPGA configuration process (see Start-Up, page 105).
GTS	**Global Three-State:** When High, asynchronously forces all I/O pins to a high-impedance state (Hi-Z, three-state).

The Global Set/Reset (GSR) signal replaces the global reset signal included in many ASIC-style designs. Use the GSR control instead of a separate global reset signal in the design to free up CLB inputs, resulting in a smaller, more efficient design. Similarly, the GSR signal is asserted automatically during the FPGA configuration process, guaranteeing that the FPGA starts-up in a known state.

The STARTUP_SPARTAN3E primitive also includes two other signals used specifically during configuration. The MBT signals are for Dynamically Loading Multiple Configuration Images Using MultiBoot Option, page 91. The CLK input is an alternate clock for configuration Start-Up, page 105.

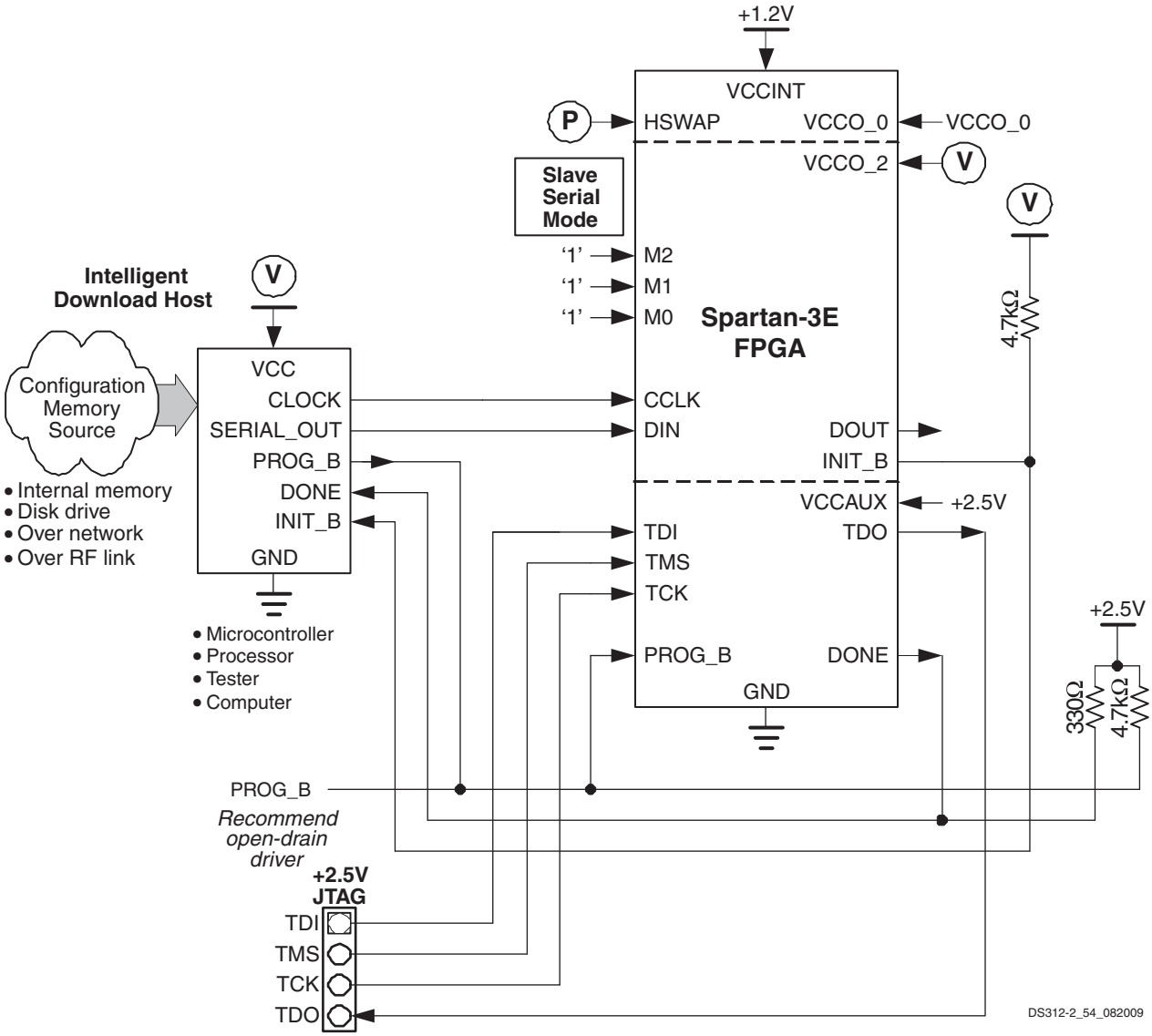


Figure 63: **Slave Serial Configuration**

The mode select pins, M[2:0], are sampled when the FPGA's INIT_B output goes High and must be at defined logic levels during this time. After configuration, when the FPGA's DONE output goes High, the mode pins are available as full-featured user-I/O pins.

(P) Similarly, the FPGA's HSWAP pin must be Low to enable pull-up resistors on all user-I/O pins or High to disable the pull-up resistors. The HSWAP control must remain at a constant logic level throughout FPGA configuration. After configuration, when the FPGA's DONE output goes High, the HSWAP pin is available as full-featured user-I/O pin and is powered by the VCCO_0 supply.

Voltage Compatibility

(V) Most Slave Serial interface signals are within the FPGA's I/O Bank 2, supplied by the VCCO_2 supply input. The VCCO_2 voltage can be 3.3V, 2.5V, or 1.8V to match the requirements of the external host, ideally 2.5V. Using 3.3V or 1.8V requires additional design considerations as the DONE and PROG_B pins are powered by the FPGA's 2.5V V_{CCAUX} supply. See XAPP453: *The 3.3V Configuration of Spartan-3 FPGAs* for additional information.

Daisy-Chaining

If the application requires multiple FPGAs with different configurations, then configure the FPGAs using a daisy chain, as shown in Figure 64. Use Slave Serial mode (M[2:0] = <1:1:1>) for all FPGAs in the daisy-chain. After the lead FPGA is filled with its configuration data, the lead

Date	Version	Revision
03/16/07	3.5	Added information about new Spartan-3 Generation user guides (Design Documentation Available). Added cross-references to UG331: *Spartan-3 Generation FPGA User Guide* and to UG332: *Spartan-3 Generation Configuration User Guide*. Added note about possible JTAG configuration issues when the FPGA mode pins are set for Master mode and using software prior to ISE 9.1.01i (JTAG Mode). Removed a few lingering references to "weak" pull-up resistors, including in Figure 12. Removed vestigial references regarding the LDC[2:0] and HDC pins during Slave Parallel Mode configuration. These pins are not used in this configuration mode.
05/29/07	3.6	Added information about HSWAP and PCI differences between steppings to Table 71. Removed "Performance Differences between Global Buffers" to match improved specs in Module 3. Updated PROG_B pulse width descriptions to match specification in Module 3.
04/18/08	3.7	Corrected Figure 6 to show six taps and updated associated text. Added note for recommended pull-up on DONE in Table 55 and elsewhere. Added a caution regarding Persist of pins A20-A23. Updated Stepping description in Table 71 to note that only Stepping 1 is in production today. Updated links.
08/26/09	3.8	Added a frequency limitation to Equation 6. Added a new Equation 7 with a frequency limitation. Added a Spread Spectrum, page 56 paragraph. Added Table 42, page 60. Updated a Flash vendor name in Table 61, page 88. Removed the $\leq$ symbol from the flash read access times in Table 62, page 88. Revised the first paragraph in Configuration Sequence, page 101. Revised the first paragraph in Power-On Behavior, page 110. Revised the second paragraph in Production Stepping, page 111. Revised the first paragraph in Ordering a Later Stepping, page 111.
10/29/12	4.0	Added Notice of Disclaimer. This product is not recommended for new designs. Updated the design note section in VARIABLE Phase Shift Mode. Added the VQ100 to the Quadrant Clock Routing section.

Notice of Disclaimer

Quiescent Current Requirements

Table 79: **Quiescent Supply Current Characteristics**

Symbol	Description	Device	Typical	Commercial Maximum(1)	Industrial Maximum(1)	Units
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC3S100E	8	27	36	mA
		XC3S250E	15	78	104	mA
		XC3S500E	25	106	145	mA
		XC3S1200E	50	259	324	mA
		XC3S1600E	65	366	457	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC3S100E	0.8	1.0	1.5	mA
		XC3S250E	0.8	1.0	1.5	mA
		XC3S500E	0.8	1.0	1.5	mA
		XC3S1200E	1.5	2.0	2.5	mA
		XC3S1600E	1.5	2.0	2.5	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC3S100E	8	12	13	mA
		XC3S250E	12	22	26	mA
		XC3S500E	18	31	34	mA
		XC3S1200E	35	52	59	mA
		XC3S1600E	45	76	86	mA

Notes:

1. The maximum numbers in this table indicate the minimum current each power rail requires in order for the FPGA to power-on successfully.
2. The numbers in this table are based on the conditions set forth in Table 77.
3. Quiescent supply current is measured with all I/O drivers in a high-impedance state and with all pull-up/pull-down resistors at the I/O pads disabled. Typical values are characterized using typical devices at room temperature (T_J of 25°C at V_{CCINT} = 1.2 V, V_{CCO} = 3.3V, and V_{CCAUX} = 2.5V). The maximum limits are tested for each device at the respective maximum specified junction temperature and at maximum voltage limits with V_{CCINT} = 1.26V, V_{CCO} = 3.465V, and V_{CCAUX} = 2.625V. The FPGA is programmed with a "blank" configuration data file (i.e., a design with no functional elements instantiated). For conditions other than those described above, (e.g., a design including functional elements), measured quiescent current levels may be different than the values in the table. For more accurate estimates for a specific design, use the Xilinx® XPower tools.
4. There are two recommended ways to estimate the total power consumption (quiescent plus dynamic) for a specific design: a) The Spartan-3E XPower Estimator provides quick, approximate, typical estimates, and does not require a netlist of the design. b) XPower Analyzer uses a netlist as input to provide maximum estimates as well as more accurate typical estimates.

Single-Ended I/O Standards

Table 80: **Recommended Operating Conditions for User I/Os Using Single-Ended Standards**

IOSTANDARD Attribute	V_{CCO} for Drivers[2]			V_{REF}			V_{IL}	V_{IH}[3]
	Min (V)	Nom (V)	Max (V)	Min (V)	Nom (V)	Max (V)	Max (V)	Min (V)
LVTTL	3.0	3.3	3.465	V_{REF} is not used for these I/O standards			0.8	2.0
LVCMOS33[4]	3.0	3.3	3.465				0.8	2.0
LVCMOS25[4,5]	2.3	2.5	2.7				0.7	1.7
LVCMOS18	1.65	1.8	1.95				0.4	0.8
LVCMOS15	1.4	1.5	1.6				0.4	0.8
LVCMOS12	1.1	1.2	1.3				0.4	0.7
PCI33_3[6]	3.0	3.3	3.465				0.3 • V_{CCO}	0.5 • V_{CCO}
PCI66_3[6]	3.0	3.3	3.465				0.3 • V_{CCO}	0.5 • V_{CCO}
HSTL_I_18	1.7	1.8	1.9	0.8	0.9	1.1	V_{REF} - 0.1	V_{REF} + 0.1
HSTL_III_18	1.7	1.8	1.9	-	1.1	-	V_{REF} - 0.1	V_{REF} + 0.1
SSTL18_I	1.7	1.8	1.9	0.833	0.900	0.969	V_{REF} - 0.125	V_{REF} + 0.125
SSTL2_I	2.3	2.5	2.7	1.15	1.25	1.35	V_{REF} - 0.125	V_{REF} + 0.125

Notes:

1. Descriptions of the symbols used in this table are as follows:
   V_{CCO} – the supply voltage for output drivers
   V_{REF} – the reference voltage for setting the input switching threshold
   V_{IL} – the input voltage that indicates a Low logic level
   V_{IH} – the input voltage that indicates a High logic level
2. The V_{CCO} rails supply only output drivers, not input circuits.
3. For device operation, the maximum signal voltage (V_{IH} max) may be as high as V_{IN} max. See Table 73.
4. There is approximately 100 mV of hysteresis on inputs using LVCMOS33 and LVCMOS25 I/O standards.
5. All Dedicated pins (PROG_B, DONE, TCK, TDI, TDO, and TMS) use the LVCMOS25 standard and draw power from the V_{CCAUX} rail (2.5V). The Dual-Purpose configuration pins use the LVCMOS standard before the User mode. When using these pins as part of a standard 2.5V configuration interface, apply 2.5V to the V_{CCO} lines of Banks 0, 1, and 2 at power-on as well as throughout configuration.
6. For information on PCI IP solutions, see www.xilinx.com/pci. The PCIX IOSTANDARD is available and has equivalent characteristics but no PCI-X IP is supported.

Table 87: **Pin-to-Pin Setup and Hold Times for the IOB Input Path (System Synchronous)**

Symbol	Description	Conditions	IFD_DELAY_VALUE=	Device	Speed Grade		Units
					-5	-4	
					Min	Min	
Setup Times							
T_{PSDCM}	When writing to the Input Flip-Flop (IFF), the time from the setup of data at the Input pin to the active transition at a Global Clock pin. The DCM is used. No Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = 0, with DCM(3)	0	XC3S100E	2.65	2.98	ns
				XC3S250E	2.25	2.59	ns
				XC3S500E	2.25	2.59	ns
				XC3S1200E	2.25	2.58	ns
				XC3S1600E	2.25	2.59	ns
T_{PSFD}	When writing to IFF, the time from the setup of data at the Input pin to an active transition at the Global Clock pin. The DCM is not used. The Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = default software setting	2	XC3S100E	3.16	3.58	ns
			3	XC3S250E	3.44	3.91	ns
			3	XC3S500E	4.00	4.73	ns
			3	XC3S1200E	2.60	3.31	ns
			3	XC3S1600E	3.33	3.77	ns
Hold Times							
T_{PHDCM}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is used. No Input Delay is programmed.	LVCMOS25(4), IFD_DELAY_VALUE = 0, with DCM(3)	0	XC3S100E	–0.54	–0.52	ns
				XC3S250E	0.06	0.14	ns
				XC3S500E	0.07	0.14	ns
				XC3S1200E	0.07	0.15	ns
				XC3S1600E	0.06	0.14	ns
T_{PHFD}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is not used. The Input Delay is programmed.	LVCMOS25(4), IFD_DELAY_VALUE = default software setting	2	XC3S100E	–0.31	–0.24	ns
			3	XC3S250E	–0.32	–0.32	ns
			3	XC3S500E	–0.77	–0.77	ns
			3	XC3S1200E	0.13	0.16	ns
			3	XC3S1600E	–0.05	–0.03	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 95 and are based on the operating conditions set forth in Table 77 and Table 80.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, subtract the appropriate adjustment from Table 91. If this is true of the data Input, add the appropriate Input adjustment from the same table.
3. DCM output jitter is included in all measurements.
4. This hold time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, add the appropriate Input adjustment from Table 91. If this is true of the data Input, subtract the appropriate Input adjustment from the same table. When the hold time is negative, it is possible to change the data before the clock's active edge.

Table 90: **Propagation Times for the IOB Input Path**

Symbol	Description	Conditions	IFD_DELAY_VALUE=	Device	Speed Grade		Units
					-5	-4	
					Min	Min	
Propagation Times							
T_{IOPLI}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with no input delay programmed	LVCMOS25(2), IFD_DELAY_VALUE = 0	0	All	1.96	2.25	ns
T_{IOPLID}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with the input delay programmed	LVCMOS25(2), IFD_DELAY_VALUE = default software setting	2	XC3S100E	5.40	5.97	ns
			3	All Others	6.30	7.20	

Notes:

1. The numbers in this table are tested using the methodology presented in Table 95 and are based on the operating conditions set forth in Table 77 and Table 80.
2. This propagation time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. When this is true, *add* the appropriate Input adjustment from Table 91.

Table 91: **Input Timing Adjustments by IOSTANDARD**

Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
Single-Ended Standards			
LVTTL	0.42	0.43	ns
LVCMOS33	0.42	0.43	ns
LVCMOS25	0	0	ns
LVCMOS18	0.96	0.98	ns
LVCMOS15	0.62	0.63	ns
LVCMOS12	0.26	0.27	ns
PCI33_3	0.41	0.42	ns
PCI66_3	0.41	0.42	ns
HSTL_I_18	0.12	0.12	ns
HSTL_III_18	0.17	0.17	ns
SSTL18_I	0.30	0.30	ns
SSTL2_I	0.15	0.15	ns

Table 91: **Input Timing Adjustments by IOSTANDARD *(Cont'd)***

Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
Differential Standards			
LVDS_25	0.48	0.49	ns
BLVDS_25	0.39	0.39	ns
MINI_LVDS_25	0.48	0.49	ns
LVPECL_25	0.27	0.27	ns
RSDS_25	0.48	0.49	ns
DIFF_HSTL_I_18	0.48	0.49	ns
DIFF_HSTL_III_18	0.48	0.49	ns
DIFF_SSTL18_I	0.30	0.30	ns
DIFF_SSTL2_I	0.32	0.32	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 95 and are based on the operating conditions set forth in Table 77, Table 80, and Table 82.
2. These adjustments are used to convert input path times originally specified for the LVCMOS25 standard to times that correspond to other signal standards.

Configuration Clock (CCLK) Characteristics

Table 112: **Master Mode CCLK Output Period by *ConfigRate* Option Setting**

Symbol	Description	*ConfigRate* Setting	Temperature Range	Minimum	Maximum	Units
T_{CCLK1}	CCLK clock period by ***ConfigRate*** setting	1 *(power-on value and default value)*	Commercial	570	1,250	ns
			Industrial	485		ns
T_{CCLK3}		3	Commercial	285	625	ns
			Industrial	242		ns
T_{CCLK6}		6	Commercial	142	313	ns
			Industrial	121		ns
T_{CCLK12}		12	Commercial	71.2	157	ns
			Industrial	60.6		ns
T_{CCLK25}		25	Commercial	35.5	78.2	ns
			Industrial	30.3		ns
T_{CCLK50}		50	Commercial	17.8	39.1	ns
			Industrial	15.1		ns

Notes:

1. Set the ***ConfigRate*** option value when generating a configuration bitstream. See Bitstream Generator (BitGen) Options in Module 2.

Table 113: **Master Mode CCLK Output Frequency by *ConfigRate* Option Setting**

Symbol	Description	*ConfigRate* Setting	Temperature Range	Minimum	Maximum	Units
F_{CCLK1}	Equivalent CCLK clock frequency by ***ConfigRate*** setting	1 *(power-on value and default value)*	Commercial	0.8	1.8	MHz
			Industrial		2.1	MHz
F_{CCLK3}		3	Commercial	1.6	3.6	MHz
			Industrial		4.2	MHz
F_{CCLK6}		6	Commercial	3.2	7.1	MHz
			Industrial		8.3	MHz
F_{CCLK12}		12	Commercial	6.4	14.1	MHz
			Industrial		16.5	MHz
F_{CCLK25}		25	Commercial	12.8	28.1	MHz
			Industrial		33.0	MHz
F_{CCLK50}		50	Commercial	25.6	56.2	MHz
			Industrial		66.0	MHz

Table 114: **Master Mode CCLK Output Minimum Low and High Time**

Symbol	Description		*ConfigRate* Setting						Units
			1	3	6	12	25	50	
T_{MCCL}, T_{MCCH}	Master mode CCLK minimum Low and High time	Commercial	276	138	69	34.5	17.1	8.5	ns
		Industrial	235	117	58	29.3	14.5	7.3	ns

Table 115: **Slave Mode CCLK Input Low and High Time**

Symbol	Description	Min	Max	Units
T_{SCCL}, T_{SCCH}	CCLK Low and High time	5	∞	ns

Master Serial and Slave Serial Mode Timing

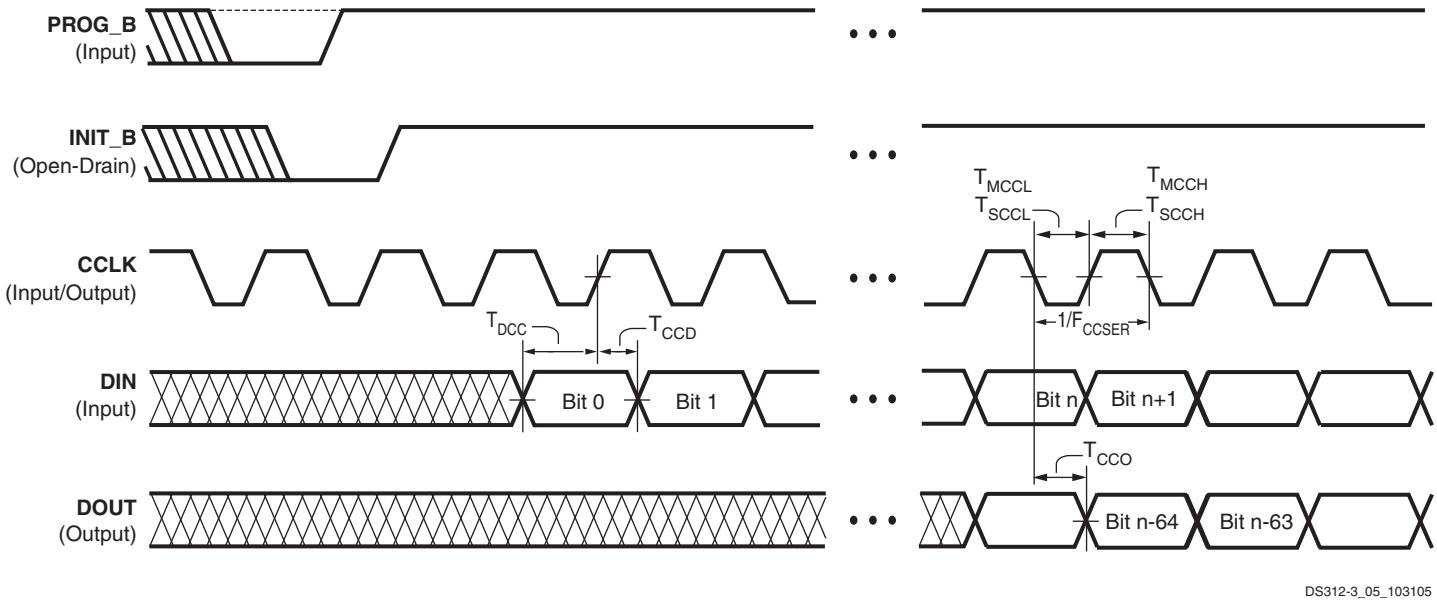


Figure 74: **Waveforms for Master Serial and Slave Serial Configuration**

Table 116: **Timing for the Master Serial and Slave Serial Configuration Modes**

Symbol	Description		Slave/ Master	All Speed Grades		Units
				Min	Max	
Clock-to-Output Times						
T_{CCO}	The time from the falling transition on the CCLK pin to data appearing at the DOUT pin		Both	1.5	10.0	ns
Setup Times						
T_{DCC}	The time from the setup of data at the DIN pin to the active edge of the CCLK pin		Both	11.0	-	ns
Hold Times						
T_{CCD}	The time from the active edge of the CCLK pin to the point when data is last held at the DIN pin		Both	0	-	ns
Clock Timing						
T_{CCH}	High pulse width at the CCLK input pin		Master	See Table 114		
			Slave	See Table 115		
T_{CCL}	Low pulse width at the CCLK input pin		Master	See Table 114		
			Slave	See Table 115		
F_{CCSER}	Frequency of the clock signal at the CCLK input pin	No bitstream compression	Slave	0	66(2)	MHz
		With bitstream compression		0	20	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 77.
2. For serial configuration with a daisy-chain of multiple FPGAs, the maximum limit is 25 MHz.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/01/05	1.0	Initial Xilinx release.
11/23/05	2.0	Added AC timing information and additional DC specifications.
03/22/06	3.0	Upgraded data sheet status to Preliminary. Finalized production timing parameters. All speed grades for all Spartan-3E FPGAs are now Production status using the v1.21 speed files, as shown in Table 84. Expanded description in Note 2, Table 78. Updated pin-to-pin and clock-to-output timing based on final characterization, shown in Table 86. Updated system-synchronous input setup and hold times based on final characterization, shown in Table 87 and Table 88. Updated other I/O timing in Table 90. Provided input and output adjustments for LVPECL_25, DIFF_SSTL and DIFF_HSTL I/O standards that supersede the v1.21 speed file values, in Table 91 and Table 94. Reduced I/O three-state and set/reset delays in Table 93. Added XC3S100E FPGA in CP132 package to Table 96. Increased T_{AS} slice flip-flop timing by 100 ps in Table 98. Updated distributed RAM timing in Table 99 and SRL16 timing in Table 100. Updated global clock timing, removed left/right clock buffer limits in Table 101. Updated block RAM timing in Table 103. Added DCM parameters for remainder of Step 0 device; added improved Step 1 DCM performance to Table 104, Table 105, Table 106, and Table 107. Added minimum INIT_B pulse width specification, T_{INIT}, in Table 111. Increased data hold time for Slave Parallel mode to 1.0 ns (T_{SMCCD}) in Table 117. Improved the DCM performance for the XC3S1200E, Stepping 0 in Table 104, Table 105, Table 106, and Table 107. Corrected links in Table 118 and Table 120. Added MultiBoot timing specifications to Table 122.
04/07/06	3.1	Improved SSO limits for LVDS_25, MINI_LVDS_25, and RSDS_25 I/O standards in the QFP packages (Table 97). Removed potentially confusing Note 2 from Table 78.
05/19/06	3.2	Clarified that 100 mV of hysteresis applies to LVCMOS33 and LVCMOS25 I/O standards (Note 4, Table 80). Other minor edits.
05/30/06	3.2.1	Corrected various typos and incorrect links.
11/09/06	3.4	Improved absolute maximum voltage specifications in Table 73, providing additional overshoot allowance. Widened the recommended voltage range for PCI and PCI-X standards in Table 80. Clarified Note 2, Table 83. Improved various timing specifications for v1.26 speed file. Added Table 85 to summarize the history of speed file releases after which time all devices became Production status. Added absolute minimum values for Table 86, Table 92, and Table 93. Updated pin-to-pin setup and hold timing based on default IFD_DELAY_VALUE settings in Table 87, Table 88, and Table 90. Added Table 89 about source-synchronous input capture sample window. Promoted Module 3 to Production status. Synchronized all modules to v3.4.
03/16/07	3.5	Based on extensive 90 nm production data, improved (reduced) the maximum quiescent current limits for the I_{CCINTQ}, I_{CCAUXQ}, and I_{CCOQ} specifications in Table 79 by an average of 50%.
05/29/07	3.6	Added note to Table 74 and Table 75 regarding HSWAP in step 0 devices. Updated t_{RPW_CLB} in Table 98 to match value in speed file. Improved CLKOUT_FREQ_CLK90 to 200 MHz for Stepping 1 in Table 105.
04/18/08	3.7	Clarified that Stepping 0 was offered only for -4C and removed Stepping 0 -5 specifications. Added reference to XAPP459 in Table 73 and Table 77. Improved recommended max V_{CCO} to 3.465V (3.3V + 5%) in Table 77. Removed minimum input capacitance from Table 78. Updated Recommended Operating Conditions for LVCMOS and PCI I/O standards in Table 80. Removed Absolute Minimums from Table 86, Table 92 and Table 93 and added footnote recommending use of Timing Analyzer for minimum values. Updated T_{PSFD} and T_{PHFD} in Table 87 to match current speed file. Update T_{RPW_IOB} in Table 88 to match current speed file and CLB equivalent spec. Added XC3S500E VQG100 to Table 96. Replaced $T_{MULCKID}$ with T_{MSCKD} for A, B, and P registers in Table 102. Updated CLKOUT_PER_JITT_FX in Table 107. Updated MAX_STEPS equation in Table 109. Updated Figure 77 and Table 120 to correct CCLK active edge. Updated links.

Table 137: **TQ144 Package Pinout *(Cont'd)***

Bank	XC3S100E Pin Name	XC3S250E Pin Name	TQ144 Pin	Type
1	IO_L02P_1/A14	IO_L02P_1/A14	P76	DUAL
1	IO_L03N_1/A11	IO_L03N_1/A11	P82	DUAL
1	IO_L03P_1/A12	IO_L03P_1/A12	P81	DUAL
1	IO_L04N_1/A9/RHCLK1	IO_L04N_1/A9/RHCLK1	P86	RHCLK/DUAL
1	IO_L04P_1/A10/RHCLK0	IO_L04P_1/A10/RHCLK0	P85	RHCLK/DUAL
1	IO_L05N_1/A7/RHCLK3/TRDY1	IO_L05N_1/A7/RHCLK3	P88	RHCLK/DUAL
1	IO_L05P_1/A8/RHCLK2	IO_L05P_1/A8/RHCLK2	P87	RHCLK/DUAL
1	IO_L06N_1/A5/RHCLK5	IO_L06N_1/A5/RHCLK5	P92	RHCLK/DUAL
1	IO_L06P_1/A6/RHCLK4/IRDY1	IO_L06P_1/A6/RHCLK4	P91	RHCLK/DUAL
1	IO_L07N_1/A3/RHCLK7	IO_L07N_1/A3/RHCLK7	P94	RHCLK/DUAL
1	IO_L07P_1/A4/RHCLK6	IO_L07P_1/A4/RHCLK6	P93	RHCLK/DUAL
1	IO_L08N_1/A1	IO_L08N_1/A1	P97	DUAL
1	IO_L08P_1/A2	IO_L08P_1/A2	P96	DUAL
1	IO_L09N_1/LDC0	IO_L09N_1/LDC0	P104	DUAL
1	IO_L09P_1/HDC	IO_L09P_1/HDC	P103	DUAL
1	IO_L10N_1/LDC2	IO_L10N_1/LDC2	P106	DUAL
1	IO_L10P_1/LDC1	IO_L10P_1/LDC1	P105	DUAL
1	IP	IP	P78	INPUT
1	IP	IP	P84	INPUT
1	IP	IP	P89	INPUT
1	IP	IP	P101	INPUT
1	IP	IP	P107	INPUT
1	IP/VREF_1	IP/VREF_1	P95	VREF
1	VCCO_1	VCCO_1	P79	VCCO
1	VCCO_1	VCCO_1	P100	VCCO
2	IO/D5	IO/D5	P52	DUAL
2	IO/M1	IO/M1	P60	DUAL
2	IP/VREF_2	IO/VREF_2	P66	***100E:*** VREF(INPUT) ***250E:*** VREF(I/O)
2	IO_L01N_2/INIT_B	IO_L01N_2/INIT_B	P40	DUAL
2	IO_L01P_2/CSO_B	IO_L01P_2/CSO_B	P39	DUAL
2	IO_L02N_2/MOSI/CSI_B	IO_L02N_2/MOSI/CSI_B	P44	DUAL
2	IO_L02P_2/DOUT/BUSY	IO_L02P_2/DOUT/BUSY	P43	DUAL
2	IO_L04N_2/D6/GCLK13	IO_L04N_2/D6/GCLK13	P51	DUAL/GCLK
2	IO_L04P_2/D7/GCLK12	IO_L04P_2/D7/GCLK12	P50	DUAL/GCLK
2	IO_L05N_2/D3/GCLK15	IO_L05N_2/D3/GCLK15	P54	DUAL/GCLK
2	IO_L05P_2/D4/GCLK14	IO_L05P_2/D4/GCLK14	P53	DUAL/GCLK
2	IO_L07N_2/D1/GCLK3	IO_L07N_2/D1/GCLK3	P59	DUAL/GCLK
2	IO_L07P_2/D2/GCLK2	IO_L07P_2/D2/GCLK2	P58	DUAL/GCLK
2	IO_L08N_2/DIN/D0	IO_L08N_2/DIN/D0	P63	DUAL
2	IO_L08P_2/M0	IO_L08P_2/M0	P62	DUAL
2	IO_L09N_2/VS1/A18	IO_L09N_2/VS1/A18	P68	DUAL
2	IO_L09P_2/VS2/A19	IO_L09P_2/VS2/A19	P67	DUAL
2	IO_L10N_2/CCLK	IO_L10N_2/CCLK	P71	DUAL
2	IO_L10P_2/VS0/A17	IO_L10P_2/VS0/A17	P70	DUAL

Table 137: **TQ144 Package Pinout *(Cont'd)***

Bank	XC3S100E Pin Name	XC3S250E Pin Name	TQ144 Pin	Type
GND	GND	GND	P27	GND
GND	GND	GND	P37	GND
GND	GND	GND	P46	GND
GND	GND	GND	P55	GND
GND	GND	GND	P61	GND
GND	GND	GND	P73	GND
GND	GND	GND	P90	GND
GND	GND	GND	P99	GND
GND	GND	GND	P118	GND
GND	GND	GND	P127	GND
GND	GND	GND	P133	GND
VCCAUX	DONE	DONE	P72	CONFIG
VCCAUX	PROG_B	PROG_B	P1	CONFIG
VCCAUX	TCK	TCK	P110	JTAG
VCCAUX	TDI	TDI	P144	JTAG
VCCAUX	TDO	TDO	P109	JTAG
VCCAUX	TMS	TMS	P108	JTAG
VCCAUX	VCCAUX	VCCAUX	P30	VCCAUX
VCCAUX	VCCAUX	VCCAUX	P65	VCCAUX
VCCAUX	VCCAUX	VCCAUX	P102	VCCAUX
VCCAUX	VCCAUX	VCCAUX	P137	VCCAUX
VCCINT	VCCINT	VCCINT	P9	VCCINT
VCCINT	VCCINT	VCCINT	P45	VCCINT
VCCINT	VCCINT	VCCINT	P80	VCCINT
VCCINT	VCCINT	VCCINT	P115	VCCINT

Table 141: **PQ208 Package Pinout *(Cont'd)***

Bank	XC3S250E XC3S500E Pin Name	PQ208 Pin	Type
3	IO_L14P_3	P41	I/O
3	IO_L15N_3	P48	I/O
3	IO_L15P_3	P47	I/O
3	IO_L16N_3	P50	I/O
3	IO_L16P_3	P49	I/O
3	IP	P6	INPUT
3	IP	P14	INPUT
3	IP	P26	INPUT
3	IP	P32	INPUT
3	IP	P43	INPUT
3	IP	P51	INPUT
3	IP/VREF_3	P20	VREF
3	VCCO_3	P21	VCCO
3	VCCO_3	P38	VCCO
3	VCCO_3	P46	VCCO
GND	GND	P10	GND
GND	GND	P17	GND
GND	GND	P27	GND
GND	GND	P37	GND
GND	GND	P52	GND
GND	GND	P53	GND
GND	GND	P70	GND
GND	GND	P79	GND
GND	GND	P85	GND
GND	GND	P95	GND
GND	GND	P105	GND
GND	GND	P121	GND
GND	GND	P131	GND
GND	GND	P141	GND
GND	GND	P156	GND
GND	GND	P173	GND
GND	GND	P182	GND
GND	GND	P188	GND
GND	GND	P198	GND
GND	GND	P208	GND
VCCAUX	DONE	P104	CONFIG
VCCAUX	PROG_B	P1	CONFIG
VCCAUX	TCK	P158	JTAG
VCCAUX	TDI	P207	JTAG
VCCAUX	TDO	P157	JTAG
VCCAUX	TMS	P155	JTAG
VCCAUX	VCCAUX	P7	VCCAUX
VCCAUX	VCCAUX	P44	VCCAUX

Table 141: **PQ208 Package Pinout *(Cont'd)***

Bank	XC3S250E XC3S500E Pin Name	PQ208 Pin	Type
VCCAUX	VCCAUX	P66	VCCAUX
VCCAUX	VCCAUX	P92	VCCAUX
VCCAUX	VCCAUX	P111	VCCAUX
VCCAUX	VCCAUX	P149	VCCAUX
VCCAUX	VCCAUX	P166	VCCAUX
VCCAUX	VCCAUX	P195	VCCAUX
VCCINT	VCCINT	P13	VCCINT
VCCINT	VCCINT	P67	VCCINT
VCCINT	VCCINT	P117	VCCINT
VCCINT	VCCINT	P170	VCCINT

FG320 Footprint

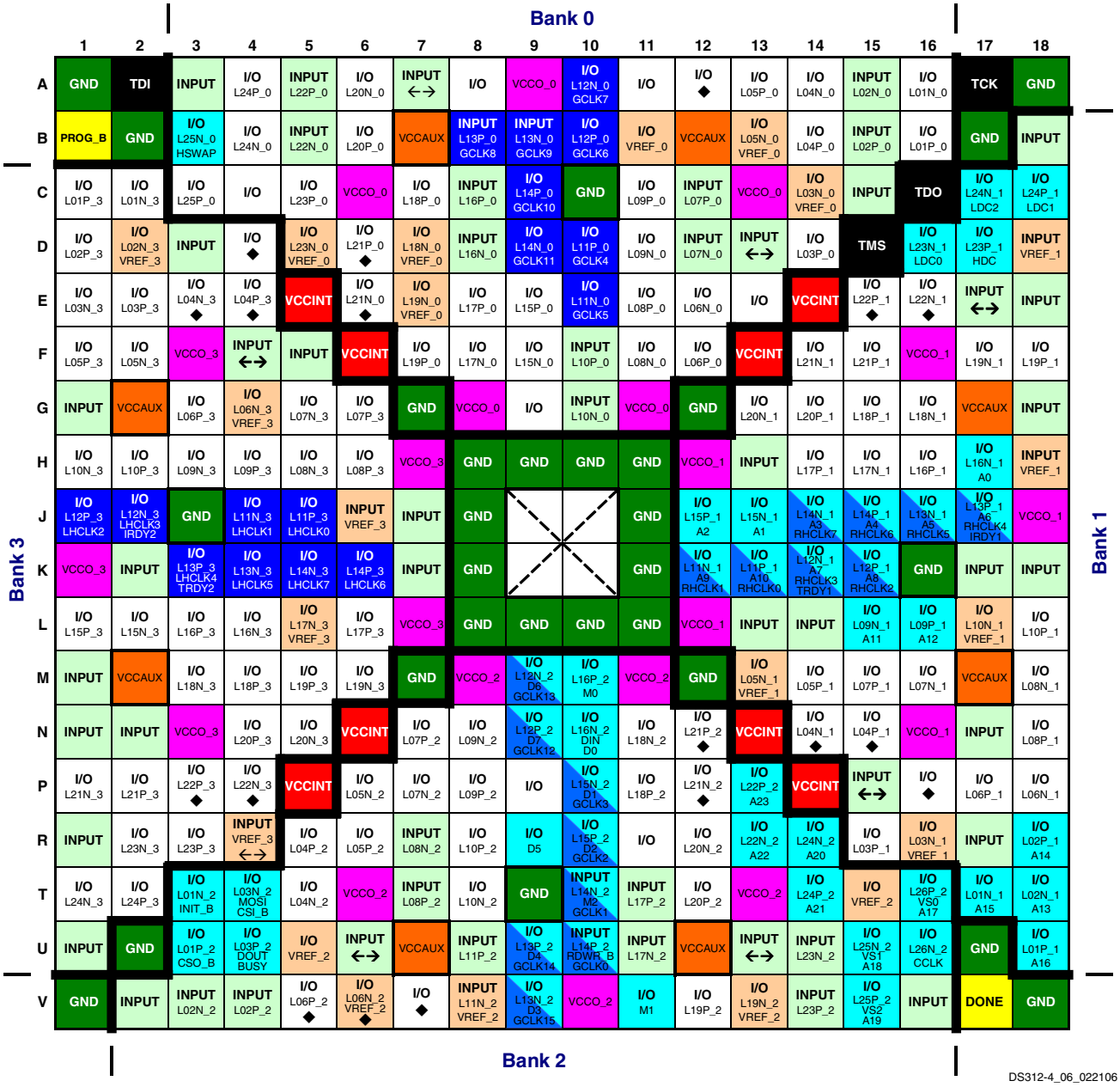


Figure 86: **FG320 Package Footprint (top view)**

102-120	**I/O:** Unrestricted, general-purpose user I/O	46	**DUAL:** Configuration pin, then possible user-I/O	20-21	**VREF:** User I/O or input voltage reference for bank
47-48	**INPUT:** Unrestricted, general-purpose input pin	16	**CLK:** User I/O, input, or global buffer input	20	**VCCO:** Output voltage supply for bank
2	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	8	**VCCINT:** Internal core supply voltage (+1.2V)
18	**N.C.:** Not connected. Only the XC3S500E has these pins (◆).	28	**GND:** Ground	8	**VCCAUX:** Auxiliary supply voltage (+2.5V)

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/01/05	1.0	Initial Xilinx release.
03/21/05	1.1	Added XC3S250E in the CP132 package to Table 129. Corrected number of differential I/O pairs on CP132. Added pinout and footprint information for the CP132, FG400, and FG484 packages. Removed IRDY and TRDY pins from the VQ100, TQ144, and PQ208 packages.
11/23/05	2.0	Corrected title of Table 153. Updated differential pair numbering for some pins in Bank 0 of the FG400 package, affecting Table 152 and Figure 87. Pin functionality and ball assignment were not affected. Added Package Thermal Characteristics section. Added package mass values to Table 125.
03/22/06	3.0	Included I/O pins, not just input-only pins under the VREF description in Table 124. Clarified that some global clock inputs are Input-only pins in Table 124. Added information on the XC3S100E in the CP132 package, affecting Table 129, Table 130, Table 133, Table 134, Table 136, and Figure 81. Ball A12 on the XC3S1600E in the FG320 package a full I/O pin, not an Input-only pin. Corrected the I/O counts for the XC3S1600E in the FG320 package, affecting Table 129, Table 150, Table 151, and Figure 86. Corrected pin type for XC3S1600E balls N14 and N15 in Table 148.
05/19/06	3.1	Minor text edits.
11/09/06	3.4	Added package thermal data for the XC3S100E in the CP132 package to Table 130. Corrected pin migration arrows for balls E17 and F4 between the XC3S500E and XC3S1600E in Table 151. Promoted Module 4 to Production status. Synchronized all modules to v3.4.
03/16/07	3.5	Minor formatting changes.
05/29/07	3.6	Corrected ‘Lxx’ to ‘Lxxy’ in Table 124. Noted that some GCLK and VREF pins are on INPUT pins in Table 124 and Table 129. Added link before Table 127 to Material Declaration Data Sheets.
04/18/08	3.7	Added XC3S500E VQG100 package. Added Material Declaration Data Sheet links in Table 127. Updated Thermal Characteristics in Table 130. Updated links.
08/26/09	3.8	Minor typographical updates.
10/29/12	4.0	Added Notice of Disclaimer. This product is not recommended for new designs. Updated the XC3S250E-FT256 in Table 129.

Notice of Disclaimer