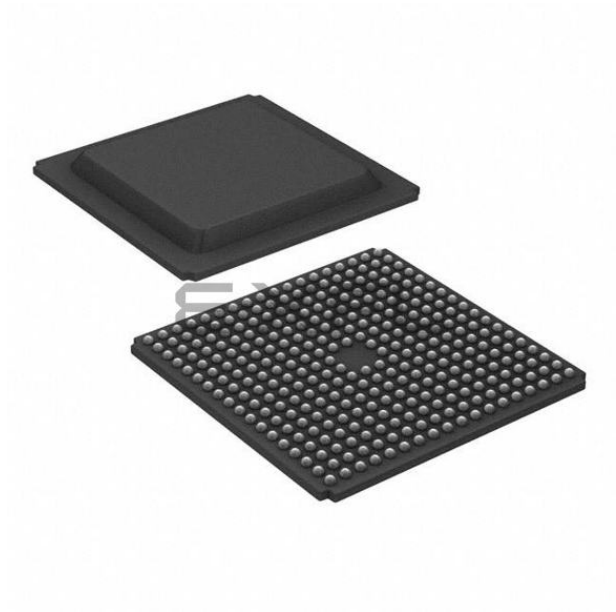
AMD Xilinx - XC3S1200E-4FG320I Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	2168
Number of Logic Elements/Cells	19512
Total RAM Bits	516096
Number of I/O	250
Number of Gates	1200000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	320-BGA
Supplier Device Package	320-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s1200e-4fg320i

Double-Data-Rate Transmission

Double-Data-Rate (DDR) transmission describes the technique of synchronizing signals to both the rising and falling edges of the clock signal. Spartan-3E devices use register pairs in all three IOB paths to perform DDR operations.

The pair of storage elements on the IOB's Output path (OFF1 and OFF2), used as registers, combine with a special multiplexer to form a DDR D-type flip-flop (ODDR2). This primitive permits DDR transmission where output data bits are synchronized to both the rising and falling edges of a clock. DDR operation requires two clock signals (usually 50% duty cycle), one the inverted form of the other. These signals trigger the two registers in alternating fashion, as shown in Figure 7. The Digital Clock Manager (DCM) generates the two clock signals by mirroring an incoming signal, and then shifting it 180 degrees. This approach ensures minimal skew between the two signals. Alternatively, the inverter inside the IOB can be used to invert the clock signal, thus only using one clock line and both rising and falling edges of that clock line as the two clocks for the DDR flip-flops.

The storage-element pair on the Three-State path (TFF1 and TFF2) also can be combined with a local multiplexer to form a DDR primitive. This permits synchronizing the output enable to both the rising and falling edges of a clock. This DDR operation is realized in the same way as for the output path.

The storage-element pair on the input path (IFF1 and IFF2) allows an I/O to receive a DDR signal. An incoming DDR clock signal triggers one register, and the inverted clock signal triggers the other register. The registers take turns capturing bits of the incoming DDR data signal. The primitive to allow this functionality is called IDDR2.

Aside from high bandwidth data transfers, DDR outputs also can be used to reproduce, or *mirror*, a clock signal on the output. This approach is used to transmit clock and data signals together (source synchronously). A similar approach is used to reproduce a clock signal at multiple outputs. The advantage for both approaches is that skew across the outputs is minimal.

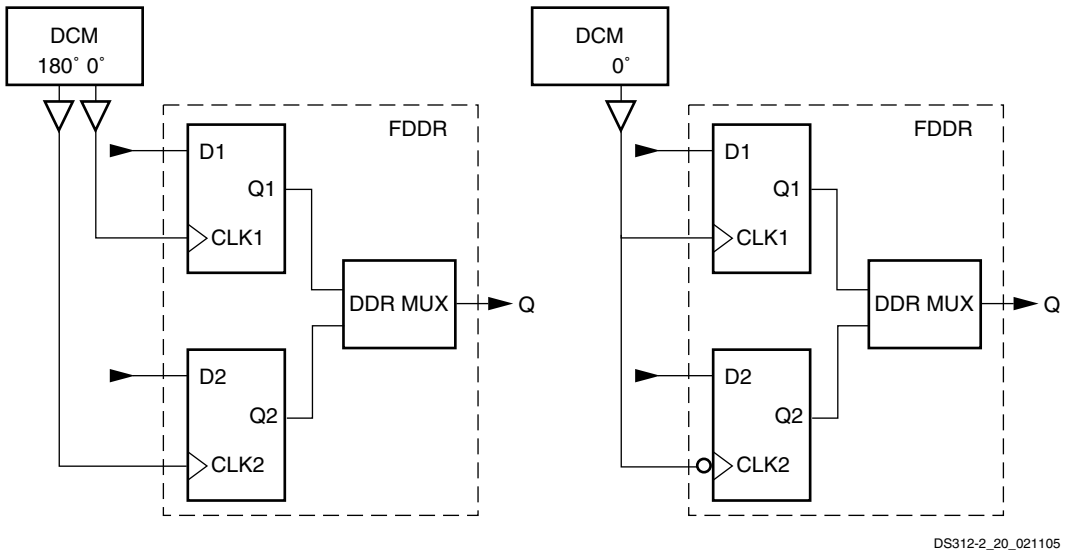

Figure 7: **Two Methods for Clocking the DDR Register**

Register Cascade Feature

In the Spartan-3E family, one of the IOBs in a differential pair can cascade its input storage elements with those in the other IOB as part of a differential pair. This is intended to make DDR operation at high speed much simpler to implement. The new DDR connections that are available are shown in Figure 5 (dashed lines), and are only available for routing between IOBs and are not accessible to the FPGA fabric. Note that this feature is only available when using the differential I/O standards LVDS, RSDS, and MINI_LVDS.

IDDR2

As a DDR input pair, the master IOB registers incoming data on the rising edge of ICLK1 (= D1) and the rising edge of ICLK2 (= D2), which is typically the same as the falling edge of ICLK1. This data is then transferred into the FPGA fabric. At some point, both signals must be brought into the same clock domain, typically ICLK1. This can be difficult at high frequencies because the available time is only one half of a clock cycle assuming a 50% duty cycle. See Figure 8 for a graphical illustration of this function.

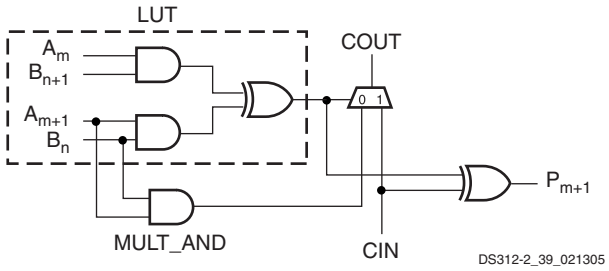

Figure 24: **Using the MULT_AND for Multiplication in Carry Logic**

The MULT_AND is useful for small multipliers. Larger multipliers can be built using the dedicated 18x18 multiplier blocks (see Dedicated Multipliers).

Storage Elements

The storage element, which is programmable as either a D-type flip-flop or a level-sensitive transparent latch, provides a means for synchronizing data to a clock signal, among other uses. The storage elements in the top and bottom portions of the slice are called FFY and FFX, respectively. FFY has a fixed multiplexer on the D input selecting either the combinatorial output Y or the bypass signal BY. FFX selects between the combinatorial output X or the bypass signal BX.

The functionality of a slice storage element is identical to that described earlier for the I/O storage elements. All signals have programmable polarity; the default active-High function is described.

Table 15: **Storage Element Signals**

Signal	Description
D	Input. For a flip-flop data on the D input is loaded when R and S (or CLR and PRE) are Low and CE is High during the Low-to-High clock transition. For a latch, Q reflects the D input while the gate (G) input and gate enable (GE) are High and R and S (or CLR and PRE) are Low. The data on the D input during the High-to-Low gate transition is stored in the latch. The data on the Q output of the latch remains unchanged as long as G or GE remains Low.
Q	Output. Toggles after the Low-to-High clock transition for a flip-flop and immediately for a latch.
C	Clock for edge-triggered flip-flops.
G	Gate for level-sensitive latches.
CE	Clock Enable for flip-flops.
GE	Gate Enable for latches.
S	Synchronous Set (Q = High). When the S input is High and R is Low, the flip-flop is set, output High, during the Low-to-High clock (C) transition. A latch output is immediately set, output High.
R	Synchronous Reset (Q = Low); has precedence over Set.
PRE	Asynchronous Preset (Q = High). When the PRE input is High and CLR is Low, the flip-flop is set, output High, during the Low-to-High clock (C) transition. A latch output is immediately set, output High.
CLR	Asynchronous Clear (Q = Low); has precedence over Preset to reset Q output Low
SR	CLB input for R, S, CLR, or PRE
REV	CLB input for opposite of SR. Must be asynchronous or synchronous to match SR.

The control inputs R, S, CE, and C are all shared between the two flip-flops in a slice.

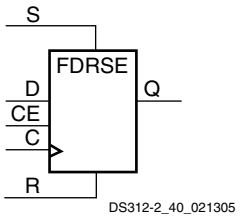

Figure 25: **FD Flip-Flop Component with Synchronous Reset, Set, and Clock Enable**

Table 16: **FD Flip-Flop Functionality with Synchronous Reset, Set, and Clock Enable**

Inputs					Outputs
R	S	CE	D	C	Q
1	X	X	X	↑	0
0	1	X	X	↑	1
0	0	0	X	X	No Change
0	0	1	1	↑	1
0	0	1	0	↑	0

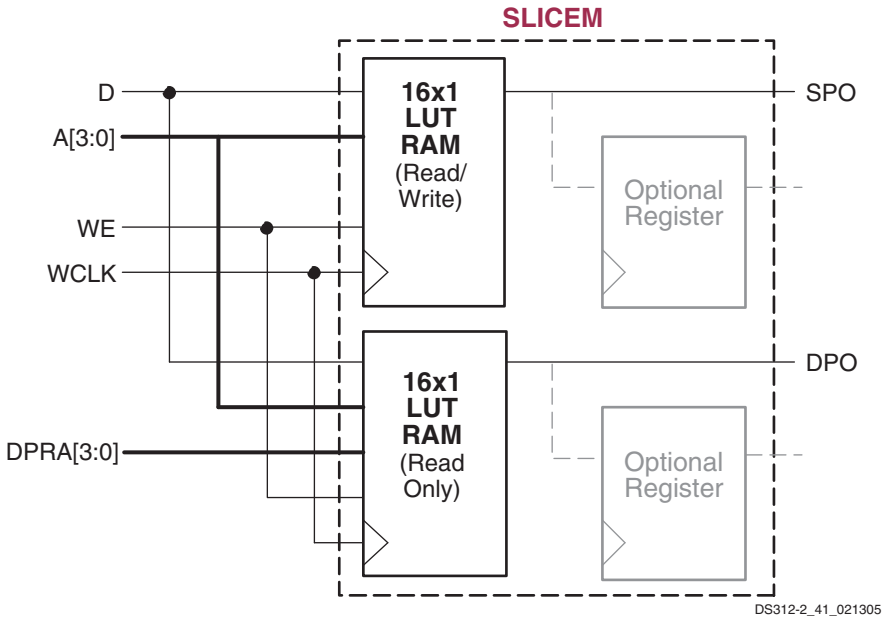

Figure 26: **RAM16X1D Dual-Port Usage**

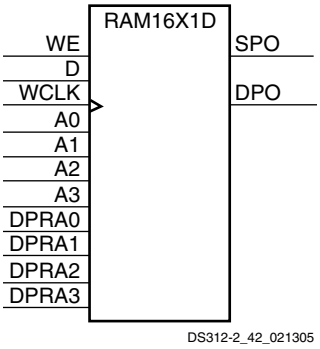

Figure 27: **Dual-Port RAM Component**

Table 18: **Dual-Port RAM Function**

Inputs			Outputs	
WE (mode)	**WCLK**	**D**	**SPO**	**DPO**
0 (read)	X	X	data_a	data_d
1 (read)	0	X	data_a	data_d
1 (read)	1	X	data_a	data_d
1 (write)	↑	D	D	data_d
1 (read)	↓	X	data_a	data_d

Notes:

1. data_a = word addressed by bits A3-A0.
2. data_d = word addressed by bits DPRA3-DPRA0.

Table 19: **Distributed RAM Signals**

Signal	Description
WCLK	The clock is used for synchronous writes. The data and the address input pins have setup times referenced to the WCLK pin. Active on the positive edge by default with built-in programmable polarity.
WE	The enable pin affects the write functionality of the port. An inactive Write Enable prevents any writing to memory cells. An active Write Enable causes the clock edge to write the data input signal to the memory location pointed to by the address inputs. Active High by default with built-in programmable polarity.
A0, A1, A2, A3 (A4, A5)	The address inputs select the memory cells for read or write. The width of the port determines the required address inputs.
D	The data input provides the new data value to be written into the RAM.
O, SPO, and DPO	The data output O on single-port RAM or the SPO and DPO outputs on dual-port RAM reflects the contents of the memory cells referenced by the address inputs. Following an active write clock edge, the data out (O or SPO) reflects the newly written data.

The INIT attribute can be used to preload the memory with data during FPGA configuration. The default initial contents for RAM is all zeros. If the WE is held Low, the element can be considered a ROM. The ROM function is possible even in the SLICEL.

The global write enable signal, GWE, is asserted automatically at the end of device configuration to enable all writable elements. The GWE signal guarantees that the

Multiplier/Block RAM Interaction

Each multiplier is located adjacent to an 18 Kbit block RAM and shares some interconnect resources. Configuring an 18 Kbit block RAM for 36-bit wide data (512 x 36 mode) prevents use of the associated dedicated multiplier.

The upper 16 bits of the 'A' multiplicand input are shared with the upper 16 bits of the block RAM's Port A Data input. Similarly, the upper 16 bits of the 'B' multiplicand input are shared with Port B's data input. See also Figure 48, page 62.

Table 27 defines each port of the MULT18X18SIO primitive.

Table 27: **MULT18X18SIO Embedded Multiplier Primitives Description**

Signal Name	Direction	Function
A[17:0]	Input	The primary 18-bit two's complement value for multiplication. The block multiplies by this value asynchronously if the optional AREG and PREG registers are omitted. When AREG and/or PREG are used, the value provided on this port is qualified by the rising edge of CLK, subject to the appropriate register controls.
B[17:0]	Input	The second 18-bit two's complement value for multiplication if the B_INPUT attribute is set to DIRECT. The block multiplies by this value asynchronously if the optional BREG and PREG registers are omitted. When BREG and/or PREG are used, the value provided on this port is qualified by the rising edge of CLK, subject to the appropriate register controls.
BCIN[17:0]	Input	The second 18-bit two's complement value for multiplication if the B_INPUT attribute is set to CASCADE. The block multiplies by this value asynchronously if the optional BREG and PREG registers are omitted. When BREG and/or PREG are used, the value provided on this port is qualified by the rising edge of CLK, subject to the appropriate register controls.
P[35:0]	Output	The 36-bit two's complement product resulting from the multiplication of the two input values applied to the multiplier. If the optional AREG, BREG and PREG registers are omitted, the output operates asynchronously. Use of PREG causes this output to respond to the rising edge of CLK with the value qualified by CEP and RSTP. If PREG is omitted, but AREG and BREG are used, this output responds to the rising edge of CLK with the value qualified by CEA, RSTA, CEB, and RSTB. If PREG is omitted and only one of AREG or BREG is used, this output responds to both asynchronous and synchronous events.
BCOUT[17:0]	Output	The value being applied to the second input of the multiplier. When the optional BREG register is omitted, this output responds asynchronously in response to changes at the B[17:0] or BCIN[17:0] ports according to the setting of the B_INPUT attribute. If BREG is used, this output responds to the rising edge of CLK with the value qualified by CEB and RSTB.
CEA	Input	Clock enable qualifier for the optional AREG register. The value provided on the A[17:0] port is captured by AREG in response to a rising edge of CLK when this signal is High, provided that RSTA is Low.
RSTA	Input	Synchronous reset for the optional AREG register. AREG content is forced to the value zero in response to a rising edge of CLK when this signal is High.
CEB	Input	Clock enable qualifier for the optional BREG register. The value provided on the B[17:0] or BCIN[17:0] port is captured by BREG in response to a rising edge of CLK when this signal is High, provided that RSTB is Low.
RSTB	Input	Synchronous reset for the optional BREG register. BREG content is forced to the value zero in response to a rising edge of CLK when this signal is High.
CEP	Input	Clock enable qualifier for the optional PREG register. The value provided on the output of the multiplier port is captured by PREG in response to a rising edge of CLK when this signal is High, provided that RSTP is Low.
RSTP	Input	Synchronous reset for the optional PREG register. PREG content is forced to the value zero in response to a rising edge of CLK when this signal is High.

Notes:

1. The control signals CLK, CEA, RSTA, CEB, RSTB, CEP, and RSTP have the option of inverted polarity.

VARIABLE Phase Shift Mode

In VARIABLE phase shift mode, the FPGA application dynamically adjusts the fine phase shift value using three inputs to the PS unit (PSEN, PSCLK, and PSINCDEC), as defined in Table 36 and shown in Figure 40.

Table 36: **Signals for Variable Phase Mode**

Signal	Direction	Description
PSEN(1)	Input	Enables the Phase Shift unit for variable phase adjustment.
PSCLK(1)	Input	Clock to synchronize phase shift adjustment.
PSINCDEC(1)	Input	When High, increments the current phase shift value. When Low, decrements the current phase shift value. This signal is synchronized to the PSCLK signal.
PSDONE	Output	Goes High to indicate that the present phase adjustment is complete and PS unit is ready for next phase adjustment request. This signal is synchronized to the PSCLK signal.

Notes:

1. This input supports either a true or inverted polarity.

The FPGA application uses the three PS inputs on the Phase Shift unit to dynamically and incrementally increase or decrease the phase shift amount on all nine DCM clock outputs.

To adjust the current phase shift value, the PSEN enable signal must be High to enable the PS unit. Coincidently, PSINCDEC must be High to increment the current phase shift amount or Low to decrement the current amount. All VARIABLE phase shift operations are controlled by the PSCLK input, which can be the CLKIN signal or any other clock signal.

Design Note

The VARIABLE phase shift feature operates differently from the Spartan-3 DCM; use the DCM_SP primitive, not the DCM primitive.

DCM_DELAY_STEP

DCM_DELAY_STEP is the finest delay resolution available in the PS unit. Its value is provided at the bottom of Table 105 in Module 3. For each enabled PSCLK cycle that PSINCDEC is High, the PS unit adds one DCM_ DELAY_STEP of phase shift to all nine DCM outputs. Similarly, for each enabled PSCLK cycle that PSINCDEC is Low, the PS unit subtracts one DCM_ DELAY_STEP of phase shift from all nine DCM outputs.

Because each DCM_DELAY_STEP has a minimum and maximum value, the actual phase shift delay for the present phase increment/decrement value (VALUE) falls within the minimum and maximum values according to Equation 4 and Equation 5.

$$T_{PS}(Max) = VALUE \bullet \text{DCM\_DELAY\_STEP\_MAX} \quad Eq\ 4$$

$$T_{PS}(Min) = VALUE \bullet \text{DCM\_DELAY\_STEP\_MIN} \quad Eq\ 5$$

The maximum variable phase shift steps, MAX_STEPS, is described in Equation 6 or Equation 7, for a given CLKIN input period, T_{CLKIN}, in nanoseconds. To convert this to a phase shift range measured in time and not steps, use MAX_STEPS derived in Equation 6 and Equation 7 for VALUE in Equation 4 and Equation 5.

If CLKIN < 60 MHz:

$$\text{MAX\_STEPS} = \pm[INTEGER(10 \bullet (T_{CLKIN} - 3))] \quad Eq\ 6$$

If CLKIN ≥ 60 MHz:

$$\text{MAX\_STEPS} = \pm[INTEGER(15 \bullet (T_{CLKIN} - 3))] \quad Eq\ 7$$

The phase adjustment might require as many as 100 CLKIN cycles plus 3 PSCLK cycles to take effect, at which point the DCM's PSDONE output goes High for one PSCLK cycle. This pulse indicates that the PS unit completed the previous adjustment and is now ready for the next request.

Asserting the Reset (RST) input returns the phase shift to zero.

By contrast, the clock switch matrixes on the top and bottom edges receive signals from any of the five following sources: two GCLK pins, two DCM outputs, or one Double-Line interconnect.

Table 41 indicates permissible connections between clock inputs and BUFGMUX elements. The I0-input provides the best input path to a clock buffer. The I1-input provides the secondary input for the clock multiplexer function.

The four BUFGMUX elements on the top edge are paired together and share inputs from the eight global clock inputs along the top edge. Each BUFGMUX pair connects to four of the eight global clock inputs, as shown in Figure 45. This optionally allows differential inputs to the global clock inputs without wasting a BUFGMUX element.

Table 41: **Connections from Clock Inputs to BUFGMUX Elements and Associated Quadrant Clock**

Quadrant Clock Line[1]	Left-Half BUFGMUX			Top or Bottom BUFGMUX			Right-Half BUFGMUX		
	Location[2]	I0 Input	I1 Input	Location[2]	I0 Input	I1 Input	Location[2]	I0 Input	I1 Input
H	*X0Y9*	LHCLK7	LHCLK6	*X1Y10*	GCLK7 or GCLK11	GCLK6 or GCLK10	*X3Y9*	RHCLK3	RHCLK2
G	*X0Y8*	LHCLK6	LHCLK7	*X1Y11*	GCLK6 or GCLK10	GCLK7 or GCLK11	*X3Y8*	RHCLK2	RHCLK3
F	*X0Y7*	LHCLK5	LHCLK4	*X2Y10*	GCLK5 or GCLK9	GCLK4 or GCLK8	*X3Y7*	RHCLK1	RHCLK0
E	*X0Y6*	LHCLK4	LHCLK5	*X2Y11*	GCLK4 or GCLK8	GCLK5 or GCLK9	*X3Y6*	RHCLK0	RHCLK1
D	*X0Y5*	LHCLK3	LHCLK2	*X1Y0*	GCLK3 or GCLK15	GCLK2 or GCLK14	*X3Y5*	RHCLK7	RHCLK6
C	*X0Y4*	LHCLK2	LHCLK3	*X1Y1*	GCLK2 or GCLK14	GCLK3 or GCLK15	*X3Y4*	RHCLK6	RHCLK7
B	*X0Y3*	LHCLK1	LHCLK0	*X2Y0*	GCLK1 or GCLK13	GCLK0 or GCLK12	*X3Y3*	RHCLK5	RHCLK4
A	*X0Y2*	LHCLK0	LHCLK1	*X2Y1*	GCLK0 or GCLK12	GCLK1 or GCLK13	*X3Y2*	RHCLK4	RHCLK5

Notes:

1. See Quadrant Clock Routing for connectivity details for the eight quadrant clocks.
2. See Figure 45 for specific BUFGMUX locations, and Figure 47 for information on how BUFGMUX elements drive onto a specific clock line within a quadrant.

Master Serial Mode

For additional information, refer to the “Master Serial Mode” chapter in UG332.

In Master Serial mode (M[2:0] = <0:0:0>), the Spartan-3E FPGA configures itself from an attached Xilinx Platform Flash PROM, as illustrated in Figure 51. The FPGA supplies the CCLK output clock from its internal oscillator to the attached Platform Flash PROM. In response, the Platform Flash PROM supplies bit-serial data to the FPGA’s DIN input, and the FPGA accepts this data on each rising CCLK edge.

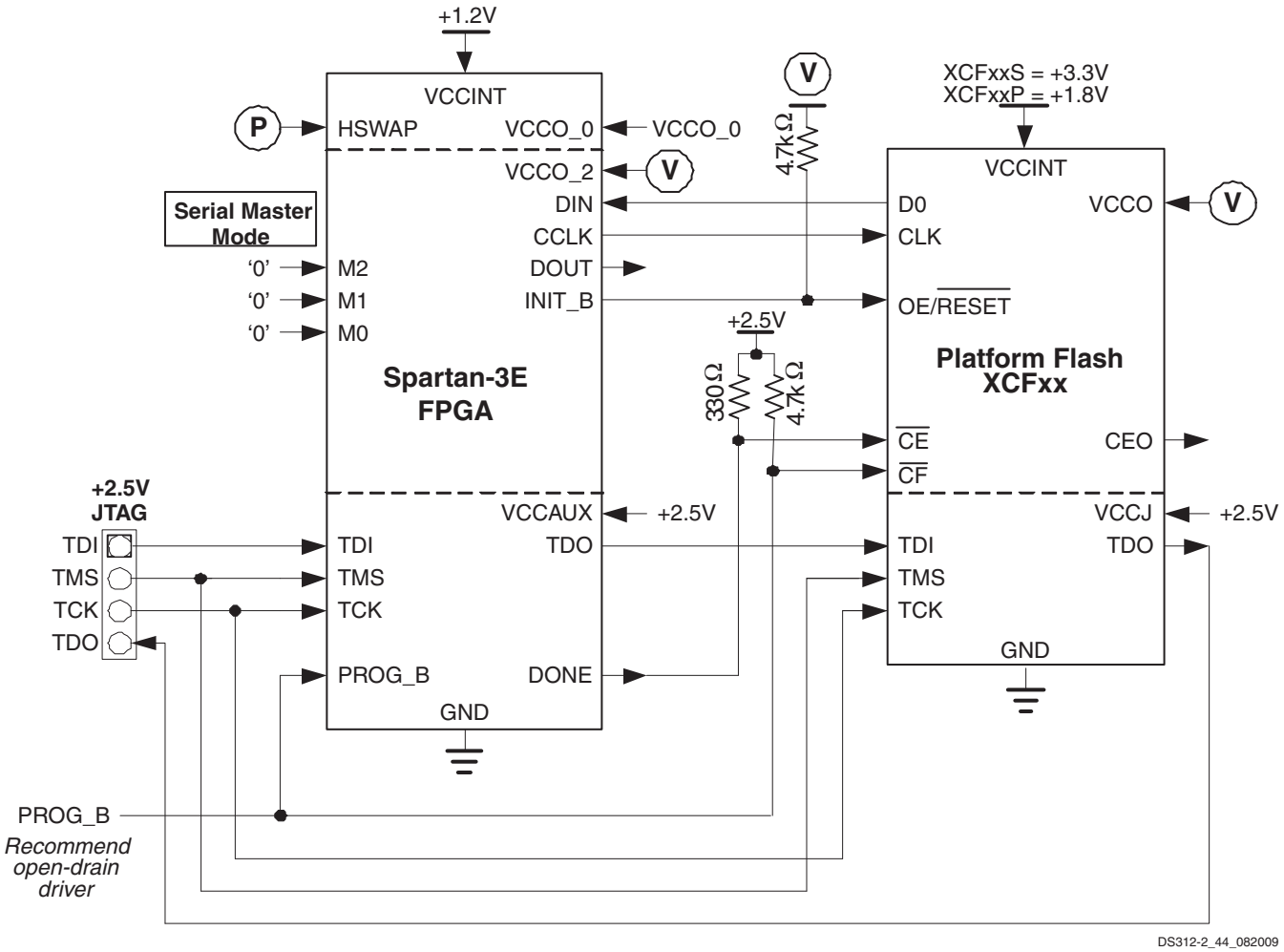

Figure 51: **Master Serial Mode using Platform Flash PROM**

All mode select pins, M[2:0], must be Low when sampled, when the FPGA’s INIT_B output goes High. After configuration, when the FPGA’s DONE output goes High, the mode select pins are available as full-featured user-I/O pins.

Stepping 0 Limitations when Reprogramming via JTAG if FPGA Set for BPI Configuration

The FPGA can always be reprogrammed via the JTAG port, regardless of the mode pin (M[2:0]) settings. However, Stepping 0 devices have a minor limitation. If a Stepping 0 FPGA is set to configure in BPI mode and the FPGA is attached to a parallel memory containing a valid FPGA configuration file, then subsequent reconfigurations using the JTAG port will fail. Potential workarounds include setting the mode pins for JTAG configuration (M[2:0] = <1:0:1>) or offsetting the initial memory location in Flash by 0x2000.

Stepping 1 devices fully support JTAG configuration even when the FPGA mode pins are set for BPI mode.

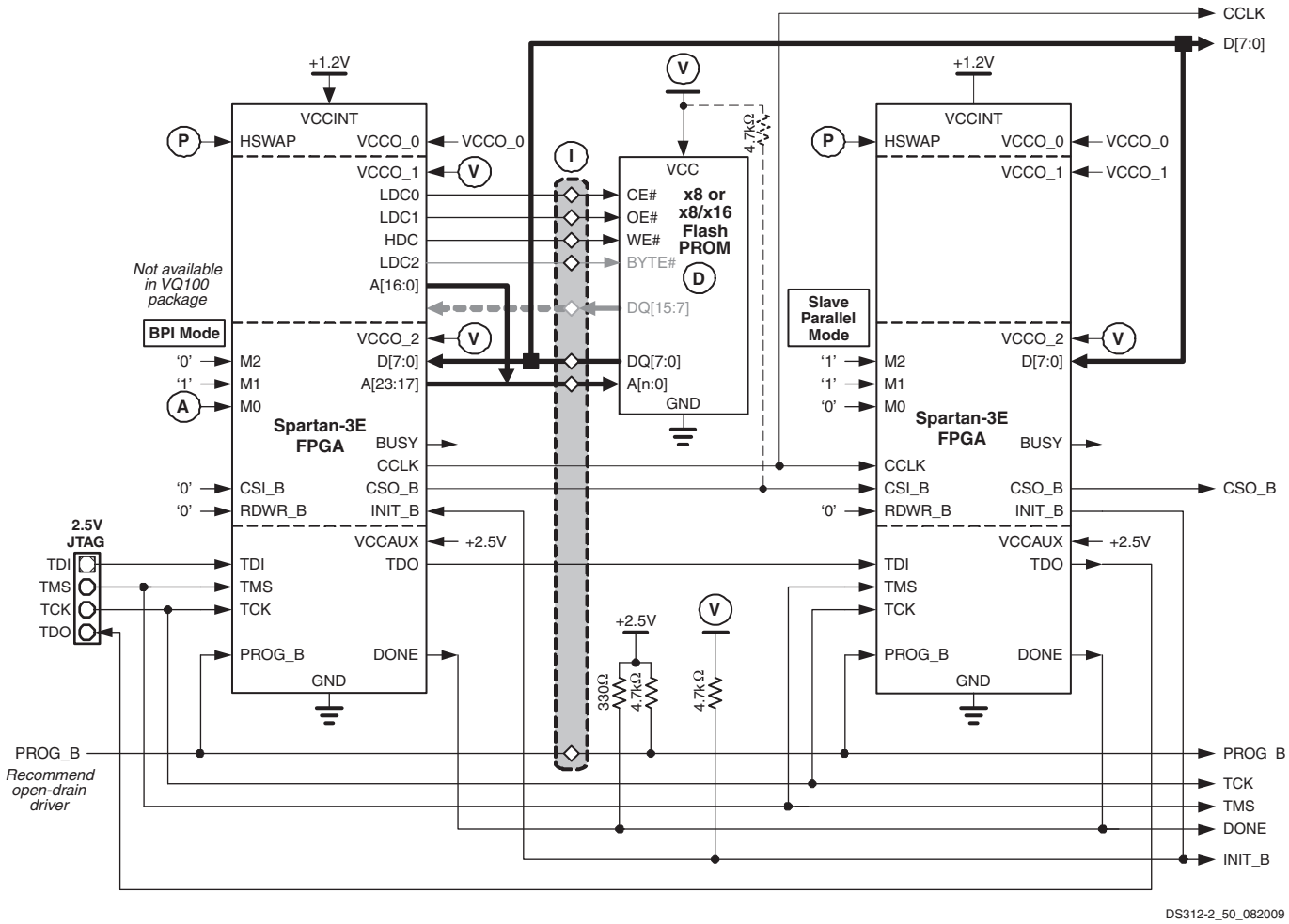

Figure 59: **Daisy-Chaining from BPI Flash Mode**

In-System Programming Support

(I) In a production application, the parallel Flash PROM is usually preprogrammed before it is mounted on the printed circuit board. In-system programming support is available from third-party boundary-scan tool vendors and from some third-party PROM programmers using a socket adapter with attached wires. To gain access to the parallel Flash signals, drive the FPGA's PROG_B input Low with an open-drain driver. This action places all FPGA I/O pins, including those attached to the parallel Flash, in high-impedance (Hi-Z). If the HSWAP input is Low, the I/Os have pull-up resistors to the V_{CCO} input on their respective I/O bank. The external programming hardware then has direct access to the parallel Flash pins. The programming access points are highlighted in the gray boxes in Figure 58 and Figure 59.

The FPGA itself can also be used as a parallel Flash PROM programmer during development and test phases. Initially, an FPGA-based programmer is downloaded into the FPGA via JTAG. Then the FPGA performs the Flash PROM programming algorithms and receives programming data from the host via the FPGA's JTAG interface. See the Embedded System Tools Reference Manual.

Dynamically Loading Multiple Configuration Images Using MultiBoot Option

For additional information, refer to the "Reconfiguration and MultiBoot" chapter in UG332.

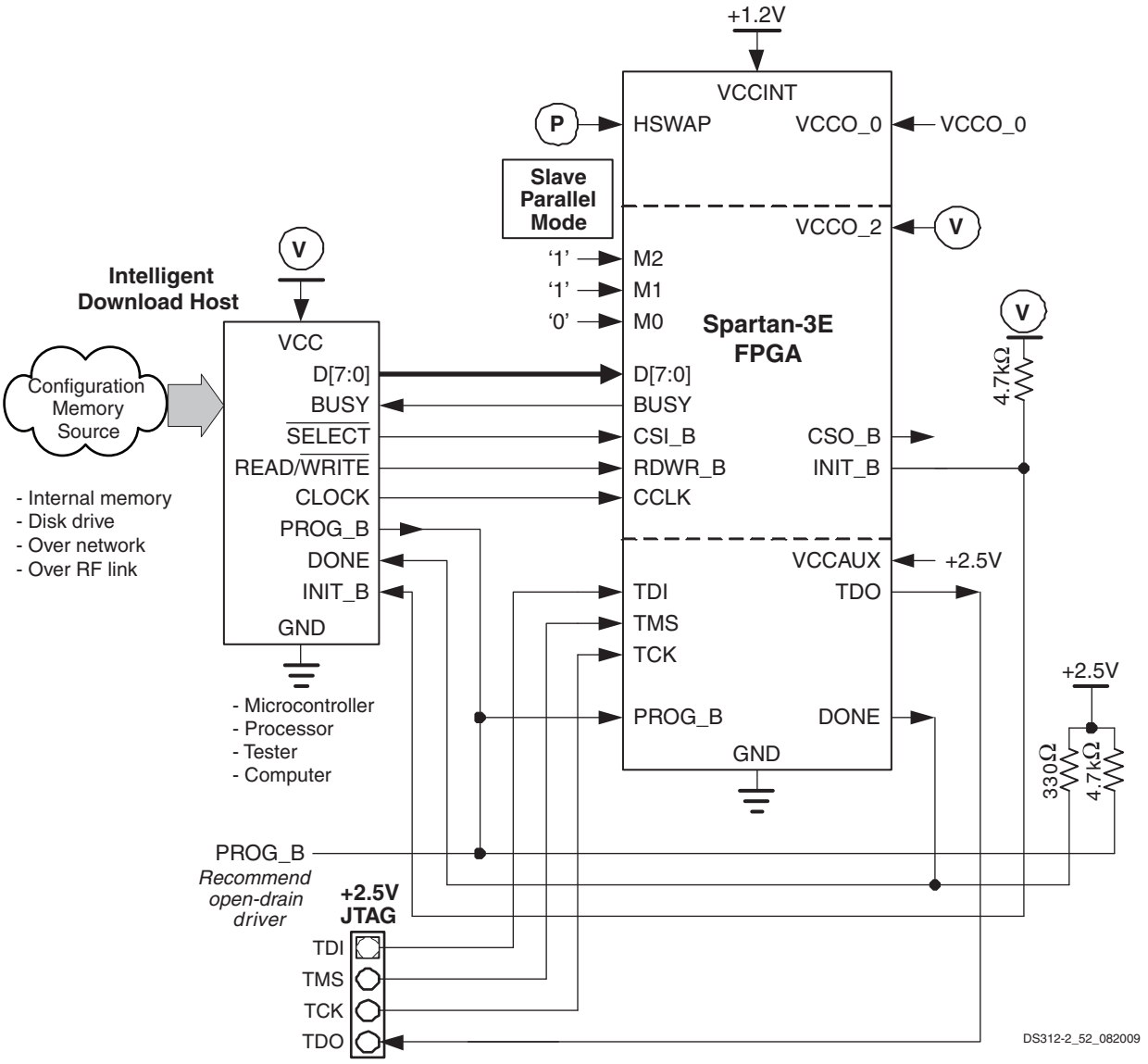

Figure 61: **Slave Parallel Configuration Mode**

Slave Parallel Mode

For additional information, refer to the "Slave Parallel (SelectMAP) Mode" chapter in UG332.

In Slave Parallel mode (M[2:0] = <1:1:0>), an external host, such as a microprocessor or microcontroller, writes byte-wide configuration data into the FPGA, using a typical peripheral interface as shown in Figure 61.

The external download host starts the configuration process by pulsing PROG_B and monitoring that the INIT_B pin goes High, indicating that the FPGA is ready to receive its first data. The host asserts the active-Low chip-select signal (CSI_B) and the active-Low Write signal (RDWR_B). The host then continues supplying data and clock signals until either the FPGA's DONE pin goes High, indicating a successful configuration, or until the FPGA's INIT_B pin goes Low, indicating a configuration error.

The FPGA captures data on the rising CCLK edge. If the CCLK frequency exceeds 50 MHz, then the host must also monitor the FPGA's BUSY output. If the FPGA asserts BUSY High, the host must hold the data for an additional clock cycle, until BUSY returns Low. If the CCLK frequency is 50 MHz or below, the BUSY pin may be ignored but actively drives during configuration.

The configuration process requires more clock cycles than indicated from the configuration file size. Additional clocks are required during the FPGA's start-up sequence, especially if the FPGA is programmed to wait for selected Digital Clock Managers (DCMs) to lock to their respective clock inputs (see Start-Up, page 105).

If the Slave Parallel interface is only used to configure the FPGA, never to read data back, then the RDWR_B signal

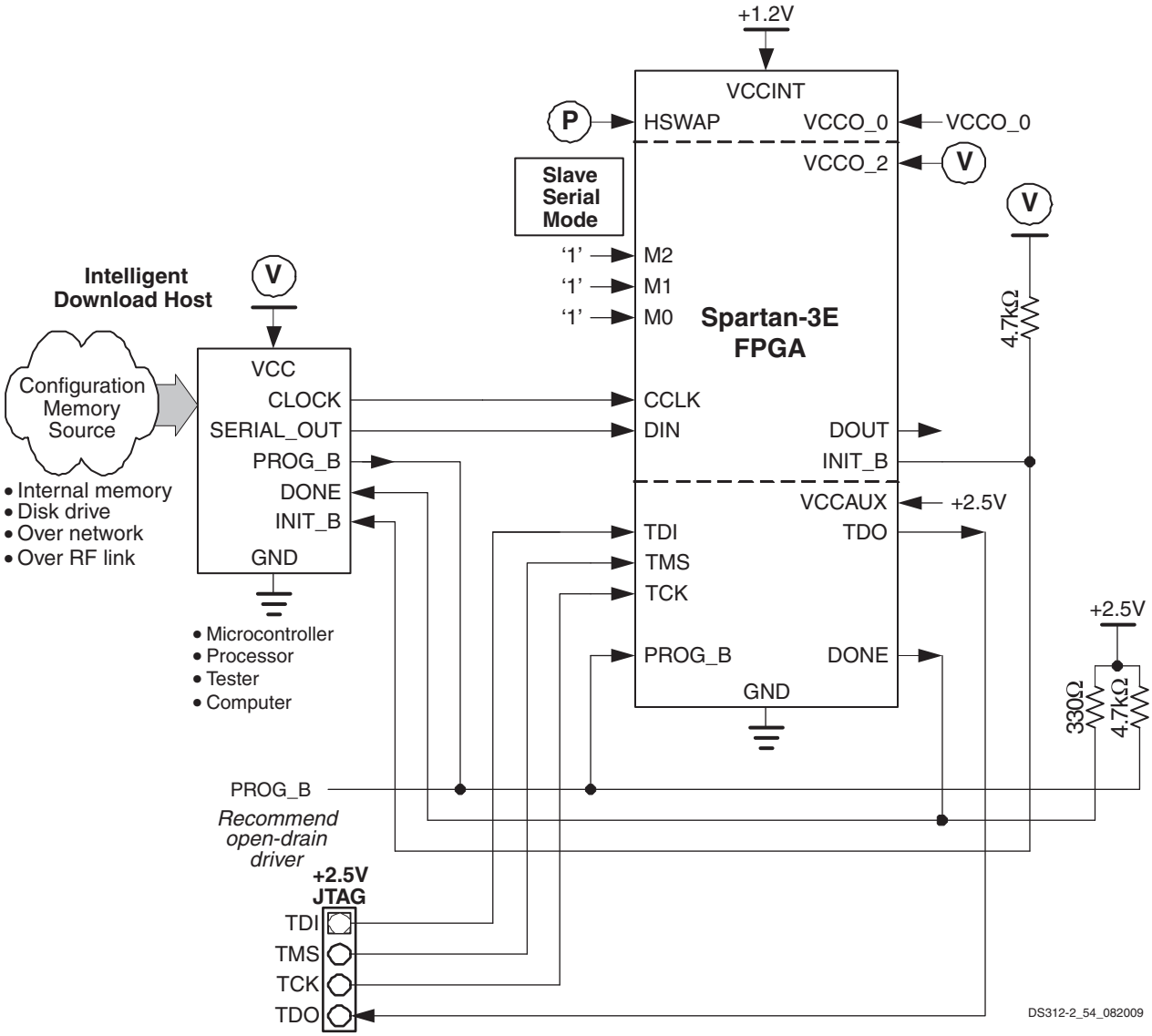

Figure 63: **Slave Serial Configuration**

The mode select pins, M[2:0], are sampled when the FPGA's INIT_B output goes High and must be at defined logic levels during this time. After configuration, when the FPGA's DONE output goes High, the mode pins are available as full-featured user-I/O pins.

(P) Similarly, the FPGA's HSWAP pin must be Low to enable pull-up resistors on all user-I/O pins or High to disable the pull-up resistors. The HSWAP control must remain at a constant logic level throughout FPGA configuration. After configuration, when the FPGA's DONE output goes High, the HSWAP pin is available as full-featured user-I/O pin and is powered by the VCCO_0 supply.

Voltage Compatibility

(V) Most Slave Serial interface signals are within the FPGA's I/O Bank 2, supplied by the VCCO_2 supply input. The VCCO_2 voltage can be 3.3V, 2.5V, or 1.8V to match the requirements of the external host, ideally 2.5V. Using 3.3V or 1.8V requires additional design considerations as the DONE and PROG_B pins are powered by the FPGA's 2.5V V_{CCAUX} supply. See XAPP453: *The 3.3V Configuration of Spartan-3 FPGAs* for additional information.

Daisy-Chaining

If the application requires multiple FPGAs with different configurations, then configure the FPGAs using a daisy chain, as shown in Figure 64. Use Slave Serial mode (M[2:0] = <1:1:1>) for all FPGAs in the daisy-chain. After the lead FPGA is filled with its configuration data, the lead

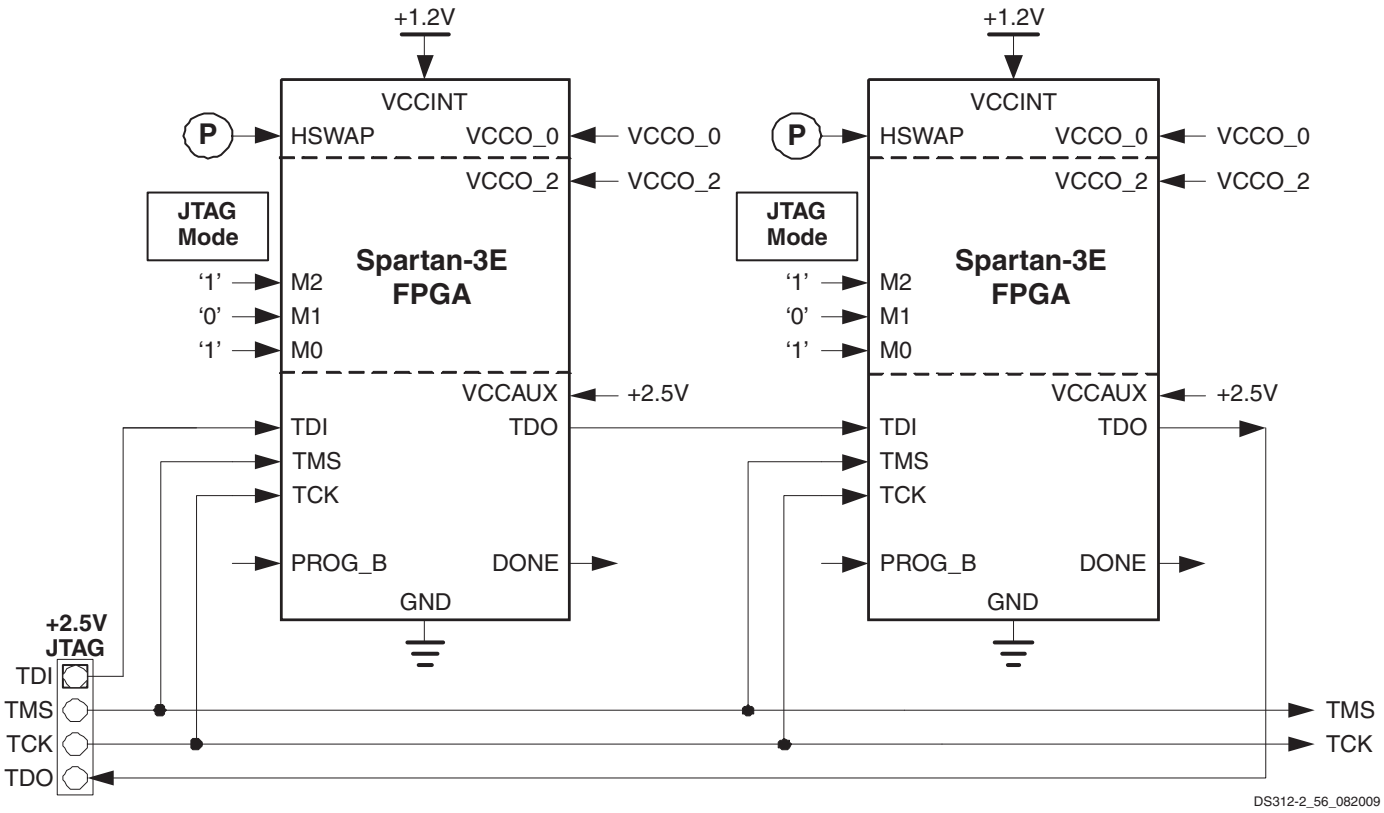

Figure 65: **JTAG Configuration Mode**

Voltage Compatibility

The 2.5V V_{CCAUX} supply powers the JTAG interface. All of the user I/Os are separately powered by their respective VCCO_# supplies.

When connecting the Spartan-3E JTAG port to a 3.3V interface, the JTAG input pins must be current-limited to 10 mA or less using series resistors. Similarly, the TDO pin is a CMOS output powered from +2.5V. The TDO output can directly drive a 3.3V input but with reduced noise immunity. See XAPP453: *The 3.3V Configuration of Spartan-3 FPGAs* for additional information.

Table 67: **Spartan-3E JTAG Device Identifiers**

Spartan-3E FPGA	4-Bit Revision Code		28-Bit Vendor/Device Identifier
	Step 0	Step 1	
XC3S100E	0x0	0x1	0x1C 10 093
XC3S250E	0x0	0x1	0x1C 1A 093
XC3S500E	0x0 0x2	0x4	0x1C 22 093
XC3S1200E	0x0 0x1	0x2	0x1C 2E 093
XC3S1600E	0x0 0x1	0x2	0x1C 3A 093

JTAG Device ID

Each Spartan-3E FPGA array type has a 32-bit device-specific JTAG device identifier as shown in Table 67. The lower 28 bits represent the device vendor (Xilinx) and device identifer. The upper four bits, ignored by most tools, represent the revision level of the silicon mounted on the printed circuit board. Table 67 associates the revision code with a specific stepping level.

JTAG User ID

The Spartan-3E JTAG interface also provides the option to store a 32-bit User ID, loaded during configuration. The User ID value is specified via the ***UserID*** configuration bitstream option, shown in Table 69, page 107.

Using JTAG Interface to Communicate to a Configured FPGA Design

After the FPGA is configured, using any of the available modes, the JTAG interface offers a possible communications channel to internal FPGA logic. The BSCAN_SPARTAN3 design primitive provides two private JTAG instructions to create an internal boundary scan chain.

DC Electrical Characteristics

In this section, specifications may be designated as Advance, Preliminary, or Production. These terms are defined as follows:

Advance: Initial estimates are based on simulation, early characterization, and/or extrapolation from the characteristics of other families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on characterization. Further changes are not expected.

Production: These specifications are approved once the silicon has been characterized over numerous production lots. Parameter values are considered stable with no future changes expected.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all Spartan®-3E devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.**

Absolute Maximum Ratings

Stresses beyond those listed under Table 73, Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to absolute maximum conditions for extended periods of time adversely affects device reliability.

Table 73: **Absolute Maximum Ratings**

Symbol	Description	Conditions		Min	Max	Units
V_{CCINT}	Internal supply voltage			–0.5	1.32	V
V_{CCAUX}	Auxiliary supply voltage			–0.5	3.00	V
V_{CCO}	Output driver supply voltage			–0.5	3.75	V
V_{REF}	Input reference voltage			–0.5	V_{CCO} + 0.5 (1)	V
V_{IN} (1,2,3,4)	Voltage applied to all User I/O pins and Dual-Purpose pins	Driver in a high-impedance state	Commercial	–0.95	4.4	V
			Industrial	–0.85	4.3	V
	Voltage applied to all Dedicated pins		All temp. ranges	–0.5	V_{CCAUX} + 0.5 (3)	V
I_{IK}	Input clamp current per I/O pin	–0.5 V < V_{IN} < (V_{CCO} + 0.5 V)		–	±100	mA
V_{ESD}	Electrostatic Discharge Voltage	Human body model		–	±2000	V
		Charged device model		–	±500	V
		Machine model		–	±200	V
T_J	Junction temperature			–	125	°C
T_{STG}	Storage temperature			–65	150	°C

Notes:

1. Each of the User I/O and Dual-Purpose pins is associated with one of the four banks' V_{CCO} rails. Keeping V_{IN} within 500 mV of the associated V_{CCO} rails or ground rail ensures that the internal diode junctions do not turn on. Table 77 specifies the V_{CCO} range used to evaluate the maximum V_{IN} voltage.
2. Input voltages outside the -0.5V to V_{CCO} + 0.5V (or V_{CCAUX} + 0.5V) voltage range are require the I_{IK} input diode clamp diode rating is met and no more than 100 pins exceed the range simultaneously. Prolonged exposure to such current may compromise device reliability. A sustained current of 10 mA will not compromise device reliability. See XAPP459: *Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins on Spartan-3 Families* for more details.
3. All Dedicated pins (PROG_B, DONE, TCK, TDI, TDO, and TMS) draw power from the V_{CCAUX} rail (2.5V). Meeting the V_{IN} max limit ensures that the internal diode junctions that exist between each of these pins and the V_{CCAUX} rail do not turn on. Table 77 specifies the V_{CCAUX} range used to evaluate the maximum V_{IN} voltage. As long as the V_{IN} max specification is met, oxide stress is not possible.
4. See XAPP459: *Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins on Spartan-3 Families*.
5. For soldering guidelines, see UG112: *Device Packaging and Thermal Characteristics* and XAPP427: *Implementation and Solder Reflow Guidelines for Pb-Free Packages*.

Table 107: **Switching Characteristics for the DFS**

Symbol	Description		Device	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Output Frequency Ranges								
CLKOUT_FREQ_FX_LF	Frequency for the CLKFX and CLKFX180 outputs, low frequencies	Stepping 0	XC3S100E XC3S250E XC3S500E XC3S1600E	N/A	N/A	5	90	MHz
CLKOUT_FREQ_FX_HF	Frequency for the CLKFX and CLKFX180 outputs, high frequencies					220	307	MHz
CLKOUT_FREQ_FX	Frequency for the CLKFX and CLKFX180 outputs	Stepping 0	XC3S1200E			5	307	MHz
		Stepping 1	All	5	333		311	MHz
Output Clock Jitter(2,3)								
CLKOUT_PER_JITT_FX	Period jitter at the CLKFX and CLKFX180 outputs.		All	Typ	Max	Typ	Max	
		CLKIN ≤ 20 MHz		Note 6				ps
		CLKIN > 20 MHz		±[1% of CLKFX period + 100]	±[1% of CLKFX period + 200]	±[1% of CLKFX period + 100]	±[1% of CLKFX period + 200]	ps
Duty Cycle(4,5)								
CLKOUT_DUTY_CYCLE_FX	Duty cycle precision for the CLKFX and CLKFX180 outputs, including the BUFGMUX and clock tree duty-cycle distortion		All	-	±[1% of CLKFX period + 400]	-	±[1% of CLKFX period + 400]	ps
Phase Alignment(5)								
CLKOUT_PHASE_FX	Phase offset between the DFS CLKFX output and the DLL CLK0 output when both the DFS and DLL are used		All	-	±200	-	±200	ps
CLKOUT_PHASE_FX180	Phase offset between the DFS CLKFX180 output and the DLL CLK0 output when both the DFS and DLL are used		All	-	±[1% of CLKFX period + 300]	-	±[1% of CLKFX period + 300]	ps
Lock Time								
LOCK_FX(2)	The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX and CLKFX180 signals are valid. If using both the DLL and the DFS, use the longer locking time.	5 MHz ≤ F_{CLKIN} ≤ 15 MHz	All	-	5	-	5	ms
		F_{CLKIN} > 15 MHz		-	450	-	450	µs

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 77 and Table 106.
2. For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
3. Maximum output jitter is characterized within a reasonable noise environment (150 ps input period jitter, 40 SSOs and 25% CLB switching). Output jitter strongly depends on the environment, including the number of SSOs, the output drive strength, CLB utilization, CLB switching activities, switching frequency, power supply and PCB design. The actual maximum output jitter depends on the system application.
4. The CLKFX and CLKFX180 outputs always have an approximate 50% duty cycle.
5. Some duty-cycle and alignment specifications include 1% of the CLKFX output period or 0.01 UI.
   Example: The data sheet specifies a maximum jitter of ±[1% of CLKFX period + 300]. Assume the CLKFX output frequency is 100 MHz. The equivalent CLKFX period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 300 ps] = ±400 ps.
6. Use the Spartan-3A Jitter Calculator (www.xilinx.com/support/documentation/data_sheets/s3a_jitter_calc.zip) to estimate DFS output jitter. Use the Clocking Wizard to determine jitter for a specific design.

Package Thermal Characteristics

The power dissipated by an FPGA application has implications on package selection and system design. The power consumed by a Spartan-3E FPGA is reported using either the XPower Estimator or the XPower Analyzer calculator integrated in the Xilinx ISE® development software. Table 130 provides the thermal characteristics for the various Spartan-3E package offerings.

The junction-to-case thermal resistance (θ_{JC}) indicates the difference between the temperature measured on the package body (case) and the die junction temperature per watt of power consumption. The junction-to-board (θ_{JB}) value similarly reports the difference between the board and junction temperature. The junction-to-ambient (θ_{JA}) value reports the temperature difference per watt between the ambient environment and the junction temperature. The θ_{JA} value is reported at different air velocities, measured in linear feet per minute (LFM). The Still Air (0 LFM) column shows the θ_{JA} value in a system without a fan. The thermal resistance drops with increasing air flow.

Table 130: **Spartan-3E Package Thermal Characteristics**

Device	Package	Junction-to-Case (θ_{JC})	Junction-to-Board (θ_{JB})	Junction-to-Ambient (θ_{JA}) at Different Air Flows				Units
				Still Air (0 LFM)	250 LFM	500 LFM	750 LFM	
XC3S100E	VQ100	13.0	30.9	49.0	40.7	37.9	37.0	°C/Watt
XC3S250E		11.0	25.9	43.3	36.0	33.6	32.7	°C/Watt
XC3S500E		9.8		40.0	33.3	31.0	30.2	°C/Watt
XC3S100E	CP132	19.3	42.0	62.1	55.3	52.8	51.2	°C/Watt
XC3S250E		11.8	28.1	48.3	41.8	39.5	38.0	°C/Watt
XC3S500E		8.5	21.3	41.5	35.2	32.9	31.5	°C/Watt
XC3S100E	TQ144	8.2	31.9	52.1	40.5	34.6	32.5	°C/Watt
XC3S250E		7.2	25.7	37.6	29.2	25.0	23.4	°C/Watt
XC3S250E	PQ208	9.8	29.0	37.0	27.3	24.1	22.4	°C/Watt
XC3S500E		8.5	26.8	36.1	26.6	23.6	21.8	°C/Watt
XC3S250E	FT256	12.4	27.7	35.8	29.3	28.4	28.1	°C/Watt
XC3S500E		9.6	22.2	31.1	25.0	24.0	23.6	°C/Watt
XC3S1200E		6.5	16.4	26.2	20.5	19.3	18.9	°C/Watt
XC3S500E	FG320	9.8	15.6	26.1	20.6	19.4	18.6	°C/Watt
XC3S1200E		8.2	12.5	23.0	17.7	16.4	15.7	°C/Watt
XC3S1600E		7.1	10.6	21.1	15.9	14.6	13.8	°C/Watt
XC3S1200E	FG400	7.5	12.4	22.3	17.2	16.0	15.3	°C/Watt
XC3S1600E		6.0	10.4	20.3	15.2	14.0	13.3	°C/Watt
XC3S1600E	FG484	5.7	9.4	18.8	12.5	11.3	10.8	°C/Watt

User I/Os by Bank

Table 132 indicates how the 66 available user-I/O pins are distributed between the four I/O banks on the VQ100 package.

Table 132: **User I/Os Per Bank for XC3S100E, XC3S250E, and XC3S500E in the VQ100 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF(1)	CLK(2)
Top	0	15	5	0	1	1	8
Right	1	15	6	0	0	1	8
Bottom	2	19	0	0	18	1	0(2)
Left	3	17	5	1	2	1	8
TOTAL		**66**	**16**	**1**	**21**	**4**	**24**

Notes:

1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

Footprint Migration Differences

The production XC3S100E, XC3S250E, and XC3S500E FPGAs have identical footprints in the VQ100 package. Designs can migrate between the devices without further consideration.

CP132: 132-ball Chip-scale Package

The XC3S100E, XC3S250E and the XC3S500E FPGAs are available in the 132-ball chip-scale package, CP132. The devices share a common footprint for this package as shown in Table 133 and Figure 81.

Table 133 lists all the CP132 package pins. They are sorted by bank number and then by pin name. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

Physically, the D14 and K2 balls on the XC3S100E and XC3S250E FPGAs are not connected but should be connected to VCCINT to maintain density migration compatibility.

Similarly, the A4, C1, and P10 balls on the XC3S100E FPGA are not connected but should be connected to GND to maintain density migration compatibility.

The XC3S100E FPGA has four fewer BPI address pins, A[19:0], whereas the XC3S250E and XC3S500E support A[23:0].

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx web site at:

http://www.xilinx.com/support/documentation/data_sheets/s3e_pin.zip

Pinout Table

Table 133: **CP132 Package Pinout**

Bank	XC3S100E Pin Name	XC3S250E XC3S500E Pin Name	CP132 Ball	Type
0	IO_L01N_0	IO_L01N_0	C12	I/O
0	IO_L01P_0	IO_L01P_0	A13	I/O
0	N.C. (◆)	IO_L02N_0	A12	***100E:*** N.C. ***Others:*** I/O
0	N.C. (◆)	IO_L02P_0	B12	***100E:*** N.C. ***Others:*** I/O
0	N.C. (◆)	IO_L03N_0/VREF_0	B11	***100E:*** N.C. ***Others:*** VREF (I/O)
0	IP	IO_L03P_0	C11	***100E:*** INPUT ***Others:*** I/O
0	IO_L04N_0/GCLK5	IO_L04N_0/GCLK5	C9	GCLK
0	IO_L04P_0/GCLK4	IO_L04P_0/GCLK4	A10	GCLK
0	IO_L05N_0/GCLK7	IO_L05N_0/GCLK7	A9	GCLK
0	IO_L05P_0/GCLK6	IO_L05P_0/GCLK6	B9	GCLK
0	IO_L07N_0/GCLK11	IO_L07N_0/GCLK11	B7	GCLK
0	IO_L07P_0/GCLK10	IO_L07P_0/GCLK10	A7	GCLK
0	IO_L08N_0/VREF_0	IO_L08N_0/VREF_0	C6	VREF
0	IO_L08P_0	IO_L08P_0	B6	I/O
0	IO_L09N_0	IO_L09N_0	C5	I/O
0	IO_L09P_0	IO_L09P_0	B5	I/O
0	N.C. (◆)	IO_L10N_0	C4	***100E:*** N.C. ***Others:*** I/O
0	IP	IO_L10P_0	B4	***100E:*** INPUT ***Others:*** I/O
0	IO_L11N_0/HSWAP	IO_L11N_0/HSWAP	B3	DUAL
0	IO_L11P_0	IO_L11P_0	A3	I/O
0	IP_L06N_0/GCLK9	IP_L06N_0/GCLK9	C8	GCLK
0	IP_L06P_0/GCLK8	IP_L06P_0/GCLK8	B8	GCLK
0	VCCO_0	VCCO_0	A6	VCCO

Table 148: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S500E Pin Name	XC3S1200E Pin Name	XC3S1600E Pin Name	FG320 Ball	Type
0	VCCO_0	VCCO_0	VCCO_0	A9	VCCO
0	VCCO_0	VCCO_0	VCCO_0	C6	VCCO
0	VCCO_0	VCCO_0	VCCO_0	C13	VCCO
0	VCCO_0	VCCO_0	VCCO_0	G8	VCCO
0	VCCO_0	VCCO_0	VCCO_0	G11	VCCO
1	N.C. (◆)	IO	IO	P16	**500E:** N.C. **1200E:** I/O **1600E:** I/O
1	IO_L01N_1/A15	IO_L01N_1/A15	IO_L01N_1/A15	T17	DUAL
1	IO_L01P_1/A16	IO_L01P_1/A16	IO_L01P_1/A16	U18	DUAL
1	IO_L02N_1/A13	IO_L02N_1/A13	IO_L02N_1/A13	T18	DUAL
1	IO_L02P_1/A14	IO_L02P_1/A14	IO_L02P_1/A14	R18	DUAL
1	IO_L03N_1/VREF_1	IO_L03N_1/VREF_1	IO_L03N_1/VREF_1	R16	VREF
1	IO_L03P_1	IO_L03P_1	IO_L03P_1	R15	I/O
1	N.C. (◆)	IO_L04N_1	IO_L04N_1	N14	**500E:** N.C. **1200E:** I/O **1600E:** I/O
1	N.C. (◆)	IO_L04P_1	IO_L04P_1	N15	**500E:** N.C. **1200E:** I/O **1600E:** I/O
1	IO_L05N_1/VREF_1	IO_L05N_1/VREF_1	IO_L05N_1/VREF_1	M13	VREF
1	IO_L05P_1	IO_L05P_1	IO_L05P_1	M14	I/O
1	IO_L06N_1	IO_L06N_1	IO_L06N_1	P18	I/O
1	IO_L06P_1	IO_L06P_1	IO_L06P_1	P17	I/O
1	IO_L07N_1	IO_L07N_1	IO_L07N_1	M16	I/O
1	IO_L07P_1	IO_L07P_1	IO_L07P_1	M15	I/O
1	IO_L08N_1	IO_L08N_1	IO_L08N_1	M18	I/O
1	IO_L08P_1	IO_L08P_1	IO_L08P_1	N18	I/O
1	IO_L09N_1/A11	IO_L09N_1/A11	IO_L09N_1/A11	L15	DUAL
1	IO_L09P_1/A12	IO_L09P_1/A12	IO_L09P_1/A12	L16	DUAL
1	IO_L10N_1/VREF_1	IO_L10N_1/VREF_1	IO_L10N_1/VREF_1	L17	VREF
1	IO_L10P_1	IO_L10P_1	IO_L10P_1	L18	I/O
1	IO_L11N_1/A9/RHCLK1	IO_L11N_1/A9/RHCLK1	IO_L11N_1/A9/RHCLK1	K12	RHCLK/DUAL
1	IO_L11P_1/A10/RHCLK0	IO_L11P_1/A10/RHCLK0	IO_L11P_1/A10/RHCLK0	K13	RHCLK/DUAL
1	IO_L12N_1/A7/RHCLK3/ TRDY1	IO_L12N_1/A7/RHCLK3/ TRDY1	IO_L12N_1/A7/RHCLK3/ TRDY1	K14	RHCLK/DUAL
1	IO_L12P_1/A8/RHCLK2	IO_L12P_1/A8/RHCLK2	IO_L12P_1/A8/RHCLK2	K15	RHCLK/DUAL
1	IO_L13N_1/A5/RHCLK5	IO_L13N_1/A5/RHCLK5	IO_L13N_1/A5/RHCLK5	J16	RHCLK/DUAL
1	IO_L13P_1/A6/RHCLK4/ IRDY1	IO_L13P_1/A6/RHCLK4/ IRDY1	IO_L13P_1/A6/RHCLK4/ IRDY1	J17	RHCLK/DUAL
1	IO_L14N_1/A3/RHCLK7	IO_L14N_1/A3/RHCLK7	IO_L14N_1/A3/RHCLK7	J14	RHCLK/DUAL
1	IO_L14P_1/A4/RHCLK6	IO_L14P_1/A4/RHCLK6	IO_L14P_1/A4/RHCLK6	J15	RHCLK/DUAL
1	IO_L15N_1/A1	IO_L15N_1/A1	IO_L15N_1/A1	J13	DUAL
1	IO_L15P_1/A2	IO_L15P_1/A2	IO_L15P_1/A2	J12	DUAL
1	IO_L16N_1/A0	IO_L16N_1/A0	IO_L16N_1/A0	H17	DUAL
1	IO_L16P_1	IO_L16P_1	IO_L16P_1	H16	I/O

Footprint Migration Differences

Table 151 summarizes any footprint and functionality differences between the XC3S500E, the XC3S1200E, and the XC3S1600E FPGAs that may affect easy migration between devices available in the FG320 package. There are 26 such balls. All other pins not listed in Table 151 unconditionally migrate between Spartan-3E devices available in the FG320 package.

The XC3S500E is duplicated on both the left and right sides of the table to show migrations to and from the XC3S1200E and the XC3S1600E. The arrows indicate the direction for easy migration. A double-ended arrow (←→) indicates that the two pins have identical functionality. A left-facing arrow (←) indicates that the pin on the device on the right unconditionally migrates to the pin on the device on the left. It may be possible to migrate the opposite direction depending on the I/O configuration. For example, an I/O pin (Type = I/O) can migrate to an input-only pin (Type = INPUT) if the I/O pin is configured as an input.

Table 151: **FG320 Footprint Migration Differences**

Pin	Bank	XC3S500E	Migration	XC3S1200E	Migration	XC3S1600E	Migration	XC3S500E
A7	0	INPUT	→	I/O	←→	I/O	←	INPUT
A12	0	N.C.	→	I/O	←→	I/O	←	N.C.
D4	3	N.C.	→	I/O	←→	I/O	←	N.C.
D6	0	N.C.	→	I/O	←→	I/O	←	N.C.
D13	0	INPUT	→	I/O	←→	I/O	←	INPUT
E3	3	N.C.	→	I/O	←→	I/O	←	N.C.
E4	3	N.C.	→	I/O	←→	I/O	←	N.C.
E6	0	N.C.	→	I/O	←→	I/O	←	N.C.
E15	1	N.C.	→	I/O	←→	I/O	←	N.C.
E16	1	N.C.	→	I/O	←→	I/O	←	N.C.
E17	1	I/O	←	INPUT	←→	INPUT	→	I/O
F4	3	I/O	←	INPUT	←→	INPUT	→	I/O
N12	2	N.C.	→	I/O	←→	I/O	←	N.C.
N14	1	N.C.	→	I/O	←→	I/O	←	N.C.
N15	1	N.C.	→	I/O	←→	I/O	←	N.C.
P3	3	N.C.	→	I/O	←→	I/O	←	N.C.
P4	3	N.C.	→	I/O	←→	I/O	←	N.C.
P12	2	N.C.	→	I/O	←→	I/O	←	N.C.
P15	1	I/O	←	INPUT	←→	INPUT	→	I/O
P16	1	N.C.	→	I/O	←→	I/O	←	N.C.
R4	3	VREF(I/O)	←	VREF(INPUT)	←→	VREF(INPUT)	→	VREF(I/O)
U6	2	INPUT	→	I/O	←→	I/O	←	INPUT
U13	2	INPUT	→	I/O	←→	I/O	←	INPUT
V5	2	N.C.	→	I/O	←→	I/O	←	N.C.
V6	2	N.C.	→	VREF	←→	VREF	←	N.C.
V7	2	N.C.	→	I/O	←→	I/O	←	N.C.
DIFFERENCES			**26**		**0**		**26**	

Legend:

←→ This pin is identical on the device on the left and the right.

→ This pin can unconditionally migrate from the device on the left to the device on the right. Migration in the other direction may be possible depending on how the pin is configured for the device on the right.

← This pin can unconditionally migrate from the device on the right to the device on the left. Migration in the other direction may be possible depending on how the pin is configured for the device on the left.

Table 152: **FG400 Package Pinout *(Cont'd)***

Bank	XC3S1200E XC3S1600E Pin Name	FG400 Ball	Type
3	IP	N5	INPUT
3	IP	P3	INPUT
3	IP	T4	INPUT
3	IP	W1	INPUT
3	IP/VREF_3	K5	VREF
3	IP/VREF_3	P6	VREF
3	VCCO_3	E2	VCCO
3	VCCO_3	H4	VCCO
3	VCCO_3	L2	VCCO
3	VCCO_3	L6	VCCO
3	VCCO_3	P4	VCCO
3	VCCO_3	U2	VCCO
GND	GND	A1	GND
GND	GND	A11	GND
GND	GND	A20	GND
GND	GND	B7	GND
GND	GND	B14	GND
GND	GND	C3	GND
GND	GND	C18	GND
GND	GND	D10	GND
GND	GND	F6	GND
GND	GND	F15	GND
GND	GND	G2	GND
GND	GND	G12	GND
GND	GND	G19	GND
GND	GND	H8	GND
GND	GND	J9	GND
GND	GND	J11	GND
GND	GND	K1	GND
GND	GND	K8	GND
GND	GND	K10	GND
GND	GND	K12	GND
GND	GND	K17	GND
GND	GND	L4	GND
GND	GND	L9	GND
GND	GND	L11	GND
GND	GND	L13	GND
GND	GND	L20	GND
GND	GND	M10	GND
GND	GND	M12	GND
GND	GND	N13	GND
GND	GND	P2	GND
GND	GND	P9	GND

Table 152: **FG400 Package Pinout *(Cont'd)***

Bank	XC3S1200E XC3S1600E Pin Name	FG400 Ball	Type
GND	GND	P19	GND
GND	GND	R6	GND
GND	GND	R15	GND
GND	GND	U11	GND
GND	GND	V3	GND
GND	GND	V18	GND
GND	GND	W7	GND
GND	GND	W14	GND
GND	GND	Y1	GND
GND	GND	Y10	GND
GND	GND	Y20	GND
VCCAUX	DONE	V17	CONFIG
VCCAUX	PROG_B	C2	CONFIG
VCCAUX	TCK	D17	JTAG
VCCAUX	TDI	B3	JTAG
VCCAUX	TDO	B19	JTAG
VCCAUX	TMS	E17	JTAG
VCCAUX	VCCAUX	D11	VCCAUX
VCCAUX	VCCAUX	H12	VCCAUX
VCCAUX	VCCAUX	J7	VCCAUX
VCCAUX	VCCAUX	K4	VCCAUX
VCCAUX	VCCAUX	L17	VCCAUX
VCCAUX	VCCAUX	M14	VCCAUX
VCCAUX	VCCAUX	N9	VCCAUX
VCCAUX	VCCAUX	U10	VCCAUX
VCCINT	VCCINT	H9	VCCINT
VCCINT	VCCINT	H11	VCCINT
VCCINT	VCCINT	H13	VCCINT
VCCINT	VCCINT	J8	VCCINT
VCCINT	VCCINT	J10	VCCINT
VCCINT	VCCINT	J12	VCCINT
VCCINT	VCCINT	K9	VCCINT
VCCINT	VCCINT	K11	VCCINT
VCCINT	VCCINT	L10	VCCINT
VCCINT	VCCINT	L12	VCCINT
VCCINT	VCCINT	M9	VCCINT
VCCINT	VCCINT	M11	VCCINT
VCCINT	VCCINT	M13	VCCINT
VCCINT	VCCINT	N8	VCCINT
VCCINT	VCCINT	N10	VCCINT
VCCINT	VCCINT	N12	VCCINT

FG484 Footprint

Left Half of Package (top view)

214 **I/O:** Unrestricted, general-purpose user I/O

72 **INPUT:** User I/O or reference resistor input for bank

46 **DUAL:** Configuration pin, then possible user I/O

28 **VREF:** User I/O or input voltage reference for bank

16 **CLK:** User I/O, input, or clock buffer input

2 **CONFIG:** Dedicated configuration pins

4 **JTAG:** Dedicated JTAG port pins

48 **GND:** Ground

28 **VCCO:** Output voltage supply for bank

16 **VCCINT:** Internal core supply voltage (+1.2V)

10 **VCCAUX:** Auxiliary supply voltage (+2.5V)

0 **N.C.:** Not connected

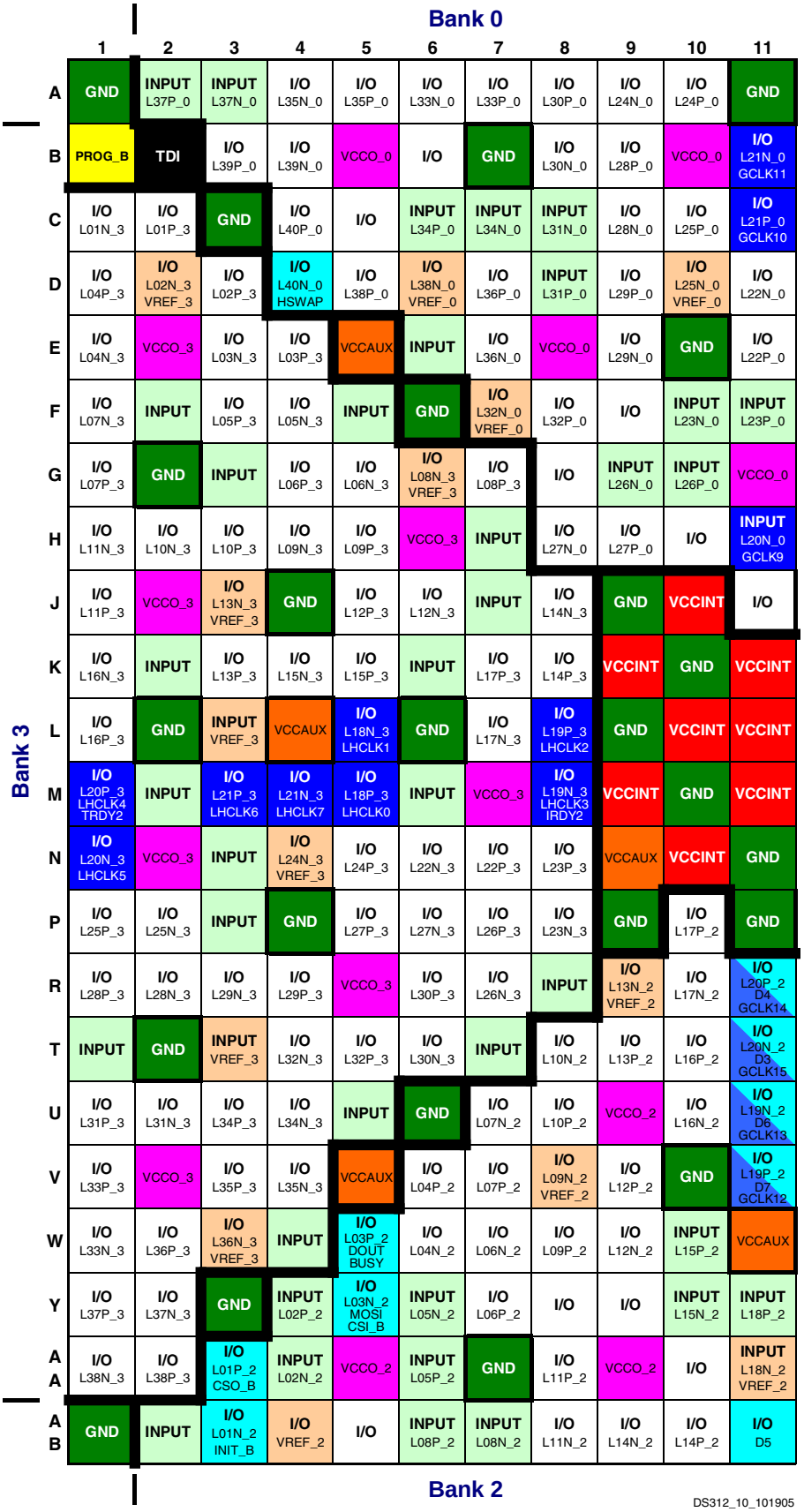

Figure 88: **FG484 Package Footprint (top view)**