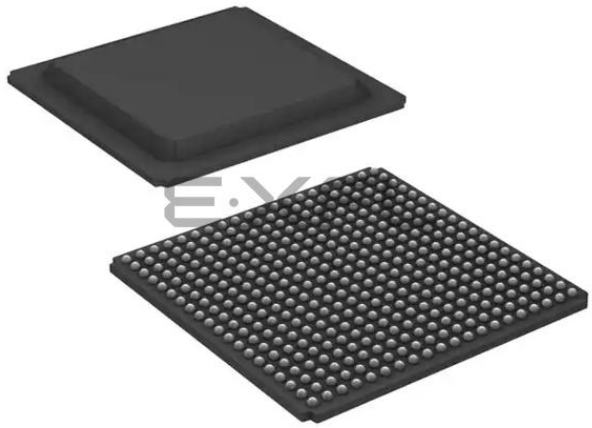

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	2168
Number of Logic Elements/Cells	19512
Total RAM Bits	516096
Number of I/O	304
Number of Gates	1200000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	400-BGA
Supplier Device Package	400-FBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s1200e-4fgg400c

Input Delay Functions

Each IOB has a programmable delay block that optionally delays the input signal. In Figure 6, the signal path has a coarse delay element that can be bypassed. The input signal then feeds a 6-tap delay line. The coarse and tap delays vary; refer to timing reports for specific delay values. All six taps are available via a multiplexer for use as an asynchronous input directly into the FPGA fabric. In this way, the delay is programmable in 12 steps. Three of the six taps are also available via a multiplexer to the D inputs of the synchronous storage elements. The delay inserted in the path to the storage element can be varied in six steps. The first, coarse delay element is common to both asynchronous and synchronous paths, and must be either used or not used for both paths.

The delay values are set up in the silicon once at configuration time—they are non-modifiable in device operation.

The primary use for the input delay element is to adjust the input delay path to ensure that there is no hold time requirement when using the input flip-flop(s) with a global clock. The default value is chosen automatically by the Xilinx software tools as the value depends on device size and the specific device edge where the flip-flop resides. The value set by the Xilinx ISE software is indicated in the Map report generated by the implementation tools, and the resulting effects on input timing are reported using the Timing Analyzer tool.

If the design uses a DCM in the clock path, then the delay element can be safely set to zero because the Delay-Locked Loop (DLL) compensation automatically ensures that there is still no input hold time requirement.

Both asynchronous and synchronous values can be modified, which is useful where extra delay is required on clock or data inputs, for example, in interfaces to various types of RAM.

These delay values are defined through the IBUF_DELAY_VALUE and the IFD_DELAY_VALUE parameters. The default IBUF_DELAY_VALUE is 0, bypassing the delay elements for the asynchronous input. The user can set this parameter to 0-12. The default IFD_DELAY_VALUE is AUTO. IBUF_DELAY_VALUE and IFD_DELAY_VALUE are independent for each input. If the same input pin uses both registered and non-registered input paths, both parameters can be used, but they must both be in the same half of the total delay (both either bypassing or using the coarse delay element).

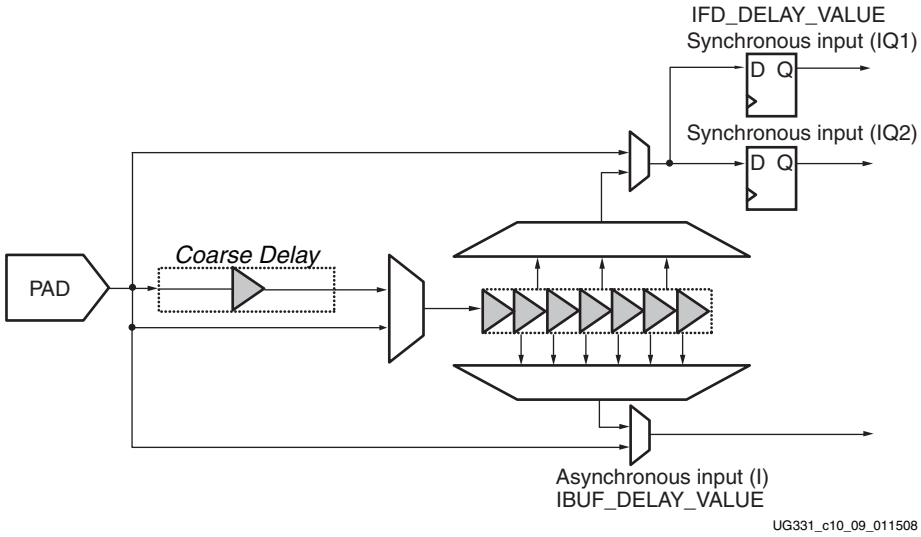


Figure 6: **Programmable Fixed Input Delay Elements**

Table 14: **Carry Logic Functions *(Cont'd)***

Function	Description
CY0G	Carry generation for top half of slice. Fixed selection of: · G1 or G2 inputs to the LUT (both equal 1 when a carry is to be generated) · GAND gate for multiplication · BY input for carry initialization · Fixed 1 or 0 input for use as a simple Boolean function
CYMUXF	Carry generation or propagation mux for bottom half of slice. Dynamic selection via CYSELF of: · CYINIT carry propagation (CYSELF = 1) · CY0F carry generation (CYSELF = 0)
CYMUXG	Carry generation or propagation mux for top half of slice. Dynamic selection via CYSELF of: · CYMUXF carry propagation (CYSELG = 1) · CY0G carry generation (CYSELG = 0)
CYSELF	Carry generation or propagation select for bottom half of slice. Fixed selection of: · F-LUT output (typically XOR result) · Fixed 1 to always propagate
CYSELG	Carry generation or propagation select for top half of slice. Fixed selection of: · G-LUT output (typically XOR result) · Fixed 1 to always propagate
XORF	Sum generation for bottom half of slice. Inputs from: · F-LUT · CYINIT carry signal from previous stage Result is sent to either the combinatorial or registered output for the top of the slice.
XORG	Sum generation for top half of slice. Inputs from: · G-LUT · CYMUXF carry signal from previous stage Result is sent to either the combinatorial or registered output for the top of the slice.
FAND	Multiplier partial product for bottom half of slice. Inputs: · F-LUT F1 input · F-LUT F2 input Result is sent through CY0F to become the carry generate signal into CYMUXF
GAND	Multiplier partial product for top half of slice. Inputs: · G-LUT G1 input · G-LUT G2 input Result is sent through CY0G to become the carry generate signal into CYMUXG

The basic usage of the carry logic is to generate a half-sum in the LUT via an XOR function, which generates or propagates a carry out COUT via the carry mux CYMUXF (or CYMUXG), and then complete the sum with the dedicated XORF (or XORG) gate and the carry input CIN. This structure allows two bits of an arithmetic function in each slice. The CYMUXF (or CYMUXG) can be instantiated using the MUXCY element, and the XORF (or XORG) can be instantiated using the XORCY element.

The FAND (or GAND) gate is used for partial product multiplication and can be instantiated using the MULT_AND component. Partial products are generated by two-input AND gates and then added. The carry logic is efficient for the adder, but one of the inputs must be outside the LUT as shown in Figure 23.

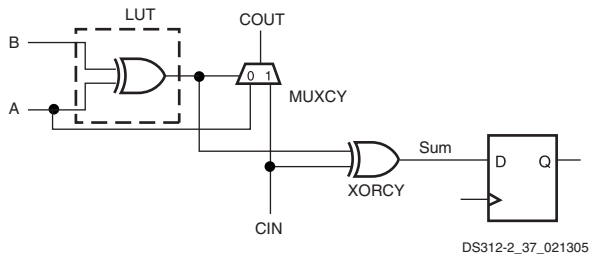


Figure 23: **Using the MUXCY and XORCY in the Carry Logic**

The FAND (or GAND) gate is used to duplicate one of the partial products, while the LUT generates both partial products and the XOR function, as shown in Figure 24.

Initialization

The CLB storage elements are initialized at power-up, during configuration, by the global GSR signal, and by the individual SR or REV inputs to the CLB. The storage elements can also be re-initialized using the GSR input on the STARTUP_SPARTAN3E primitive. See Global Controls (STARTUP_SPARTAN3E).

Table 17: **Slice Storage Element Initialization**

Signal	Description
SR	Set/Reset input. Forces the storage element into the state specified by the attribute SRHIGH or SRLOW. SRHIGH forces a logic 1 when SR is asserted. SRLOW forces a logic 0. For each slice, set and reset can be set to be synchronous or asynchronous.
REV	Reverse of Set/Reset input. A second input (BY) forces the storage element into the opposite state. The reset condition is predominant over the set condition if both are active. Same synchronous/asynchronous setting as for SR.
GSR	Global Set/Reset. GSR defaults to active High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN3E element. The initial state after configuration or GSR is defined by a separate INIT0 and INIT1 attribute. By default, setting the SRLOW attribute sets INIT0, and setting the SRHIGH attribute sets INIT1.

Distributed RAM

For additional information, refer to the “Using Look-Up Tables as Distributed RAM” chapter in UG331.

The LUTs in the SLICEM can be programmed as distributed RAM. This type of memory affords moderate amounts of data buffering anywhere along a data path. One SLICEM LUT stores 16 bits (RAM16). The four LUT inputs F[4:1] or G[4:1] become the address lines labeled A[4:1] in the device model and A[3:0] in the design components, providing a 16x1 configuration in one LUT. Multiple SLICEM LUTs can be combined in various ways to store larger amounts of data, including 16x4, 32x2, or 64x1 configurations in one CLB. The fifth and sixth address lines required for the 32-deep and 64-deep configurations, respectively, are implemented using the BX and BY inputs, which connect to the write enable logic for writing and the F5MUX and F6MUX for reading.

Writing to distributed RAM is always synchronous to the SLICEM clock (WCLK for distributed RAM) and enabled by the SLICEM SR input which functions as the active-High Write Enable (WE). The read operation is asynchronous, and, therefore, during a write, the output initially reflects the old data at the address being written.

The distributed RAM outputs can be captured using the flip-flops within the SLICEM element. The WE write-enable control for the RAM and the CE clock-enable control for the flip-flop are independent, but the WCLK and CLK clock inputs are shared. Because the RAM read operation is asynchronous, the output data always reflects the currently addressed RAM location.

A dual-port option combines two LUTs so that memory access is possible from two independent data lines. The same data is written to both 16x1 memories but they have independent read address lines and outputs. The dual-port function is implemented by cascading the G-LUT address lines, which are used for both read and write, to the F-LUT write address lines (WF[4:1] in Figure 15), and by cascading the G-LUT data input D1 through the DIF_MUX in Figure 15 and to the D1 input on the F-LUT. One CLB provides a 16x1 dual-port memory as shown in Figure 26.

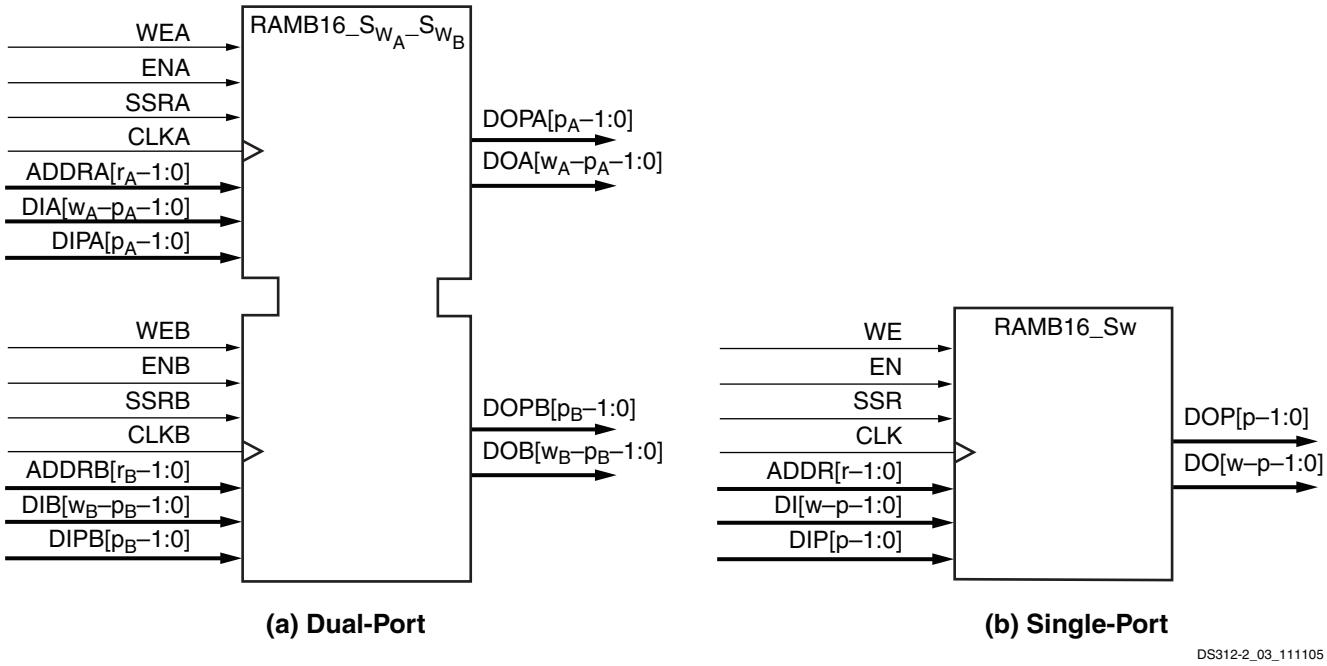
Any write operation on the D input and any read operation on the SPO output can occur simultaneously with and independently from a read operation on the second read-only port, DPO.

Block RAM Port Signal Definitions

Representations of the dual-port primitive RAMB16_S[w_A]_S[w_B] and the single-port primitive RAMB16_S[w] with their associated signals are shown in Figure 32a and Figure 32b, respectively. These signals are defined in Table 23. The control signals (WE, EN, CLK, and SSR) on the block RAM are active High. However, optional inverters on the control signals change the polarity of the active edge to active Low.

Design Note

Whenever a block RAM port is enabled (ENA or ENB = High), all address transitions must meet the data sheet setup and hold times with respect to the port clock (CLKA or CLKB), as shown in Table 103, page 138.This requirement must be met even if the RAM read output is of no interest.



Notes:

1. w_A and w_B are integers representing the total data path width (i.e., data bits plus parity bits) at Ports A and B, respectively.
2. p_A and p_B are integers that indicate the number of data path lines serving as parity bits.
3. r_A and r_B are integers representing the address bus width at ports A and B, respectively.
4. The control signals CLK, WE, EN, and SSR on both ports have the option of inverted polarity.

Figure 32: **Block RAM Primitives**

Table 23: **Block RAM Port Signals**

Signal Description	Port A Signal Name	Port B Signal Name	Direction	Function
Address Bus	ADDRA	ADDRB	Input	The Address Bus selects a memory location for read or write operations. The width (w) of the port's associated data path determines the number of available address lines (r), as per Table 22. Whenever a port is enabled (ENA or ENB = High), address transitions must meet the data sheet setup and hold times with respect to the port clock (CLKA or CLKB), as shown in Table 103, page 138.This requirement must be met even if the RAM read output is of no interest.
Data Input Bus	DIA	DIB	Input	Data at the DI input bus is written to the RAM location specified by the address input bus (ADDR) during the active edge of the CLK input, when the clock enable (EN) and write enable (WE) inputs are active. It is possible to configure a port's DI input bus width (w-p) based on Table 22. This selection applies to both the DI and DO paths of a given port.
Parity Data Input(s)	DIPA	DIPB	Input	Parity inputs represent additional bits included in the data input path. Although referred to herein as "parity" bits, the parity inputs and outputs have no special functionality for generating or checking parity and can be used as additional data bits. The number of parity bits 'p' included in the DI (same as for the DO bus) depends on a port's total data path width (w). See Table 22.
Data Output Bus	DOA	DOB	Output	Data is written to the DO output bus from the RAM location specified by the address input bus, ADDR. See the DI signal description for DO port width configurations. Basic data access occurs on the active edge of the CLK when WE is inactive and EN is active. The DO outputs mirror the data stored in the address ADDR memory location. Data access with WE active if the WRITE_MODE attribute is set to the value: WRITE_FIRST, which accesses data after the write takes place. READ_FIRST accesses data before the write occurs. A third attribute, NO_CHANGE, latches the DO outputs upon the assertion of WE. See Block RAM Data Operations for details on the WRITE_MODE attribute.
Parity Data Output(s)	DOPA	DOPB	Output	Parity outputs represent additional bits included in the data input path. The number of parity bits 'p' included in the DI bus (same as for the DO bus) depends on a port's total data path width (w). See the DIP signal description for configuration details.
Write Enable	WEA	WEB	Input	When asserted together with EN, this input enables the writing of data to the RAM. When WE is inactive with EN asserted, read operations are still possible. In this case, a latch passes data from the addressed memory location to the DO outputs.
Clock Enable	ENA	ENB	Input	When asserted, this input enables the CLK signal to perform read and write operations to the block RAM. When inactive, the block RAM does not perform any read or write operations.
Set/Reset	SSRA	SSRB	Input	When asserted, this pin forces the DO output latch to the value of the SRVAL attribute. It is synchronized to the CLK signal.
Clock	CLKA	CLKB	Input	This input accepts the clock signal to which read and write operations are synchronized. All associated port inputs are required to meet setup times with respect to the clock signal's active edge. The data output bus responds after a clock-to-out delay referenced to the clock signal's active edge.

DLL Clock Output and Feedback Connections

As many as four of the nine DCM clock outputs can simultaneously drive four of the BUFGMUX buffers on the same die edge. All DCM clock outputs can simultaneously drive general routing resources, including interconnect leading to OBUF buffers.

The feedback loop is essential for DLL operation. Either the CLK0 or CLK2X outputs feed back to the CLKFB input via a BUFGMUX global buffer to eliminate the clock distribution delay. The specific BUFGMUX buffer used to feed back the CLK0 or CLK2X signal is ideally one of the BUFGMUX buffers associated with a specific DCM, as shown in Table 30, Table 31, and Table 32.

The feedback path also phase-aligns the other seven DLL outputs: CLK0, CLK90, CLK180, CLK270, CLKDV, CLK2X, or CLK2X180. The CLK_FEEDBACK attribute value must agree with the physical feedback connection. Use “1X” for CLK0 feedback and “2X” for CLK2X feedback. If the DFS unit is used stand-alone, without the DLL, then no feedback is required and set the CLK_FEEDBACK attribute to “NONE”.

Two basic cases determine how to connect the DLL clock outputs and feedback connections: on-chip synchronization and off-chip synchronization, which are illustrated in Figure 42a through Figure 42d.

In the on-chip synchronization case in Figure 42a and Figure 42b, it is possible to connect any of the DLL’s seven output clock signals through general routing resources to the FPGA’s internal registers. Either a Global Clock Buffer (BUFG) or a BUFGMUX affords access to the global clock network. As shown in Figure 42a, the feedback loop is created by routing CLK0 (or CLK2X) in Figure 42b to a global clock net, which in turn drives the CLKFB input.

In the off-chip synchronization case in Figure 42c and Figure 42d, CLK0 (or CLK2X) plus any of the DLL’s other output clock signals exit the FPGA using output buffers (OBUF) to drive an external clock network plus registers on the board. As shown in Figure 42c, the feedback loop is formed by feeding CLK0 (or CLK2X) in Figure 42d back into the FPGA, then to the DCM’s CLKFB input via a Global Buffer Input, specified in Table 30.

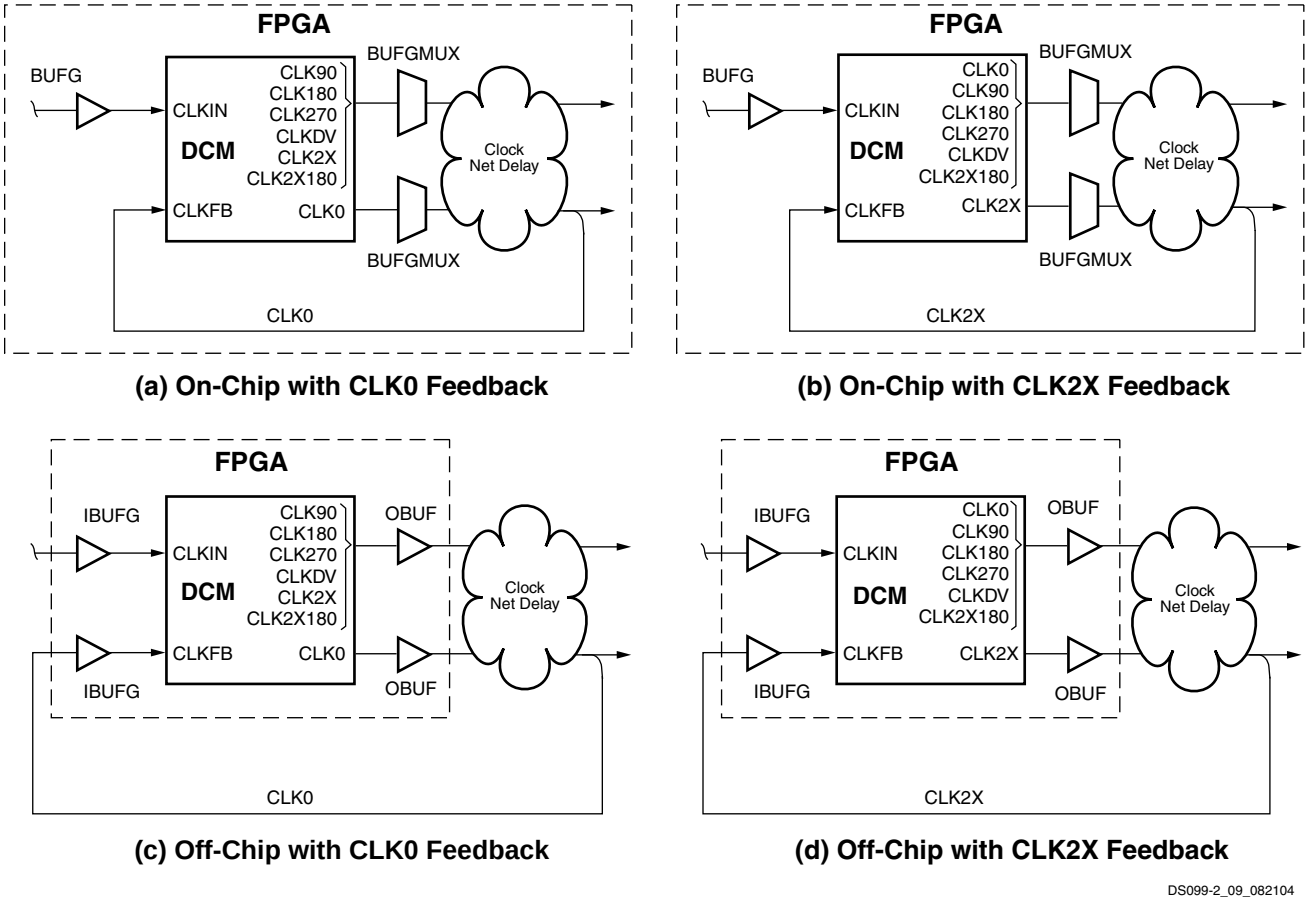


Figure 42: **Input Clock, Output Clock, and Feedback Connections for the DLL**

FIXED Phase Shift Mode

The FIXED phase shift mode shifts the DCM outputs by a fixed amount (T_{PS}), controlled by the user-specified PHASE_SHIFT attribute. The PHASE_SHIFT value (shown as P in Figure 44) must be an integer ranging from –255 to +255. PHASE_SHIFT specifies a phase shift delay as a fraction of the T_{CLKIN}. The phase shift behavior is different between ISE 8.1, Service Pack 3 and prior software versions, as described below.

Design Note

Prior to ISE 8.1i, Service Pack 3, the FIXED phase shift feature operated differently than the Spartan-3 DCM design primitive and simulation model. Designs using software prior to ISE 8.1i, Service Pack 3 require recompilation using the latest ISE software release. The following Answer Record contains additional information:

http://www.xilinx.com/support/answers/23153.htm.

FIXED Phase Shift using ISE 8.1i, Service Pack 3 and later: See Equation 2. The value corresponds to a phase shift range of –360° to +360°, which matches behavior of the Spartan-3 DCM design primitive and simulation model.

$$t_{PS} = \left(\frac{PHASESHIFT}{256}\right) \bullet T_{CLKIN} \qquad Eq\ 2$$

FIXED Phase Shift prior to ISE 8.1i, Service Pack 3: See Equation 3. The value corresponds to a phase shift range of –180° to +180° degrees, which is different from the Spartan-3 DCM design primitive and simulation model. Designs created prior to ISE 8.1i, Service Pack 3 must be recompiled using the most recent ISE development software.

$$t_{PS} = \left(\frac{PHASESHIFT}{512}\right) \bullet T_{CLKIN} \qquad Eq\ 3$$

When the PHASE_SHIFT value is zero, CLKFB and CLKIN are in phase, the same as when the PS unit is disabled. When the PHASE_SHIFT value is positive, the DCM outputs are shifted later in time with respect to CLKIN input. When the attribute value is negative, the DCM outputs are shifted earlier in time with respect to CLKIN.

Figure 44b illustrates the relationship between CLKFB and CLKIN in the Fixed Phase mode. In the Fixed Phase mode, the PSEN, PSCLK, and PSINCDEC inputs are not used and must be tied to GND.

Equation 2 or Equation 3 applies only to FIXED phase shift mode. The VARIABLE phase shift mode operates differently.

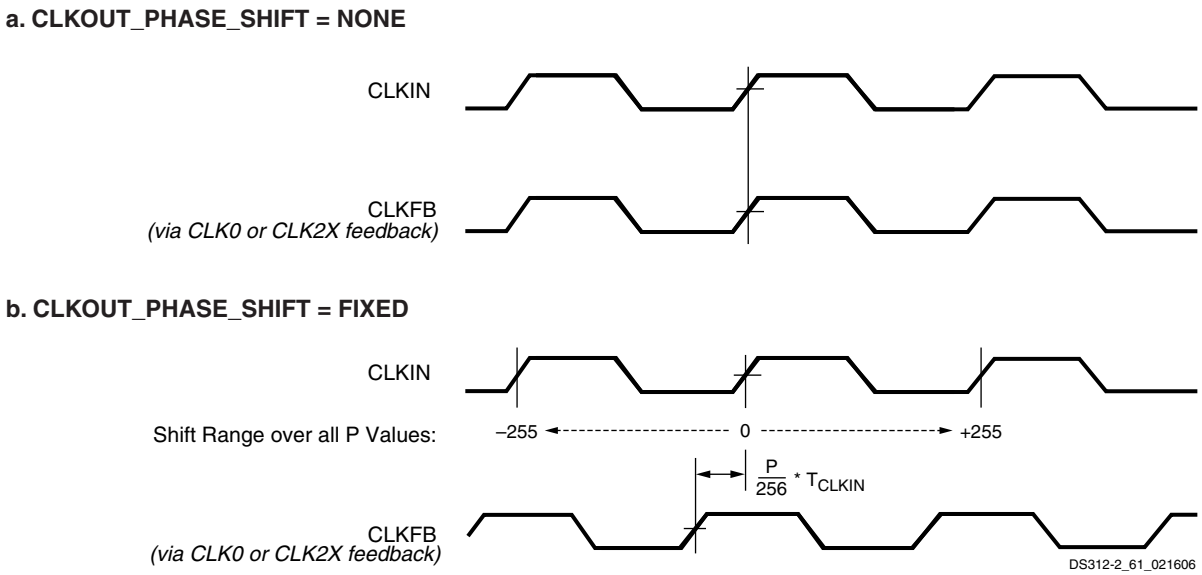


Figure 44: **NONE and FIXED Phase Shifter Waveforms (ISE 8.1i, Service Pack 3 and later)**

VARIABLE Phase Shift Mode

In VARIABLE phase shift mode, the FPGA application dynamically adjusts the fine phase shift value using three inputs to the PS unit (PSEN, PSCLK, and PSINCDEC), as defined in Table 36 and shown in Figure 40.

Table 36: **Signals for Variable Phase Mode**

Signal	Direction	Description
PSEN(1)	Input	Enables the Phase Shift unit for variable phase adjustment.
PSCLK(1)	Input	Clock to synchronize phase shift adjustment.
PSINCDEC(1)	Input	When High, increments the current phase shift value. When Low, decrements the current phase shift value. This signal is synchronized to the PSCLK signal.
PSDONE	Output	Goes High to indicate that the present phase adjustment is complete and PS unit is ready for next phase adjustment request. This signal is synchronized to the PSCLK signal.

Notes:

1. This input supports either a true or inverted polarity.

The FPGA application uses the three PS inputs on the Phase Shift unit to dynamically and incrementally increase or decrease the phase shift amount on all nine DCM clock outputs.

To adjust the current phase shift value, the PSEN enable signal must be High to enable the PS unit. Coincidently, PSINCDEC must be High to increment the current phase shift amount or Low to decrement the current amount. All VARIABLE phase shift operations are controlled by the PSCLK input, which can be the CLKIN signal or any other clock signal.

Design Note

The VARIABLE phase shift feature operates differently from the Spartan-3 DCM; use the DCM_SP primitive, not the DCM primitive.

DCM_DELAY_STEP

DCM_DELAY_STEP is the finest delay resolution available in the PS unit. Its value is provided at the bottom of Table 105 in Module 3. For each enabled PSCLK cycle that PSINCDEC is High, the PS unit adds one DCM_ DELAY_STEP of phase shift to all nine DCM outputs. Similarly, for each enabled PSCLK cycle that PSINCDEC is Low, the PS unit subtracts one DCM_ DELAY_STEP of phase shift from all nine DCM outputs.

Because each DCM_DELAY_STEP has a minimum and maximum value, the actual phase shift delay for the present phase increment/decrement value (VALUE) falls within the minimum and maximum values according to Equation 4 and Equation 5.

$$T_{PS}(Max) = VALUE \bullet \text{DCM\_DELAY\_STEP\_MAX} \quad Eq\ 4$$

$$T_{PS}(Min) = VALUE \bullet \text{DCM\_DELAY\_STEP\_MIN} \quad Eq\ 5$$

The maximum variable phase shift steps, MAX_STEPS, is described in Equation 6 or Equation 7, for a given CLKIN input period, T_{CLKIN}, in nanoseconds. To convert this to a phase shift range measured in time and not steps, use MAX_STEPS derived in Equation 6 and Equation 7 for VALUE in Equation 4 and Equation 5.

If CLKIN < 60 MHz:

$$\text{MAX\_STEPS} = \pm[INTEGER(10 \bullet (T_{CLKIN} - 3))] \quad Eq\ 6$$

If CLKIN ≥ 60 MHz:

$$\text{MAX\_STEPS} = \pm[INTEGER(15 \bullet (T_{CLKIN} - 3))] \quad Eq\ 7$$

The phase adjustment might require as many as 100 CLKIN cycles plus 3 PSCLK cycles to take effect, at which point the DCM's PSDONE output goes High for one PSCLK cycle. This pulse indicates that the PS unit completed the previous adjustment and is now ready for the next request.

Asserting the Reset (RST) input returns the phase shift to zero.

By contrast, the clock switch matrixes on the top and bottom edges receive signals from any of the five following sources: two GCLK pins, two DCM outputs, or one Double-Line interconnect.

Table 41 indicates permissible connections between clock inputs and BUFGMUX elements. The I0-input provides the best input path to a clock buffer. The I1-input provides the secondary input for the clock multiplexer function.

The four BUFGMUX elements on the top edge are paired together and share inputs from the eight global clock inputs along the top edge. Each BUFGMUX pair connects to four of the eight global clock inputs, as shown in Figure 45. This optionally allows differential inputs to the global clock inputs without wasting a BUFGMUX element.

Table 41: **Connections from Clock Inputs to BUFGMUX Elements and Associated Quadrant Clock**

Quadrant Clock Line[1]	Left-Half BUFGMUX			Top or Bottom BUFGMUX			Right-Half BUFGMUX		
	Location[2]	I0 Input	I1 Input	Location[2]	I0 Input	I1 Input	Location[2]	I0 Input	I1 Input
H	*X0Y9*	LHCLK7	LHCLK6	*X1Y10*	GCLK7 or GCLK11	GCLK6 or GCLK10	*X3Y9*	RHCLK3	RHCLK2
G	*X0Y8*	LHCLK6	LHCLK7	*X1Y11*	GCLK6 or GCLK10	GCLK7 or GCLK11	*X3Y8*	RHCLK2	RHCLK3
F	*X0Y7*	LHCLK5	LHCLK4	*X2Y10*	GCLK5 or GCLK9	GCLK4 or GCLK8	*X3Y7*	RHCLK1	RHCLK0
E	*X0Y6*	LHCLK4	LHCLK5	*X2Y11*	GCLK4 or GCLK8	GCLK5 or GCLK9	*X3Y6*	RHCLK0	RHCLK1
D	*X0Y5*	LHCLK3	LHCLK2	*X1Y0*	GCLK3 or GCLK15	GCLK2 or GCLK14	*X3Y5*	RHCLK7	RHCLK6
C	*X0Y4*	LHCLK2	LHCLK3	*X1Y1*	GCLK2 or GCLK14	GCLK3 or GCLK15	*X3Y4*	RHCLK6	RHCLK7
B	*X0Y3*	LHCLK1	LHCLK0	*X2Y0*	GCLK1 or GCLK13	GCLK0 or GCLK12	*X3Y3*	RHCLK5	RHCLK4
A	*X0Y2*	LHCLK0	LHCLK1	*X2Y1*	GCLK0 or GCLK12	GCLK1 or GCLK13	*X3Y2*	RHCLK4	RHCLK5

Notes:

1. See Quadrant Clock Routing for connectivity details for the eight quadrant clocks.
2. See Figure 45 for specific BUFGMUX locations, and Figure 47 for information on how BUFGMUX elements drive onto a specific clock line within a quadrant.

Interconnect

For additional information, refer to the “Using Interconnect” chapter in UG331.

Interconnect is the programmable network of signal pathways between the inputs and outputs of functional elements within the FPGA, such as IOBs, CLBs, DCMs, and block RAM.

Overview

Interconnect, also called routing, is segmented for optimal connectivity. Functionally, interconnect resources are identical to that of the Spartan-3 architecture. There are four kinds of interconnects: long lines, hex lines, double lines, and direct lines. The Xilinx Place and Route (PAR) software exploits the rich interconnect array to deliver optimal system performance and the fastest compile times.

Switch Matrix

The switch matrix connects to the different kinds of interconnects across the device. An interconnect tile, shown in Figure 48, is defined as a single switch matrix connected to a functional element, such as a CLB, IOB, or DCM. If a functional element spans across multiple switch matrices such as the block RAM or multipliers, then an interconnect tile is defined by the number of switch matrices connected to that functional element. A Spartan-3E device can be represented as an array of interconnect tiles where interconnect resources are for the channel between any two adjacent interconnect tile rows or columns as shown in Figure 49.

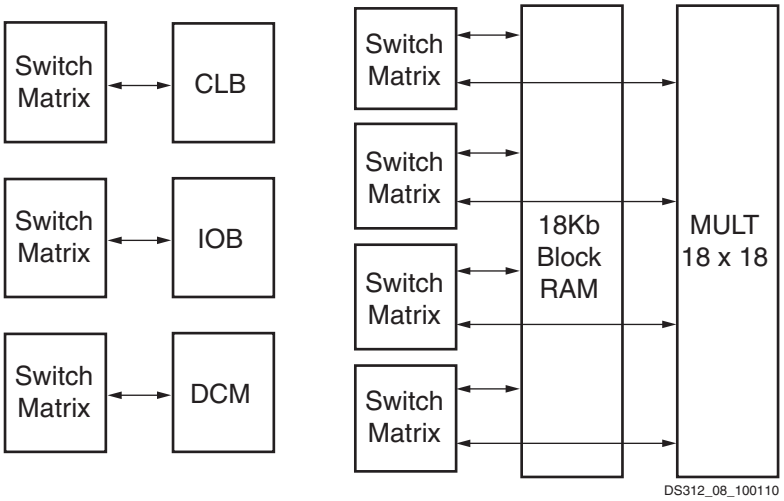


Figure 48: **Four Types of Interconnect Tiles (CLBs, IOBs, DCMs, and Block RAM/Multiplier)**

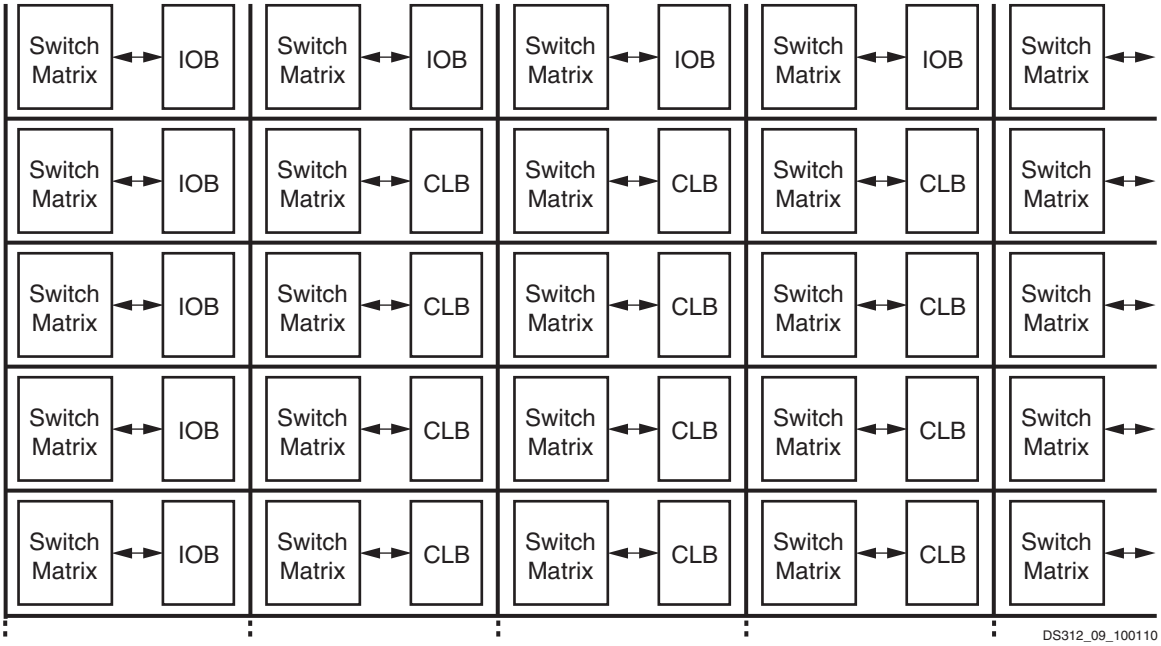


Figure 49: **Array of Interconnect Tiles in Spartan-3E FPGA**

read operations at this time. Spartan-3E FPGAs issue the read command just once. If the SPI Flash is not ready, then the FPGA does not properly configure.

If the 3.3V supply is last in the sequence and does not ramp fast enough, or if the SPI Flash PROM cannot be ready when required by the FPGA, delay the FPGA configuration process by holding either the FPGA's PROG_B input or INIT_B input Low, as highlighted in Figure 54. Release the FPGA when the SPI Flash PROM is ready. For example, a simple R-C delay circuit attached to the INIT_B pin forces the FPGA to wait for a preselected amount of time. Alternately, a Power Good signal from the 3.3V supply or a system reset signal accomplishes the same purpose. Use an open-drain or open-collector output when driving PROG_B or INIT_B.

SPI Flash PROM Density Requirements

Table 57 shows the smallest usable SPI Flash PROM to program a single Spartan-3E FPGA. Commercially available SPI Flash PROMs range in density from 1 Mbit to 128 Mbits. A multiple-FPGA daisy-chained application requires a SPI Flash PROM large enough to contain the sum of the FPGA file sizes. An application can also use a larger-density SPI Flash PROM to hold additional data beyond just FPGA configuration data. For example, the SPI Flash PROM can also store application code for a MicroBlaze™ RISC processor core integrated in the Spartan-3E FPGA. See Using the SPI Flash Interface after Configuration.

Table 57: **Number of Bits to Program a Spartan-3E FPGA and Smallest SPI Flash PROM**

Device	Number of Configuration Bits	Smallest Usable SPI Flash PROM
XC3S100E	581,344	1 Mbit
XC3S250E	1,353,728	2 Mbit
XC3S500E	2,270,208	4 Mbit
XC3S1200E	3,841,184	4 Mbit
XC3S1600E	5,969,696	8 Mbit

CCLK Frequency

In SPI Flash mode, the FPGA's internal oscillator generates the configuration clock frequency. The FPGA provides this clock on its CCLK output pin, driving the PROM's clock input pin. The FPGA starts configuration at its lowest frequency and increases its frequency for the remainder of the configuration process if so specified in the configuration bitstream. The maximum frequency is specified using the ***ConfigRate*** bitstream generator option. The maximum frequency supported by the FPGA configuration logic depends on the timing for the SPI Flash device. Without examining the timing for a specific SPI Flash PROM, use ***ConfigRate*** = 12 or lower. SPI Flash PROMs that support the FAST READ command support higher data rates. Some such PROMs support up to ***ConfigRate*** = 25 and beyond but require careful data sheet analysis. See Serial Peripheral Interface (SPI) Configuration Timing for more detailed timing analysis.

Using the SPI Flash Interface after Configuration

After the FPGA successfully completes configuration, all of the pins connected to the SPI Flash PROM are available as user-I/O pins.

If not using the SPI Flash PROM after configuration, drive CSO_B High to disable the PROM. The MOSI, DIN, and CCLK pins are then available to the FPGA application.

Because all the interface pins are user I/O after configuration, the FPGA application can continue to use the SPI Flash interface pins to communicate with the SPI Flash PROM, as shown in Figure 56. SPI Flash PROMs offer random-accessible, byte-addressable, read/write, non-volatile storage to the FPGA application.

SPI Flash PROMs are available in densities ranging from 1 Mbit up to 128 Mbits. However, a single Spartan-3E FPGA requires less than 6 Mbits. If desired, use a larger SPI Flash PROM to contain additional non-volatile application data, such as MicroBlaze processor code, or other user data such as serial numbers and Ethernet MAC IDs. In the example shown in Figure 56, the FPGA configures from SPI Flash PROM. Then using FPGA logic after configuration, the FPGA copies MicroBlaze code from SPI Flash into external DDR SDRAM for code execution. Similarly, the FPGA application can store non-volatile application data within the SPI Flash PROM.

The FPGA configuration data is stored starting at location 0. Store any additional data beginning in the next available SPI Flash PROM sector or page. Do not mix configuration data and user data in the same sector or page.

Similarly, the SPI bus can be expanded to additional SPI peripherals. Because SPI is a common industry-standard interface, various SPI-based peripherals are available, such as analog-to-digital (A/D) converters, digital-to-analog (D/A) converters, CAN controllers, and temperature sensors. However, if sufficient I/O pins are available in the application, Xilinx recommends creating a separate SPI bus to control peripherals. Creating a second port reduces the loading on the CCLK and DIN pins, which are crucial for configuration.

The MOSI, DIN, and CCLK pins are common to all SPI peripherals. Connect the select input on each additional SPI peripheral to one of the FPGA user I/O pins. If HSWAP = 0 during configuration, the FPGA holds the select line High. If HSWAP = 1, connect the select line to +3.3V via an external 4.7 kΩ pull-up resistor to avoid spurious read or write operations. After configuration, drive the select line Low to select the desired SPI peripheral.

Daisy-Chaining

If the application requires multiple FPGAs with different configurations, then configure the FPGAs using a daisy chain, as shown in Figure 57. Daisy-chaining from a single SPI serial Flash PROM is supported in Stepping 1 devices. It is not supported in Stepping 0 devices. Use SPI Flash mode (M[2:0] = <0:0:1>) for the FPGA connected to the Platform Flash PROM and Slave Serial mode (M[2:0] = <1:1:1>) for all other FPGAs in the daisy-chain. After the master FPGA—the FPGA on the left in the diagram—finishes loading its configuration data from the SPI Flash PROM, the master device uses its DOUT output pin to supply data to the next device in the daisy-chain, on the falling CCLK edge.

Design Note

SPI mode daisy chains are supported only in Stepping 1 silicon versions.

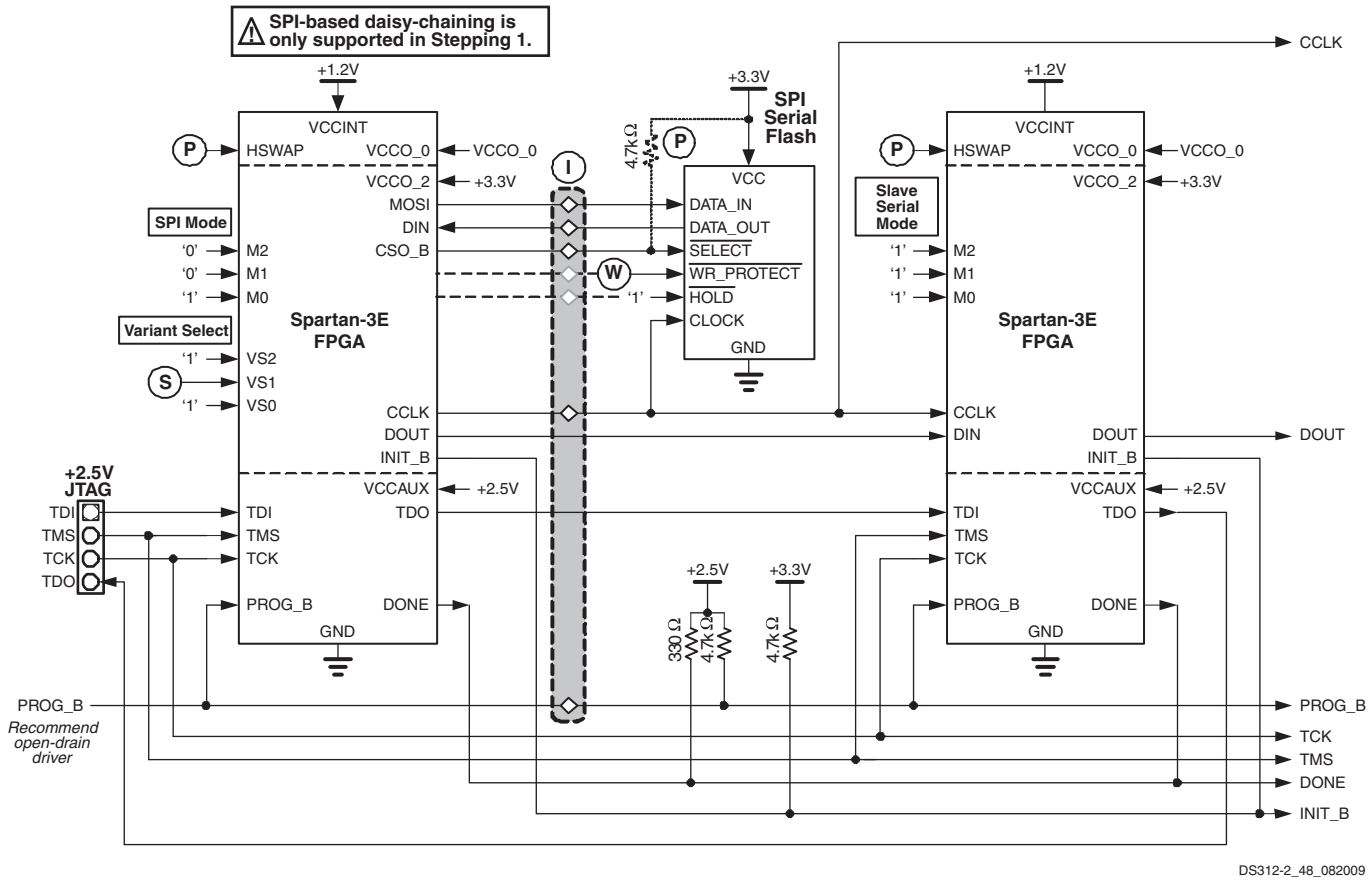


Figure 57: **Daisy-Chaining from SPI Flash Mode (Stepping 1)**

Programming Support

For successful daisy-chaining, the ***DONE_cycle*** configuration option must be set to cycle 5 or sooner. The default cycle is 4. See Table 69 and the Start-Up section for additional information.

(I) In production applications, the SPI Flash PROM is usually pre-programmed before it is mounted on the printed circuit board. The Xilinx ISE development software produces industry-standard programming files that can be used with third-party gang programmers. Consult your specific SPI Flash vendor for recommended production programming solutions.

In-system programming support is available from some third-party PROM programmers using a socket adapter with attached wires. To gain access to the SPI Flash signals, drive the FPGA's PROG_B input Low with an open-drain driver. This action places all FPGA I/O pins, including those attached to the SPI Flash, in high-impedance (Hi-Z). If the HSWAP input is Low, the I/Os have pull-up resistors to the V_{CCO} input on their respective I/O bank. The external programming hardware then has direct access to the SPI Flash pins. The programming access points are highlighted in the gray box in Figure 53, Figure 54, and Figure 57.

Beginning with the Xilinx ISE 8.2i software release, the iMPACT programming utility provides direct, in-system prototype programming support for STMicro M25P-series

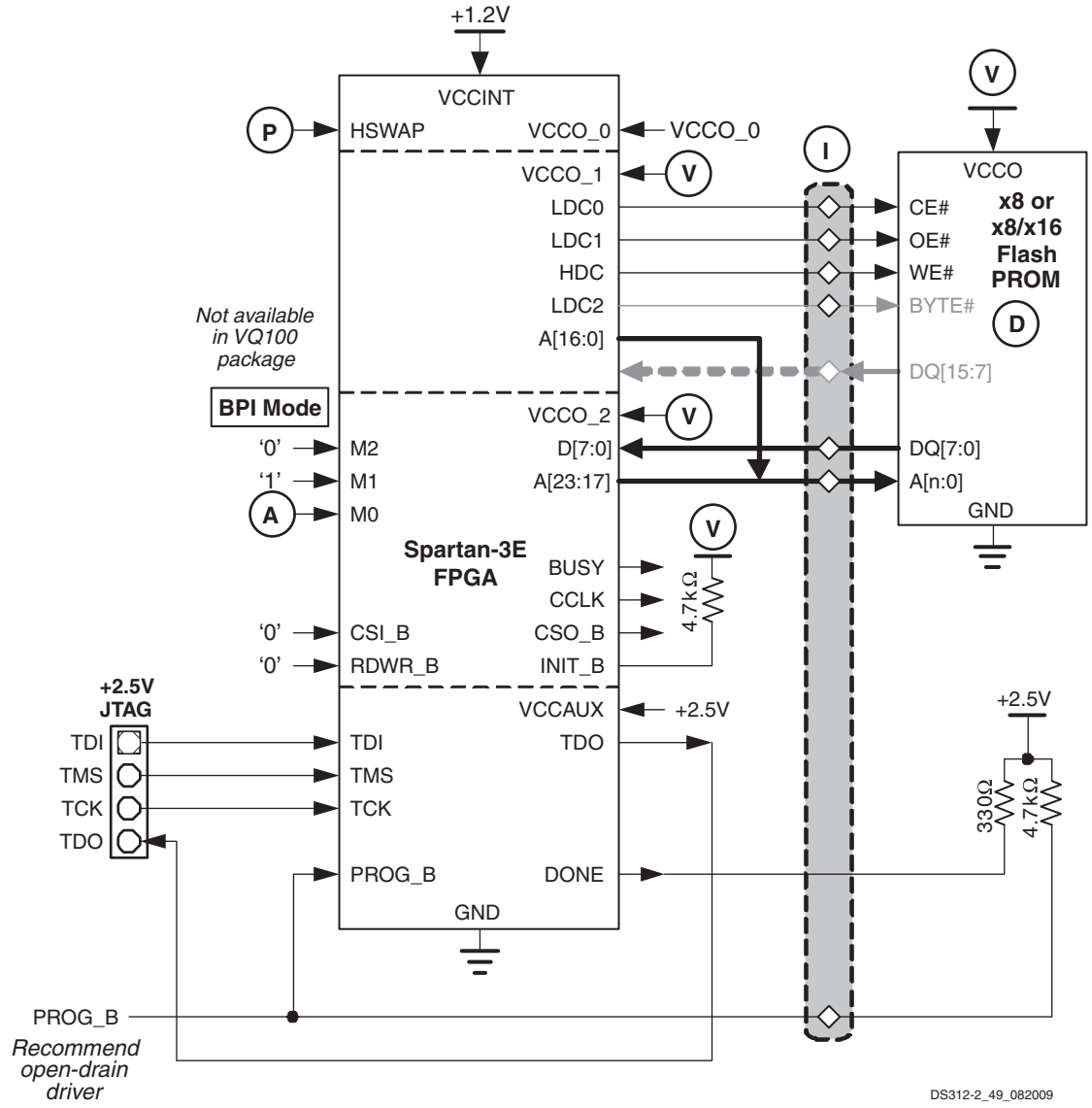


Figure 58: **Byte-wide Peripheral Interface (BPI) Mode Configured from Parallel NOR Flash PROMs**

(A) During configuration, the value of the M0 mode pin determines how the FPGA generates addresses, as shown Table 58. When M0 = 0, the FPGA generates addresses starting at 0 and increments the address on every falling CCLK edge. Conversely, when M0 = 1, the FPGA generates addresses starting at `0xFF_FFFF` (all ones) and decrements the address on every falling CCLK edge.

Table 58: **BPI Addressing Control**

M2	M1	M0	Start Address	Addressing
0	1	0	0	Incrementing
		1	`0xFF_FFFF`	Decrementing

Voltage Regulators

Various power supply manufacturers offer complete power solutions for Xilinx FPGAs including some with integrated three-rail regulators specifically designed for Spartan-3 and Spartan-3E FPGAs. The Xilinx Power Corner website provides links to vendor solution guides and Xilinx power estimation and analysis tools.

Power Distribution System (PDS) Design and Decoupling/Bypass Capacitors

Good power distribution system (PDS) design is important for all FPGA designs, but especially so for high performance applications, greater than 100 MHz. Proper design results in better overall performance, lower clock and DCM jitter, and a generally more robust system. Before designing the printed circuit board (PCB) for the FPGA design, please review XAPP623: *Power Distribution System (PDS) Design: Using Bypass/Decoupling Capacitors*.

Power-On Behavior

For additional power-on behavior information, including I/O behavior before and during configuration, refer to the "Sequence of Events" chapter in UG332.

Spartan-3E FPGAs have a built-in Power-On Reset (POR) circuit that monitors the three power rails required to successfully configure the FPGA. At power-up, the POR circuit holds the FPGA in a reset state until the V_{CCINT}, V_{CCAUX}, and V_{CCO} Bank 2 supplies reach their respective input threshold levels (see Table 74 in Module 3). After all three supplies reach their respective thresholds, the POR reset is released and the FPGA begins its configuration process.

Supply Sequencing

Because the three FPGA supply inputs must be valid to release the POR reset and can be supplied in any order, there are no FPGA-specific voltage sequencing requirements. Applying the FPGA's V_{CCAUX} supply before the V_{CCINT} supply uses the least I_{CCINT} current.

Although the FPGA has no specific voltage sequence requirements, be sure to consider any potential sequencing requirement of the configuration device attached to the FPGA, such as an SPI serial Flash PROM, a parallel NOR Flash PROM, or a microcontroller. For example, Flash PROMs have a minimum time requirement before the PROM can be selected and this must be considered if the 3.3V supply is the last in the sequence. See Power-On Precautions if 3.3V Supply is Last in Sequence for more details.

When all three supplies are valid, the minimum current required to power-on the FPGA equals the worst-case quiescent current, specified in Table 79. Spartan-3E FPGAs do not require Power-On Surge (POS) current to successfully configure.

Surplus I_{CCINT} if V_{CCINT} Applied before V_{CCAUX}

If the V_{CCINT} supply is applied before the V_{CCAUX} supply, the FPGA might draw a surplus I_{CCINT} current in addition to the I_{CCINT} quiescent current levels specified in Table 79, page 118. The momentary additional I_{CCINT} surplus current might be a few hundred milliamperes under nominal conditions, significantly less than the instantaneous current consumed by the bypass capacitors at power-on. However, the surplus current immediately disappears when the V_{CCAUX} supply is applied, and, in response, the FPGA's I_{CCINT} quiescent current demand drops to the levels specified in Table 79. The FPGA does not use or require the surplus current to successfully power-on and configure. If applying V_{CCINT} before V_{CCAUX}, ensure that the regulator does not have a foldback feature that could inadvertently shut down in the presence of the surplus current.

Configuration Data Retention, Brown-Out

The FPGA's configuration data is stored in robust CMOS configuration latches. The data in these latches is retained even when the voltages drop to the minimum levels necessary to preserve RAM contents, as specified in Table 76.

If, after configuration, the V_{CCAUX} or V_{CCINT} supply drops below its data retention voltage, the current device configuration must be cleared using one of the following methods:

- Force the V_{CCAUX} or V_{CCINT} supply voltage below the minimum Power On Reset (POR) voltage threshold (Table 74).
- Assert PROG_B Low.

The POR circuit does not monitor the VCCO_2 supply after configuration. Consequently, dropping the VCCO_2 voltage does not reset the device by triggering a Power-On Reset (POR) event.

No Internal Charge Pumps or Free-Running Oscillators

Some system applications are sensitive to sources of analog noise. Spartan-3E FPGA circuitry is fully static and does not employ internal charge pumps.

The CCLK configuration clock is active during the FPGA configuration process. After configuration completes, the CCLK oscillator is automatically disabled unless the Bitstream Generator (BitGen) option ***Persist=Yes***.

General Recommended Operating Conditions

Table 77: **General Recommended Operating Conditions**

Symbol	Description			Min	Nominal	Max	Units
T_J	Junction temperature	Commercial		0	–	85	°C
		Industrial		–40	–	100	°C
V_{CCINT}	Internal supply voltage			1.140	1.200	1.260	V
V_{CCO} (1)	Output driver supply voltage			1.100	-	3.465	V
V_{CCAUX}	Auxiliary supply voltage			2.375	2.500	2.625	V
V_{IN} (2,3)	Input voltage extremes to avoid turning on I/O protection diodes	I/O, Input-only, and Dual-Purpose pins (4)	IP or IO_#	–0.5	–	V_{CCO} + 0.5	V
			IO_Lxxy_# (5)	–0.5	–	V_{CCO} + 0.5	V
		Dedicated pins (6)		–0.5	–	V_{CCAUX} + 0.5	V
T_{IN}	Input signal transition time (7)			–	–	500	ns

Notes:

1. This V_{CCO} range spans the lowest and highest operating voltages for all supported I/O standards. Table 80 lists the recommended V_{CCO} range specific to each of the single-ended I/O standards, and Table 82 lists that specific to the differential standards.
2. Input voltages outside the recommended range require the I_{IK} input clamp diode rating is met and no more than 100 pins exceed the range simultaneously. Refer to Table 73.
3. See XAPP459: *Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins on Spartan-3 Families*.
4. Each of the User I/O and Dual-Purpose pins is associated with one of the four banks' V_{CCO} rails. Meeting the V_{IN} limit ensures that the internal diode junctions that exist between these pins and their associated V_{CCO} and GND rails do not turn on. The absolute maximum rating is provided in Table 73.
5. For single-ended signals that are placed on a differential-capable I/O, V_{IN} of –0.2V to –0.5V is supported but can cause increased leakage between the two pins. See *Parasitic Leakage* in UG331, *Spartan-3 Generation FPGA User Guide*.
6. All Dedicated pins (PROG_B, DONE, TCK, TDI, TDO, and TMS) draw power from the V_{CCAUX} rail (2.5V). Meeting the V_{IN} max limit ensures that the internal diode junctions that exist between each of these pins and the V_{CCAUX} and GND rails do not turn on.
7. Measured between 10% and 90% V_{CCO}. Follow Signal Integrity recommendations.

18 x 18 Embedded Multiplier Timing

Table 102: **18 x 18 Embedded Multiplier Timing**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Combinatorial Delay						
T_{MULT}	Combinatorial multiplier propagation delay from the A and B inputs to the P outputs, assuming 18-bit inputs and a 36-bit product (AREG, BREG, and PREG registers unused)	-	4.34(1)	-	4.88(1)	ns
Clock-to-Output Times						
T_{MSCKP_P}	Clock-to-output delay from the active transition of the CLK input to valid data appearing on the P outputs when using the PREG register(2)	-	0.98	-	1.10	ns
T_{MSCKP_A} T_{MSCKP_B}	Clock-to-output delay from the active transition of the CLK input to valid data appearing on the P outputs when using either the AREG or BREG register(3)	-	4.42	-	4.97	ns
Setup Times						
T_{MSDCK_P}	Data setup time at the A or B input before the active transition at the CLK when using only the PREG output register (AREG, BREG registers unused)(2)	3.54	-	3.98	-	ns
T_{MSDCK_A}	Data setup time at the A input before the active transition at the CLK when using the AREG input register(3)	0.20	-	0.23	-	ns
T_{MSDCK_B}	Data setup time at the B input before the active transition at the CLK when using the BREG input register(3)	0.35	-	0.39	-	ns
Hold Times						
T_{MSCKD_P}	Data hold time at the A or B input after the active transition at the CLK when using only the PREG output register (AREG, BREG registers unused)(2)	–0.97	-	–0.97	-	ns
T_{MSCKD_A}	Data hold time at the A input after the active transition at the CLK when using the AREG input register(3)	0.03	-	0.04	-	ns
T_{MSCKD_B}	Data hold time at the B input after the active transition at the CLK when using the BREG input register(3)	0.04	-	0.05	-	ns
Clock Frequency						
F_{MULT}	Internal operating frequency for a two-stage 18x18 multiplier using the AREG and BREG input registers and the PREG output register(1)	0	270	0	240	MHz

Notes:

1. Combinatorial delay is less and pipelined performance is higher when multiplying input data with less than 18 bits.
2. The PREG register is typically used in both single-stage and two-stage pipelined multiplier implementations.
3. Input registers AREG or BREG are typically used when inferring a two-stage multiplier.

Table 105: **Switching Characteristics for the DLL**

Symbol	Description		Device	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Output Frequency Ranges								
CLKOUT_FREQ_CLK0	Frequency for the CLK0 and CLK180 outputs	Stepping 0	XC3S100E XC3S250E XC3S500E XC3S1600E	N/A	N/A	5	90	MHz
			XC3S1200E				200	MHz
		Stepping 1	All	5	275		240	MHz
CLKOUT_FREQ_CLK90	Frequency for the CLK90 and CLK270 outputs	Stepping 0	XC3S100E XC3S250E XC3S500E XC3S1600E	N/A	N/A	5	90	MHz
			XC3S1200E				167	MHz
		Stepping 1	All	5	200		200	MHz
CLKOUT_FREQ_2X	Frequency for the CLK2X and CLK2X180 outputs	Stepping 0	XC3S100E XC3S250E XC3S500E XC3S1600E	N/A	N/A	10	180	MHz
			XC3S1200E				311	MHz
		Stepping 1	All	10	333		311	MHz
CLKOUT_FREQ_DV	Frequency for the CLKDV output	Stepping 0	XC3S100E XC3S250E XC3S500E XC3S1600E	N/A	N/A	0.3125	60	MHz
			XC3S1200E				133	MHz
		Stepping 1	All	0.3125	183		160	MHz
Output Clock Jitter(2,3,4)								
CLKOUT_PER_JITT_0	Period jitter at the CLK0 output		All	-	±100	-	±100	ps
CLKOUT_PER_JITT_90	Period jitter at the CLK90 output			-	±150	-	±150	ps
CLKOUT_PER_JITT_180	Period jitter at the CLK180 output			-	±150	-	±150	ps
CLKOUT_PER_JITT_270	Period jitter at the CLK270 output			-	±150	-	±150	ps
CLKOUT_PER_JITT_2X	Period jitter at the CLK2X and CLK2X180 outputs			-	±[1% of CLKIN period + 150]	-	±[1% of CLKIN period + 150]	ps
CLKOUT_PER_JITT_DV1	Period jitter at the CLKDV output when performing integer division			-	±150	-	±150	ps
CLKOUT_PER_JITT_DV2	Period jitter at the CLKDV output when performing non-integer division			-	±[1% of CLKIN period + 200]	-	±[1% of CLKIN period + 200]	ps
Duty Cycle(4)								
CLKOUT_DUTY_CYCLE_DLL	Duty cycle variation for the CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV outputs, including the BUFGMUX and clock tree duty-cycle distortion		All	-	±[1% of CLKIN period + 400]	-	±[1% of CLKIN period + 400]	ps

VQ100 Footprint

In Figure 80, note pin 1 indicator in top-left corner and logo orientation.

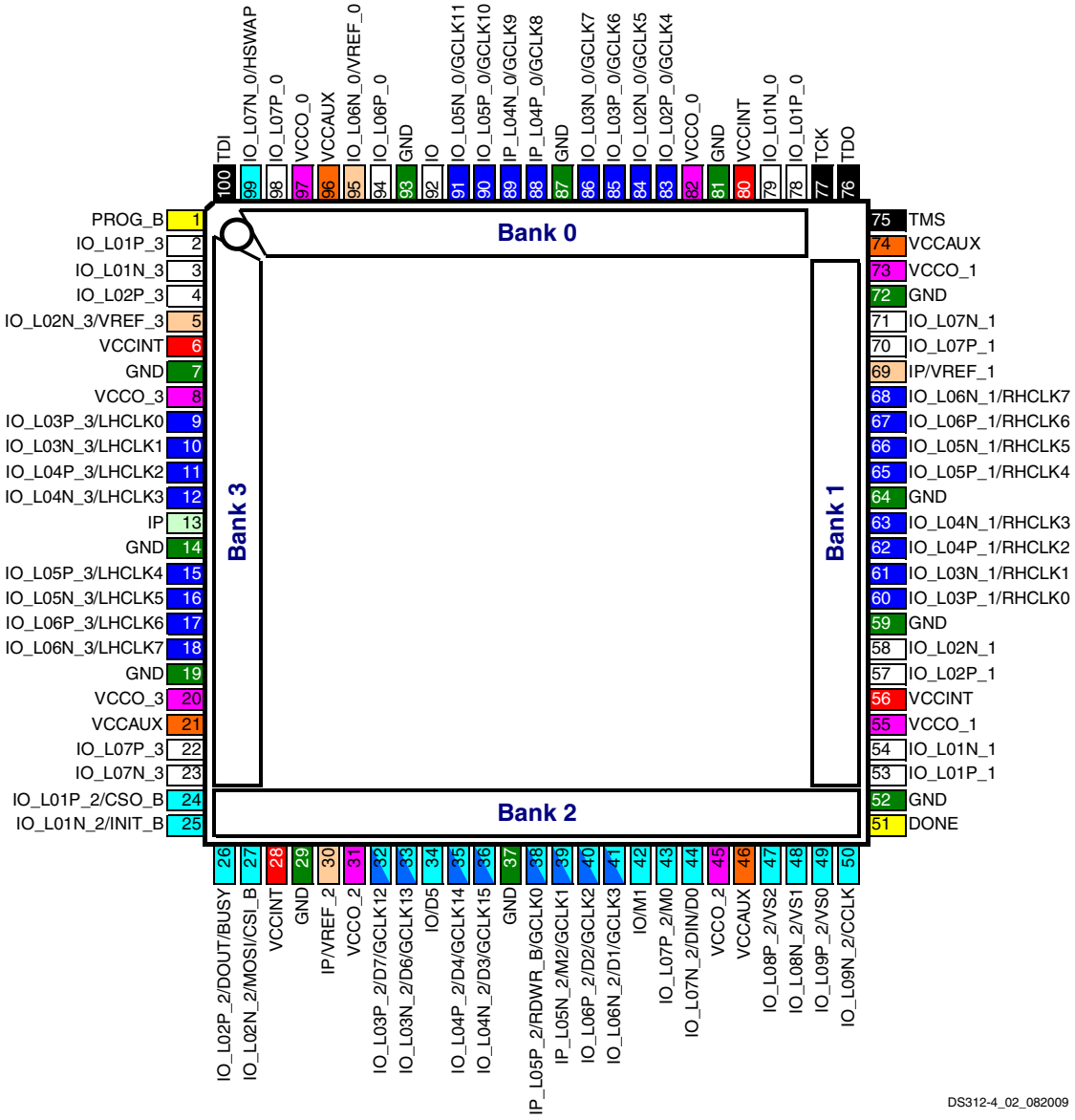


Figure 80: **VQ100 Package Footprint (top view)**

16	**I/O:** Unrestricted, general-purpose user I/O	21	**DUAL:** Configuration pin, then possible user-I/O	4	**VREF:** User I/O or input voltage reference for bank
1	**INPUT:** Unrestricted, general-purpose input pin	24	**CLK:** User I/O, input, or global buffer input	8	**VCCO:** Output voltage supply for bank
2	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	4	**VCCINT:** Internal core supply voltage (+1.2V)
0	**N.C.:** Not connected	12	**GND:** Ground	4	**VCCAUX:** Auxiliary supply voltage (+2.5V)

Footprint Migration Differences

Table 136 summarizes any footprint and functionality differences between the XC3S100E, the XC3S250E, and the XC3S500E FPGAs that may affect easy migration between devices in the CP132 package. There are 14 such balls. All other pins not listed in Table 136 unconditionally migrate between Spartan-3E devices available in the CP132 package.

The XC3S100E is duplicated on both the left and right sides of the table to show migrations to and from the XC3S250E and the XC3S500E. The arrows indicate the direction for easy migration. A double-ended arrow (←→) indicates that the two pins have identical functionality. A left-facing arrow (←) indicates that the pin on the device on the right unconditionally migrates to the pin on the device on the left. It may be possible to migrate the opposite direction depending on the I/O configuration. For example, an I/O pin (Type = I/O) can migrate to an input-only pin (Type = INPUT) if the I/O pin is configured as an input.

The XC3S100E FPGA in the CP132 package has four fewer BPI-mode address lines than the XC3S250E and XC3S500E.

Table 136: **CP132 Footprint Migration Differences**

CP132 Ball	Bank	XC3S100E Type	Migration	XC3S250E Type	Migration	XC3S500E Type	Migration	XC3S100E Type
A12	0	N.C.	→	I/O	←→	I/O	←	N.C.
B4	0	INPUT	→	I/O	←→	I/O	←	INPUT
B11	0	N.C.	→	I/O	←→	I/O	←	N.C.
B12	0	N.C.	→	I/O	←→	I/O	←	N.C.
C4	0	N.C.	→	I/O	←→	I/O	←	N.C.
C11	0	INPUT	→	I/O	←→	I/O	←	INPUT
D1	3	N.C.	→	I/O	←→	I/O	←	N.C.
D2	3	I/O	→	I/O (Diff)	←→	I/O (Diff)	←	I/O
K3	3	VREF(INPUT)	→	VREF(I/O)	←→	VREF(I/O)	←	VREF(INPUT)
M9	2	N.C.	→	DUAL	←→	DUAL	←	N.C.
M10	2	N.C.	→	DUAL	←→	DUAL	←	N.C.
N9	2	N.C.	→	DUAL	←→	DUAL	←	N.C.
N10	2	N.C.	→	DUAL	←→	DUAL	←	N.C.
P11	2	VREF(INPUT)	→	VREF(I/O)	←→	VREF(I/O)	←	VREF(INPUT)
DIFFERENCES			**14**		**0**		**14**	

Legend:

←→ This pin is identical on the device on the left and the right.

→ This pin can unconditionally migrate from the device on the left to the device on the right. Migration in the other direction may be possible depending on how the pin is configured for the device on the right.

← This pin can unconditionally migrate from the device on the right to the device on the left. Migration in the other direction may be possible depending on how the pin is configured for the device on the left.

Table 143: **FT256 Package Pinout *(Cont'd)***

Bank	XC3S250E Pin Name	XC3S500E Pin Name	XC3S1200E Pin Name	FT256 Ball	Type
2	N.C. (◆)	IO_L14N_2/VREF_2	IO_L14N_2/VREF_2	R10	***250E:*** N.C. ***500E:*** VREF ***1200E:*** VREF
2	N.C. (◆)	IO_L14P_2	IO_L14P_2	P10	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O
2	IO_L15N_2	IO_L15N_2	IO_L15N_2	M10	I/O
2	IO_L15P_2	IO_L15P_2	IO_L15P_2	N10	I/O
2	IO_L16N_2/A22	IO_L16N_2/A22	IO_L16N_2/A22	P11	DUAL
2	IO_L16P_2/A23	IO_L16P_2/A23	IO_L16P_2/A23	R11	DUAL
2	IO_L18N_2/A20	IO_L18N_2/A20	IO_L18N_2/A20	N12	DUAL
2	IO_L18P_2/A21	IO_L18P_2/A21	IO_L18P_2/A21	P12	DUAL
2	IO_L19N_2/VS1/A18	IO_L19N_2/VS1/A18	IO_L19N_2/VS1/A18	R13	DUAL
2	IO_L19P_2/VS2/A19	IO_L19P_2/VS2/A19	IO_L19P_2/VS2/A19	T13	DUAL
2	IO_L20N_2/CCLK	IO_L20N_2/CCLK	IO_L20N_2/CCLK	R14	DUAL
2	IO_L20P_2/VS0/A17	IO_L20P_2/VS0/A17	IO_L20P_2/VS0/A17	P14	DUAL
2	IP	IP	IP	T2	INPUT
2	IP	IP	IP	T14	INPUT
2	IP_L02N_2	IP_L02N_2	IP_L02N_2	R3	INPUT
2	IP_L02P_2	IP_L02P_2	IP_L02P_2	T3	INPUT
2	IP_L08N_2/VREF_2	IP_L08N_2/VREF_2	IP_L08N_2/VREF_2	T7	VREF
2	IP_L08P_2	IP_L08P_2	IP_L08P_2	R7	INPUT
2	IP_L11N_2/M2/GCLK1	IP_L11N_2/M2/GCLK1	IP_L11N_2/M2/GCLK1	R9	DUAL/GCLK
2	IP_L11P_2/RDWR_B/ GCLK0	IP_L11P_2/RDWR_B/ GCLK0	IP_L11P_2/RDWR_B/ GCLK0	T9	DUAL/GCLK
2	IP_L17N_2	IP_L17N_2	IP_L17N_2	M11	INPUT
2	IP_L17P_2	IP_L17P_2	IP_L17P_2	N11	INPUT
2	VCCO_2	VCCO_2	VCCO_2	L7	VCCO
2	VCCO_2	VCCO_2	VCCO_2	L10	VCCO
2	VCCO_2	VCCO_2	VCCO_2	R5	VCCO
2	VCCO_2	VCCO_2	VCCO_2	R12	VCCO
3	IO_L01N_3	IO_L01N_3	IO_L01N_3	B2	I/O
3	IO_L01P_3	IO_L01P_3	IO_L01P_3	B1	I/O
3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	C2	VREF
3	IO_L02P_3	IO_L02P_3	IO_L02P_3	C1	I/O
3	IO_L03N_3	IO_L03N_3	IO_L03N_3	E4	I/O
3	IO_L03P_3	IO_L03P_3	IO_L03P_3	E3	I/O
3	N.C. (◆)	IO_L04N_3/VREF_3	IO_L04N_3/VREF_3	F4	***250E:*** N.C. ***500E:*** VREF ***1200E:*** VREF
3	N.C. (◆)	IO_L04P_3	IO_L04P_3	F3	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O
3	IO_L05N_3	IO_L05N_3	IO_L05N_3	E1	I/O
3	IO_L05P_3	IO_L05P_3	IO_L05P_3	D1	I/O
3	IO_L06N_3	IO_L06N_3	IO_L06N_3	G4	I/O