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Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Active
Number of LABs/CLBs	2168
Number of Logic Elements/Cells	19512
Total RAM Bits	516096
Number of I/O	190
Number of Gates	1200000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s1200e-4ftg256c

Architectural Overview

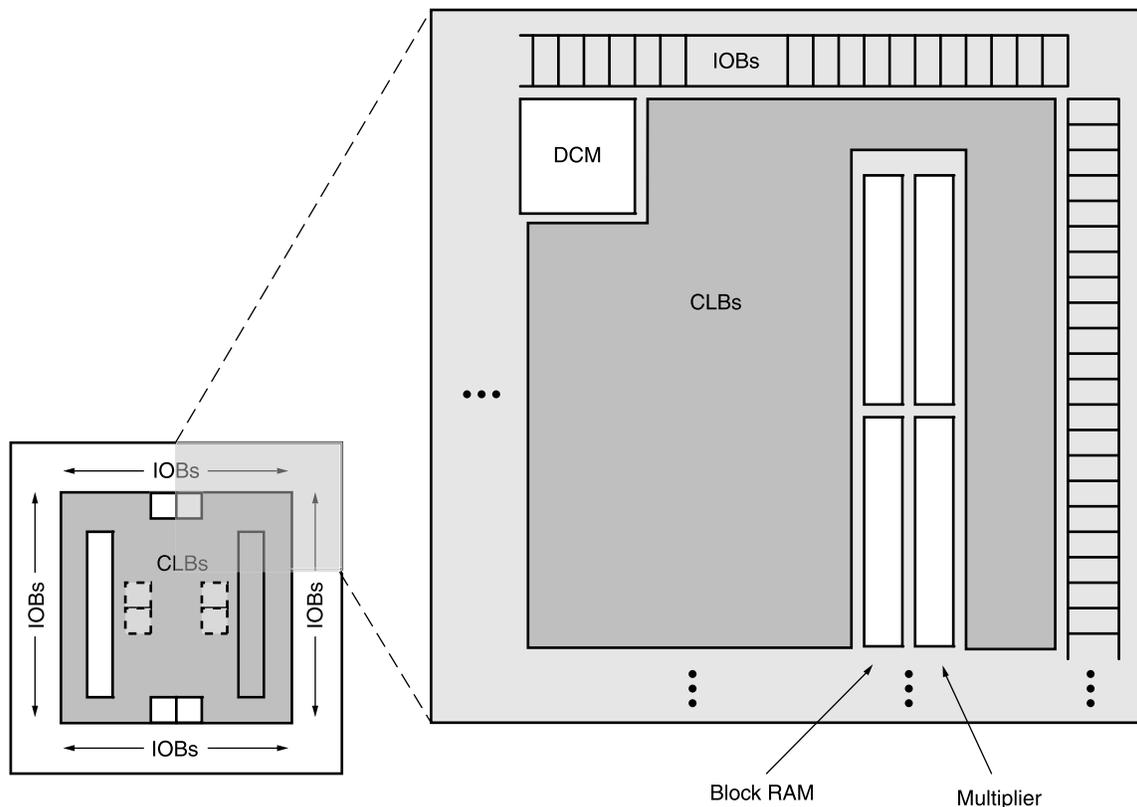
The Spartan-3E family architecture consists of five fundamental programmable functional elements:

- **Configurable Logic Blocks (CLBs)** contain flexible Look-Up Tables (LUTs) that implement logic plus storage elements used as flip-flops or latches. CLBs perform a wide variety of logical functions as well as store data.
- **Input/Output Blocks (IOBs)** control the flow of data between the I/O pins and the internal logic of the device. Each IOB supports bidirectional data flow plus 3-state operation. Supports a variety of signal standards, including four high-performance differential standards. Double Data-Rate (DDR) registers are included.
- **Block RAM** provides data storage in the form of 18-Kbit dual-port blocks.
- **Multiplier Blocks** accept two 18-bit binary numbers as inputs and calculate the product.

- **Digital Clock Manager (DCM) Blocks** provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase-shifting clock signals.

These elements are organized as shown in Figure 1. A ring of IOBs surrounds a regular array of CLBs. Each device has two columns of block RAM except for the XC3S100E, which has one column. Each RAM column consists of several 18-Kbit RAM blocks. Each block RAM is associated with a dedicated multiplier. The DCMs are positioned in the center with two at the top and two at the bottom of the device. The XC3S100E has only one DCM at the top and bottom, while the XC3S1200E and XC3S1600E add two DCMs in the middle of the left and right sides.

The Spartan-3E family features a rich network of traces that interconnect all five functional elements, transmitting signals among them. Each functional element has an associated switch matrix that permits multiple connections to the routing.



DS312_01_111904

Figure 1: Spartan-3E Family Architecture

Introduction

As described in [Architectural Overview](#), the Spartan-3E FPGA architecture consists of five fundamental functional elements:

- [Input/Output Blocks \(IOBs\)](#)
- [Configurable Logic Block \(CLB\) and Slice Resources](#)
- [Block RAM](#)
- [Dedicated Multipliers](#)
- [Digital Clock Managers \(DCMs\)](#)

The following sections provide detailed information on each of these functions. In addition, this section also describes the following functions:

- [Clocking Infrastructure](#)
- [Interconnect](#)
- [Configuration](#)
- [Powering Spartan-3E FPGAs](#)

Input/Output Blocks (IOBs)

For additional information, refer to the “Using I/O Resources” chapter in [UG331](#).

IOB Overview

The Input/Output Block (IOB) provides a programmable, unidirectional or bidirectional interface between a package pin and the FPGA’s internal logic. The IOB is similar to that of the Spartan-3 family with the following differences:

- Input-only blocks are added
- Programmable input delays are added to all blocks
- DDR flip-flops can be shared between adjacent IOBs

The unidirectional input-only block has a subset of the full IOB capabilities. Thus there are no connections or logic for an output path. The following paragraphs assume that any reference to output functionality does not apply to the input-only blocks. The number of input-only blocks varies with device size, but is never more than 25% of the total IOB count.

[Figure 5](#) is a simplified diagram of the IOB’s internal structure. There are three main signal paths within the IOB: the output path, input path, and 3-state path. Each path has its own pair of storage elements that can act as either registers or latches. For more information, see [Storage Element Functions](#). The three main signal paths are as follows:

- The input path carries data from the pad, which is bonded to a package pin, through an optional programmable delay element directly to the I line. After the delay element, there are alternate routes through a

pair of storage elements to the IQ1 and IQ2 lines. The IOB outputs I, IQ1, and IQ2 lead to the FPGA’s internal logic. The delay element can be set to ensure a hold time of zero (see [Input Delay Functions](#)).

- The output path, starting with the O1 and O2 lines, carries data from the FPGA’s internal logic through a multiplexer and then a three-state driver to the IOB pad. In addition to this direct path, the multiplexer provides the option to insert a pair of storage elements.
- The 3-state path determines when the output driver is high impedance. The T1 and T2 lines carry data from the FPGA’s internal logic through a multiplexer to the output driver. In addition to this direct path, the multiplexer provides the option to insert a pair of storage elements.
- All signal paths entering the IOB, including those associated with the storage elements, have an inverter option. Any inverter placed on these paths is automatically absorbed into the IOB.

Initialization

The CLB storage elements are initialized at power-up, during configuration, by the global GSR signal, and by the individual SR or REV inputs to the CLB. The storage elements can also be re-initialized using the GSR input on the STARTUP_SPARTAN3E primitive. See [Global Controls \(STARTUP_SPARTAN3E\)](#).

Table 17: Slice Storage Element Initialization

Signal	Description
SR	Set/Reset input. Forces the storage element into the state specified by the attribute SRHIGH or SRLOW. SRHIGH forces a logic 1 when SR is asserted. SRLOW forces a logic 0. For each slice, set and reset can be set to be synchronous or asynchronous.
REV	Reverse of Set/Reset input. A second input (BY) forces the storage element into the opposite state. The reset condition is predominant over the set condition if both are active. Same synchronous/asynchronous setting as for SR.
GSR	Global Set/Reset. GSR defaults to active High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN3E element. The initial state after configuration or GSR is defined by a separate INIT0 and INIT1 attribute. By default, setting the SRLOW attribute sets INIT0, and setting the SRHIGH attribute sets INIT1.

Distributed RAM

For additional information, refer to the “Using Look-Up Tables as Distributed RAM” chapter in [UG331](#).

The LUTs in the SLICEM can be programmed as distributed RAM. This type of memory affords moderate amounts of data buffering anywhere along a data path. One SLICEM LUT stores 16 bits (RAM16). The four LUT inputs F[4:1] or G[4:1] become the address lines labeled A[4:1] in the device model and A[3:0] in the design components, providing a 16x1 configuration in one LUT. Multiple SLICEM LUTs can be combined in various ways to store larger amounts of data, including 16x4, 32x2, or 64x1 configurations in one CLB. The fifth and sixth address lines required for the 32-deep and 64-deep configurations, respectively, are implemented using the BX and BY inputs, which connect to the write enable logic for writing and the F5MUX and F6MUX for reading.

Writing to distributed RAM is always synchronous to the SLICEM clock (WCLK for distributed RAM) and enabled by the SLICEM SR input which functions as the active-High Write Enable (WE). The read operation is asynchronous, and, therefore, during a write, the output initially reflects the old data at the address being written.

The distributed RAM outputs can be captured using the flip-flops within the SLICEM element. The WE write-enable control for the RAM and the CE clock-enable control for the flip-flop are independent, but the WCLK and CLK clock inputs are shared. Because the RAM read operation is asynchronous, the output data always reflects the currently addressed RAM location.

A dual-port option combines two LUTs so that memory access is possible from two independent data lines. The same data is written to both 16x1 memories but they have independent read address lines and outputs. The dual-port function is implemented by cascading the G-LUT address lines, which are used for both read and write, to the F-LUT write address lines (WF[4:1] in [Figure 15](#)), and by cascading the G-LUT data input D1 through the DIF_MUX in [Figure 15](#) and to the D1 input on the F-LUT. One CLB provides a 16x1 dual-port memory as shown in [Figure 26](#).

Any write operation on the D input and any read operation on the SPO output can occur simultaneously with and independently from a read operation on the second read-only port, DPO.

Delay-Locked Loop (DLL)

The most basic function of the DLL component is to eliminate clock skew. The main signal path of the DLL consists of an input stage, followed by a series of discrete delay elements or *steps*, which in turn leads to an output stage. This path together with logic for phase detection and control forms a system complete with feedback as shown in Figure 41. In Spartan-3E FPGAs, the DLL is implemented using a counter-based delay line.

The DLL component has two clock inputs, CLKIN and CLKFB, as well as seven clock outputs, CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV as described in Table 28. The clock outputs drive simultaneously. Signals that initialize and report the state of the DLL are discussed in Status Logic.

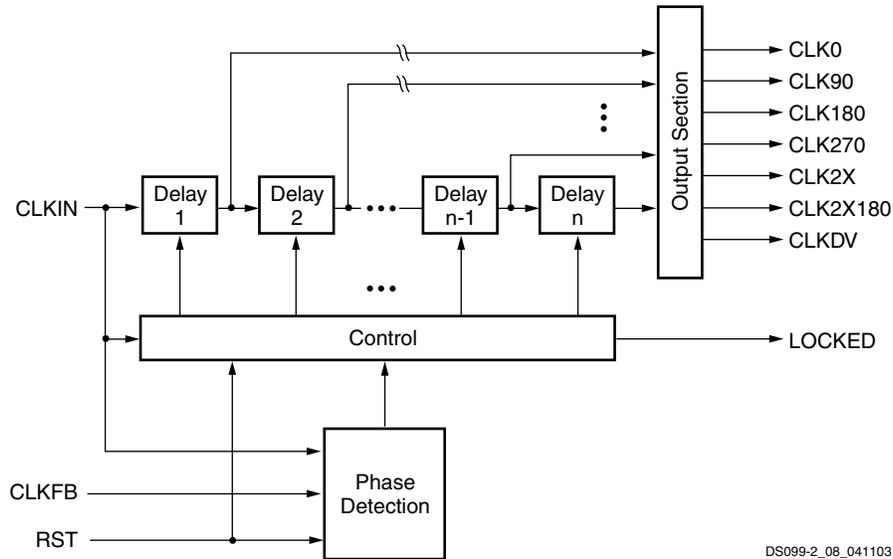


Figure 41: Simplified Functional Diagram of DLL

Table 28: DLL Signals

Signal	Direction	Description
CLKIN	Input	Receives the incoming clock signal. See Table 30, Table 31, and Table 32 for optimal external inputs to a DCM.
CLKFB	Input	Accepts either CLK0 or CLK2X as the feedback signal. (Set the CLK_FEEDBACK attribute accordingly).
CLK0	Output	Generates a clock signal with the same frequency and phase as CLKIN.
CLK90	Output	Generates a clock signal with the same frequency as CLKIN, phase-shifted by 90°.
CLK180	Output	Generates a clock signal with the same frequency as CLKIN, phase-shifted by 180°.
CLK270	Output	Generates a clock signal with the same frequency as CLKIN, phase-shifted by 270°.
CLK2X	Output	Generates a clock signal with the same phase as CLKIN, and twice the frequency.
CLK2X180	Output	Generates a clock signal with twice the frequency of CLKIN, and phase-shifted 180° with respect to CLK2X.
CLKDV	Output	Divides the CLKIN frequency by CLKDV_DIVIDE value to generate lower frequency clock signal that is phase-aligned to CLKIN.

The clock signal supplied to the CLKIN input serves as a reference waveform. The DLL seeks to align the rising-edge of feedback signal at the CLKFB input with the rising-edge of CLKIN input. When eliminating clock skew, the common approach to using the DLL is as follows: The CLK0 signal is passed through the clock distribution network that feeds all the registers it synchronizes. These registers are either

internal or external to the FPGA. After passing through the clock distribution network, the clock signal returns to the DLL via a feedback line called CLKFB. The control block inside the DLL measures the phase error between CLKFB and CLKIN. This phase error is a measure of the clock skew that the clock distribution network introduces. The control block activates the appropriate number of delay steps to

VARIABLE Phase Shift Mode

In VARIABLE phase shift mode, the FPGA application dynamically adjusts the fine phase shift value using three

inputs to the PS unit (PSEN, PSCLK, and PSINCDEC), as defined in Table 36 and shown in Figure 40.

Table 36: Signals for Variable Phase Mode

Signal	Direction	Description
PSEN ⁽¹⁾	Input	Enables the Phase Shift unit for variable phase adjustment.
PSCLK ⁽¹⁾	Input	Clock to synchronize phase shift adjustment.
PSINCDEC ⁽¹⁾	Input	When High, increments the current phase shift value. When Low, decrements the current phase shift value. This signal is synchronized to the PSCLK signal.
PSDONE	Output	Goes High to indicate that the present phase adjustment is complete and PS unit is ready for next phase adjustment request. This signal is synchronized to the PSCLK signal.

Notes:

- This input supports either a true or inverted polarity.

The FPGA application uses the three PS inputs on the Phase Shift unit to dynamically and incrementally increase or decrease the phase shift amount on all nine DCM clock outputs.

To adjust the current phase shift value, the PSEN enable signal must be High to enable the PS unit. Coincidentally, PSINCDEC must be High to increment the current phase shift amount or Low to decrement the current amount. All VARIABLE phase shift operations are controlled by the PSCLK input, which can be the CLKIN signal or any other clock signal.

Design Note

The VARIABLE phase shift feature operates differently from the Spartan-3 DCM; use the DCM_SP primitive, not the DCM primitive.

DCM_DELAY_STEP

DCM_DELAY_STEP is the finest delay resolution available in the PS unit. Its value is provided at the bottom of Table 105 in Module 3. For each enabled PSCLK cycle that PSINCDEC is High, the PS unit adds one DCM_DELAY_STEP of phase shift to all nine DCM outputs. Similarly, for each enabled PSCLK cycle that PSINCDEC is Low, the PS unit subtracts one DCM_DELAY_STEP of phase shift from all nine DCM outputs.

Because each DCM_DELAY_STEP has a minimum and maximum value, the actual phase shift delay for the present phase increment/decrement value (VALUE) falls within the minimum and maximum values according to Equation 4 and Equation 5.

$$T_{PS}(Max) = VALUE \cdot DCM_DELAY_STEP_MAX \quad Eq\ 4$$

$$T_{PS}(Min) = VALUE \cdot DCM_DELAY_STEP_MIN \quad Eq\ 5$$

The maximum variable phase shift steps, MAX_STEPS, is described in Equation 6 or Equation 7, for a given CLKIN input period, T_{CLKIN} , in nanoseconds. To convert this to a

phase shift range measured in time and not steps, use MAX_STEPS derived in Equation 6 and Equation 7 for VALUE in Equation 4 and Equation 5.

If $CLKIN < 60$ MHz:

$$MAX_STEPS = \pm [INTEGER(10 \cdot (T_{CLKIN} - 3))] \quad Eq\ 6$$

If $CLKIN \geq 60$ MHz:

$$MAX_STEPS = \pm [INTEGER(15 \cdot (T_{CLKIN} - 3))] \quad Eq\ 7$$

The phase adjustment might require as many as 100 CLKIN cycles plus 3 PSCLK cycles to take effect, at which point the DCM's PSDONE output goes High for one PSCLK cycle. This pulse indicates that the PS unit completed the previous adjustment and is now ready for the next request.

Asserting the Reset (RST) input returns the phase shift to zero.

Clocking Infrastructure

For additional information, refer to the “Using Global Clock Resources” chapter in [UG331](#).

The Spartan-3E clocking infrastructure, shown in [Figure 45](#), provides a series of low-capacitance, low-skew interconnect lines well-suited to carrying high-frequency signals throughout the FPGA. The infrastructure also includes the clock inputs and BUFGMUX clock buffers/multiplexers. The Xilinx Place-and-Route (PAR) software automatically routes high-fanout clock signals using these resources.

Clock Inputs

Clock pins accept external clock signals and connect directly to DCMs and BUFGMUX elements. Each Spartan-3E FPGA has:

- 16 Global Clock inputs (GCLK0 through GCLK15) located along the top and bottom edges of the FPGA
- 8 Right-Half Clock inputs (RHCLK0 through RHCLK7) located along the right edge
- 8 Left-Half Clock inputs (LHCLK0 through LHCLK7) located along the left edge

Clock inputs optionally connect directly to DCMs using dedicated connections. [Table 30](#), [Table 31](#), and [Table 32](#) show the clock inputs that best feed a specific DCM within a given Spartan-3E part number. Different Spartan-3E FPGA densities have different numbers of DCMs. The XC3S1200E and XC3S1600E are the only two densities with the left- and right-edge DCMs.

Each clock input is also optionally a user-I/O pin and connects to internal interconnect. Some clock pad pins are input-only pins as indicated in Module 4, [Pinout Descriptions](#).

Design Note

Avoid using global clock input GCLK1 as it is always shared with the M2 mode select pin. Global clock inputs GCLK0, GCLK2, GCLK3, GCLK12, GCLK13, GCLK14, and GCLK15 have shared functionality in some configuration modes.

Clock Buffers/Multiplexers

Clock Buffers/Multiplexers either drive clock input signals directly onto a clock line (BUFG) or optionally provide a multiplexer to switch between two unrelated, possibly asynchronous clock signals (BUFGMUX).

Each BUFGMUX element, shown in [Figure 46](#), is a 2-to-1 multiplexer. The select line, S, chooses which of the two inputs, I0 or I1, drives the BUFGMUX’s output signal, O, as described in [Table 40](#). The switching from one clock to the other is glitch-less, and done in such a way that the output High and Low times are never shorter than the shortest

High or Low time of either input clock. The two clock inputs can be asynchronous with regard to each other, and the S input can change at any time, except for a short setup time prior to the rising edge of the presently selected clock (I0 or I1). This setup time is specified as TGS1 in [Table 101](#), [page 136](#). Violating this setup time requirement possibly results in an undefined runt pulse output.

Table 40: BUFGMUX Select Mechanism

S Input	O Output
0	I0 Input
1	I1 Input

The BUFG clock buffer primitive drives a single clock signal onto the clock network and is essentially the same element as a BUFGMUX, just without the clock select mechanism. Similarly, the BUFGCE primitive creates an enabled clock buffer using the BUFGMUX select mechanism.

The I0 and I1 inputs to an BUFGMUX element originate from clock input pins, DCMs, or Double-Line interconnect, as shown in [Figure 46](#). As shown in [Figure 45](#), there are 24 BUFGMUX elements distributed around the four edges of the device. Clock signals from the four BUFGMUX elements at the top edge and the four at the bottom edge are truly global and connect to all clocking quadrants. The eight left-edge BUFGMUX elements only connect to the two clock quadrants in the left half of the device. Similarly, the eight right-edge BUFGMUX elements only connect to the right half of the device.

BUFGMUX elements are organized in pairs and share I0 and I1 connections with adjacent BUFGMUX elements from a common clock switch matrix as shown in [Figure 46](#). For example, the input on I0 of one BUFGMUX is also a shared input to I1 of the adjacent BUFGMUX.

The clock switch matrix for the left- and right-edge BUFGMUX elements receive signals from any of the three following sources: an LHCLK or RHCLK pin as appropriate, a Double-Line interconnect, or a DCM in the XC3S1200E and XC3S1600E devices.

By contrast, the clock switch matrixes on the top and bottom edges receive signals from any of the five following sources: two GCLK pins, two DCM outputs, or one Double-Line interconnect.

Table 41 indicates permissible connections between clock inputs and BUFGMUX elements. The I0-input provides the best input path to a clock buffer. The I1-input provides the secondary input for the clock multiplexer function.

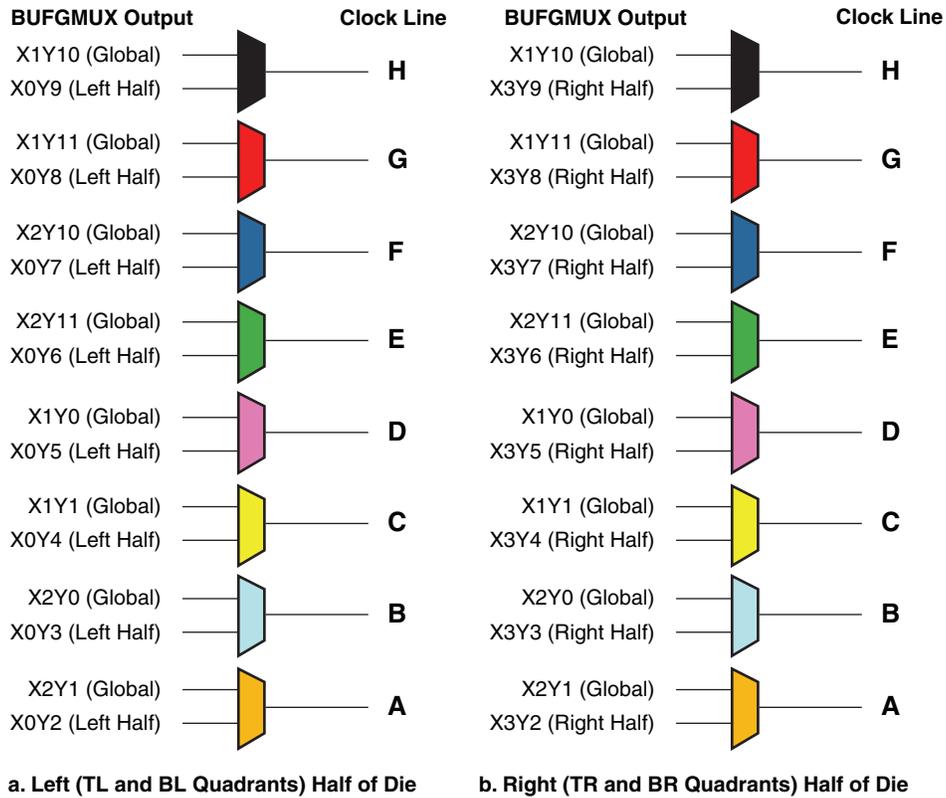
The four BUFGMUX elements on the top edge are paired together and share inputs from the eight global clock inputs along the top edge. Each BUFGMUX pair connects to four of the eight global clock inputs, as shown in Figure 45. This optionally allows differential inputs to the global clock inputs without wasting a BUFGMUX element.

Table 41: Connections from Clock Inputs to BUFGMUX Elements and Associated Quadrant Clock

Quadrant Clock Line ⁽¹⁾	Left-Half BUFGMUX			Top or Bottom BUFGMUX			Right-Half BUFGMUX		
	Location ⁽²⁾	I0 Input	I1 Input	Location ⁽²⁾	I0 Input	I1 Input	Location ⁽²⁾	I0 Input	I1 Input
H	X0Y9	LHCLK7	LHCLK6	X1Y10	GCLK7 or GCLK11	GCLK6 or GCLK10	X3Y9	RHCLK3	RHCLK2
G	X0Y8	LHCLK6	LHCLK7	X1Y11	GCLK6 or GCLK10	GCLK7 or GCLK11	X3Y8	RHCLK2	RHCLK3
F	X0Y7	LHCLK5	LHCLK4	X2Y10	GCLK5 or GCLK9	GCLK4 or GCLK8	X3Y7	RHCLK1	RHCLK0
E	X0Y6	LHCLK4	LHCLK5	X2Y11	GCLK4 or GCLK8	GCLK5 or GCLK9	X3Y6	RHCLK0	RHCLK1
D	X0Y5	LHCLK3	LHCLK2	X1Y0	GCLK3 or GCLK15	GCLK2 or GCLK14	X3Y5	RHCLK7	RHCLK6
C	X0Y4	LHCLK2	LHCLK3	X1Y1	GCLK2 or GCLK14	GCLK3 or GCLK15	X3Y4	RHCLK6	RHCLK7
B	X0Y3	LHCLK1	LHCLK0	X2Y0	GCLK1 or GCLK13	GCLK0 or GCLK12	X3Y3	RHCLK5	RHCLK4
A	X0Y2	LHCLK0	LHCLK1	X2Y1	GCLK0 or GCLK12	GCLK1 or GCLK13	X3Y2	RHCLK4	RHCLK5

Notes:

1. See [Quadrant Clock Routing](#) for connectivity details for the eight quadrant clocks.
2. See [Figure 45](#) for specific BUFGMUX locations, and [Figure 47](#) for information on how BUFGMUX elements drive onto a specific clock line within a quadrant.



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Figure 47: Clock Sources for the Eight Clock Lines within a Clock Quadrant

The outputs of the top or bottom BUFGMUX elements connect to two vertical spines, each comprising four vertical clock lines as shown in Figure 45. At the center of the die, these clock signals connect to the eight-line horizontal clock spine.

Outputs of the left and right BUFGMUX elements are routed onto the left or right horizontal spines, each comprising eight horizontal clock lines.

Each of the eight clock signals in a clock quadrant derives either from a global clock signal or a half clock signal. In other words, there are up to 24 total potential clock inputs to the FPGA, eight of which can connect to clocked elements in a single clock quadrant. Figure 47 shows how the clock lines in each quadrant are selected from associated BUFGMUX sources. For example, if quadrant clock 'A' in the bottom left (BL) quadrant originates from BUFGMUX_X2Y1, then the clock signal from BUFGMUX_X0Y2 is unavailable in the bottom left quadrant. However, the top left (TL) quadrant clock 'A' can still solely use the output from either BUFGMUX_X2Y1 or BUFGMUX_X0Y2 as the source.

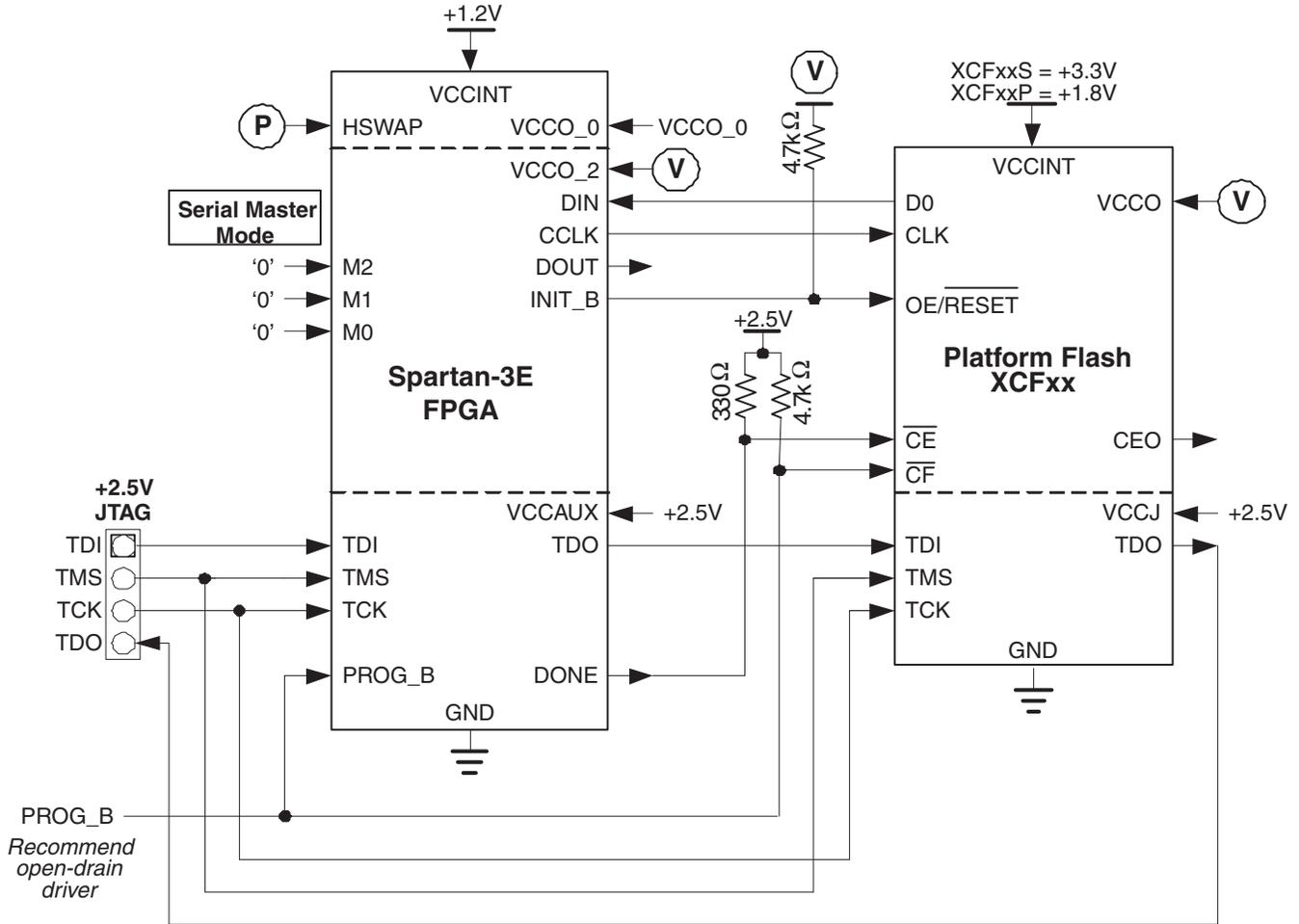
To minimize the dynamic power dissipation of the clock network, the Xilinx development software automatically disables all clock segments not in use.

Master Serial Mode

For additional information, refer to the “Master Serial Mode” chapter in [UG332](#).

In Master Serial mode (M[2:0] = <0:0:0>), the Spartan-3E FPGA configures itself from an attached Xilinx Platform

Flash PROM, as illustrated in [Figure 51](#). The FPGA supplies the CCLK output clock from its internal oscillator to the attached Platform Flash PROM. In response, the Platform Flash PROM supplies bit-serial data to the FPGA’s DIN input, and the FPGA accepts this data on each rising CCLK edge.



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Figure 51: Master Serial Mode using Platform Flash PROM

All mode select pins, M[2:0], must be Low when sampled, when the FPGA’s INIT_B output goes High. After configuration, when the FPGA’s DONE output goes High, the mode select pins are available as full-featured user-I/O pins.

Table 55: Serial Peripheral Interface (SPI) Connections (Cont'd)

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
VS[2:0] 	Input	Variant Select. Instructs the FPGA how to communicate with the attached SPI Flash PROM. See Design Considerations for the HSWAP, M[2:0], and VS[2:0] Pins.	Must be at the logic levels shown in Table 53 . Sampled when INIT_B goes High.	User I/O
MOSI	Output	Serial Data Output.	FPGA sends SPI Flash memory read commands and starting address to the PROM's serial data input.	User I/O
DIN	Input	Serial Data Input.	FPGA receives serial data from PROM's serial data output.	User I/O
CSO_B	Output	Chip Select Output. Active Low.	Connects to the SPI Flash PROM's chip-select input. If HSWAP = 1, connect this signal to a 4.7 kΩ pull-up resistor to 3.3V.	Drive CSO_B High after configuration to disable the SPI Flash and reclaim the MOSI, DIN, and CCLK pins. Optionally, re-use this pin and MOSI, DIN, and CCLK to continue communicating with SPI Flash.
CCLK	Output	Configuration Clock. Generated by FPGA internal oscillator. Frequency controlled by ConfigRate bitstream generator option. If CCLK PCB trace is long or has multiple connections, terminate this output to maintain signal integrity. See CCLK Design Considerations.	Drives PROM's clock input.	User I/O
DOUT	Output	Serial Data Output.	Actively drives. Not used in single-FPGA designs. In a daisy-chain configuration, this pin connects to DIN input of the next FPGA in the chain.	User I/O
INIT_B	Open-drain bidirectional I/O	Initialization Indicator. Active Low. Goes Low at start of configuration during Initialization memory clearing process. Released at end of memory clearing, when mode select pins are sampled. In daisy-chain applications, this signal requires an external 4.7 kΩ pull-up resistor to VCCO_2.	Active during configuration. If SPI Flash PROM requires > 2 ms to awake after powering on, hold INIT_B Low until PROM is ready. If CRC error detected during configuration, FPGA drives INIT_B Low.	User I/O. If unused in the application, drive INIT_B High.
DONE	Open-drain bidirectional I/O	FPGA Configuration Done. Low during configuration. Goes High when FPGA successfully completes configuration. Requires external 330 Ω pull-up resistor to 2.5V.	Low indicates that the FPGA is not yet configured.	Pulled High via external pull-up. When High, indicates that the FPGA successfully configured.
PROG_B	Input	Program FPGA. Active Low. When asserted Low for 500 ns or longer, forces the FPGA to restart its configuration process by clearing configuration memory and resetting the DONE and INIT_B pins once PROG_B returns High. Recommend external 4.7 kΩ pull-up resistor to 2.5V. Internal pull-up value may be weaker (see Table 78). If driving externally with a 3.3V output, use an open-drain or open-collector driver or use a current limiting series resistor.	Must be High to allow configuration to start.	Drive PROG_B Low and release to reprogram FPGA. Hold PROG_B to force FPGA I/O pins into Hi-Z, allowing direct programming access to SPI Flash PROM pins.

This addressing flexibility allows the FPGA to share the parallel Flash PROM with an external or embedded processor. Depending on the specific processor architecture, the processor boots either from the top or bottom of memory. The FPGA is flexible and boots from the opposite end of memory from the processor. Only the processor or the FPGA can boot at any given time. The FPGA can configure first, holding the processor in reset or the processor can boot first, asserting the FPGA's PROG_B pin.

The mode select pins, M[2:0], are sampled when the FPGA's INIT_B output goes High and must be at defined logic levels during this time. After configuration, when the FPGA's DONE output goes High, the mode pins are available as full-featured user-I/O pins.

Ⓟ Similarly, the FPGA's HSWAP pin must be Low to enable pull-up resistors on all user-I/O pins or High to disable the pull-up resistors. The HSWAP control must remain at a constant logic level throughout FPGA configuration. After configuration, when the FPGA's DONE output goes High, the HSWAP pin is available as

full-featured user-I/O pin and is powered by the VCCO_0 supply.

The RDWR_B and CSI_B must be Low throughout the configuration process. After configuration, these pins also become user I/O.

In a single-FPGA application, the FPGA's CSO_B and CCLK pins are not used but are actively driving during the configuration process. The BUSY pin is not used but also actively drives during configuration and is available as a user I/O after configuration.

After configuration, all of the interface pins except DONE and PROG_B are available as user I/Os. Furthermore, the bidirectional SelectMAP configuration peripheral interface (see [Slave Parallel Mode](#)) is available after configuration. To continue using SelectMAP mode, set the *Persist* bitstream generator option to **Yes**. An external host can then read and verify configuration data.

The Persist option will maintain A20-A23 as configuration pins although they are not used in SelectMAP mode.

Table 59: Byte-Wide Peripheral Interface (BPI) Connections

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
HSWAP Ⓟ	Input	User I/O Pull-Up Control. When Low during configuration, enables pull-up resistors in all I/O pins to respective I/O bank V _{CCO} input. 0: Pull-ups during configuration 1: No pull-ups	Drive at valid logic level throughout configuration.	User I/O
M[2:0] Ⓐ	Input	Mode Select. Selects the FPGA configuration mode. See Design Considerations for the HSWAP, M[2:0], and VS[2:0] Pins .	M2 = 0, M1 = 1. Set M0 = 0 to start at address 0, increment addresses. Set M0 = 1 to start at address 0xFFFFF and decrement addresses. Sampled when INIT_B goes High.	User I/O
CSI_B	Input	Chip Select Input. Active Low.	Must be Low throughout configuration.	User I/O. If bitstream option Persist=Yes , becomes part of SelectMap parallel peripheral interface.
RDWR_B	Input	Read/Write Control. Active Low write enable. Read functionality typically only used after configuration, if bitstream option Persist=Yes .	Must be Low throughout configuration.	User I/O. If bitstream option Persist=Yes , becomes part of SelectMap parallel peripheral interface.
LDC0	Output	PROM Chip Enable	Connect to PROM chip-select input (CE#). FPGA drives this signal Low throughout configuration.	User I/O. If the FPGA does not access the PROM after configuration, drive this pin High to deselect the PROM. A[23:0], D[7:0], LDC[2:1], and HDC then become available as user I/O.
LDC1	Output	PROM Output Enable	Connect to the PROM output-enable input (OE#). The FPGA drives this signal Low throughout configuration.	User I/O

Powering Spartan-3E FPGAs

For additional information, refer to the “Powering Spartan-3 Generation FPGAs” chapter in [UG331](#).

Voltage Supplies

Like Spartan-3 FPGAs, Spartan-3E FPGAs have multiple voltage supply inputs, as shown in [Table 70](#). There are two

supply inputs for internal logic functions, V_{CCINT} and V_{CCAUX} . Each of the four I/O banks has a separate V_{CCO} supply input that powers the output buffers within the associated I/O bank. All of the V_{CCO} connections to a specific I/O bank must be connected and must connect to the same voltage.

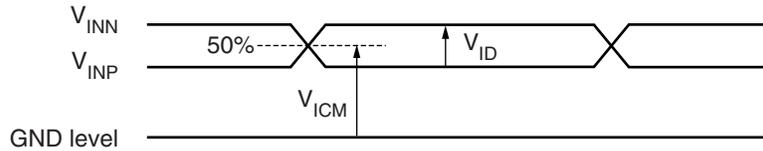
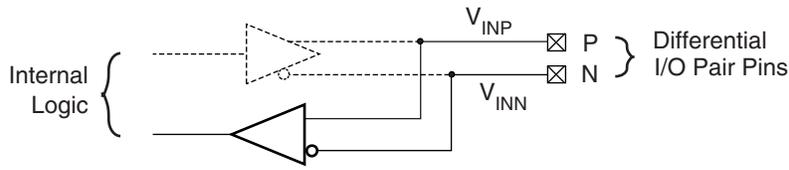
Table 70: Spartan-3E Voltage Supplies

Supply Input	Description	Nominal Supply Voltage
V_{CCINT}	Internal core supply voltage. Supplies all internal logic functions, such as CLBs, block RAM, and multipliers. Input to Power-On Reset (POR) circuit.	1.2V
V_{CCAUX}	Auxiliary supply voltage. Supplies Digital Clock Managers (DCMs), differential drivers, dedicated configuration pins, JTAG interface. Input to Power-On Reset (POR) circuit.	2.5V
V_{CCO_0}	Supplies the output buffers in I/O Bank 0, the bank along the top edge of the FPGA.	Selectable, 3.3V, 2.5V, 1.8, 1.5V, or 1.2V
V_{CCO_1}	Supplies the output buffers in I/O Bank 1, the bank along the right edge of the FPGA. In Byte-Wide Peripheral Interface (BPI) Parallel Flash Mode , connects to the same voltage as the Flash PROM.	Selectable, 3.3V, 2.5V, 1.8, 1.5V, or 1.2V
V_{CCO_2}	Supplies the output buffers in I/O Bank 2, the bank along the bottom edge of the FPGA. Connects to the same voltage as the FPGA configuration source. Input to Power-On Reset (POR) circuit.	Selectable, 3.3V, 2.5V, 1.8, 1.5V, or 1.2V
V_{CCO_3}	Supplies the output buffers in I/O Bank 3, the bank along the left edge of the FPGA.	Selectable, 3.3V, 2.5V, 1.8, 1.5V, or 1.2V

In a 3.3V-only application, all four V_{CCO} supplies connect to 3.3V. However, Spartan-3E FPGAs provide the ability to bridge between different I/O voltages and standards by applying different voltages to the V_{CCO} inputs of different banks. Refer to [I/O Banking Rules](#) for which I/O standards can be intermixed within a single I/O bank.

Each I/O bank also has an separate, optional input voltage reference supply, called V_{REF} . If the I/O bank includes an I/O standard that requires a voltage reference such as HSTL or SSTL, then all V_{REF} pins within the I/O bank must be connected to the same voltage.

Differential I/O Standards



$$V_{ICM} = \text{Input common mode voltage} = \frac{V_{INP} + V_{INN}}{2}$$

$$V_{ID} = \text{Differential input voltage} = |V_{INP} - V_{INN}|$$

DS099-3_01_012304

Figure 69: Differential Input Voltages

Table 82: Recommended Operating Conditions for User I/Os Using Differential Signal Standards

IOSTANDARD Attribute	V _{CCO} for Drivers ⁽¹⁾			V _{ID}			V _{ICM}		
	Min (V)	Nom (V)	Max (V)	Min (mV)	Nom (mV)	Max (mV)	Min (V)	Nom (V)	Max (V)
LVDS_25	2.375	2.50	2.625	100	350	600	0.30	1.25	2.20
BLVDS_25	2.375	2.50	2.625	100	350	600	0.30	1.25	2.20
MINI_LVDS_25	2.375	2.50	2.625	200	-	600	0.30	-	2.2
LVPECL_25 ⁽²⁾	Inputs Only			100	800	1000	0.5	1.2	2.0
RSDS_25	2.375	2.50	2.625	100	200	-	0.3	1.20	1.4
DIFF_HSTL_I_18	1.7	1.8	1.9	100	-	-	0.8	-	1.1
DIFF_HSTL_III_18	1.7	1.8	1.9	100	-	-	0.8	-	1.1
DIFF_SSTL18_I	1.7	1.8	1.9	100	-	-	0.7	-	1.1
DIFF_SSTL2_I	2.3	2.5	2.7	100	-	-	1.0	-	1.5

Notes:

1. The V_{CCO} rails supply only differential output drivers, not input circuits.
2. V_{REF} inputs are not used for any of the differential I/O standards.

Table 90: Propagation Times for the IOB Input Path

Symbol	Description	Conditions	IFD_DELAY_VALUE=	Device	Speed Grade		Units
					-5	-4	
					Min	Min	
Propagation Times							
T _{IOPLI}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with no input delay programmed	LVC MOS25 ⁽²⁾ , IFD_DELAY_VALUE = 0	0	All	1.96	2.25	ns
T _{IOPLID}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with the input delay programmed	LVC MOS25 ⁽²⁾ , IFD_DELAY_VALUE = default software setting	2	XC3S100E	5.40	5.97	ns
			3	All Others	6.30	7.20	

Notes:

1. The numbers in this table are tested using the methodology presented in Table 95 and are based on the operating conditions set forth in Table 77 and Table 80.
2. This propagation time requires adjustment whenever a signal standard other than LVC MOS25 is assigned to the data Input. When this is true, add the appropriate Input adjustment from Table 91.

Table 91: Input Timing Adjustments by IOSTANDARD

Convert Input Time from LVC MOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
Single-Ended Standards			
LVTTTL	0.42	0.43	ns
LVC MOS33	0.42	0.43	ns
LVC MOS25	0	0	ns
LVC MOS18	0.96	0.98	ns
LVC MOS15	0.62	0.63	ns
LVC MOS12	0.26	0.27	ns
PCI33_3	0.41	0.42	ns
PCI66_3	0.41	0.42	ns
HSTL_I_18	0.12	0.12	ns
HSTL_III_18	0.17	0.17	ns
SSTL18_I	0.30	0.30	ns
SSTL2_I	0.15	0.15	ns

Table 91: Input Timing Adjustments by IOSTANDARD (Cont'd)

Convert Input Time from LVC MOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
Differential Standards			
LVDS_25	0.48	0.49	ns
BLVDS_25	0.39	0.39	ns
MINI_LVDS_25	0.48	0.49	ns
LVPECL_25	0.27	0.27	ns
RSDS_25	0.48	0.49	ns
DIFF_HSTL_I_18	0.48	0.49	ns
DIFF_HSTL_III_18	0.48	0.49	ns
DIFF_SSTL18_I	0.30	0.30	ns
DIFF_SSTL2_I	0.32	0.32	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 95 and are based on the operating conditions set forth in Table 77, Table 80, and Table 82.
2. These adjustments are used to convert input path times originally specified for the LVC MOS25 standard to times that correspond to other signal standards.

Table 92: Timing for the IOB Output Path

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Min	Min	
Clock-to-Output Times						
T_{IOCKP}	When reading from the Output Flip-Flop (OFF), the time from the active transition at the OCLK input to data appearing at the Output pin	LVC MOS25 ⁽²⁾ , 12 mA output drive, Fast slew rate	All	2.18	2.50	ns
Propagation Times						
T_{IOOP}	The time it takes for data to travel from the IOB's O input to the Output pin	LVC MOS25 ⁽²⁾ , 12 mA output drive, Fast slew rate	All	2.24	2.58	ns
T_{IOOLP}	The time it takes for data to travel from the O input through the OFF latch to the Output pin			2.32	2.67	ns
Set/Reset Times						
T_{IOSRP}	Time from asserting the OFF's SR input to setting/resetting data at the Output pin	LVC MOS25 ⁽²⁾ , 12 mA output drive, Fast slew rate	All	3.27	3.76	ns
T_{IOGSRQ}	Time from asserting the Global Set Reset (GSR) input on the STARTUP_SPARTAN3E primitive to setting/resetting data at the Output pin			8.40	9.65	ns

Notes:

1. The numbers in this table are tested using the methodology presented in [Table 95](#) and are based on the operating conditions set forth in [Table 77](#) and [Table 80](#).
2. This time requires adjustment whenever a signal standard other than LVC MOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from [Table 94](#).
3. For minimum delays use the values reported by the Timing Analyzer.

Table 105: Switching Characteristics for the DLL (Cont'd)

Symbol	Description		Device	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Phase Alignment⁽⁴⁾								
CLKIN_CLKFB_PHASE	Phase offset between the CLKIN and CLKFB inputs		All	-	±200	-	±200	ps
CLKOUT_PHASE_DLL	Phase offset between DLL outputs	CLK0 to CLK2X (not CLK2X180)		-	±[1% of CLKIN period + 100]	-	±[1% of CLKIN period + 100]	ps
		All others		-	±[1% of CLKIN period + 200]	-	±[1% of CLKIN period + 200]	ps
Lock Time								
LOCK_DLL ⁽³⁾	When using the DLL alone: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase	5 MHz ≤ F _{CLKIN} ≤ 15 MHz	All	-	5	-	5	ms
		F _{CLKIN} > 15 MHz		-	600	-	600	µs
Delay Lines								
DCM_DELAY_STEP	Finest delay resolution		All	20	40	20	40	ps

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 77 and Table 104.
2. Indicates the maximum amount of output jitter that the DCM adds to the jitter on the CLKIN input.
3. For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
4. Some jitter and duty-cycle specifications include 1% of input clock period or 0.01 UI.
Example: The data sheet specifies a maximum jitter of ±[1% of CLKIN period + 150]. Assume the CLKIN frequency is 100 MHz. The equivalent CLKIN period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 150 ps] = ±250 ps.

Digital Frequency Synthesizer (DFS)

Table 106: Recommended Operating Conditions for the DFS

Symbol	Description		Speed Grade				Units
			-5		-4		
			Min	Max	Min	Max	
Input Frequency Ranges⁽²⁾							
F _{CLKIN}	CLKIN_FREQ_FX	Frequency for the CLKIN input	0.200	333 ⁽⁴⁾	0.200	333 ⁽⁴⁾	MHz
Input Clock Jitter Tolerance⁽³⁾							
CLKIN_CYC_JITT_FX_LF	Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency	F _{CLKFX} ≤ 150 MHz	-	±300	-	±300	ps
CLKIN_CYC_JITT_FX_HF		F _{CLKFX} > 150 MHz	-	±150	-	±150	ps
CLKIN_PER_JITT_FX	Period jitter at the CLKIN input		-	±1	-	±1	ns

Notes:

1. DFS specifications apply when either of the DFS outputs (CLKFX or CLKFX180) are used.
2. If both DFS and DLL outputs are used on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 104.
3. CLKIN input jitter beyond these limits may cause the DCM to lose lock.
4. To support double the maximum effective FCLKIN limit, set the CLKIN_DIVIDE_BY_2 attribute to TRUE. This attribute divides the incoming clock frequency by two as it enters the DCM.

Table 152: FG400 Package Pinout (Cont'd)

Bank	XC3S1200E XC3S1600E Pin Name	FG400 Ball	Type
2	IP_L14P_2	T9	INPUT
2	IP_L17N_2/M2/GCLK1	P12	DUAL/ GCLK
2	IP_L17P_2/RDWR_B/ GCLK0	P11	DUAL/ GCLK
2	IP_L20N_2	T12	INPUT
2	IP_L20P_2	R12	INPUT
2	IP_L23N_2/VREF_2	T13	VREF
2	IP_L23P_2	T14	INPUT
2	IP_L26N_2	V14	INPUT
2	IP_L26P_2	V15	INPUT
2	IP_L29N_2	W16	INPUT
2	IP_L29P_2	Y16	INPUT
2	VCCO_2	R11	VCCO
2	VCCO_2	U8	VCCO
2	VCCO_2	U14	VCCO
2	VCCO_2	W5	VCCO
2	VCCO_2	W11	VCCO
2	VCCO_2	W17	VCCO
3	IO_L01N_3	D2	I/O
3	IO_L01P_3	D3	I/O
3	IO_L02N_3/VREF_3	E3	VREF
3	IO_L02P_3	E4	I/O
3	IO_L03N_3	C1	I/O
3	IO_L03P_3	B1	I/O
3	IO_L04N_3	E1	I/O
3	IO_L04P_3	D1	I/O
3	IO_L05N_3	F3	I/O
3	IO_L05P_3	F4	I/O
3	IO_L06N_3	F1	I/O
3	IO_L06P_3	F2	I/O
3	IO_L07N_3	G4	I/O
3	IO_L07P_3	G3	I/O
3	IO_L08N_3	G5	I/O
3	IO_L08P_3	H5	I/O
3	IO_L09N_3/VREF_3	H3	VREF
3	IO_L09P_3	H2	I/O
3	IO_L10N_3	H7	I/O
3	IO_L10P_3	H6	I/O
3	IO_L11N_3	J4	I/O
3	IO_L11P_3	J3	I/O
3	IO_L12N_3	J1	I/O
3	IO_L12P_3	J2	I/O
3	IO_L13N_3	J6	I/O

Table 152: FG400 Package Pinout (Cont'd)

Bank	XC3S1200E XC3S1600E Pin Name	FG400 Ball	Type
3	IO_L13P_3	K6	I/O
3	IO_L14N_3/LHCLK1	K2	LHCLK
3	IO_L14P_3/LHCLK0	K3	LHCLK
3	IO_L15N_3/LHCLK3/IRDY2	L7	LHCLK
3	IO_L15P_3/LHCLK2	K7	LHCLK
3	IO_L16N_3/LHCLK5	L1	LHCLK
3	IO_L16P_3/LHCLK4/TRDY2	M1	LHCLK
3	IO_L17N_3/LHCLK7	L3	LHCLK
3	IO_L17P_3/LHCLK6	M3	LHCLK
3	IO_L18N_3	M7	I/O
3	IO_L18P_3	M8	I/O
3	IO_L19N_3	M4	I/O
3	IO_L19P_3	M5	I/O
3	IO_L20N_3/VREF_3	N6	VREF
3	IO_L20P_3	M6	I/O
3	IO_L21N_3	N2	I/O
3	IO_L21P_3	N1	I/O
3	IO_L22N_3	P7	I/O
3	IO_L22P_3	N7	I/O
3	IO_L23N_3	N4	I/O
3	IO_L23P_3	N3	I/O
3	IO_L24N_3	R1	I/O
3	IO_L24P_3	P1	I/O
3	IO_L25N_3	R5	I/O
3	IO_L25P_3	P5	I/O
3	IO_L26N_3	T2	I/O
3	IO_L26P_3	R2	I/O
3	IO_L27N_3	R4	I/O
3	IO_L27P_3	R3	I/O
3	IO_L28N_3/VREF_3	T1	VREF
3	IO_L28P_3	U1	I/O
3	IO_L29N_3	T3	I/O
3	IO_L29P_3	U3	I/O
3	IO_L30N_3	V1	I/O
3	IO_L30P_3	V2	I/O
3	IP	F5	INPUT
3	IP	G1	INPUT
3	IP	G6	INPUT
3	IP	H1	INPUT
3	IP	J5	INPUT
3	IP	L5	INPUT
3	IP	L8	INPUT
3	IP	M2	INPUT

Table 154: FG484 Package Pinout (Cont'd)

Bank	XC3S1600E Pin Name	FG484 Ball	Type
0	IP	E6	INPUT
0	IP_L02N_0	D17	INPUT
0	IP_L02P_0	D18	INPUT
0	IP_L05N_0	C17	INPUT
0	IP_L05P_0	B17	INPUT
0	IP_L08N_0	E15	INPUT
0	IP_L08P_0	D15	INPUT
0	IP_L14N_0	D13	INPUT
0	IP_L14P_0	C13	INPUT
0	IP_L17N_0	A12	INPUT
0	IP_L17P_0	A13	INPUT
0	IP_L20N_0/GCLK9	H11	GCLK
0	IP_L20P_0/GCLK8	H12	GCLK
0	IP_L23N_0	F10	INPUT
0	IP_L23P_0	F11	INPUT
0	IP_L26N_0	G9	INPUT
0	IP_L26P_0	G10	INPUT
0	IP_L31N_0	C8	INPUT
0	IP_L31P_0	D8	INPUT
0	IP_L34N_0	C7	INPUT
0	IP_L34P_0	C6	INPUT
0	IP_L37N_0	A3	INPUT
0	IP_L37P_0	A2	INPUT
0	VCCO_0	B5	VCCO
0	VCCO_0	B10	VCCO
0	VCCO_0	B14	VCCO
0	VCCO_0	B18	VCCO
0	VCCO_0	E8	VCCO
0	VCCO_0	F14	VCCO
0	VCCO_0	G11	VCCO
1	IO_L01N_1/A15	Y22	DUAL
1	IO_L01P_1/A16	AA22	DUAL
1	IO_L02N_1/A13	W21	DUAL
1	IO_L02P_1/A14	Y21	DUAL
1	IO_L03N_1/VREF_1	W20	VREF
1	IO_L03P_1	V20	I/O
1	IO_L04N_1	U19	I/O
1	IO_L04P_1	V19	I/O
1	IO_L05N_1	V22	I/O
1	IO_L05P_1	W22	I/O
1	IO_L06N_1	T19	I/O
1	IO_L06P_1	T18	I/O
1	IO_L07N_1/VREF_1	U20	VREF
1	IO_L07P_1	U21	I/O

Table 154: FG484 Package Pinout (Cont'd)

Bank	XC3S1600E Pin Name	FG484 Ball	Type
1	IO_L08N_1	T22	I/O
1	IO_L08P_1	U22	I/O
1	IO_L09N_1	R19	I/O
1	IO_L09P_1	R18	I/O
1	IO_L10N_1	R16	I/O
1	IO_L10P_1	T16	I/O
1	IO_L11N_1	R21	I/O
1	IO_L11P_1	R20	I/O
1	IO_L12N_1/VREF_1	P18	VREF
1	IO_L12P_1	P17	I/O
1	IO_L13N_1	P22	I/O
1	IO_L13P_1	R22	I/O
1	IO_L14N_1	P15	I/O
1	IO_L14P_1	P16	I/O
1	IO_L15N_1	N18	I/O
1	IO_L15P_1	N19	I/O
1	IO_L16N_1/A11	N16	DUAL
1	IO_L16P_1/A12	N17	DUAL
1	IO_L17N_1/VREF_1	M20	VREF
1	IO_L17P_1	N20	I/O
1	IO_L18N_1/A9/RHCLK1	M22	RHCLK/ DUAL
1	IO_L18P_1/A10/RHCLK0	N22	RHCLK/ DUAL
1	IO_L19N_1/A7/RHCLK3/ TRDY1	M16	RHCLK/ DUAL
1	IO_L19P_1/A8/RHCLK2	M15	RHCLK/ DUAL
1	IO_L20N_1/A5/RHCLK5	L21	RHCLK/ DUAL
1	IO_L20P_1/A6/RHCLK4/ IRDY1	L20	RHCLK/ DUAL
1	IO_L21N_1/A3/RHCLK7	L19	RHCLK/ DUAL
1	IO_L21P_1/A4/RHCLK6	L18	RHCLK/ DUAL
1	IO_L22N_1/A1	K22	DUAL
1	IO_L22P_1/A2	L22	DUAL
1	IO_L23N_1/A0	K17	DUAL
1	IO_L23P_1	K16	I/O
1	IO_L24N_1	K19	I/O
1	IO_L24P_1	K18	I/O
1	IO_L25N_1	K15	I/O
1	IO_L25P_1	J15	I/O
1	IO_L26N_1	J20	I/O
1	IO_L26P_1	J21	I/O

Table 154: FG484 Package Pinout (Cont'd)

Bank	XC3S1600E Pin Name	FG484 Ball	Type
2	IO_L19N_2/D6/GCLK13	U11	DUAL/GCLK
2	IO_L19P_2/D7/GCLK12	V11	DUAL/GCLK
2	IO_L20N_2/D3/GCLK15	T11	DUAL/GCLK
2	IO_L20P_2/D4/GCLK14	R11	DUAL/GCLK
2	IO_L22N_2/D1/GCLK3	W12	DUAL/GCLK
2	IO_L22P_2/D2/GCLK2	Y12	DUAL/GCLK
2	IO_L23N_2/DIN/D0	U12	DUAL
2	IO_L23P_2/M0	V12	DUAL
2	IO_L25N_2	Y13	I/O
2	IO_L25P_2	W13	I/O
2	IO_L26N_2/VREF_2	U14	VREF
2	IO_L26P_2	U13	I/O
2	IO_L27N_2	T14	I/O
2	IO_L27P_2	R14	I/O
2	IO_L28N_2	Y14	I/O
2	IO_L28P_2	AA14	I/O
2	IO_L29N_2	W14	I/O
2	IO_L29P_2	V14	I/O
2	IO_L30N_2	AB15	I/O
2	IO_L30P_2	AA15	I/O
2	IO_L32N_2	W15	I/O
2	IO_L32P_2	Y15	I/O
2	IO_L33N_2	U16	I/O
2	IO_L33P_2	V16	I/O
2	IO_L35N_2/A22	AB17	DUAL
2	IO_L35P_2/A23	AA17	DUAL
2	IO_L36N_2	W17	I/O
2	IO_L36P_2	Y17	I/O
2	IO_L38N_2/A20	Y18	DUAL
2	IO_L38P_2/A21	W18	DUAL
2	IO_L39N_2/VS1/A18	AA20	DUAL
2	IO_L39P_2/VS2/A19	AB20	DUAL
2	IO_L40N_2/CCLK	W19	DUAL
2	IO_L40P_2/VS0/A17	Y19	DUAL
2	IP	V17	INPUT
2	IP	AB2	INPUT
2	IP_L02N_2	AA4	INPUT
2	IP_L02P_2	Y4	INPUT
2	IP_L05N_2	Y6	INPUT
2	IP_L05P_2	AA6	INPUT

Table 154: FG484 Package Pinout (Cont'd)

Bank	XC3S1600E Pin Name	FG484 Ball	Type
2	IP_L08N_2	AB7	INPUT
2	IP_L08P_2	AB6	INPUT
2	IP_L15N_2	Y10	INPUT
2	IP_L15P_2	W10	INPUT
2	IP_L18N_2/VREF_2	AA11	VREF
2	IP_L18P_2	Y11	INPUT
2	IP_L21N_2/M2/GCLK1	P12	DUAL/GCLK
2	IP_L21P_2/RDWR_B/ GCLK0	R12	DUAL/GCLK
2	IP_L24N_2	R13	INPUT
2	IP_L24P_2	T13	INPUT
2	IP_L31N_2/VREF_2	T15	VREF
2	IP_L31P_2	U15	INPUT
2	IP_L34N_2	Y16	INPUT
2	IP_L34P_2	W16	INPUT
2	IP_L37N_2	AA19	INPUT
2	IP_L37P_2	AB19	INPUT
2	VCCO_2	T12	VCCO
2	VCCO_2	U9	VCCO
2	VCCO_2	V15	VCCO
2	VCCO_2	AA5	VCCO
2	VCCO_2	AA9	VCCO
2	VCCO_2	AA13	VCCO
2	VCCO_2	AA18	VCCO
3	IO_L01N_3	C1	I/O
3	IO_L01P_3	C2	I/O
3	IO_L02N_3/VREF_3	D2	VREF
3	IO_L02P_3	D3	I/O
3	IO_L03N_3	E3	I/O
3	IO_L03P_3	E4	I/O
3	IO_L04N_3	E1	I/O
3	IO_L04P_3	D1	I/O
3	IO_L05N_3	F4	I/O
3	IO_L05P_3	F3	I/O
3	IO_L06N_3	G5	I/O
3	IO_L06P_3	G4	I/O
3	IO_L07N_3	F1	I/O
3	IO_L07P_3	G1	I/O
3	IO_L08N_3/VREF_3	G6	VREF
3	IO_L08P_3	G7	I/O
3	IO_L09N_3	H4	I/O
3	IO_L09P_3	H5	I/O
3	IO_L10N_3	H2	I/O
3	IO_L10P_3	H3	I/O