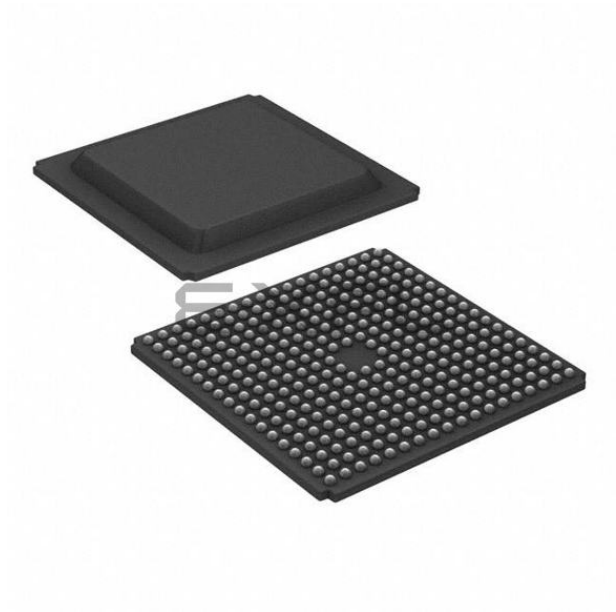
# AMD Xilinx - XC3S1200E-5FGG320C Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 2168 |
| Number of Logic Elements/Cells | 19512 |
| Total RAM Bits | 516096 |
| Number of I/O | 250 |
| Number of Gates | 1200000 |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 320-BGA |
| Supplier Device Package | 320-FBGA (19x19) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc3s1200e-5fgg320c |

## Introduction

As described in Architectural Overview, the Spartan-3E FPGA architecture consists of five fundamental functional elements:

- Input/Output Blocks (IOBs)
- Configurable Logic Block (CLB) and Slice Resources
- Block RAM
- Dedicated Multipliers
- Digital Clock Managers (DCMs)

The following sections provide detailed information on each of these functions. In addition, this section also describes the following functions:

- Clocking Infrastructure
- Interconnect
- Configuration
- Powering Spartan-3E FPGAs

## Input/Output Blocks (IOBs)

For additional information, refer to the “Using I/O Resources” chapter in UG331.

### IOB Overview

The Input/Output Block (IOB) provides a programmable, unidirectional or bidirectional interface between a package pin and the FPGA’s internal logic. The IOB is similar to that of the Spartan-3 family with the following differences:

- Input-only blocks are added
- Programmable input delays are added to all blocks
- DDR flip-flops can be shared between adjacent IOBs

The unidirectional input-only block has a subset of the full IOB capabilities. Thus there are no connections or logic for an output path. The following paragraphs assume that any reference to output functionality does not apply to the input-only blocks. The number of input-only blocks varies with device size, but is never more than 25% of the total IOB count.

Figure 5 is a simplified diagram of the IOB’s internal structure. There are three main signal paths within the IOB: the output path, input path, and 3-state path. Each path has its own pair of storage elements that can act as either registers or latches. For more information, see Storage Element Functions. The three main signal paths are as follows:

- The input path carries data from the pad, which is bonded to a package pin, through an optional programmable delay element directly to the I line. After the delay element, there are alternate routes through a pair of storage elements to the IQ1 and IQ2 lines. The IOB outputs I, IQ1, and IQ2 lead to the FPGA’s internal logic. The delay element can be set to ensure a hold time of zero (see Input Delay Functions).
- The output path, starting with the O1 and O2 lines, carries data from the FPGA’s internal logic through a multiplexer and then a three-state driver to the IOB pad. In addition to this direct path, the multiplexer provides the option to insert a pair of storage elements.
- The 3-state path determines when the output driver is high impedance. The T1 and T2 lines carry data from the FPGA’s internal logic through a multiplexer to the output driver. In addition to this direct path, the multiplexer provides the option to insert a pair of storage elements.
- All signal paths entering the IOB, including those associated with the storage elements, have an inverter option. Any inverter placed on these paths is automatically absorbed into the IOB.

## Storage Element Functions

There are three pairs of storage elements in each IOB, one pair for each of the three paths. It is possible to configure each of these storage elements as an edge-triggered D-type flip-flop (FD) or a level-sensitive latch (LD).

The storage-element pair on either the Output path or the Three-State path can be used together with a special multiplexer to produce Double-Data-Rate (DDR) transmission. This is accomplished by taking data synchronized to the clock signal's rising edge and converting it to bits synchronized on both the rising and the falling edge. The combination of two registers and a multiplexer is referred to as a Double-Data-Rate D-type flip-flop (ODDR2).

Table 4 describes the signal paths associated with the storage element.

*Table 4:* **Storage Element Signal Description**

| Storage Element Signal | Description | Function |
|---|---|---|
| D | Data input | Data at this input is stored on the active edge of CK and enabled by CE. For latch operation when the input is enabled, data passes directly to the output Q. |
| Q | Data output | The data on this output reflects the state of the storage element. For operation as a latch in transparent mode, Q mirrors the data at D. |
| CK | Clock input | Data is loaded into the storage element on this input's active edge with CE asserted. |
| CE | Clock Enable input | When asserted, this input enables CK. If not connected, CE defaults to the asserted state. |
| SR | Set/Reset input | This input forces the storage element into the state specified by the SRHIGH/SRLOW attributes. The SYNC/ASYNC attribute setting determines if the SR input is synchronized to the clock or not. If both SR and REV are active at the same time, the storage element gets a value of 0. |
| REV | Reverse input | This input is used together with SR. It forces the storage element into the state opposite from what SR does. The SYNC/ASYNC attribute setting determines whether the REV input is synchronized to the clock or not. If both SR and REV are active at the same time, the storage element gets a value of 0. |

As shown in Figure 5, the upper registers in both the output and three-state paths share a common clock. The OTCLK1 clock signal drives the CK clock inputs of the upper registers on the output and three-state paths. Similarly, OTCLK2 drives the CK inputs for the lower registers on the output and three-state paths. The upper and lower registers on the input path have independent clock lines: ICLK1 and ICLK2.

The OCE enable line controls the CE inputs of the upper and lower registers on the output path. Similarly, TCE controls the CE inputs for the register pair on the three-state path and ICE does the same for the register pair on the input path.

The Set/Reset (SR) line entering the IOB controls all six registers, as is the Reverse (REV) line.

In addition to the signal polarity controls described in IOB Overview, each storage element additionally supports the controls described in Table 5.

*Table 5:* **Storage Element Options**

| Option Switch | Function | Specificity |
|---|---|---|
| FF/Latch | Chooses between an edge-triggered flip-flop or a level-sensitive latch | Independent for each storage element |
| SYNC/ASYNC | Determines whether the SR set/reset control is synchronous or asynchronous | Independent for each storage element |
| SRHIGH/SRLOW | Determines whether SR acts as a Set, which forces the storage element to a logic 1 (SRHIGH) or a Reset, which forces a logic 0 (SRLOW) | Independent for each storage element, except when using ODDR2. In the latter case, the selection for the upper element will apply to both elements. |
| INIT1/INIT0 | When Global Set/Reset (GSR) is asserted or after configuration this option specifies the initial state of the storage element, either set (INIT1) or reset (INIT0). By default, choosing SRLOW also selects INIT0; choosing SRHIGH also selects INIT1. | Independent for each storage element, except when using ODDR2, which uses two IOBs. In the ODDR2 case, selecting INIT0 for one IOBs applies to both elements within the IOB, although INIT1 could be selected for the elements in the other IOB. |

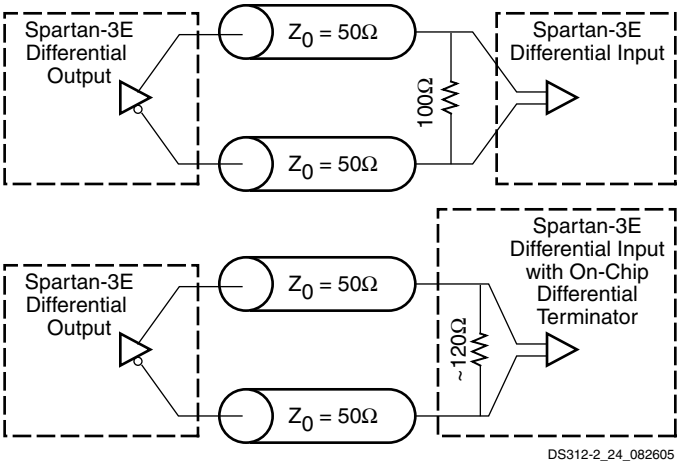


*Figure 11:* **Differential Inputs and Outputs**

## Pull-Up and Pull-Down Resistors

Pull-up and pull-down resistors inside each IOB optionally force a floating I/O or Input-only pin to a determined state. Pull-up and pull-down resistors are commonly applied to unused I/Os, inputs, and three-state outputs, but can be used on any I/O or Input-only pin. The pull-up resistor connects an IOB to $V_{CCO}$ through a resistor. The resistance value depends on the $V_{CCO}$ voltage (see Module 3, DC and Switching Characteristics for the specifications). The pull-down resistor similarly connects an IOB to ground with a resistor. The PULLUP and PULLDOWN attributes and library primitives turn on these optional resistors.

By default, PULLDOWN resistors terminate all unused I/O and Input-only pins. Unused I/O and Input-only pins can alternatively be set to PULLUP or FLOAT. To change the unused I/O Pad setting, set the Bitstream Generator (BitGen) option ***UnusedPin*** to PULLUP, PULLDOWN, or FLOAT. The ***UnusedPin*** option is accessed through the Properties for Generate Programming File in ISE. See Bitstream Generator (BitGen) Options.

During configuration a Low logic level on the HSWAP pin activates pull-up resistors on all I/O and Input-only pins not actively used in the selected configuration mode.

## Keeper Circuit

Each I/O has an optional keeper circuit (see Figure 12) that keeps bus lines from floating when not being actively driven. The KEEPER circuit retains the last logic level on a line after all drivers have been turned off. Apply the KEEPER attribute or use the KEEPER library primitive to use the KEEPER circuitry. Pull-up and pull-down resistors override the KEEPER settings.

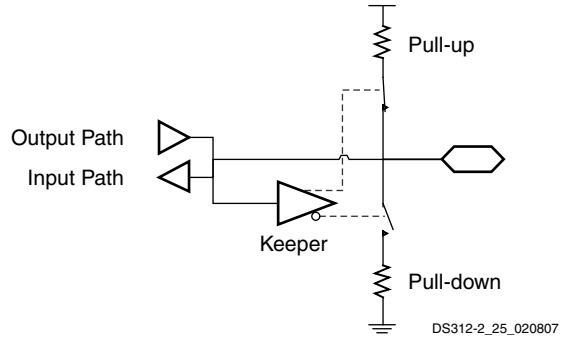


*Figure 12:* **Keeper Circuit**

## Slew Rate Control and Drive Strength

Each IOB has a slew-rate control that sets the output switching edge-rate for LVCMOS and LVTTL outputs. The SLEW attribute controls the slew rate and can either be set to SLOW (default) or FAST.

Each LVCMOS and LVTTL output additionally supports up to six different drive current strengths as shown in Table 8. To adjust the drive strength for each output, the DRIVE attribute is set to the desired drive strength: 2, 4, 6, 8, 12, and 16. Unless otherwise specified in the FPGA application, the software default IOSTANDARD is LVCMOS25, SLOW slew rate, and 12 mA output drive.

*Table 8:* **Programmable Output Drive Current**

| IOSTANDARD | Output Drive Current (mA) | | | | | |
|---|---|---|---|---|---|---|
| | 2 | 4 | 6 | 8 | 12 | 16 |
| LVTTL | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ |
| LVCMOS33 | ✔ | ✔ | ✔ | ✔ | ✔ | ✔ |
| LVCMOS25 | ✔ | ✔ | ✔ | ✔ | ✔ | - |
| LVCMOS18 | ✔ | ✔ | ✔ | ✔ | - | - |
| LVCMOS15 | ✔ | ✔ | ✔ | - | - | - |
| LVCMOS12 | ✔ | - | - | - | - | - |

High output current drive strength and FAST output slew rates generally result in fastest I/O performance. However, these same settings generally also result in transmission line effects on the printed circuit board (PCB) for all but the shortest board traces. Each IOB has independent slew rate and drive strength controls. Use the slowest slew rate and lowest output drive current that meets the performance requirements for the end application.

Likewise, due to lead inductance, a given package supports a limited number of simultaneous switching outputs (SSOs) when using fast, high-drive outputs. Only use fast, high-drive outputs when required by the application.

The wide multiplexers can be used by the automatic tools or instantiated in a design using a component such as the F5MUX. The symbol, signals, and function are described in Figure 21, Table 12, and Table 13. The description is similar for the F6MUX, F7MUX, and F8MUX. Each has versions with a general output, local output, or both.

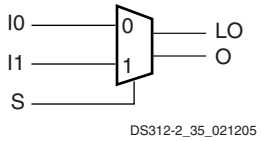


*Figure 21:* **F5MUX with Local and General Outputs**

*Table 12:* **F5MUX Inputs and Outputs**

| Signal | Function |
|---|---|
| I0 | Input selected when S is Low |
| I1 | Input selected when S is High |
| S | Select input |
| LO | Local Output that connects to the F5 or FX CLB pins, which use local feedback to the FXIN inputs to the FiMUX for cascading |
| O | General Output that connects to the general-purpose combinatorial or registered outputs of the CLB |

*Table 13:* **F5MUX Function**

| Inputs | | | Outputs | |
|---|---|---|---|---|
| **S** | **I0** | **I1** | **O** | **LO** |
| 0 | 1 | X | 1 | 1 |
| 0 | 0 | X | 0 | 0 |
| 1 | X | 1 | 1 | 1 |
| 1 | X | 0 | 0 | 0 |

### Initialization

The CLB storage elements are initialized at power-up, during configuration, by the global GSR signal, and by the individual SR or REV inputs to the CLB. The storage elements can also be re-initialized using the GSR input on the STARTUP_SPARTAN3E primitive. See Global Controls (STARTUP_SPARTAN3E).

*Table 17:* **Slice Storage Element Initialization**

| Signal | Description |
|---|---|
| SR | Set/Reset input. Forces the storage element into the state specified by the attribute SRHIGH or SRLOW. SRHIGH forces a logic 1 when SR is asserted. SRLOW forces a logic 0. For each slice, set and reset can be set to be synchronous or asynchronous. |
| REV | Reverse of Set/Reset input. A second input (BY) forces the storage element into the opposite state. The reset condition is predominant over the set condition if both are active. Same synchronous/asynchronous setting as for SR. |
| GSR | Global Set/Reset. GSR defaults to active High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN3E element. The initial state after configuration or GSR is defined by a separate INIT0 and INIT1 attribute. By default, setting the SRLOW attribute sets INIT0, and setting the SRHIGH attribute sets INIT1. |

## Distributed RAM

For additional information, refer to the “Using Look-Up Tables as Distributed RAM” chapter in UG331.

The LUTs in the SLICEM can be programmed as distributed RAM. This type of memory affords moderate amounts of data buffering anywhere along a data path. One SLICEM LUT stores 16 bits (RAM16). The four LUT inputs F[4:1] or G[4:1] become the address lines labeled A[4:1] in the device model and A[3:0] in the design components, providing a 16x1 configuration in one LUT. Multiple SLICEM LUTs can be combined in various ways to store larger amounts of data, including 16x4, 32x2, or 64x1 configurations in one CLB. The fifth and sixth address lines required for the 32-deep and 64-deep configurations, respectively, are implemented using the BX and BY inputs, which connect to the write enable logic for writing and the F5MUX and F6MUX for reading.

Writing to distributed RAM is always synchronous to the SLICEM clock (WCLK for distributed RAM) and enabled by the SLICEM SR input which functions as the active-High Write Enable (WE). The read operation is asynchronous, and, therefore, during a write, the output initially reflects the old data at the address being written.

The distributed RAM outputs can be captured using the flip-flops within the SLICEM element. The WE write-enable control for the RAM and the CE clock-enable control for the flip-flop are independent, but the WCLK and CLK clock inputs are shared. Because the RAM read operation is asynchronous, the output data always reflects the currently addressed RAM location.

A dual-port option combines two LUTs so that memory access is possible from two independent data lines. The same data is written to both 16x1 memories but they have independent read address lines and outputs. The dual-port function is implemented by cascading the G-LUT address lines, which are used for both read and write, to the F-LUT write address lines (WF[4:1] in Figure 15), and by cascading the G-LUT data input D1 through the DIF_MUX in Figure 15 and to the D1 input on the F-LUT. One CLB provides a 16x1 dual-port memory as shown in Figure 26.

Any write operation on the D input and any read operation on the SPO output can occur simultaneously with and independently from a read operation on the second read-only port, DPO.

initialized distributed RAM contents are not disturbed during the configuration process.

The distributed RAM is useful for smaller amounts of memory. Larger memory requirements can use the dedicated 18Kbit RAM blocks (see Block RAM).

## Shift Registers

For additional information, refer to the “Using Look-Up Tables as Shift Registers (SRL16)” chapter in UG331.

It is possible to program each SLICEM LUT as a 16-bit shift register (see Figure 28). Used in this way, each LUT can delay serial data anywhere from 1 to 16 clock cycles without using any of the dedicated flip-flops. The resulting programmable delays can be used to balance the timing of data pipelines.

The SLICEM LUTs cascade from the G-LUT to the F-LUT through the DIFMUX (see Figure 15). SHIFTIN and SHIFTOUT lines cascade a SLICEM to the SLICEM below to form larger shift registers. The four SLICEM LUTs of a single CLB can be combined to produce delays up to 64 clock cycles. It is also possible to combine shift registers across more than one CLB.

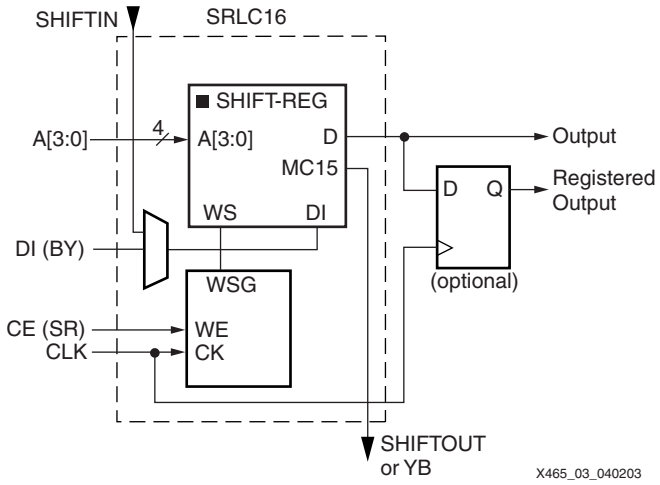


*Figure 28:* **Logic Cell SRL16 Structure**

Each shift register provides a shift output MC15 for the last bit in each LUT, in addition to providing addressable access to any bit in the shift register through the normal D output. The address inputs A[3:0] are the same as the distributed RAM address lines, which come from the LUT inputs F[4:1] or G[4:1]. At the end of the shift register, the CLB flip-flop can be used to provide one more shift delay for the addressable bit.

The shift register element is known as the SRL16 (Shift Register LUT 16-bit), with a ‘C’ added to signify a cascade ability (Q15 output) and ‘E’ to indicate a Clock Enable. See Figure 29 for an example of the SRLC16E component.

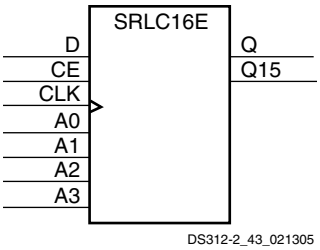


*Figure 29:* **SRL16 Shift Register Component with Cascade and Clock Enable**

The functionality of the shift register is shown in Table 20. The SRL16 shifts on the rising edge of the clock input when the Clock Enable control is High. This shift register cannot be initialized either during configuration or during operation except by shifting data into it. The clock enable and clock inputs are shared between the two LUTs in a SLICEM. The clock enable input is automatically kept active if unused.

*Table 20:* **SRL16 Shift Register Function**

| Inputs | | | | Outputs | |
|---|---|---|---|---|---|
| **Am** | **CLK** | **CE** | **D** | **Q** | **Q15** |
| Am | X | 0 | X | Q[Am] | Q[15] |
| Am | ↑ | 1 | D | Q[Am-1] | Q[15] |

**Notes:**

1. m = 0, 1, 2, 3.

### DLL Clock Output and Feedback Connections

As many as four of the nine DCM clock outputs can simultaneously drive four of the BUFGMUX buffers on the same die edge. All DCM clock outputs can simultaneously drive general routing resources, including interconnect leading to OBUF buffers.

The feedback loop is essential for DLL operation. Either the CLK0 or CLK2X outputs feed back to the CLKFB input via a BUFGMUX global buffer to eliminate the clock distribution delay. The specific BUFGMUX buffer used to feed back the CLK0 or CLK2X signal is ideally one of the BUFGMUX buffers associated with a specific DCM, as shown in Table 30, Table 31, and Table 32.

The feedback path also phase-aligns the other seven DLL outputs: CLK0, CLK90, CLK180, CLK270, CLKDV, CLK2X, or CLK2X180. The CLK_FEEDBACK attribute value must agree with the physical feedback connection. Use “1X” for CLK0 feedback and “2X” for CLK2X feedback. If the DFS unit is used stand-alone, without the DLL, then no feedback is required and set the CLK_FEEDBACK attribute to “NONE”.

Two basic cases determine how to connect the DLL clock outputs and feedback connections: on-chip synchronization and off-chip synchronization, which are illustrated in Figure 42a through Figure 42d.

In the on-chip synchronization case in Figure 42a and Figure 42b, it is possible to connect any of the DLL’s seven output clock signals through general routing resources to the FPGA’s internal registers. Either a Global Clock Buffer (BUFG) or a BUFGMUX affords access to the global clock network. As shown in Figure 42a, the feedback loop is created by routing CLK0 (or CLK2X) in Figure 42b to a global clock net, which in turn drives the CLKFB input.

In the off-chip synchronization case in Figure 42c and Figure 42d, CLK0 (or CLK2X) plus any of the DLL’s other output clock signals exit the FPGA using output buffers (OBUF) to drive an external clock network plus registers on the board. As shown in Figure 42c, the feedback loop is formed by feeding CLK0 (or CLK2X) in Figure 42d back into the FPGA, then to the DCM’s CLKFB input via a Global Buffer Input, specified in Table 30.

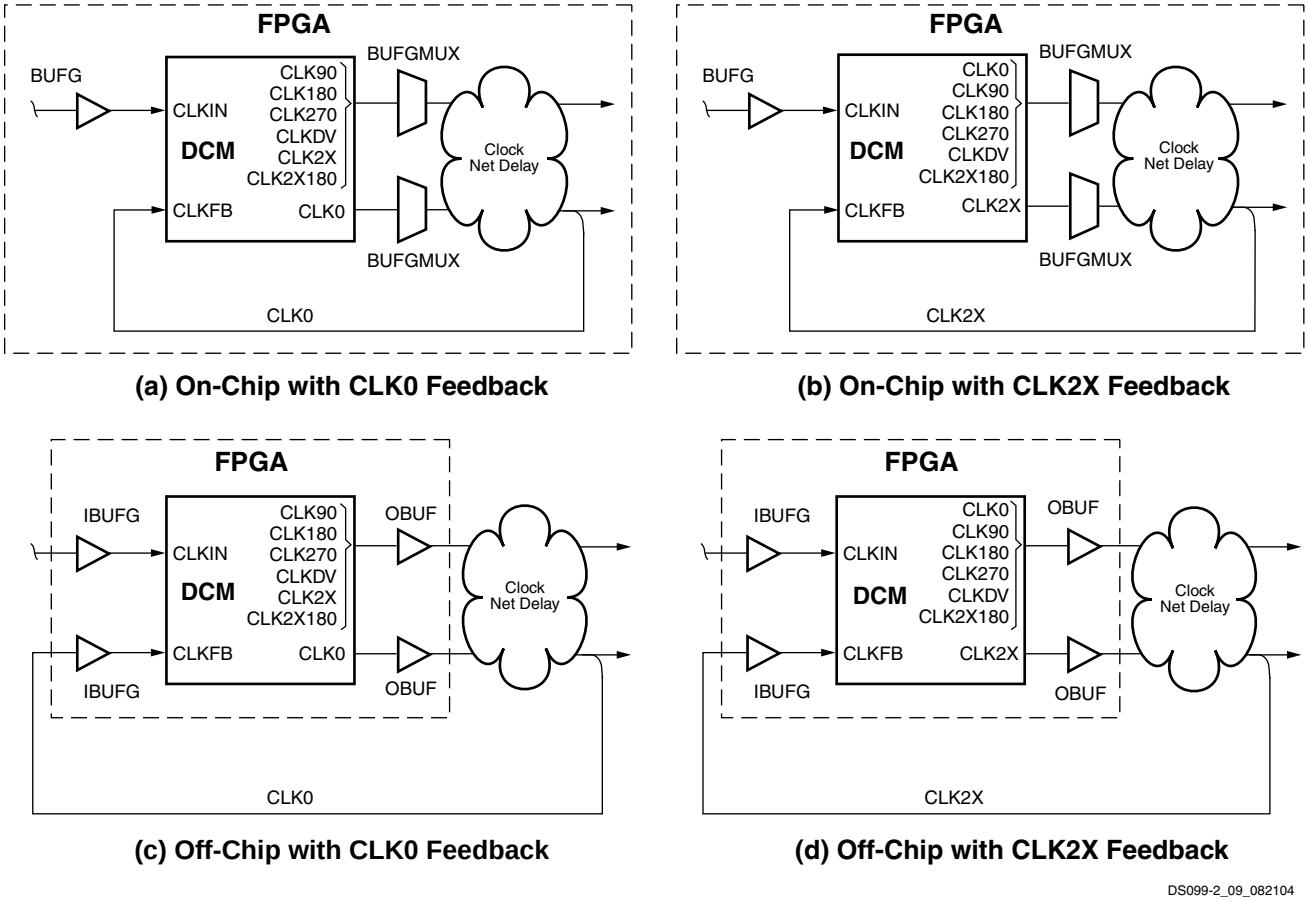


*Figure 42:* **Input Clock, Output Clock, and Feedback Connections for the DLL**

## SPI Serial Flash Mode

For additional information, refer to the “Master SPI Mode” chapter in UG332.

In SPI Serial Flash mode (M[2:0] = <0:0:1>), the Spartan-3E FPGA configures itself from an attached industry-standard SPI serial Flash PROM, as illustrated in Figure 53 and Figure 54. The FPGA supplies the CCLK output clock from its internal oscillator to the clock input of the attached SPI Flash PROM.

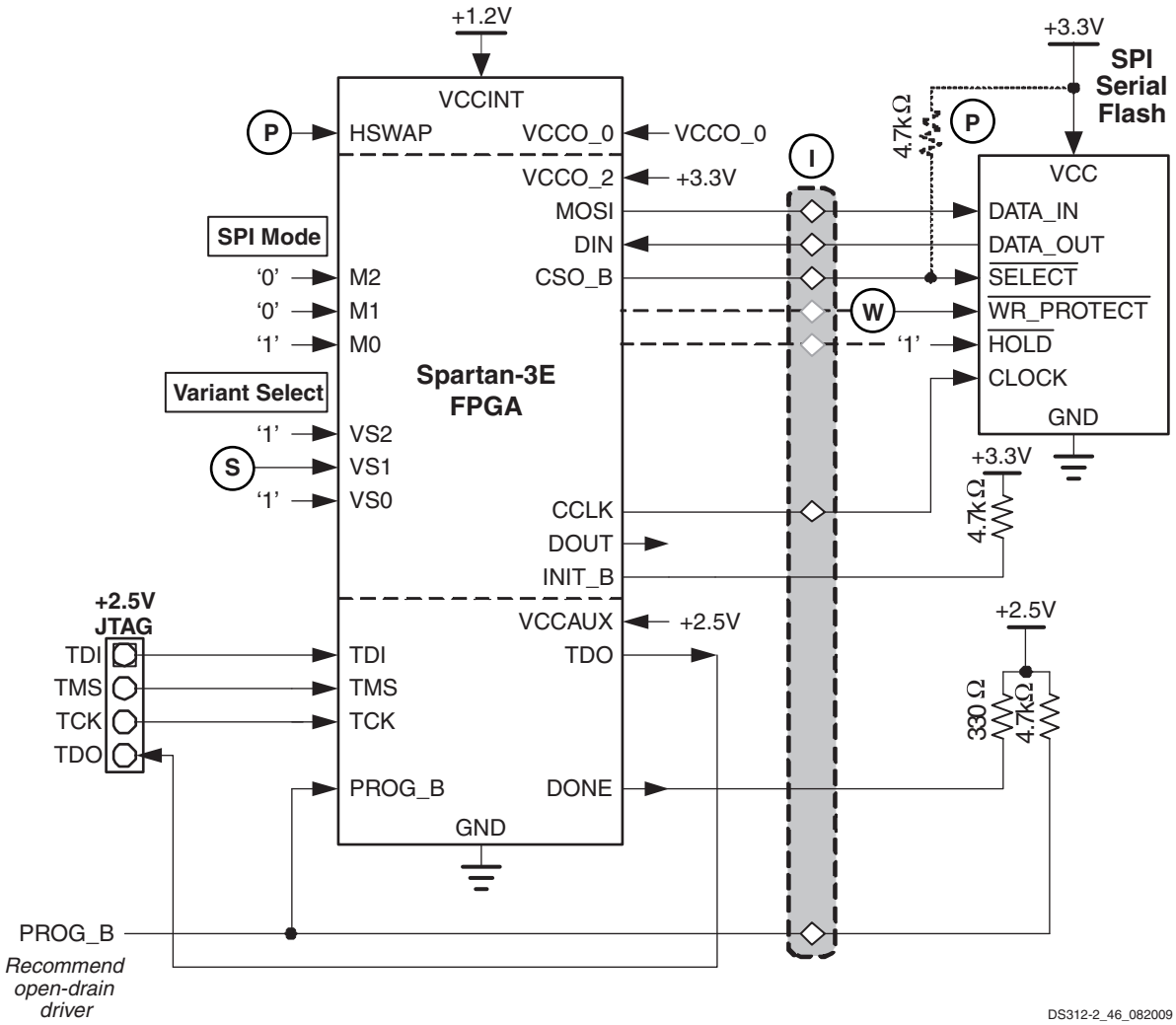


*Figure 53:* **SPI Flash PROM Interface for PROMs Supporting READ (0x03) and FAST_READ (0x0B) Commands**

S Although SPI is a standard four-wire interface, various available SPI Flash PROMs use different command protocols. The FPGA’s variant select pins, VS[2:0], define how the FPGA communicates with the SPI Flash, including which SPI Flash command the FPGA issues to start the read operation and the number of dummy bytes inserted before the FPGA expects to receive valid data from the SPI Flash. Table 53 shows the available SPI Flash PROMs expected to operate with Spartan-3E FPGAs. Other compatible devices might work but have not been tested for suitability with Spartan-3E FPGAs. All other VS[2:0] values are reserved for future use. Consult the data sheet for the desired SPI Flash device to determine its suitability. The basic timing requirements and waveforms are provided in Serial Peripheral Interface (SPI) Configuration Timing in Module 3.

Figure 53 shows the general connection diagram for those SPI Flash PROMs that support the 0x03 READ command or the 0x0B FAST READ commands.

Figure 54 shows the connection diagram for Atmel DataFlash serial PROMs, which also use an SPI-based protocol. ‘B’-series DataFlash devices are limited to FPGA applications operating over the commercial temperature range. Industrial temperature range applications must use ‘C’- or ‘D’-series DataFlash devices, which have a shorter DataFlash select setup time, because of the faster FPGA CCLK frequency at cold temperatures.

*Table 53:* **Variant Select Codes for Various SPI Serial Flash PROMs**

| VS2 | VS1 | VS0 | SPI Read Command | Dummy Bytes | SPI Serial Flash Vendor | SPI Flash Family | iMPACT Programming Support |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | FAST READ (0x0B) (see Figure 53) | 1 | STMicroelectronics (ST) | M25Pxx<br>M25PExx/M45PExx | Yes |
| | | | | | Atmel | AT45DB 'D'-Series Data Flash | Yes |
| | | | | | | AT26 / AT25(1) | |
| | | | | | Intel | S33 | |
| | | | | | Spansion *(AMD, Fujitsu)* | S25FLxxxA | |
| | | | | | Winbond *(NexFlash)* | NX25 / W25 | |
| | | | | | Macronix | MX25Lxxxx | |
| | | | | | Silicon Storage Technology (SST) | SST25LFxxxA<br>SST25VFxxxA | |
| | | | | | Programmable Microelectronics Corp. (PMC) | Pm25LVxxx | |
| | | | | | AMIC Technology | A25L | |
| | | | | | Eon Silicon Solution, Inc. | EN25 | |
| 1 | 0 | 1 | READ (0x03) (see Figure 53) | 0 | STMicroelectronics (ST) | M25Pxx<br>M25PExx/M45PExx | Yes |
| | | | | | Spansion *(AMD, Fujitsu)* | S25FLxxxA | |
| | | | | | Winbond *(NexFlash)* | NX25 / W25 | |
| | | | | | Macronix | MX25Lxxxx | |
| | | | | | Silicon Storage Technology (SST) | SST25LFxxxA<br>SST25VFxxxA<br>SST25VFxxx | |
| | | | | | Programmable Microelectronics Corp. (PMC) | Pm25LVxxx | |
| 1 | 1 | 0 | READ ARRAY (0xE8) (see Figure 54) | 4 | Atmel Corporation | AT45DB DataFlash *(use only 'C' or 'D' Series for Industrial temperature range)* | Yes |
| Others | | | Reserved | | | | |

**Notes:**
1. See iMPACT documentation for specific device support.

***WRITER NOTE:*** Many of the URLs in this table are obsolete or otherwise broken.

During the configuration process, CCLK is controlled by the FPGA and limited to the frequencies generated by the FPGA. After configuration, the FPGA application can use other clock signals to drive the CCLK pin and can further optimize SPI-based communication.

Refer to the individual SPI peripheral data sheet for specific interface and communication protocol requirements.

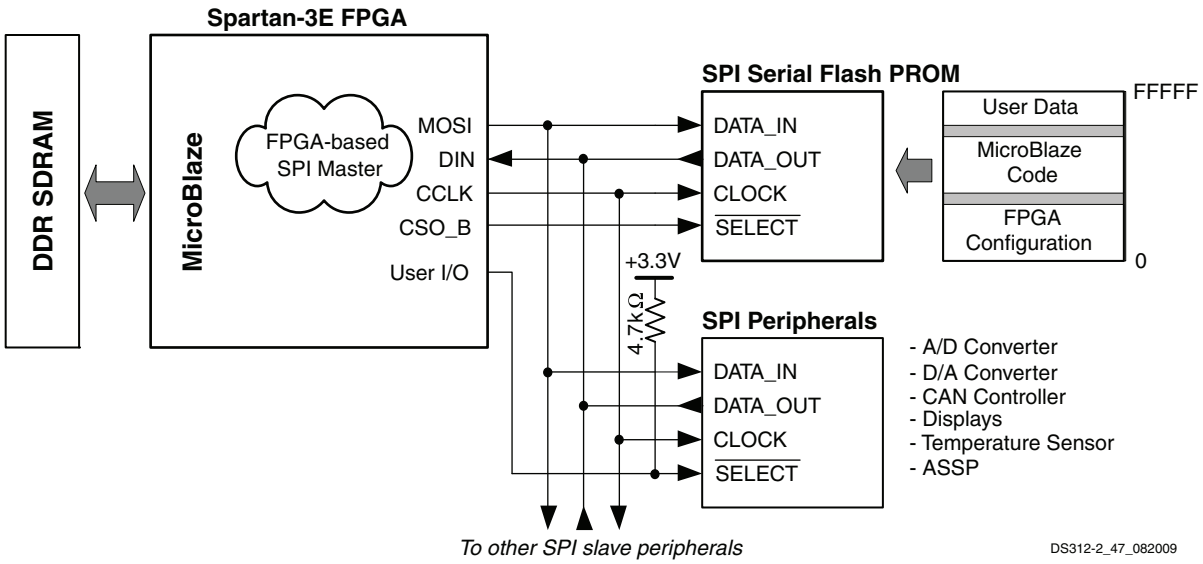


*Figure 56:* **Using the SPI Flash Interface After Configuration**

Also, in a multi-FPGA daisy-chain configuration of more than two devices, all intermediate FPGAs between the first and last devices must be Spartan-3E or Virtex-5 FPGAs. The last FPGA in the chain can be from any Xilinx FPGA family.

### BPI Mode Interaction with Right and Bottom Edge Global Clock Inputs

Some of the BPI mode configuration pins are shared with global clock inputs along the right and bottom edges of the device (Bank 1 and Bank 2, respectively). These pins are not easily reclaimable for clock inputs after configuration, especially if the FPGA application access the parallel NOR Flash after configuration. Table 64 summarizes the shared pins.

*Table 64:* **Shared BPI Configuration Mode and Global Buffer Input Pins**

| Device Edge | Global Buffer Input Pin | BPI Mode Configuration Pin |
|---|---|---|
| Bottom | GCLK0 | RDWR_B |
| | GCLK2 | D2 |
| | GCLK3 | D1 |
| | GCLK12 | D7 |
| | GCLK13 | D6 |
| | GCLK14 | D4 |
| | GCLK15 | D3 |
| Right | RHCLK0 | A10 |
| | RHCLK1 | A9 |
| | RHCLK2 | A8 |
| | RHCLK3 | A7 |
| | RHCLK4 | A6 |
| | RHCLK5 | A5 |
| | RHCLK6 | A4 |
| | RHCLK7 | A3 |

can also be eliminated from the interface. However, RDWR_B must remain Low during configuration.

After configuration, all of the interface pins except DONE and PROG_B are available as user I/Os. Alternatively, the bidirectional SelectMAP configuration interface is available after configuration. To continue using SelectMAP mode, set the ***Persist*** bitstream generator option to ***Yes***. The external host can then read and verify configuration data.

The Persist option will maintain A20-A23 as configuration pins although they are not used in SelectMAP mode.

The Slave Parallel mode is also used with BPI mode to create multi-FPGA daisy-chains. The lead FPGA is set for BPI mode configuration; all the downstream daisy-chain FPGAs are set for Slave Parallel configuration, as highlighted in Figure 59.

*Table 65:* **Slave Parallel Mode Connections**

| Pin Name | FPGA Direction | Description | During Configuration | After Configuration |
|---|---|---|---|---|
| HSWAP | Input | **User I/O Pull-Up Control**. When Low during configuration, enables pull-up resistors in all I/O pins to respective I/O bank $V_{CCO}$ input.<br>0: Pull-ups during configuration<br>1: No pull-ups | Drive at valid logic level throughout configuration. | User I/O |
| M[2:0] | Input | **Mode Select**. Selects the FPGA configuration mode. See Design Considerations for the HSWAP, M[2:0], and VS[2:0] Pins. | M2 = 1, M1 = 1, M0 = 0 Sampled when INIT_B goes High. | User I/O |
| D[7:0] | Input | **Data Input**. | Byte-wide data provided by host. FPGA captures data on rising CCLK edge. | User I/O. If bitstream option ***Persist=Yes***, becomes part of SelectMap parallel peripheral interface. |
| BUSY | Output | **Busy Indicator**. | If CCLK frequency is < 50 MHz, this pin may be ignored. When High, indicates that the FPGA is not ready to receive additional configuration data. Host must hold data an additional clock cycle. | User I/O. If bitstream option ***Persist=Yes***, becomes part of SelectMap parallel peripheral interface. |
| CSI_B | Input | **Chip Select Input**. Active Low. | Must be Low throughout configuration. | User I/O. If bitstream option ***Persist=Yes***, becomes part of SelectMap parallel peripheral interface. |
| RDWR_B | Input | **Read/Write Control**. Active Low write enable. | Must be Low throughout configuration. | User I/O. If bitstream option ***Persist=Yes***, becomes part of SelectMap parallel peripheral interface. |
| CCLK | Input | **Configuration Clock**. If CCLK PCB trace is long or has multiple connections, terminate this output to maintain signal integrity. See CCLK Design Considerations. | External clock. | User I/O If bitstream option ***Persist=Yes***, becomes part of SelectMap parallel peripheral interface. |
| CSO_B | Output | **Chip Select Output**. Active Low. | Not used in single FPGA applications. In a daisy-chain configuration, this pin connects to the CSI_B pin of the next FPGA in the chain. Actively drives. | User I/O |

## Bitstream Generator (BitGen) Options

For additional information, refer to the "Configuration Bitstream Generator (BitGen) Settings" chapter in UG332.

Various Spartan-3E FPGA functions are controlled by specific bits in the configuration bitstream image. These values are specified when creating the bitstream image with the Bitstream Generator (BitGen) software.

Table 69 provides a list of all BitGen options for Spartan-3E FPGAs.

*Table 69:* **Spartan-3E FPGA Bitstream Generator (BitGen) Options**

| Option Name | Pins/Function Affected | Values (***default***) | Description |
|---|---|---|---|
| ConfigRate | CCLK, Configuration | ***1***, 3, 6, 12, 25, 50 | Sets the approximate frequency, in MHz, of the internal oscillator using for Master Serial, SPI, and BPI configuration modes. The internal oscillator powers up at its lowest frequency, and the new setting is loaded as part of the configuration bitstream. The software default value is 1 (~1.5 MHz) starting with ISE 8.1, Service Pack 1. |
| StartupClk | Configuration, Startup | ***Cclk*** | ***Default.*** The CCLK signal (internally or externally generated) controls the startup sequence when the FPGA transitions from configuration mode to the user mode. See Start-Up. |
| | | UserClk | A clock signal from within the FPGA application controls the startup sequence when the FPGA transitions from configuration mode to the user mode. See Start-Up. The FPGA application supplies the user clock on the CLK pin on the STARTUP_SPARTAN3E primitive. |
| | | Jtag | The JTAG TCK input controls the startup sequence when the FPGA transitions from the configuration mode to the user mode. See Start-Up. |
| UnusedPin | Unused I/O Pins | ***Pulldown*** | ***Default.*** All unused I/O pins and input-only pins have a pull-down resistor to GND. |
| | | Pullup | All unused I/O pins and input-only pins have a pull-up resistor to the VCCO_# supply for its associated I/O bank. |
| | | Pullnone | All unused I/O pins and input-only pins are left floating (Hi-Z, high-impedance, three-state). Use external pull-up or pull-down resistors or logic to apply a valid signal level. |
| DONE_cycle | DONE pin, Configuration Startup | 1, 2, 3, ***4***, 5, 6 | Selects the Configuration Startup phase that activates the FPGA's DONE pin. See Start-Up. |
| GWE_cycle | All flip-flops, LUT RAMs, and SRL16 shift registers, Block RAM, Configuration Startup | 1, 2, 3, 4, 5, ***6*** | Selects the Configuration Startup phase that asserts the internal write-enable signal to all flip-flops, LUT RAMs and shift registers (SRL16). It also enables block RAM read and write operations. See Start-Up. |
| | | Done | Waits for the DONE pin input to go High before asserting the internal write-enable signal to all flip-flops, LUT RAMs and shift registers (SRL16). Block RAM read and write operations are enabled at this time. |
| | | Keep | Retains the current GWE_cycle setting for partial reconfiguration applications. |
| GTS_cycle | All I/O pins, Configuration | 1, 2, 3, 4, ***5***, 6 | Selects the Configuration Startup phase that releases the internal three-state control, holding all I/O buffers in high-impedance (Hi-Z). Output buffers actively drive, if so configured, after this point. See Start-Up. |
| | | Done | Waits for the DONE pin input to go High before releasing the internal three-state control, holding all I/O buffers in high-impedance (Hi-Z). Output buffers actively drive, if so configured, after this point. |
| | | Keep | Retains the current GTS_cycle setting for partial reconfiguration applications. |
| LCK_cycle | DCMs, Configuration Startup | ***NoWait*** | The FPGA does not wait for selected DCMs to lock before completing configuration. |
| | | 0, 1, 2, 3, 4, 5, 6 | If one or more DCMs in the design have the STARTUP_WAIT attribute set to TRUE, the FPGA waits for such DCMs to acquire their respective input clock and assert their LOCKED output. This setting selects the Configuration Startup phase where the FPGA waits for the DCMs to lock. |
| DonePin | DONE pin | ***Pullup*** | Internally connects a pull-up resistor between DONE pin and $V_{CCAUX}$. An external 330 Ω pull-up resistor to $V_{CCAUX}$ is still recommended. |
| | | Pullnone | No internal pull-up resistor on DONE pin. An external 330 Ω pull-up resistor to $V_{CCAUX}$ is required. |

## I/O Timing

*Table 86:* **Pin-to-Pin Clock-to-Output Times for the IOB Output Path**

| Symbol | Description | Conditions | Device | Speed Grade | | Units |
|---|---|---|---|---|---|---|
| | | | | -5 | -4 | |
| | | | | Max[2] | Max[2] | |
| **Clock-to-Output Times** | | | | | | |
| $T_{ICKOFDCM}$ | When reading from the Output Flip-Flop (OFF), the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is used. | LVCMOS25[3], 12 mA output drive, Fast slew rate, with DCM[4] | XC3S100E | 2.66 | 2.79 | ns |
| | | | XC3S250E | 3.00 | 3.45 | ns |
| | | | XC3S500E | 3.01 | 3.46 | ns |
| | | | XC3S1200E | 3.01 | 3.46 | ns |
| | | | XC3S1600E | 3.00 | 3.45 | ns |
| $T_{ICKOF}$ | When reading from OFF, the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is not used. | LVCMOS25[3], 12 mA output drive, Fast slew rate, without DCM | XC3S100E | 5.60 | 5.92 | ns |
| | | | XC3S250E | 4.91 | 5.43 | ns |
| | | | XC3S500E | 4.98 | 5.51 | ns |
| | | | XC3S1200E | 5.36 | 5.94 | ns |
| | | | XC3S1600E | 5.45 | 6.05 | ns |

**Notes:**

1. The numbers in this table are tested using the methodology presented in Table 95 and are based on the operating conditions set forth in Table 77 and Table 80.
2. For minimums, use the values reported by the Xilinx timing analyzer.
3. This clock-to-output time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or a standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. If the former is true, *add* the appropriate Input adjustment from Table 91. If the latter is true, *add* the appropriate Output adjustment from Table 94.
4. DCM output jitter is included in all measurements.

*Table 121:* **Configuration Timing Requirements for Attached Parallel NOR Flash**

| Symbol | Description | Requirement | Units |
|---|---|---|---|
| $T_{CE}$ ($t_{ELQV}$) | Parallel NOR Flash PROM chip-select time | $T_{CE} \leq T_{INITADDR}$ | ns |
| $T_{OE}$ ($t_{GLQV}$) | Parallel NOR Flash PROM output-enable time | $T_{OE} \leq T_{INITADDR}$ | ns |
| $T_{ACC}$ ($t_{AVQV}$) | Parallel NOR Flash PROM read access time | $T_{ACC} \leq 0.5\,T_{CCLKn(min)} - T_{CCO} - T_{DCC} - PCB$ | ns |
| $T_{BYTE}$ ($t_{FLQV}$, $t_{FHQV}$) | For x8/x16 PROMs only: BYTE# to output valid time(3) | $T_{BYTE} \leq T_{INITADDR}$ | ns |

**Notes:**

1. These requirements are for successful FPGA configuration in BPI mode, where the FPGA provides the CCLK frequency. The post configuration timing can be different to support the specific needs of the application loaded int o the FPGA and the resulting clock source.
2. Subtract additional printed circuit board routing delay as required by the application.
3. The initial BYTE# timing can be extended using an external, appropriately sized pull-down resistor on the FPGA's LDC2 pin. The resistor value also depends on whether the FPGA's HSWAP pin is High or Low.

*Table 122:* **MultiBoot Trigger (MBT) Timing**

| Symbol | Description | Minimum | Maximum | Units |
|---|---|---|---|---|
| $T_{MBT}$ | MultiBoot Trigger (MBT) Low pulse width required to initiate MultiBoot reconfiguration | 300 | ∞ | ns |

**Notes:**

1. MultiBoot re-configuration starts on the rising edge after MBT is Low for at least the prescribed minimum period.

## CP132 Footprint

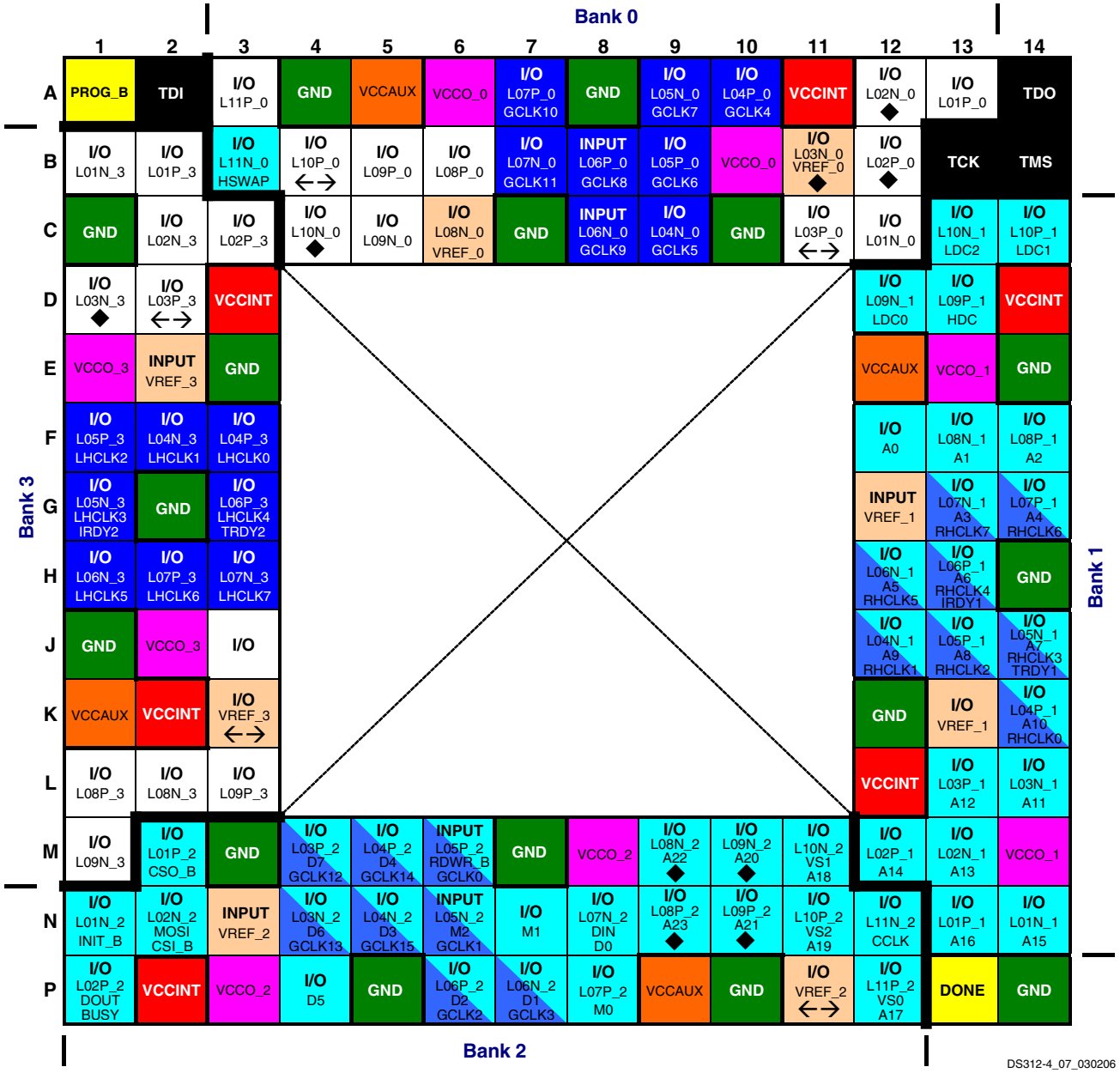


*Figure 81:* **CP132 Package Footprint (top view)**

| | | | | | |
|---|---|---|---|---|---|
| 16-22 | **I/O:** Unrestricted, general-purpose user I/O | 42-46 | **DUAL:** Configuration pin, then possible user I/O | 7-8 | **VREF:** User I/O or input voltage reference for bank |
| 0-2 | **INPUT:** Unrestricted, general-purpose input pin | 16 | **CLK:** User I/O, input, or global buffer input | 8 | **VCCO:** Output voltage supply for bank |
| 2 | **CONFIG:** Dedicated configuration pins | 4 | **JTAG:** Dedicated JTAG port pins | 6 | **VCCINT:** Internal core supply voltage (+1.2V) |
| 9 | **N.C.:** Unconnected balls on the XC3S100E FPGA (◆) | 16 | **GND:** Ground | 4 | **VCCAUX:** Auxiliary supply voltage (+2.5V) |

*Table 137:* **TQ144 Package Pinout *(Cont'd)***

| Bank | XC3S100E Pin Name | XC3S250E Pin Name | TQ144 Pin | Type |
|---|---|---|---|---|
| GND | GND | GND | P27 | GND |
| GND | GND | GND | P37 | GND |
| GND | GND | GND | P46 | GND |
| GND | GND | GND | P55 | GND |
| GND | GND | GND | P61 | GND |
| GND | GND | GND | P73 | GND |
| GND | GND | GND | P90 | GND |
| GND | GND | GND | P99 | GND |
| GND | GND | GND | P118 | GND |
| GND | GND | GND | P127 | GND |
| GND | GND | GND | P133 | GND |
| VCCAUX | DONE | DONE | P72 | CONFIG |
| VCCAUX | PROG_B | PROG_B | P1 | CONFIG |
| VCCAUX | TCK | TCK | P110 | JTAG |
| VCCAUX | TDI | TDI | P144 | JTAG |
| VCCAUX | TDO | TDO | P109 | JTAG |
| VCCAUX | TMS | TMS | P108 | JTAG |
| VCCAUX | VCCAUX | VCCAUX | P30 | VCCAUX |
| VCCAUX | VCCAUX | VCCAUX | P65 | VCCAUX |
| VCCAUX | VCCAUX | VCCAUX | P102 | VCCAUX |
| VCCAUX | VCCAUX | VCCAUX | P137 | VCCAUX |
| VCCINT | VCCINT | VCCINT | P9 | VCCINT |
| VCCINT | VCCINT | VCCINT | P45 | VCCINT |
| VCCINT | VCCINT | VCCINT | P80 | VCCINT |
| VCCINT | VCCINT | VCCINT | P115 | VCCINT |

## User I/Os by Bank

Table 144, Table 145, and Table 146 indicate how the available user-I/O pins are distributed between the four I/O banks on the FT256 package.

The XC3S250E FPGA in the FT256 package has 18 unconnected balls, labeled with an "N.C." type. These pins are also indicated with the black diamond (◆) symbol in Figure 85.

*Table 144:* **User I/Os Per Bank on XC3S250E in the FT256 Package**

| Package Edge | I/O Bank | Maximum I/O | All Possible I/O Pins by Type | | | | |
|---|---|---|---|---|---|---|---|
| | | | I/O | INPUT | DUAL | VREF(1) | CLK(2) |
| Top | 0 | 44 | 20 | 10 | 1 | 5 | 8 |
| Right | 1 | 42 | 10 | 7 | 21 | 4 | 0(2) |
| Bottom | 2 | 44 | 8 | 9 | 24 | 3 | 0(2) |
| Left | 3 | 42 | 24 | 7 | 0 | 3 | 8 |
| **TOTAL** | | **172** | **62** | **33** | **46** | **15** | **16** |

**Notes:**

1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

*Table 145:* **User I/Os Per Bank on XC3S500E in the FT256 Package**

| Package Edge | I/O Bank | Maximum I/O | All Possible I/O Pins by Type | | | | |
|---|---|---|---|---|---|---|---|
| | | | I/O | INPUT | DUAL | VREF(1) | CLK(2) |
| Top | 0 | 46 | 22 | 10 | 1 | 5 | 8 |
| Right | 1 | 48 | 15 | 7 | 21 | 5 | 0(2) |
| Bottom | 2 | 48 | 11 | 9 | 24 | 4 | 0(2) |
| Left | 3 | 48 | 28 | 7 | 0 | 5 | 8 |
| **TOTAL** | | **190** | **76** | **33** | **46** | **19** | **16** |

**Notes:**

1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

*Table 146:* **User I/Os Per Bank on XC3S1200E in the FT256 Package**

| Package Edge | I/O Bank | Maximum I/O | All Possible I/O Pins by Type | | | | |
|---|---|---|---|---|---|---|---|
| | | | I/O | INPUT | DUAL | VREF(1) | CLK(2) |
| Top | 0 | 46 | 24 | 8 | 1 | 5 | 8 |
| Right | 1 | 48 | 14 | 8 | 21 | 5 | 0(2) |
| Bottom | 2 | 48 | 13 | 7 | 24 | 4 | 0(2) |
| Left | 3 | 48 | 27 | 8 | 0 | 5 | 8 |
| **TOTAL** | | **190** | **78** | **31** | **46** | **19** | **16** |

**Notes:**

1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

*Table 148:* **FG320 Package Pinout *(Cont'd)***

| Bank | XC3S500E Pin Name | XC3S1200E Pin Name | XC3S1600E Pin Name | FG320 Ball | Type |
|---|---|---|---|---|---|
| 0 | VCCO_0 | VCCO_0 | VCCO_0 | A9 | VCCO |
| 0 | VCCO_0 | VCCO_0 | VCCO_0 | C6 | VCCO |
| 0 | VCCO_0 | VCCO_0 | VCCO_0 | C13 | VCCO |
| 0 | VCCO_0 | VCCO_0 | VCCO_0 | G8 | VCCO |
| 0 | VCCO_0 | VCCO_0 | VCCO_0 | G11 | VCCO |
| 1 | N.C. (◆) | IO | IO | P16 | **500E:** N.C.<br>**1200E:** I/O<br>**1600E:** I/O |
| 1 | IO_L01N_1/A15 | IO_L01N_1/A15 | IO_L01N_1/A15 | T17 | DUAL |
| 1 | IO_L01P_1/A16 | IO_L01P_1/A16 | IO_L01P_1/A16 | U18 | DUAL |
| 1 | IO_L02N_1/A13 | IO_L02N_1/A13 | IO_L02N_1/A13 | T18 | DUAL |
| 1 | IO_L02P_1/A14 | IO_L02P_1/A14 | IO_L02P_1/A14 | R18 | DUAL |
| 1 | IO_L03N_1/VREF_1 | IO_L03N_1/VREF_1 | IO_L03N_1/VREF_1 | R16 | VREF |
| 1 | IO_L03P_1 | IO_L03P_1 | IO_L03P_1 | R15 | I/O |
| 1 | N.C. (◆) | IO_L04N_1 | IO_L04N_1 | N14 | **500E:** N.C.<br>**1200E:** I/O<br>**1600E:** I/O |
| 1 | N.C. (◆) | IO_L04P_1 | IO_L04P_1 | N15 | **500E:** N.C.<br>**1200E:** I/O<br>**1600E:** I/O |
| 1 | IO_L05N_1/VREF_1 | IO_L05N_1/VREF_1 | IO_L05N_1/VREF_1 | M13 | VREF |
| 1 | IO_L05P_1 | IO_L05P_1 | IO_L05P_1 | M14 | I/O |
| 1 | IO_L06N_1 | IO_L06N_1 | IO_L06N_1 | P18 | I/O |
| 1 | IO_L06P_1 | IO_L06P_1 | IO_L06P_1 | P17 | I/O |
| 1 | IO_L07N_1 | IO_L07N_1 | IO_L07N_1 | M16 | I/O |
| 1 | IO_L07P_1 | IO_L07P_1 | IO_L07P_1 | M15 | I/O |
| 1 | IO_L08N_1 | IO_L08N_1 | IO_L08N_1 | M18 | I/O |
| 1 | IO_L08P_1 | IO_L08P_1 | IO_L08P_1 | N18 | I/O |
| 1 | IO_L09N_1/A11 | IO_L09N_1/A11 | IO_L09N_1/A11 | L15 | DUAL |
| 1 | IO_L09P_1/A12 | IO_L09P_1/A12 | IO_L09P_1/A12 | L16 | DUAL |
| 1 | IO_L10N_1/VREF_1 | IO_L10N_1/VREF_1 | IO_L10N_1/VREF_1 | L17 | VREF |
| 1 | IO_L10P_1 | IO_L10P_1 | IO_L10P_1 | L18 | I/O |
| 1 | IO_L11N_1/A9/RHCLK1 | IO_L11N_1/A9/RHCLK1 | IO_L11N_1/A9/RHCLK1 | K12 | RHCLK/DUAL |
| 1 | IO_L11P_1/A10/RHCLK0 | IO_L11P_1/A10/RHCLK0 | IO_L11P_1/A10/RHCLK0 | K13 | RHCLK/DUAL |
| 1 | IO_L12N_1/A7/RHCLK3/ TRDY1 | IO_L12N_1/A7/RHCLK3/ TRDY1 | IO_L12N_1/A7/RHCLK3/ TRDY1 | K14 | RHCLK/DUAL |
| 1 | IO_L12P_1/A8/RHCLK2 | IO_L12P_1/A8/RHCLK2 | IO_L12P_1/A8/RHCLK2 | K15 | RHCLK/DUAL |
| 1 | IO_L13N_1/A5/RHCLK5 | IO_L13N_1/A5/RHCLK5 | IO_L13N_1/A5/RHCLK5 | J16 | RHCLK/DUAL |
| 1 | IO_L13P_1/A6/RHCLK4/ IRDY1 | IO_L13P_1/A6/RHCLK4/ IRDY1 | IO_L13P_1/A6/RHCLK4/ IRDY1 | J17 | RHCLK/DUAL |
| 1 | IO_L14N_1/A3/RHCLK7 | IO_L14N_1/A3/RHCLK7 | IO_L14N_1/A3/RHCLK7 | J14 | RHCLK/DUAL |
| 1 | IO_L14P_1/A4/RHCLK6 | IO_L14P_1/A4/RHCLK6 | IO_L14P_1/A4/RHCLK6 | J15 | RHCLK/DUAL |
| 1 | IO_L15N_1/A1 | IO_L15N_1/A1 | IO_L15N_1/A1 | J13 | DUAL |
| 1 | IO_L15P_1/A2 | IO_L15P_1/A2 | IO_L15P_1/A2 | J12 | DUAL |
| 1 | IO_L16N_1/A0 | IO_L16N_1/A0 | IO_L16N_1/A0 | H17 | DUAL |
| 1 | IO_L16P_1 | IO_L16P_1 | IO_L16P_1 | H16 | I/O |

## Revision History

The following table shows the revision history for this document.

| Date | Version | Revision |
|---|---|---|
| 03/01/05 | 1.0 | Initial Xilinx release. |
| 03/21/05 | 1.1 | Added XC3S250E in the CP132 package to Table 129. Corrected number of differential I/O pairs on CP132. Added pinout and footprint information for the CP132, FG400, and FG484 packages. Removed IRDY and TRDY pins from the VQ100, TQ144, and PQ208 packages. |
| 11/23/05 | 2.0 | Corrected title of Table 153. Updated differential pair numbering for some pins in Bank 0 of the FG400 package, affecting Table 152 and Figure 87. Pin functionality and ball assignment were not affected. Added Package Thermal Characteristics section. Added package mass values to Table 125. |
| 03/22/06 | 3.0 | Included I/O pins, not just input-only pins under the VREF description in Table 124. Clarified that some global clock inputs are Input-only pins in Table 124. Added information on the XC3S100E in the CP132 package, affecting Table 129, Table 130, Table 133, Table 134, Table 136, and Figure 81. Ball A12 on the XC3S1600E in the FG320 package a full I/O pin, not an Input-only pin. Corrected the I/O counts for the XC3S1600E in the FG320 package, affecting Table 129, Table 150, Table 151, and Figure 86. Corrected pin type for XC3S1600E balls N14 and N15 in Table 148. |
| 05/19/06 | 3.1 | Minor text edits. |
| 11/09/06 | 3.4 | Added package thermal data for the XC3S100E in the CP132 package to Table 130. Corrected pin migration arrows for balls E17 and F4 between the XC3S500E and XC3S1600E in Table 151. Promoted Module 4 to Production status. Synchronized all modules to v3.4. |
| 03/16/07 | 3.5 | Minor formatting changes. |
| 05/29/07 | 3.6 | Corrected ‘Lxx’ to ‘Lxxy’ in Table 124. Noted that some GCLK and VREF pins are on INPUT pins in Table 124 and Table 129. Added link before Table 127 to Material Declaration Data Sheets. |
| 04/18/08 | 3.7 | Added XC3S500E VQG100 package. Added Material Declaration Data Sheet links in Table 127. Updated Thermal Characteristics in Table 130. Updated links. |
| 08/26/09 | 3.8 | Minor typographical updates. |
| 10/29/12 | 4.0 | Added Notice of Disclaimer. This product is not recommended for new designs.<br>Updated the XC3S250E-FT256 in Table 129. |

## Notice of Disclaimer