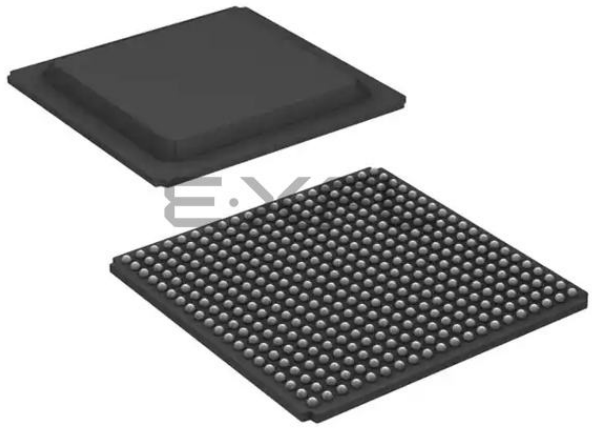
AMD Xilinx - XC3S1200E-5FGG400C Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	2168
Number of Logic Elements/Cells	19512
Total RAM Bits	516096
Number of I/O	304
Number of Gates	1200000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	400-BGA
Supplier Device Package	400-FBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s1200e-5fgg400c

Architectural Overview

The Spartan-3E family architecture consists of five fundamental programmable functional elements:

- **Configurable Logic Blocks (CLBs)** contain flexible Look-Up Tables (LUTs) that implement logic plus storage elements used as flip-flops or latches. CLBs perform a wide variety of logical functions as well as store data.
- **Input/Output Blocks (IOBs)** control the flow of data between the I/O pins and the internal logic of the device. Each IOB supports bidirectional data flow plus 3-state operation. Supports a variety of signal standards, including four high-performance differential standards. Double Data-Rate (DDR) registers are included.
- **Block RAM** provides data storage in the form of 18-Kbit dual-port blocks.
- **Multiplier Blocks** accept two 18-bit binary numbers as inputs and calculate the product.
- **Digital Clock Manager (DCM) Blocks** provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase-shifting clock signals.

These elements are organized as shown in Figure 1. A ring of IOBs surrounds a regular array of CLBs. Each device has two columns of block RAM except for the XC3S100E, which has one column. Each RAM column consists of several 18-Kbit RAM blocks. Each block RAM is associated with a dedicated multiplier. The DCMs are positioned in the center with two at the top and two at the bottom of the device. The XC3S100E has only one DCM at the top and bottom, while the XC3S1200E and XC3S1600E add two DCMs in the middle of the left and right sides.

The Spartan-3E family features a rich network of traces that interconnect all five functional elements, transmitting signals among them. Each functional element has an associated switch matrix that permits multiple connections to the routing.

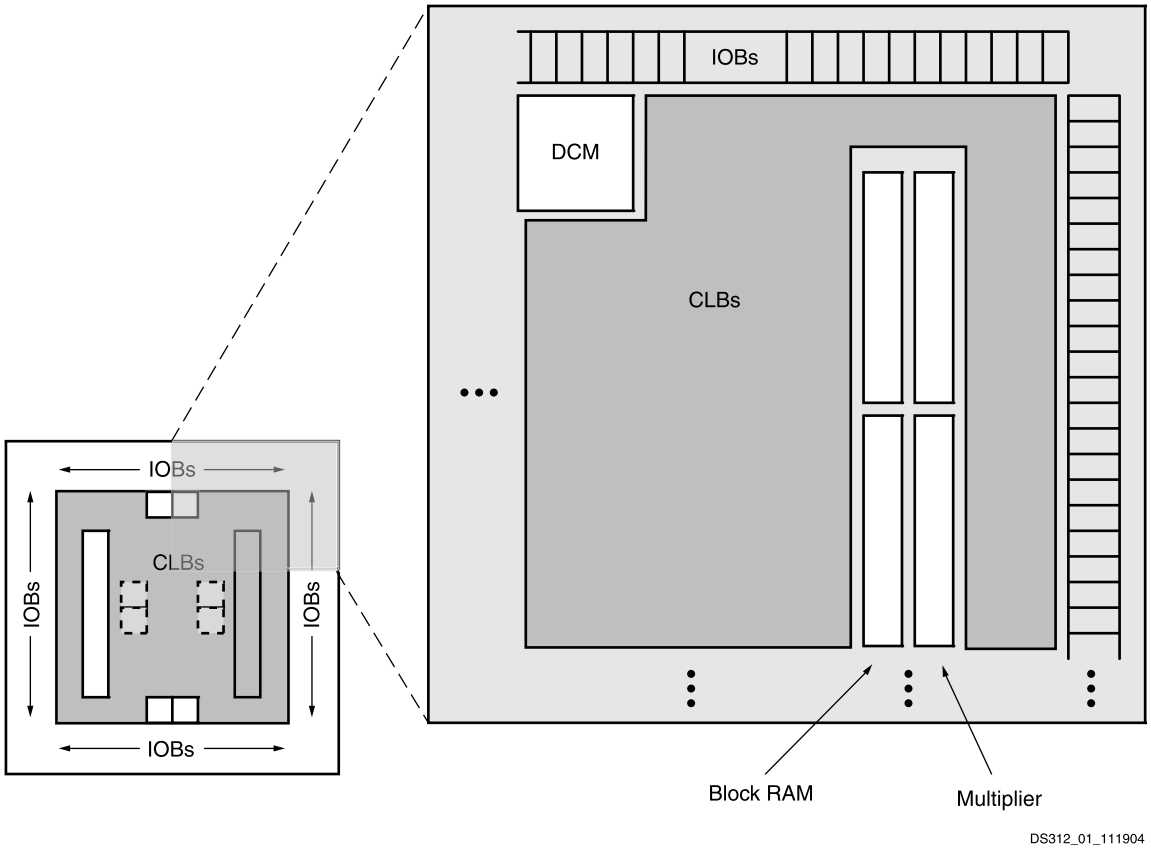

Figure 1: **Spartan-3E Family Architecture**

Configuration

Spartan-3E FPGAs are programmed by loading configuration data into robust, reprogrammable, static CMOS configuration latches (CCLs) that collectively control all functional elements and routing resources. The FPGA's configuration data is stored externally in a PROM or some other non-volatile medium, either on or off the board. After applying power, the configuration data is written to the FPGA using any of seven different modes:

- Master Serial from a Xilinx Platform Flash PROM
- Serial Peripheral Interface (SPI) from an industry-standard SPI serial Flash
- Byte Peripheral Interface (BPI) Up or Down from an industry-standard x8 or x8/x16 parallel NOR Flash
- Slave Serial, typically downloaded from a processor
- Slave Parallel, typically downloaded from a processor
- Boundary Scan (JTAG), typically downloaded from a processor or system tester.

Furthermore, Spartan-3E FPGAs support MultiBoot configuration, allowing two or more FPGA configuration bitstreams to be stored in a single parallel NOR Flash. The FPGA application controls which configuration to load next and when to load it.

I/O Capabilities

The Spartan-3E FPGA SelectIO interface supports many popular single-ended and differential standards. Table 2 shows the number of user I/Os as well as the number of differential I/O pairs available for each device/package combination.

Spartan-3E FPGAs support the following single-ended standards:

- 3.3V low-voltage TTL (LVTTL)
- Low-voltage CMOS (LVCMOS) at 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V
- 3V PCI at 33 MHz, and in some devices, 66 MHz
- HSTL I and III at 1.8V, commonly used in memory applications
- SSTL I at 1.8V and 2.5V, commonly used for memory applications

Spartan-3E FPGAs support the following differential standards:

- LVDS
- Bus LVDS
- mini-LVDS
- RSDS
- Differential HSTL (1.8V, Types I and III)
- Differential SSTL (2.5V and 1.8V, Type I)
- 2.5V LVPECL inputs

Table 2: **Available User I/Os and Differential (Diff) I/O Pairs**

Package	VQ100 VQG100		CP132 CPG132		TQ144 TQG144		PQ208 PQG208		FT256 FTG256		FG320 FGG320		FG400 FGG400		FG484 FGG484	
Footprint Size (mm)	**16 x 16**		**8 x 8**		**22 x 22**		**30.5 x 30.5**		**17 x 17**		**19 x 19**		**21 x 21**		**23 x 23**	
Device	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**
XC3S100E	**66**(2) *9(7)*	**30** *(2)*	**83** *(11)*	**35** *(2)*	**108** *(28)*	**40** *(4)*	-	-	-	-	-	-	-	-	-	-
XC3S250E	**66** *(7)*	**30** *(2)*	**92** *(7)*	**41** *(2)*	**108** *(28)*	**40** *(4)*	**158** *(32)*	**65** *(5)*	**172** *(40)*	**68** *(8)*	-	-	-	-	-	-
XC3S500E	**66**(3) *(7)*	**30** *(2)*	**92** *(7)*	**41** *(2)*	-	-	**158** *(32)*	**65** *(5)*	**190** *(41)*	**77** *(8)*	**232** *(56)*	**92** *(12)*	-	-	-	-
XC3S1200E	-	-	-	-	-	-	-	-	**190** *(40)*	**77** *(8)*	**250** *(56)*	**99** *(12)*	**304** *(72)*	**124** *(20)*	-	-
XC3S1600E	-	-	-	-	-	-	-	-	-	-	**250** *(56)*	**99** *(12)*	**304** *(72)*	**124** *(20)*	**376** *(82)*	**156** *(21)*

Notes:

1. All Spartan-3E devices provided in the same package are pin-compatible as further described in Module 4, Pinout Descriptions.
2. The number shown in **bold** indicates the maximum number of I/O and input-only pins. The number shown in (*italics*) indicates the number of input-only pins.
3. The XC3S500E is available in the VQG100 Pb-free package and not the standard VQ100. The VQG100 and VQ100 pin-outs are identical and general references to the VQ100 will apply to the XC3S500E.

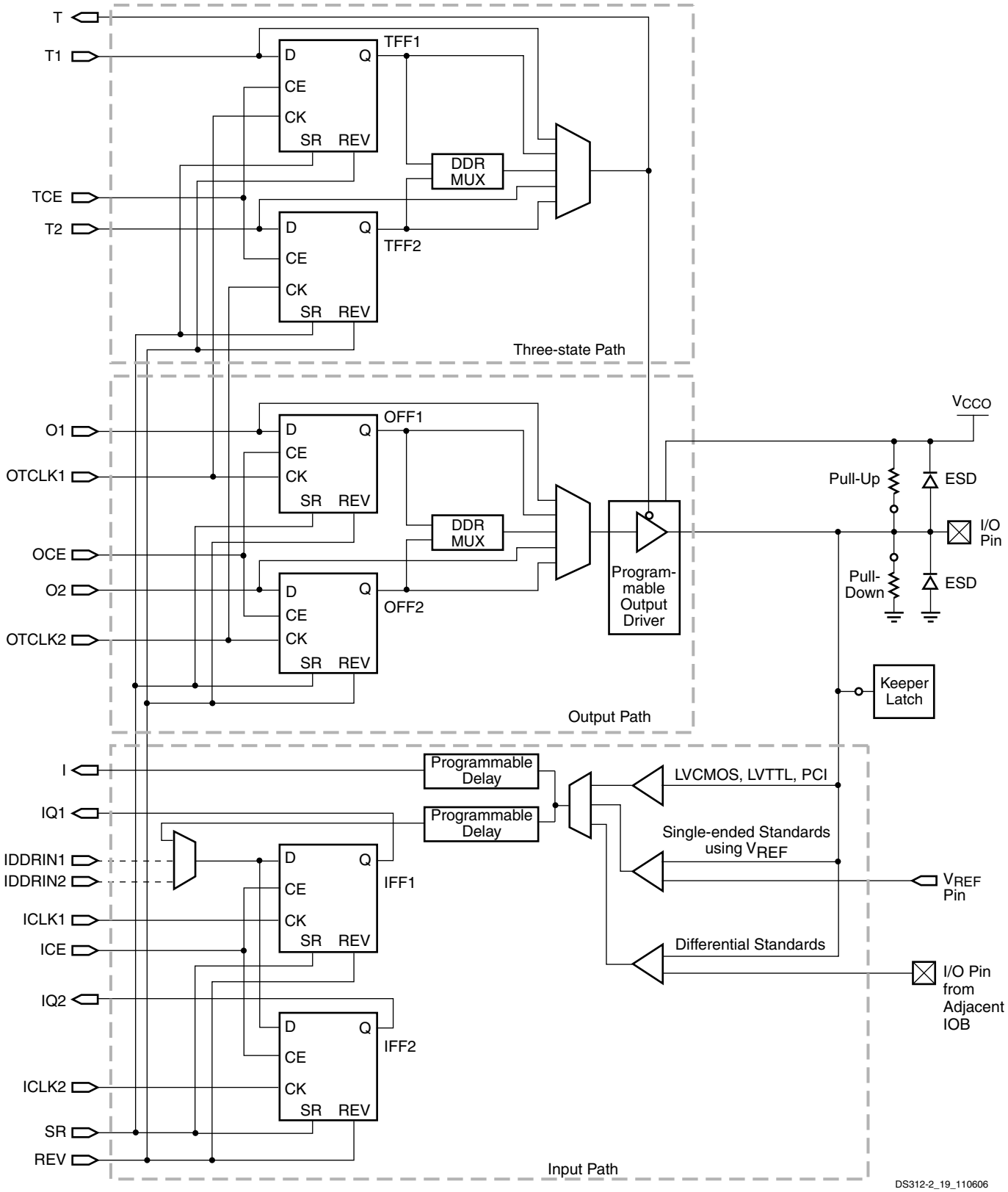

Figure 5: **Simplified IOB Diagram**

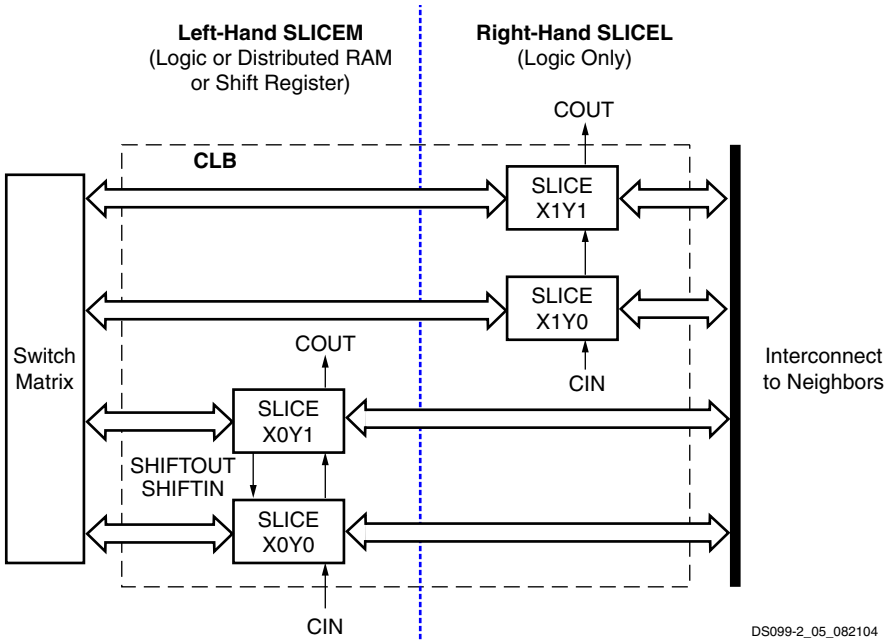

Figure 16: **Arrangement of Slices within the CLB**

Slice Location Designations

The Xilinx development software designates the location of a slice according to its X and Y coordinates, starting in the bottom left corner, as shown in Figure 14. The letter 'X' followed by a number identifies columns of slices, incrementing from the left side of the die to the right. The letter 'Y' followed by a number identifies the position of each slice in a pair as well as indicating the CLB row, incrementing from the bottom of the die. Figure 16 shows the CLB located in the lower left-hand corner of the die. The SLICEM always has an even 'X' number, and the SLICEL always has an odd 'X' number.

Slice Overview

A slice includes two LUT function generators and two storage elements, along with additional logic, as shown in Figure 17.

Both SLICEM and SLICEL have the following elements in common to provide logic, arithmetic, and ROM functions:

- Two 4-input LUT function generators, F and G
- Two storage elements
- Two wide-function multiplexers, F5MUX and FiMUX
- Carry and arithmetic logic

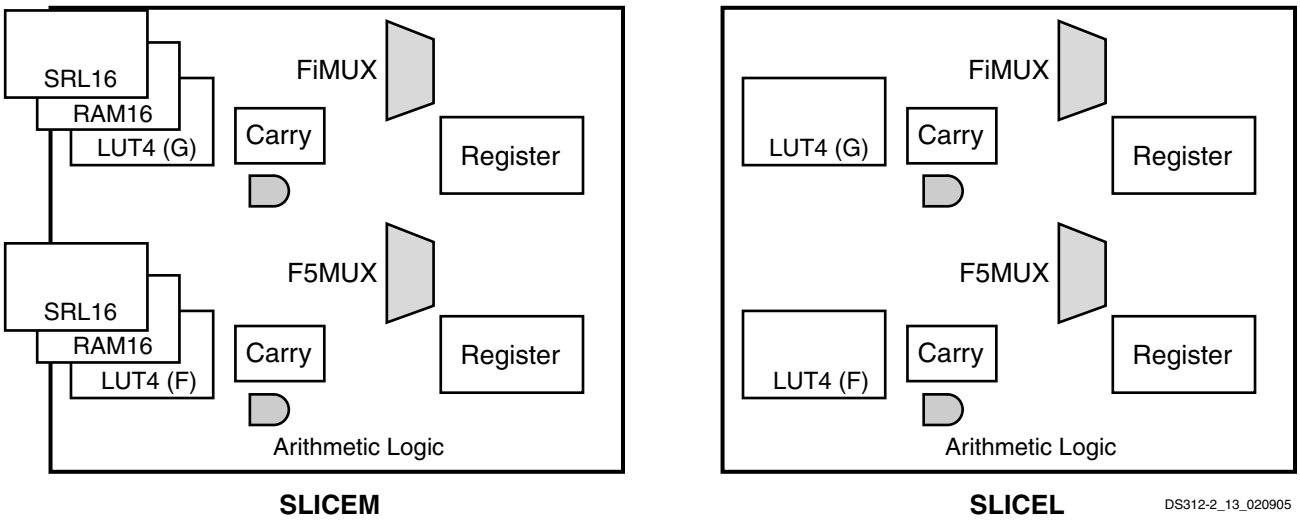

Figure 17: **Resources in a Slice**

Carry and Arithmetic Logic

For additional information, refer to the “Using Carry and Arithmetic Logic” chapter in UG331.

The carry chain, together with various dedicated arithmetic logic gates, support fast and efficient implementations of math operations. The carry logic is automatically used for most arithmetic functions in a design. The gates and multiplexers of the carry and arithmetic logic can also be used for general-purpose logic, including simple wide Boolean functions.

The carry chain enters the slice as CIN and exits as COUT, controlled by several multiplexers. The carry chain connects directly from one CLB to the CLB above. The carry chain can be initialized at any point from the BX (or BY) inputs.

The dedicated arithmetic logic includes the exclusive-OR gates XORF and XORG (upper and lower portions of the slice, respectively) as well as the AND gates GAND and FAND (upper and lower portions, respectively). These gates work in conjunction with the LUTs to implement efficient arithmetic functions, including counters and multipliers, typically at two bits per slice. See Figure 22 and Table 14.

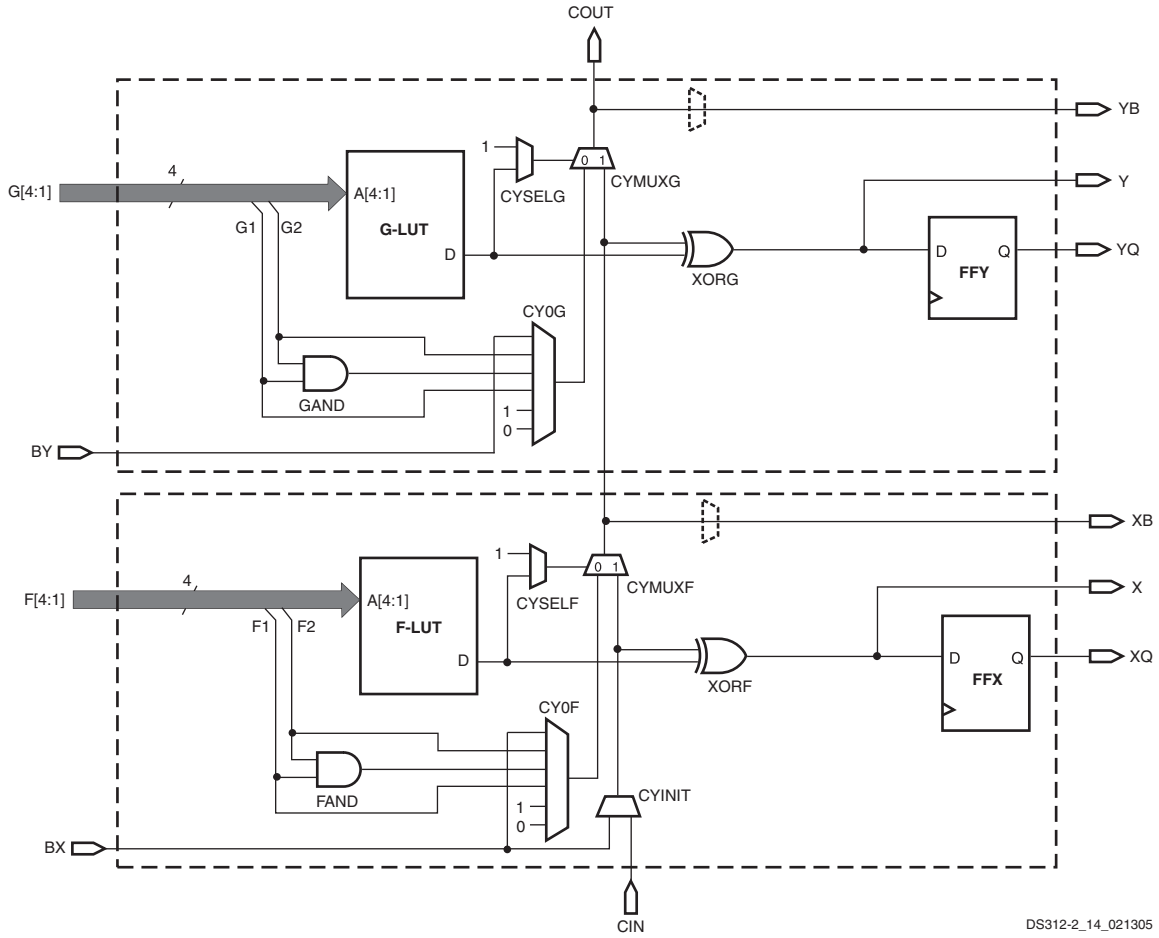

Figure 22: **Carry Logic**

Table 14: **Carry Logic Functions**

Function	Description
CYINIT	Initializes carry chain for a slice. Fixed selection of: · CIN carry input from the slice below · BX input
CY0F	Carry generation for bottom half of slice. Fixed selection of: · F1 or F2 inputs to the LUT (both equal 1 when a carry is to be generated) · FAND gate for multiplication · BX input for carry initialization · Fixed 1 or 0 input for use as a simple Boolean function

Table 55: **Serial Peripheral Interface (SPI) Connections *(Cont'd)***

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
VS[2:0] Ⓢ	Input	**Variant Select**. Instructs the FPGA how to communicate with the attached SPI Flash PROM. See Design Considerations for the HSWAP, M[2:0], and VS[2:0] Pins.	Must be at the logic levels shown in Table 53. Sampled when INIT_B goes High.	User I/O
MOSI	Output	**Serial Data Output**.	FPGA sends SPI Flash memory read commands and starting address to the PROM's serial data input.	User I/O
DIN	Input	**Serial Data Input**.	FPGA receives serial data from PROM's serial data output.	User I/O
CSO_B	Output	**Chip Select Output**. Active Low.	Connects to the SPI Flash PROM's chip-select input. If HSWAP = 1, connect this signal to a 4.7 kΩ pull-up resistor to 3.3V.	Drive CSO_B High after configuration to disable the SPI Flash and reclaim the MOSI, DIN, and CCLK pins. Optionally, re-use this pin and MOSI, DIN, and CCLK to continue communicating with SPI Flash.
CCLK	Output	**Configuration Clock**. Generated by FPGA internal oscillator. Frequency controlled by ***ConfigRate*** bitstream generator option. If CCLK PCB trace is long or has multiple connections, terminate this output to maintain signal integrity. See CCLK Design Considerations.	Drives PROM's clock input.	User I/O
DOUT	Output	**Serial Data Output**.	Actively drives. Not used in single-FPGA designs. In a daisy-chain configuration, this pin connects to DIN input of the next FPGA in the chain.	User I/O
INIT_B	Open-drain bidirectional I/O	**Initialization Indicator**. Active Low. Goes Low at start of configuration during Initialization memory clearing process. Released at end of memory clearing, when mode select pins are sampled. In daisy-chain applications, this signal requires an external 4.7 kΩ pull-up resistor to VCCO_2.	Active during configuration. If SPI Flash PROM requires > 2 ms to awake after powering on, hold INIT_B Low until PROM is ready. If CRC error detected during configuration, FPGA drives INIT_B Low.	User I/O. If unused in the application, drive INIT_B High.
DONE	Open-drain bidirectional I/O	**FPGA Configuration Done**. Low during configuration. Goes High when FPGA successfully completes configuration. Requires external 330 Ω pull-up resistor to 2.5V.	Low indicates that the FPGA is not yet configured.	Pulled High via external pull-up. When High, indicates that the FPGA successfully configured.
PROG_B	Input	**Program FPGA**. Active Low. When asserted Low for 500 ns or longer, forces the FPGA to restart its configuration process by clearing configuration memory and resetting the DONE and INIT_B pins once PROG_B returns High. Recommend external 4.7 kΩ pull-up resistor to 2.5V. Internal pull-up value may be weaker (see Table 78). If driving externally with a 3.3V output, use an open-drain or open-collector driver or use a current limiting series resistor.	Must be High to allow configuration to start.	Drive PROG_B Low and release to reprogram FPGA. Hold PROG_B to force FPGA I/O pins into Hi-Z, allowing direct programming access to SPI Flash PROM pins.

Table 59: **Byte-Wide Peripheral Interface (BPI) Connections *(Cont'd)***

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
DONE	Open-drain bidirectional I/O	**FPGA Configuration Done**. Low during configuration. Goes High when FPGA successfully completes configuration. Requires external 330 Ω pull-up resistor to 2.5V.	Low indicates that the FPGA is not yet configured.	Pulled High via external pull-up. When High, indicates that the FPGA is successfully configured.
PROG_B	Input	**Program FPGA**. Active Low. When asserted Low for 500 ns or longer, forces the FPGA to restart its configuration process by clearing configuration memory and resetting the DONE and INIT_B pins once PROG_B returns High. Recommend external 4.7 kΩ pull-up resistor to 2.5V. Internal pull-up value may be weaker (see Table 78). If driving externally with a 3.3V output, use an open-drain or open-collector driver or use a current limiting series resistor.	Must be High to allow configuration to start.	Drive PROG_B Low and release to reprogram FPGA. Hold PROG_B to force FPGA I/O pins into Hi-Z, allowing direct programming access to Flash PROM pins.

Voltage Compatibility

The FPGA's parallel Flash interface signals are within I/O Banks 1 and 2. The majority of parallel Flash PROMs use a single 3.3V supply voltage. Consequently, in most cases, the FPGA's VCCO_1 and VCCO_2 supply voltages must also be 3.3V to match the parallel Flash PROM. There are some 1.8V parallel Flash PROMs available and the FPGA interfaces with these devices if the VCCO_1 and VCCO_2 supplies are also 1.8V.

Power-On Precautions if PROM Supply is Last in Sequence

Like SPI Flash PROMs, parallel Flash PROMs typically require some amount of internal initialization time when the supply voltage reaches its minimum value.

The PROM supply voltage also connects to the FPGA's VCCO_2 supply input. In many systems, the PROM supply feeding the FPGA's VCCO_2 input is valid before the FPGA's other V_{CCINT} and V_{CCAUX} supplies, and consequently, there is no issue. However, if the PROM supply is last in the sequence, a potential race occurs between the FPGA and the parallel Flash PROM. See Power-On Precautions if 3.3V Supply is Last in Sequence for a similar description of the issue for SPI Flash PROMs.

Supported Parallel NOR Flash PROM Densities

Table 60 indicates the smallest usable parallel Flash PROM to program a single Spartan-3E FPGA. Parallel Flash density is specified in bits but addressed as bytes. The FPGA presents up to 24 address lines during configuration but not all are required for single FPGA applications. Table 60 shows the minimum required number of address lines between the FPGA and parallel Flash PROM. The actual number of address line required depends on the density of the attached parallel Flash PROM.

A multiple-FPGA daisy-chained application requires a parallel Flash PROM large enough to contain the sum of the FPGA file sizes. An application can also use a larger-density parallel Flash PROM to hold additional data beyond just FPGA configuration data. For example, the parallel Flash PROM can also contain the application code for a MicroBlaze RISC processor core implemented within the Spartan-3E FPGA. After configuration, the MicroBlaze processor can execute directly from external Flash or can copy the code to other, faster system memory before executing the code.

Table 60: **Number of Bits to Program a Spartan-3E FPGA and Smallest Parallel Flash PROM**

Spartan-3E FPGA	Uncompressed File Sizes (bits)	Smallest Usable Parallel Flash PROM	Minimum Required Address Lines
XC3S100E	581,344	1 Mbit	A[16:0]
XC3S250E	1,353,728	2 Mbit	A[17:0]
XC3S500E	2,270,208	4 Mbit	A[18:0]
XC3S1200E	3,841,184	4 Mbit	A[18:0]
XC3S1600E	5,969,696	8 Mbit	A[19:0]

Powering Spartan-3E FPGAs

For additional information, refer to the “Powering Spartan-3 Generation FPGAs” chapter in UG331.

Voltage Supplies

Like Spartan-3 FPGAs, Spartan-3E FPGAs have multiple voltage supply inputs, as shown in Table 70. There are two supply inputs for internal logic functions, V_{CCINT} and V_{CCAUX}. Each of the four I/O banks has a separate V_{CCO} supply input that powers the output buffers within the associated I/O bank. All of the V_{CCO} connections to a specific I/O bank must be connected and must connect to the same voltage.

Table 70: **Spartan-3E Voltage Supplies**

Supply Input	Description	Nominal Supply Voltage
V_{CCINT}	Internal core supply voltage. Supplies all internal logic functions, such as CLBs, block RAM, and multipliers. Input to Power-On Reset (POR) circuit.	1.2V
V_{CCAUX}	Auxiliary supply voltage. Supplies Digital Clock Managers (DCMs), differential drivers, dedicated configuration pins, JTAG interface. Input to Power-On Reset (POR) circuit.	2.5V
VCCO_0	Supplies the output buffers in I/O Bank 0, the bank along the top edge of the FPGA.	Selectable, 3.3V, 2.5V, 1.8, 1.5V, or 1.2V
VCCO_1	Supplies the output buffers in I/O Bank 1, the bank along the right edge of the FPGA. In Byte-Wide Peripheral Interface (BPI) Parallel Flash Mode, connects to the same voltage as the Flash PROM.	Selectable, 3.3V, 2.5V, 1.8, 1.5V, or 1.2V
VCCO_2	Supplies the output buffers in I/O Bank 2, the bank along the bottom edge of the FPGA. Connects to the same voltage as the FPGA configuration source. Input to Power-On Reset (POR) circuit.	Selectable, 3.3V, 2.5V, 1.8, 1.5V, or 1.2V
VCCO_3	Supplies the output buffers in I/O Bank 3, the bank along the left edge of the FPGA.	Selectable, 3.3V, 2.5V, 1.8, 1.5V, or 1.2V

In a 3.3V-only application, all four V_{CCO} supplies connect to 3.3V. However, Spartan-3E FPGAs provide the ability to bridge between different I/O voltages and standards by applying different voltages to the V_{CCO} inputs of different banks. Refer to I/O Banking Rules for which I/O standards can be intermixed within a single I/O bank.

Each I/O bank also has an separate, optional input voltage reference supply, called V_{REF}. If the I/O bank includes an I/O standard that requires a voltage reference such as HSTL or SSTL, then all V_{REF} pins within the I/O bank must be connected to the same voltage.

DC Electrical Characteristics

In this section, specifications may be designated as Advance, Preliminary, or Production. These terms are defined as follows:

Advance: Initial estimates are based on simulation, early characterization, and/or extrapolation from the characteristics of other families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on characterization. Further changes are not expected.

Production: These specifications are approved once the silicon has been characterized over numerous production lots. Parameter values are considered stable with no future changes expected.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all Spartan®-3E devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.**

Absolute Maximum Ratings

Stresses beyond those listed under Table 73, Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to absolute maximum conditions for extended periods of time adversely affects device reliability.

Table 73: **Absolute Maximum Ratings**

Symbol	Description	Conditions		Min	Max	Units
V_{CCINT}	Internal supply voltage			–0.5	1.32	V
V_{CCAUX}	Auxiliary supply voltage			–0.5	3.00	V
V_{CCO}	Output driver supply voltage			–0.5	3.75	V
V_{REF}	Input reference voltage			–0.5	V_{CCO} + 0.5 (1)	V
V_{IN} (1,2,3,4)	Voltage applied to all User I/O pins and Dual-Purpose pins	Driver in a high-impedance state	Commercial	–0.95	4.4	V
			Industrial	–0.85	4.3	V
	Voltage applied to all Dedicated pins		All temp. ranges	–0.5	V_{CCAUX} + 0.5 (3)	V
I_{IK}	Input clamp current per I/O pin	–0.5 V < V_{IN} < (V_{CCO} + 0.5 V)		–	±100	mA
V_{ESD}	Electrostatic Discharge Voltage	Human body model		–	±2000	V
		Charged device model		–	±500	V
		Machine model		–	±200	V
T_J	Junction temperature			–	125	°C
T_{STG}	Storage temperature			–65	150	°C

Notes:

1. Each of the User I/O and Dual-Purpose pins is associated with one of the four banks' V_{CCO} rails. Keeping V_{IN} within 500 mV of the associated V_{CCO} rails or ground rail ensures that the internal diode junctions do not turn on. Table 77 specifies the V_{CCO} range used to evaluate the maximum V_{IN} voltage.
2. Input voltages outside the -0.5V to V_{CCO} + 0.5V (or V_{CCAUX} + 0.5V) voltage range are require the I_{IK} input diode clamp diode rating is met and no more than 100 pins exceed the range simultaneously. Prolonged exposure to such current may compromise device reliability. A sustained current of 10 mA will not compromise device reliability. See XAPP459: *Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins on Spartan-3 Families* for more details.
3. All Dedicated pins (PROG_B, DONE, TCK, TDI, TDO, and TMS) draw power from the V_{CCAUX} rail (2.5V). Meeting the V_{IN} max limit ensures that the internal diode junctions that exist between each of these pins and the V_{CCAUX} rail do not turn on. Table 77 specifies the V_{CCAUX} range used to evaluate the maximum V_{IN} voltage. As long as the V_{IN} max specification is met, oxide stress is not possible.
4. See XAPP459: *Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins on Spartan-3 Families*.
5. For soldering guidelines, see UG112: *Device Packaging and Thermal Characteristics* and XAPP427: *Implementation and Solder Reflow Guidelines for Pb-Free Packages*.

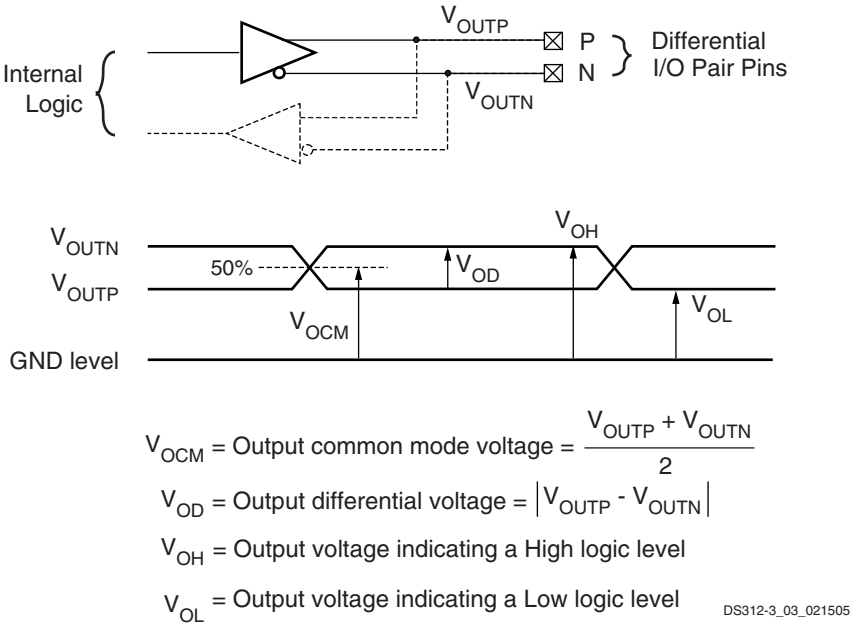

Figure 70: **Differential Output Voltages**

Table 83: **DC Characteristics of User I/Os Using Differential Signal Standards**

IOSTANDARD Attribute	V_{OD}			ΔV_{OD}		V_{OCM}			ΔV_{OCM}		V_{OH}	V_{OL}
	Min (mV)	Typ (mV)	Max (mV)	Min (mV)	Max (mV)	Min (V)	Typ (V)	Max (V)	Min (mV)	Max (mV)	Min (V)	Max (V)
LVDS_25	250	350	450	–	–	1.125	–	1.375	–	–	–	–
BLVDS_25	250	350	450	–	–	–	1.20	–	–	–	–	–
MINI_LVDS_25	300	–	600	–	50	1.0	–	1.4	–	50	–	–
RSDS_25	100	–	400	–	–	1.1	–	1.4	–	–	–	–
DIFF_HSTL_I_18	–	–	–	–	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_III_18	–	–	–	–	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_SSTL18_I	–	–	–	–	–	–	–	–	–	–	V_{TT} + 0.475	V_{TT} – 0.475
DIFF_SSTL2_I	–	–	–	–	–	–	–	–	–	–	V_{TT} + 0.61	V_{TT} – 0.61

Notes:

1. The numbers in this table are based on the conditions set forth in Table 77 and Table 82.
2. Output voltage measurements for all differential standards are made with a termination resistor (R_T) of 100Ω across the N and P pins of the differential signal pair. The exception is for BLVDS, shown in Figure 71.
3. At any given time, no more than two of the following differential output standards may be assigned to an I/O bank: LVDS_25, RSDS_25, MINI_LVDS_25

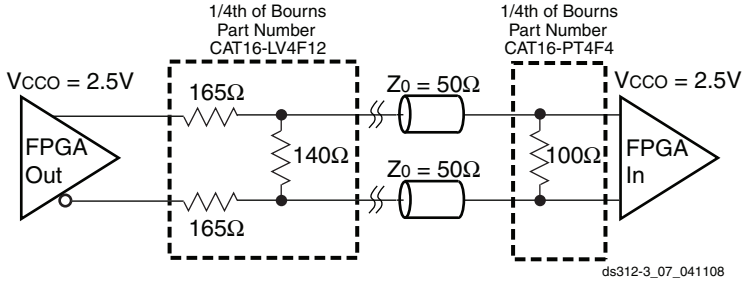

Figure 71: **External Termination Resistors for BLVDS Transmitter and BLVDS Receiver**

Table 94: **Output Timing Adjustments for IOB**

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
Single-Ended Standards					
LVTTL	Slow	2 mA	5.20	5.41	ns
		4 mA	2.32	2.41	ns
		6 mA	1.83	1.90	ns
		8 mA	0.64	0.67	ns
		12 mA	0.68	0.70	ns
		16 mA	0.41	0.43	ns
	Fast	2 mA	4.80	5.00	ns
		4 mA	1.88	1.96	ns
		6 mA	1.39	1.45	ns
		8 mA	0.32	0.34	ns
		12 mA	0.28	0.30	ns
		16 mA	0.28	0.30	ns
LVCMOS33	Slow	2 mA	5.08	5.29	ns
		4 mA	1.82	1.89	ns
		6 mA	1.00	1.04	ns
		8 mA	0.66	0.69	ns
		12 mA	0.40	0.42	ns
		16 mA	0.41	0.43	ns
	Fast	2 mA	4.68	4.87	ns
		4 mA	1.46	1.52	ns
		6 mA	0.38	0.39	ns
		8 mA	0.33	0.34	ns
		12 mA	0.28	0.30	ns
		16 mA	0.28	0.30	ns
LVCMOS25	Slow	2 mA	4.04	4.21	ns
		4 mA	2.17	2.26	ns
		6 mA	1.46	1.52	ns
		8 mA	1.04	1.08	ns
		12 mA	0.65	0.68	ns
	Fast	2 mA	3.53	3.67	ns
		4 mA	1.65	1.72	ns
		6 mA	0.44	0.46	ns
		8 mA	0.20	0.21	ns
		12 mA	0	0	ns

Table 94: **Output Timing Adjustments for IOB *(Cont'd)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVCMOS18	Slow	2 mA	5.03	5.24	ns
		4 mA	3.08	3.21	ns
		6 mA	2.39	2.49	ns
		8 mA	1.83	1.90	ns
	Fast	2 mA	3.98	4.15	ns
		4 mA	2.04	2.13	ns
		6 mA	1.09	1.14	ns
		8 mA	0.72	0.75	ns
LVCMOS15	Slow	2 mA	4.49	4.68	ns
		4 mA	3.81	3.97	ns
		6 mA	2.99	3.11	ns
	Fast	2 mA	3.25	3.38	ns
		4 mA	2.59	2.70	ns
		6 mA	1.47	1.53	ns
LVCMOS12	Slow	2 mA	6.36	6.63	ns
	Fast	2 mA	4.26	4.44	ns
HSTL_I_18			0.33	0.34	ns
HSTL_III_18			0.53	0.55	ns
PCI33_3			0.44	0.46	ns
PCI66_3			0.44	0.46	ns
SSTL18_I			0.24	0.25	ns
SSTL2_I			–0.20	–0.20	ns
Differential Standards					
LVDS_25			–0.55	–0.55	ns
BLVDS_25			0.04	0.04	ns
MINI_LVDS_25			–0.56	–0.56	ns
LVPECL_25			Input Only		ns
RSDS_25			–0.48	–0.48	ns
DIFF_HSTL_I_18			0.42	0.42	ns
DIFF_HSTL_III_18			0.53	0.55	ns
DIFF_SSTL18_I			0.40	0.40	ns
DIFF_SSTL2_I			0.44	0.44	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 95 and are based on the operating conditions set forth in Table 77, Table 80, and Table 82.
2. These adjustments are used to convert output- and three-state-path times originally specified for the LVCMOS25 standard with 12 mA drive and Fast slew rate to times that correspond to other signal standards. Do not adjust times that measure when outputs go into a high-impedance state.

Phase Shifter (PS)

Table 108: **Recommended Operating Conditions for the PS in Variable Phase Mode**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Operating Frequency Ranges						
PSCLK_FREQ (F_{PSCLK})	Frequency for the PSCLK input	1	167	1	167	MHz
Input Pulse Requirements						
PSCLK_PULSE	PSCLK pulse width as a percentage of the PSCLK period	40%	60%	40%	60%	-

Table 109: **Switching Characteristics for the PS in Variable Phase Mode**

Symbol	Description	Equation		Units
Phase Shifting Range				
MAX_STEPS(2)	Maximum allowed number of DCM_DELAY_STEP steps for a given CLKIN clock period, where T = CLKIN clock period in ns. If using CLKIN_DIVIDE_BY_2 = TRUE, double the effective clock period.(3)	CLKIN < 60 MHz	±[INTEGER(10 • (T_{CLKIN} – 3 ns))]	steps
		CLKIN ≥ 60 MHz	±[INTEGER(15 • (T_{CLKIN} – 3 ns))]	steps
FINE_SHIFT_RANGE_MIN	Minimum guaranteed delay for variable phase shifting	±[MAX_STEPS • DCM_DELAY_STEP_MIN]		ns
FINE_SHIFT_RANGE_MAX	Maximum guaranteed delay for variable phase shifting	±[MAX_STEPS • DCM_DELAY_STEP_MAX]		ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 77 and Table 108.
2. The maximum variable phase shift range, MAX_STEPS, is only valid when the DCM is has no initial fixed phase shifting, i.e., the PHASE_SHIFT attribute is set to 0.
3. The DCM_DELAY_STEP values are provided at the bottom of Table 105.

Miscellaneous DCM Timing

Table 110: **Miscellaneous DCM Timing**

Symbol	Description	Min	Max	Units
DCM_RST_PW_MIN(1)	Minimum duration of a RST pulse width	3	-	CLKIN cycles
DCM_RST_PW_MAX(2)	Maximum duration of a RST pulse width	N/A	N/A	seconds
DCM_CONFIG_LAG_TIME(3)	Maximum duration from V_{CCINT} applied to FPGA configuration successfully completed (DONE pin goes High) and clocks applied to DCM DLL	N/A	N/A	minutes

Notes:

1. This limit only applies to applications that use the DCM DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV). The DCM DFS outputs (CLKFX, CLKFX180) are unaffected.
2. This specification is equivalent to the Virtex-4 DCM_RESET specfication.This specification does not apply for Spartan-3E FPGAs.
3. This specification is equivalent to the Virtex-4 TCONFIG specification. This specification does not apply for Spartan-3E FPGAs.

Byte Peripheral Interface (BPI) Configuration Timing

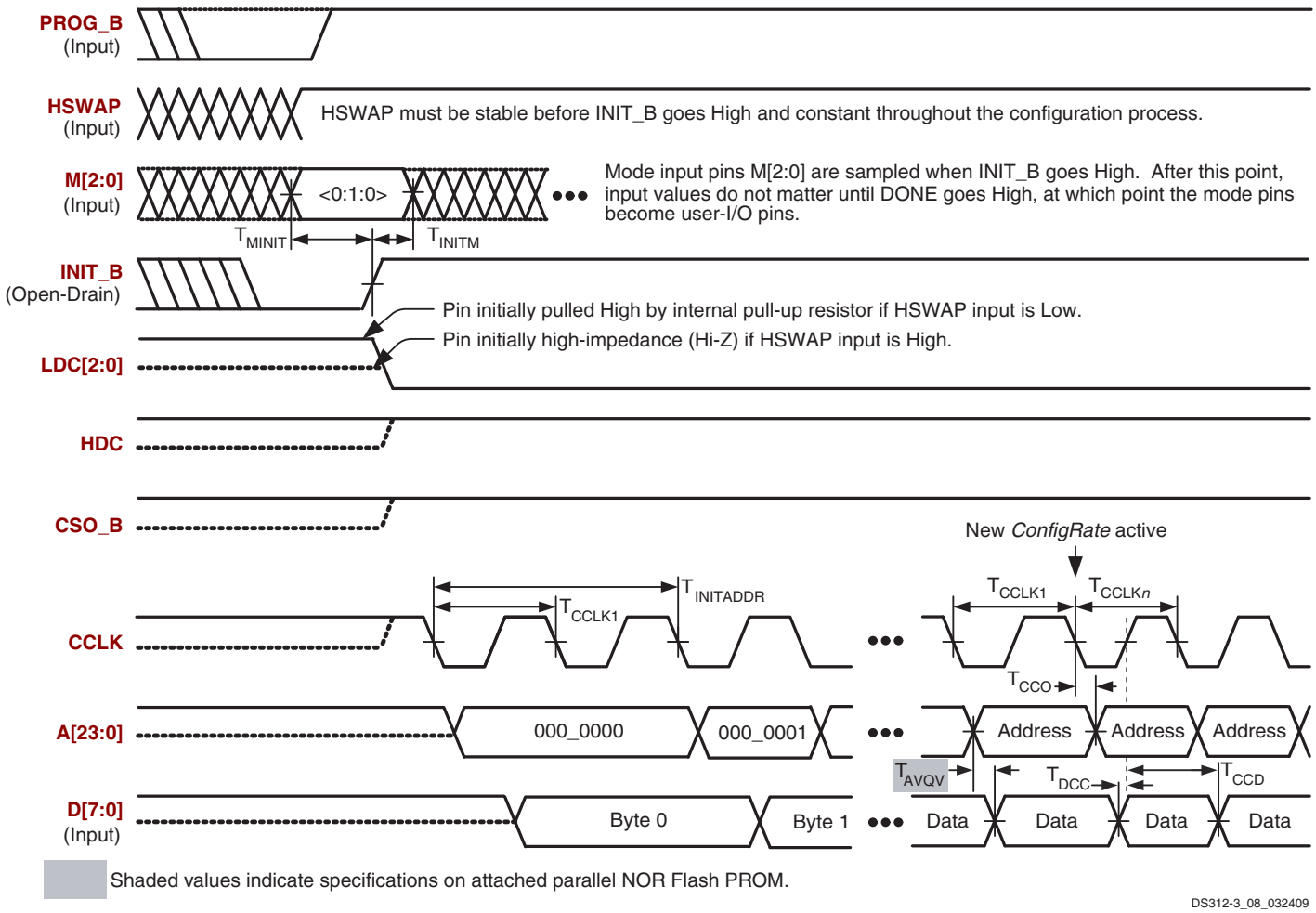

Figure 77: **Waveforms for Byte-wide Peripheral Interface (BPI) Configuration (BPI-DN mode shown)**

Table 120: **Timing for Byte-wide Peripheral Interface (BPI) Configuration Mode**

Symbol	Description		Minimum	Maximum	Units
T_{CCLK1}	Initial CCLK clock period		See Table 112		
T_{CCLKn}	CCLK clock period after FPGA loads ConfigRate setting		See Table 112		
T_{MINIT}	Setup time on CSI_B, RDWR_B, and M[2:0] mode pins before the rising edge of INIT_B		50	-	ns
T_{INITM}	Hold time on CSI_B, RDWR_B, and M[2:0] mode pins after the rising edge of INIT_B		0	-	ns
$T_{INITADDR}$	Minimum period of initial A[23:0] address cycle; LDC[2:0] and HDC are asserted and valid	BPI-UP: (M[2:0] = <0:1:0>)	5	5	T_{CCLK1} cycles
		BPI-DN: (M[2:0] = <0:1:1>)	2	2	
T_{CCO}	Address A[23:0] outputs valid after CCLK falling edge		See Table 116		
T_{DCC}	Setup time on D[7:0] data inputs before CCLK rising edge		See Table 116		
T_{CCD}	Hold time on D[7:0] data inputs after CCLK rising edge		See Table 116		

Spartan-3 FPGA Family: Pinout Descriptions

DS312 (4.0) October 29, 2012 **Product Specification**

Introduction

This section describes the various pins on a Spartan®-3E FPGA and how they connect within the supported component packages.

Pin Types

Most pins on a Spartan-3E FPGA are general-purpose, user-defined I/O pins. There are, however, up to 11 different functional types of pins on Spartan-3E packages, as outlined in Table 124. In the package footprint drawings that follow, the individual pins are color-coded according to pin type as in the table.

Table 124: **Types of Pins on Spartan-3E FPGAs**

Type / Color Code	Description	Pin Name(s) in Type[1]
I/O	Unrestricted, general-purpose user-I/O pin. Most pins can be paired together to form differential I/Os.	IO IO_Lxxy_#
INPUT	Unrestricted, general-purpose input-only pin. This pin does not have an output structure, differential termination resistor, or PCI clamp diode.	IP IP_Lxxy_#
DUAL	Dual-purpose pin used in some configuration modes during the configuration process and then usually available as a user I/O after configuration. If the pin is not used during configuration, this pin behaves as an I/O-type pin. Some of the dual-purpose pins are also shared with bottom-edge global (GCLK) or right-half (RHCLK) clock inputs. See the Configuration section in Module 2 for additional information on these signals.	M[2:0] HSWAP CCLK MOSI/CSI_B D[7:1] D0/DIN CSO_B RDWR_B BUSY/DOUT INIT_B A[23:20] A19/VS2 A18/VS1 A17/VS0 A[16:0] LDC[2:0] HDC
VREF	Dual-purpose pin that is either a user-I/O pin or Input-only pin, or, along with all other VREF pins in the same bank, provides a reference voltage input for certain I/O standards. If used for a reference voltage within a bank, all VREF pins within the bank must be connected.	IP/VREF_# IP_Lxxy_#/VREF_# IO/VREF_# IO_Lxxy_#/VREF_#
CLK	Either a user-I/O pin or Input-only pin, or an input to a specific clock buffer driver. Every package has 16 global clock inputs that optionally clock the entire device. The RHCLK inputs optionally clock the right-half of the device. The LHCLK inputs optionally clock the left-half of the device. Some of the clock pins are shared with the dual-purpose configuration pins and are considered DUAL-type. See the Clocking Infrastructure section in Module 2 for additional information on these signals.	IO_Lxxy_#/GCLK[15:10, 7:2] IP_Lxxy_#/GCLK[9:8, 1:0] IO_Lxxy_#/LHCLK[7:0] IO_Lxxy_#/RHCLK[7:0]
CONFIG	Dedicated configuration pin. Not available as a user-I/O pin. Every package has two dedicated configuration pins. These pins are powered by VCCAUX. See the Configuration section in Module 2 for details.	DONE, PROG_B
JTAG	Dedicated JTAG pin. Not available as a user-I/O pin. Every package has four dedicated JTAG pins. These pins are powered by VCCAUX.	TDI, TMS, TCK, TDO
GND	Dedicated ground pin. The number of GND pins depends on the package used. All must be connected.	GND

Package Thermal Characteristics

The power dissipated by an FPGA application has implications on package selection and system design. The power consumed by a Spartan-3E FPGA is reported using either the XPower Estimator or the XPower Analyzer calculator integrated in the Xilinx ISE® development software. Table 130 provides the thermal characteristics for the various Spartan-3E package offerings.

The junction-to-case thermal resistance (θ_{JC}) indicates the difference between the temperature measured on the package body (case) and the die junction temperature per watt of power consumption. The junction-to-board (θ_{JB}) value similarly reports the difference between the board and junction temperature. The junction-to-ambient (θ_{JA}) value reports the temperature difference per watt between the ambient environment and the junction temperature. The θ_{JA} value is reported at different air velocities, measured in linear feet per minute (LFM). The Still Air (0 LFM) column shows the θ_{JA} value in a system without a fan. The thermal resistance drops with increasing air flow.

Table 130: **Spartan-3E Package Thermal Characteristics**

Device	Package	Junction-to-Case (θ_{JC})	Junction-to-Board (θ_{JB})	Junction-to-Ambient (θ_{JA}) at Different Air Flows				Units
				Still Air (0 LFM)	250 LFM	500 LFM	750 LFM	
XC3S100E	VQ100	13.0	30.9	49.0	40.7	37.9	37.0	°C/Watt
XC3S250E		11.0	25.9	43.3	36.0	33.6	32.7	°C/Watt
XC3S500E		9.8		40.0	33.3	31.0	30.2	°C/Watt
XC3S100E	CP132	19.3	42.0	62.1	55.3	52.8	51.2	°C/Watt
XC3S250E		11.8	28.1	48.3	41.8	39.5	38.0	°C/Watt
XC3S500E		8.5	21.3	41.5	35.2	32.9	31.5	°C/Watt
XC3S100E	TQ144	8.2	31.9	52.1	40.5	34.6	32.5	°C/Watt
XC3S250E		7.2	25.7	37.6	29.2	25.0	23.4	°C/Watt
XC3S250E	PQ208	9.8	29.0	37.0	27.3	24.1	22.4	°C/Watt
XC3S500E		8.5	26.8	36.1	26.6	23.6	21.8	°C/Watt
XC3S250E	FT256	12.4	27.7	35.8	29.3	28.4	28.1	°C/Watt
XC3S500E		9.6	22.2	31.1	25.0	24.0	23.6	°C/Watt
XC3S1200E		6.5	16.4	26.2	20.5	19.3	18.9	°C/Watt
XC3S500E	FG320	9.8	15.6	26.1	20.6	19.4	18.6	°C/Watt
XC3S1200E		8.2	12.5	23.0	17.7	16.4	15.7	°C/Watt
XC3S1600E		7.1	10.6	21.1	15.9	14.6	13.8	°C/Watt
XC3S1200E	FG400	7.5	12.4	22.3	17.2	16.0	15.3	°C/Watt
XC3S1600E		6.0	10.4	20.3	15.2	14.0	13.3	°C/Watt
XC3S1600E	FG484	5.7	9.4	18.8	12.5	11.3	10.8	°C/Watt

Table 133: **CP132 Package Pinout *(Cont'd)***

Bank	XC3S100E Pin Name	XC3S250E XC3S500E Pin Name	CP132 Ball	Type
2	N.C. (◆)	IO_L08P_2/A23	N9	***100E:*** N.C. ***Others:*** DUAL
2	N.C. (◆)	IO_L09N_2/A20	M10	***100E:*** N.C. ***Others:*** DUAL
2	N.C. (◆)	IO_L09P_2/A21	N10	***100E:*** N.C. ***Others:*** DUAL
2	IO_L10N_2/VS1/A18	IO_L10N_2/VS1/A18	M11	DUAL
2	IO_L10P_2/VS2/A19	IO_L10P_2/VS2/A19	N11	DUAL
2	IO_L11N_2/CCLK	IO_L11N_2/CCLK	N12	DUAL
2	IO_L11P_2/VS0/A17	IO_L11P_2/VS0/A17	P12	DUAL
2	IP/VREF_2	IP/VREF_2	N3	VREF
2	IP_L05N_2/M2/GCLK1	IP_L05N_2/M2/GCLK1	N6	DUAL/GCLK
2	IP_L05P_2/RDWR_B/GCLK0	IP_L05P_2/RDWR_B/GCLK0	M6	DUAL/GCLK
2	VCCO_2	VCCO_2	M8	VCCO
2	VCCO_2	VCCO_2	P3	VCCO
3	IO	IO	J3	I/O
3	IP/VREF_3	IO/VREF_3	K3	***100E:*** VREF(INPUT) ***Others:*** VREF(I/O)
3	IO_L01N_3	IO_L01N_3	B1	I/O
3	IO_L01P_3	IO_L01P_3	B2	I/O
3	IO_L02N_3	IO_L02N_3	C2	I/O
3	IO_L02P_3	IO_L02P_3	C3	I/O
3	N.C. (◆)	IO_L03N_3	D1	***100E:*** N.C. ***Others:*** I/O
3	IO	IO_L03P_3	D2	I/O
3	IO_L04N_3/LHCLK1	IO_L04N_3/LHCLK1	F2	LHCLK
3	IO_L04P_3/LHCLK0	IO_L04P_3/LHCLK0	F3	LHCLK
3	IO_L05N_3/LHCLK3/IRDY2	IO_L05N_3/LHCLK3/IRDY2	G1	LHCLK
3	IO_L05P_3/LHCLK2	IO_L05P_3/LHCLK2	F1	LHCLK
3	IO_L06N_3/LHCLK5	IO_L06N_3/LHCLK5	H1	LHCLK
3	IO_L06P_3/LHCLK4/TRDY2	IO_L06P_3/LHCLK4/TRDY2	G3	LHCLK
3	IO_L07N_3/LHCLK7	IO_L07N_3/LHCLK7	H3	LHCLK
3	IO_L07P_3/LHCLK6	IO_L07P_3/LHCLK6	H2	LHCLK
3	IO_L08N_3	IO_L08N_3	L2	I/O
3	IO_L08P_3	IO_L08P_3	L1	I/O
3	IO_L09N_3	IO_L09N_3	M1	I/O
3	IO_L09P_3	IO_L09P_3	L3	I/O
3	IP/VREF_3	IP/VREF_3	E2	VREF
3	VCCO_3	VCCO_3	E1	VCCO
3	VCCO_3	VCCO_3	J2	VCCO
GND	N.C. (GND)	GND	A4	GND
GND	GND	GND	A8	GND
GND	N.C. (GND)	GND	C1	GND
GND	GND	GND	C7	GND

PQ208 Footprint (Right)

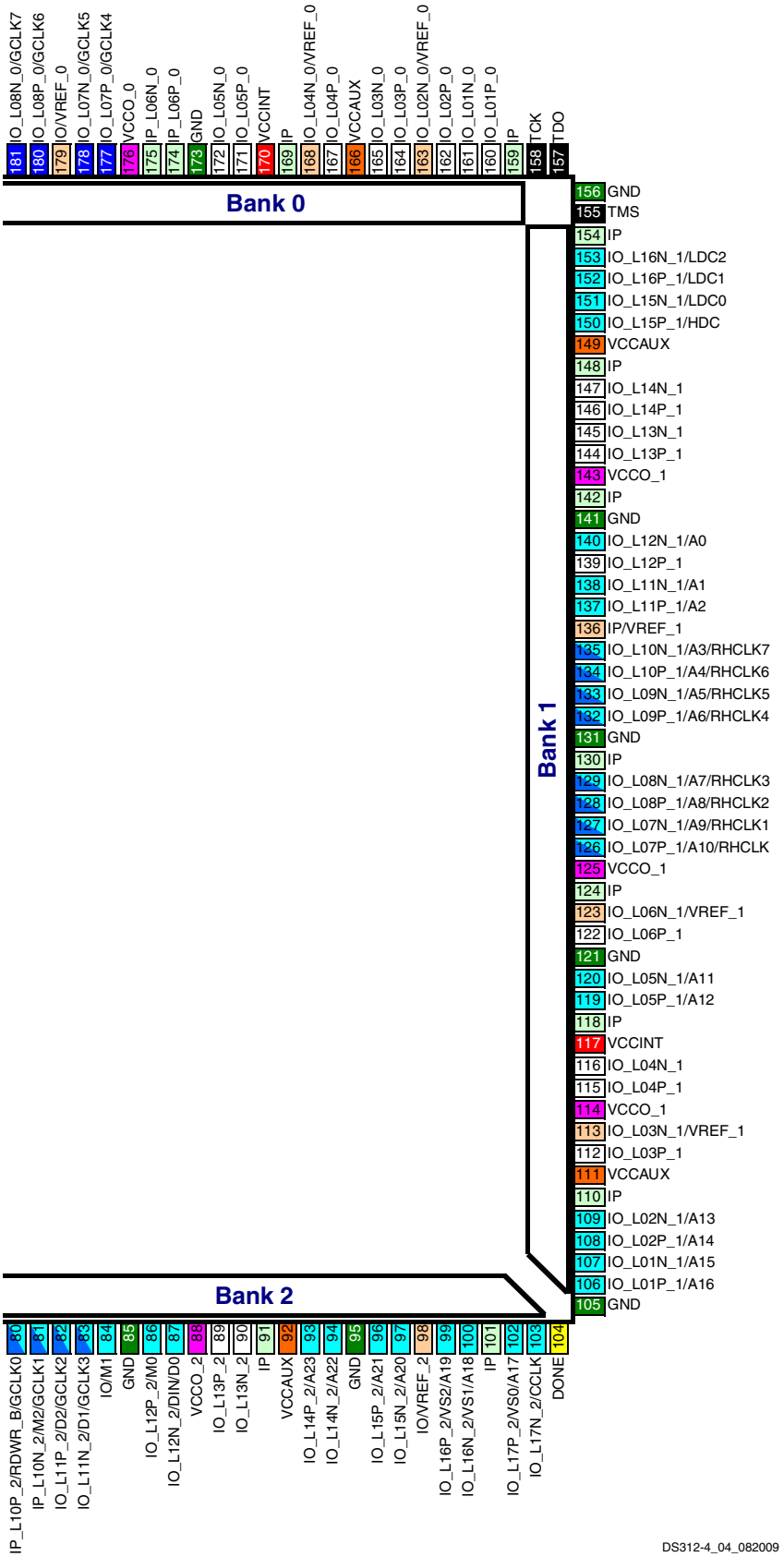

Figure 84: **PQ208 Footprint (Right)**

Table 148: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S500E Pin Name	XC3S1200E Pin Name	XC3S1600E Pin Name	FG320 Ball	Type
2	IO_L20P_2	IO_L20P_2	IO_L20P_2	T12	I/O
2	N.C. (◆)	IO_L21N_2	IO_L21N_2	P12	**500E:** N.C. **1200E:** I/O **1600E:** I/O
2	N.C. (◆)	IO_L21P_2	IO_L21P_2	N12	**500E:** N.C. **1200E:** I/O **1600E:** I/O
2	IO_L22N_2/A22	IO_L22N_2/A22	IO_L22N_2/A22	R13	DUAL
2	IO_L22P_2/A23	IO_L22P_2/A23	IO_L22P_2/A23	P13	DUAL
2	IO_L24N_2/A20	IO_L24N_2/A20	IO_L24N_2/A20	R14	DUAL
2	IO_L24P_2/A21	IO_L24P_2/A21	IO_L24P_2/A21	T14	DUAL
2	IO_L25N_2/VS1/A18	IO_L25N_2/VS1/A18	IO_L25N_2/VS1/A18	U15	DUAL
2	IO_L25P_2/VS2/A19	IO_L25P_2/VS2/A19	IO_L25P_2/VS2/A19	V15	DUAL
2	IO_L26N_2/CCLK	IO_L26N_2/CCLK	IO_L26N_2/CCLK	U16	DUAL
2	IO_L26P_2/VS0/A17	IO_L26P_2/VS0/A17	IO_L26P_2/VS0/A17	T16	DUAL
2	IP	IP	IP	V2	INPUT
2	IP	IP	IP	V16	INPUT
2	IP_L02N_2	IP_L02N_2	IP_L02N_2	V3	INPUT
2	IP_L02P_2	IP_L02P_2	IP_L02P_2	V4	INPUT
2	IP_L08N_2	IP_L08N_2	IP_L08N_2	R7	INPUT
2	IP_L08P_2	IP_L08P_2	IP_L08P_2	T7	INPUT
2	IP_L11N_2/VREF_2	IP_L11N_2/VREF_2	IP_L11N_2/VREF_2	V8	VREF
2	IP_L11P_2	IP_L11P_2	IP_L11P_2	U8	INPUT
2	IP_L14N_2/M2/GCLK1	IP_L14N_2/M2/GCLK1	IP_L14N_2/M2/GCLK1	T10	DUAL/GCLK
2	IP_L14P_2/RDWR_B/ GCLK0	IP_L14P_2/RDWR_B/ GCLK0	IP_L14P_2/RDWR_B/ GCLK0	U10	DUAL/GCLK
2	IP_L17N_2	IP_L17N_2	IP_L17N_2	U11	INPUT
2	IP_L17P_2	IP_L17P_2	IP_L17P_2	T11	INPUT
2	IP_L23N_2	IP_L23N_2	IP_L23N_2	U14	INPUT
2	IP_L23P_2	IP_L23P_2	IP_L23P_2	V14	INPUT
2	VCCO_2	VCCO_2	VCCO_2	M8	VCCO
2	VCCO_2	VCCO_2	VCCO_2	M11	VCCO
2	VCCO_2	VCCO_2	VCCO_2	T6	VCCO
2	VCCO_2	VCCO_2	VCCO_2	T13	VCCO
2	VCCO_2	VCCO_2	VCCO_2	V10	VCCO
3	N.C. (◆)	IO	IO	D4	**500E:** N.C. **1200E:** I/O **1600E:** I/O
3	IO_L01N_3	IO_L01N_3	IO_L01N_3	C2	I/O
3	IO_L01P_3	IO_L01P_3	IO_L01P_3	C1	I/O
3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	D2	VREF
3	IO_L02P_3	IO_L02P_3	IO_L02P_3	D1	I/O
3	IO_L03N_3	IO_L03N_3	IO_L03N_3	E1	I/O
3	IO_L03P_3	IO_L03P_3	IO_L03P_3	E2	I/O

FG400: 400-ball Fine-pitch Ball Grid Array

The 400-ball fine-pitch ball grid array, FG400, supports two different Spartan-3E FPGAs, including the XC3S1200E and the XC3S1600E. Both devices share a common footprint for this package as shown in Table 152 and Figure 87.

Table 152 lists all the FG400 package pins. They are sorted by bank number and then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at:

http://www.xilinx.com/support/documentation/data_sheets/s3e_pin.zip

Pinout Table

Table 152: **FG400 Package Pinout**

Bank	XC3S1200E XC3S1600E Pin Name	FG400 Ball	Type
0	IO	A3	I/O
0	IO	A8	I/O
0	IO	A12	I/O
0	IO	C7	I/O
0	IO	C10	I/O
0	IO	E8	I/O
0	IO	E13	I/O
0	IO	E16	I/O
0	IO	F13	I/O
0	IO	F14	I/O
0	IO	G7	I/O
0	IO/VREF_0	C11	VREF
0	IO_L01N_0	B17	I/O
0	IO_L01P_0	C17	I/O
0	IO_L03N_0/VREF_0	A18	VREF
0	IO_L03P_0	A19	I/O
0	IO_L04N_0	A17	I/O
0	IO_L04P_0	A16	I/O
0	IO_L06N_0	A15	I/O
0	IO_L06P_0	B15	I/O
0	IO_L07N_0	C14	I/O
0	IO_L07P_0	D14	I/O
0	IO_L09N_0/VREF_0	A13	VREF
0	IO_L09P_0	A14	I/O
0	IO_L10N_0	B13	I/O
0	IO_L10P_0	C13	I/O
0	IO_L12N_0	C12	I/O
0	IO_L12P_0	D12	I/O
0	IO_L13N_0	E12	I/O
0	IO_L13P_0	F12	I/O
0	IO_L15N_0/GCLK5	G11	GCLK
0	IO_L15P_0/GCLK4	F11	GCLK
0	IO_L16N_0/GCLK7	E10	GCLK
0	IO_L16P_0/GCLK6	E11	GCLK
0	IO_L18N_0/GCLK11	A9	GCLK
0	IO_L18P_0/GCLK10	A10	GCLK
0	IO_L19N_0	F9	I/O
0	IO_L19P_0	E9	I/O
0	IO_L21N_0	C9	I/O
0	IO_L21P_0	D9	I/O
0	IO_L22N_0/VREF_0	B8	VREF
0	IO_L22P_0	B9	I/O
0	IO_L24N_0/VREF_0	F7	VREF
0	IO_L24P_0	F8	I/O
0	IO_L25N_0	A6	I/O
0	IO_L25P_0	A7	I/O
0	IO_L27N_0	B5	I/O
0	IO_L27P_0	B6	I/O
0	IO_L28N_0	D6	I/O
0	IO_L28P_0	C6	I/O
0	IO_L30N_0/VREF_0	C5	VREF
0	IO_L30P_0	D5	I/O
0	IO_L31N_0	A2	I/O
0	IO_L31P_0	B2	I/O
0	IO_L32N_0/HSWAP	D4	DUAL
0	IO_L32P_0	C4	I/O
0	IP	B18	INPUT
0	IP	E5	INPUT
0	IP_L02N_0	C16	INPUT
0	IP_L02P_0	D16	INPUT
0	IP_L05N_0	D15	INPUT
0	IP_L05P_0	C15	INPUT
0	IP_L08N_0	E14	INPUT
0	IP_L08P_0	E15	INPUT
0	IP_L11N_0	G14	INPUT
0	IP_L11P_0	G13	INPUT
0	IP_L14N_0	B11	INPUT
0	IP_L14P_0	B12	INPUT
0	IP_L17N_0/GCLK9	G10	GCLK

Table 154: **FG484 Package Pinout *(Cont'd)***

Bank	XC3S1600E Pin Name	FG484 Ball	Type
1	IO_L27N_1	J17	I/O
1	IO_L27P_1	J18	I/O
1	IO_L28N_1/VREF_1	H21	VREF
1	IO_L28P_1	H22	I/O
1	IO_L29N_1	H20	I/O
1	IO_L29P_1	H19	I/O
1	IO_L30N_1	H17	I/O
1	IO_L30P_1	G17	I/O
1	IO_L31N_1	F22	I/O
1	IO_L31P_1	G22	I/O
1	IO_L32N_1	F20	I/O
1	IO_L32P_1	G20	I/O
1	IO_L33N_1	G18	I/O
1	IO_L33P_1	G19	I/O
1	IO_L34N_1	D22	I/O
1	IO_L34P_1	E22	I/O
1	IO_L35N_1	F19	I/O
1	IO_L35P_1	F18	I/O
1	IO_L36N_1	E20	I/O
1	IO_L36P_1	E19	I/O
1	IO_L37N_1/LDC0	C21	DUAL
1	IO_L37P_1/HDC	C22	DUAL
1	IO_L38N_1/LDC2	B21	DUAL
1	IO_L38P_1/LDC1	B22	DUAL
1	IP	D20	INPUT
1	IP	F21	INPUT
1	IP	G16	INPUT
1	IP	H16	INPUT
1	IP	J16	INPUT
1	IP	J22	INPUT
1	IP	K20	INPUT
1	IP	L15	INPUT
1	IP	M18	INPUT
1	IP	N15	INPUT
1	IP	N21	INPUT
1	IP	P20	INPUT
1	IP	R15	INPUT
1	IP	T17	INPUT
1	IP	T20	INPUT
1	IP	U18	INPUT
1	IP/VREF_1	D21	VREF
1	IP/VREF_1	L17	VREF
1	VCCO_1	E21	VCCO
1	VCCO_1	H18	VCCO

Table 154: **FG484 Package Pinout *(Cont'd)***

Bank	XC3S1600E Pin Name	FG484 Ball	Type
1	VCCO_1	K21	VCCO
1	VCCO_1	L16	VCCO
1	VCCO_1	P21	VCCO
1	VCCO_1	R17	VCCO
1	VCCO_1	V21	VCCO
2	IO	Y8	I/O
2	IO	Y9	I/O
2	IO	AA10	I/O
2	IO	AB5	I/O
2	IO	AB13	I/O
2	IO	AB14	I/O
2	IO	AB16	I/O
2	IO	AB18	I/O
2	IO/D5	AB11	DUAL
2	IO/M1	AA12	DUAL
2	IO/VREF_2	AB4	VREF
2	IO/VREF_2	AB21	VREF
2	IO_L01N_2/INIT_B	AB3	DUAL
2	IO_L01P_2/CSO_B	AA3	DUAL
2	IO_L03N_2/MOSI/CSI_B	Y5	DUAL
2	IO_L03P_2/DOUT/BUSY	W5	DUAL
2	IO_L04N_2	W6	I/O
2	IO_L04P_2	V6	I/O
2	IO_L06N_2	W7	I/O
2	IO_L06P_2	Y7	I/O
2	IO_L07N_2	U7	I/O
2	IO_L07P_2	V7	I/O
2	IO_L09N_2/VREF_2	V8	VREF
2	IO_L09P_2	W8	I/O
2	IO_L10N_2	T8	I/O
2	IO_L10P_2	U8	I/O
2	IO_L11N_2	AB8	I/O
2	IO_L11P_2	AA8	I/O
2	IO_L12N_2	W9	I/O
2	IO_L12P_2	V9	I/O
2	IO_L13N_2/VREF_2	R9	VREF
2	IO_L13P_2	T9	I/O
2	IO_L14N_2	AB9	I/O
2	IO_L14P_2	AB10	I/O
2	IO_L16N_2	U10	I/O
2	IO_L16P_2	T10	I/O
2	IO_L17N_2	R10	I/O
2	IO_L17P_2	P10	I/O