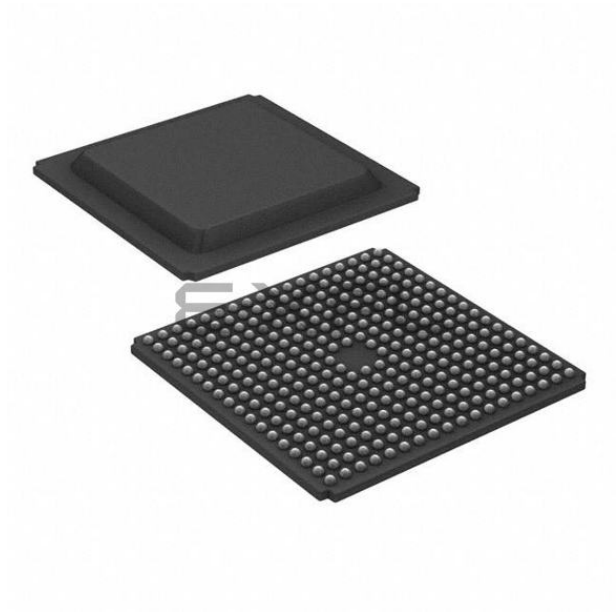
AMD Xilinx - XC3S1600E-4FG320C Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	3688
Number of Logic Elements/Cells	33192
Total RAM Bits	663552
Number of I/O	250
Number of Gates	1600000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	320-BGA
Supplier Device Package	320-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s1600e-4fg320c

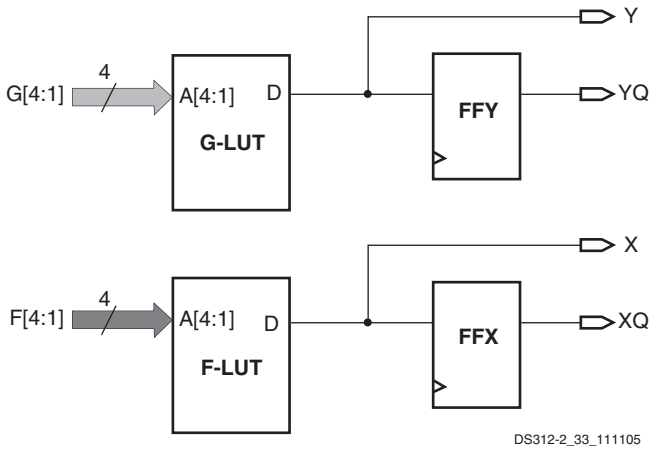

Figure 18: **LUT Resources in a Slice**

Wide Multiplexers

For additional information, refer to the “Using Dedicated Multiplexers” chapter in UG331.

Wide-function multiplexers effectively combine LUTs in order to permit more complex logic operations. Each slice has two of these multiplexers with F5MUX in the bottom portion of the slice and FiMUX in the top portion. The F5MUX multiplexes the two LUTs in a slice. The FiMUX multiplexes two CLB inputs which connect directly to the F5MUX and FiMUX results from the same slice or from other slices. See Figure 19.

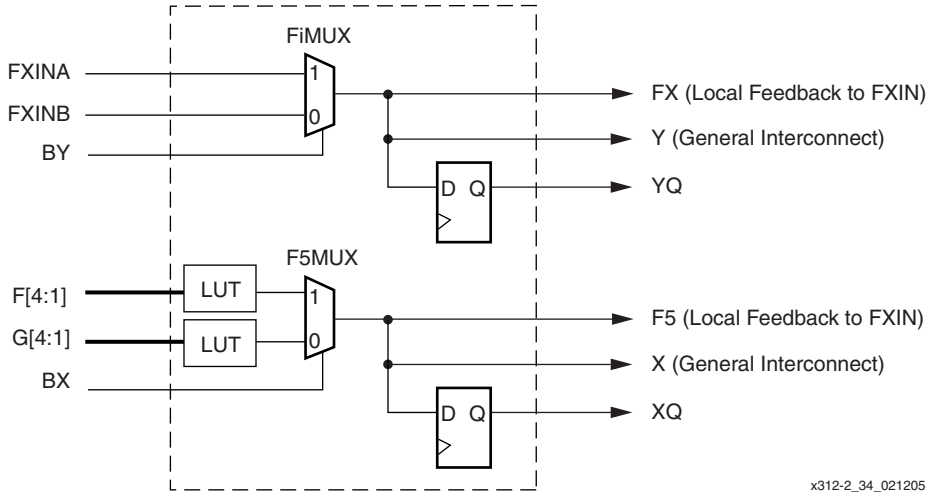

Figure 19: **Dedicated Multiplexers in Spartan-3E CLB**

Depending on the slice, FiMUX takes on the name F6MUX, F7MUX, or F8MUX. The designation indicates the number of inputs possible without restriction on the function. For example, an F7MUX can generate any function of seven inputs. Figure 20 shows the names of the multiplexers in each position in the Spartan-3E CLB. The figure also includes the direct connections within the CLB, along with the F7MUX connection to the CLB below.

Each mux can create logic functions of more inputs than indicated by its name. The F5MUX, for example, can generate any function of five inputs, with four inputs duplicated to two LUTs and the fifth input controlling the mux. Because each LUT can implement independent 2:1 muxes, the F5MUX can combine them to create a 4:1 mux, which is a six-input function. If the two LUTs have completely independent sets of inputs, some functions of all nine inputs can be implemented. Table 11 shows the connections for each multiplexer and the number of inputs possible for different types of functions.

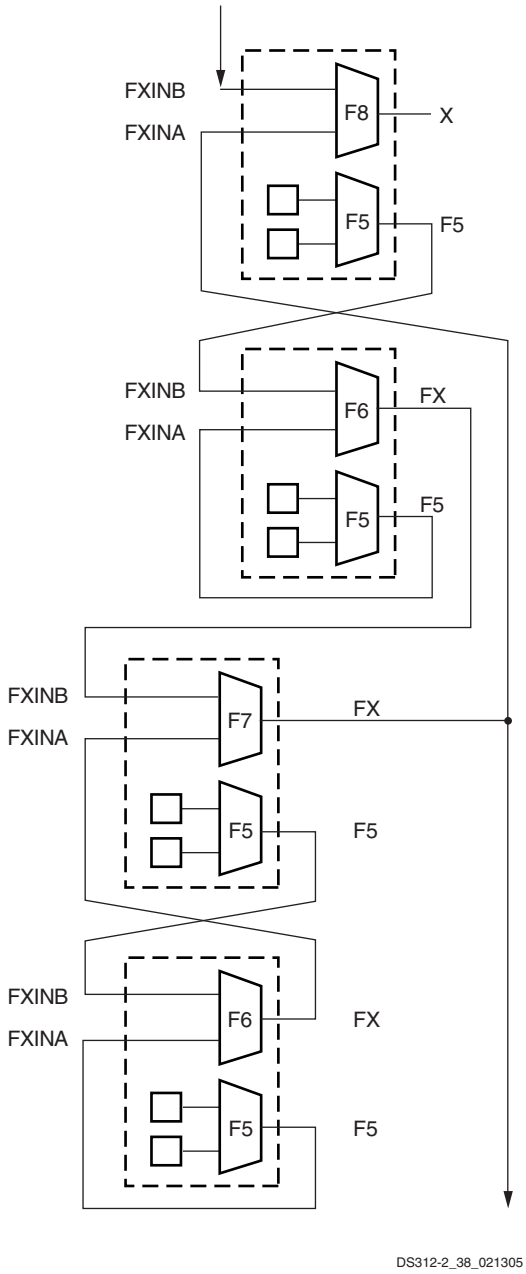

Figure 20: **MUXes and Dedicated Feedback in Spartan-3E CLB**

Table 11: **MUX Capabilities**

MUX	Usage	Input Source	Total Number of Inputs per Function		
			For Any Function	For MUX	For Limited Functions
F5MUX	F5MUX	LUTs	5	6 (4:1 MUX)	9
FiMUX	F6MUX	F5MUX	6	11 (8:1 MUX)	19
	F7MUX	F6MUX	7	20 (16:1 MUX)	39
	F8MUX	F7MUX	8	37 (32:1 MUX)	79

Table 14: **Carry Logic Functions *(Cont'd)***

Function	Description
CY0G	Carry generation for top half of slice. Fixed selection of: · G1 or G2 inputs to the LUT (both equal 1 when a carry is to be generated) · GAND gate for multiplication · BY input for carry initialization · Fixed 1 or 0 input for use as a simple Boolean function
CYMUXF	Carry generation or propagation mux for bottom half of slice. Dynamic selection via CYSELF of: · CYINIT carry propagation (CYSELF = 1) · CY0F carry generation (CYSELF = 0)
CYMUXG	Carry generation or propagation mux for top half of slice. Dynamic selection via CYSELF of: · CYMUXF carry propagation (CYSELG = 1) · CY0G carry generation (CYSELG = 0)
CYSELF	Carry generation or propagation select for bottom half of slice. Fixed selection of: · F-LUT output (typically XOR result) · Fixed 1 to always propagate
CYSELG	Carry generation or propagation select for top half of slice. Fixed selection of: · G-LUT output (typically XOR result) · Fixed 1 to always propagate
XORF	Sum generation for bottom half of slice. Inputs from: · F-LUT · CYINIT carry signal from previous stage Result is sent to either the combinatorial or registered output for the top of the slice.
XORG	Sum generation for top half of slice. Inputs from: · G-LUT · CYMUXF carry signal from previous stage Result is sent to either the combinatorial or registered output for the top of the slice.
FAND	Multiplier partial product for bottom half of slice. Inputs: · F-LUT F1 input · F-LUT F2 input Result is sent through CY0F to become the carry generate signal into CYMUXF
GAND	Multiplier partial product for top half of slice. Inputs: · G-LUT G1 input · G-LUT G2 input Result is sent through CY0G to become the carry generate signal into CYMUXG

The basic usage of the carry logic is to generate a half-sum in the LUT via an XOR function, which generates or propagates a carry out COUT via the carry mux CYMUXF (or CYMUXG), and then complete the sum with the dedicated XORF (or XORG) gate and the carry input CIN. This structure allows two bits of an arithmetic function in each slice. The CYMUXF (or CYMUXG) can be instantiated using the MUXCY element, and the XORF (or XORG) can be instantiated using the XORCY element.

The FAND (or GAND) gate is used for partial product multiplication and can be instantiated using the MULT_AND component. Partial products are generated by two-input AND gates and then added. The carry logic is efficient for the adder, but one of the inputs must be outside the LUT as shown in Figure 23.

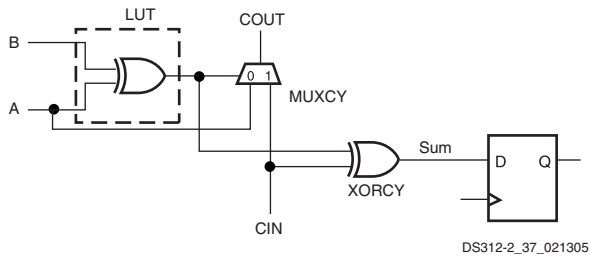

Figure 23: **Using the MUXCY and XORCY in the Carry Logic**

The FAND (or GAND) gate is used to duplicate one of the partial products, while the LUT generates both partial products and the XOR function, as shown in Figure 24.

VARIABLE Phase Shift Mode

In VARIABLE phase shift mode, the FPGA application dynamically adjusts the fine phase shift value using three inputs to the PS unit (PSEN, PSCLK, and PSINCDEC), as defined in Table 36 and shown in Figure 40.

Table 36: **Signals for Variable Phase Mode**

Signal	Direction	Description
PSEN(1)	Input	Enables the Phase Shift unit for variable phase adjustment.
PSCLK(1)	Input	Clock to synchronize phase shift adjustment.
PSINCDEC(1)	Input	When High, increments the current phase shift value. When Low, decrements the current phase shift value. This signal is synchronized to the PSCLK signal.
PSDONE	Output	Goes High to indicate that the present phase adjustment is complete and PS unit is ready for next phase adjustment request. This signal is synchronized to the PSCLK signal.

Notes:

1. This input supports either a true or inverted polarity.

The FPGA application uses the three PS inputs on the Phase Shift unit to dynamically and incrementally increase or decrease the phase shift amount on all nine DCM clock outputs.

To adjust the current phase shift value, the PSEN enable signal must be High to enable the PS unit. Coincidently, PSINCDEC must be High to increment the current phase shift amount or Low to decrement the current amount. All VARIABLE phase shift operations are controlled by the PSCLK input, which can be the CLKIN signal or any other clock signal.

Design Note

The VARIABLE phase shift feature operates differently from the Spartan-3 DCM; use the DCM_SP primitive, not the DCM primitive.

DCM_DELAY_STEP

DCM_DELAY_STEP is the finest delay resolution available in the PS unit. Its value is provided at the bottom of Table 105 in Module 3. For each enabled PSCLK cycle that PSINCDEC is High, the PS unit adds one DCM_ DELAY_STEP of phase shift to all nine DCM outputs. Similarly, for each enabled PSCLK cycle that PSINCDEC is Low, the PS unit subtracts one DCM_ DELAY_STEP of phase shift from all nine DCM outputs.

Because each DCM_DELAY_STEP has a minimum and maximum value, the actual phase shift delay for the present phase increment/decrement value (VALUE) falls within the minimum and maximum values according to Equation 4 and Equation 5.

$$T_{PS}(Max) = VALUE \bullet \text{DCM\_DELAY\_STEP\_MAX} \quad Eq\ 4$$

$$T_{PS}(Min) = VALUE \bullet \text{DCM\_DELAY\_STEP\_MIN} \quad Eq\ 5$$

The maximum variable phase shift steps, MAX_STEPS, is described in Equation 6 or Equation 7, for a given CLKIN input period, T_{CLKIN}, in nanoseconds. To convert this to a phase shift range measured in time and not steps, use MAX_STEPS derived in Equation 6 and Equation 7 for VALUE in Equation 4 and Equation 5.

If CLKIN < 60 MHz:

$$\text{MAX\_STEPS} = \pm[INTEGER(10 \bullet (T_{CLKIN} - 3))] \quad Eq\ 6$$

If CLKIN ≥ 60 MHz:

$$\text{MAX\_STEPS} = \pm[INTEGER(15 \bullet (T_{CLKIN} - 3))] \quad Eq\ 7$$

The phase adjustment might require as many as 100 CLKIN cycles plus 3 PSCLK cycles to take effect, at which point the DCM's PSDONE output goes High for one PSCLK cycle. This pulse indicates that the PS unit completed the previous adjustment and is now ready for the next request.

Asserting the Reset (RST) input returns the phase shift to zero.

By contrast, the clock switch matrixes on the top and bottom edges receive signals from any of the five following sources: two GCLK pins, two DCM outputs, or one Double-Line interconnect.

Table 41 indicates permissible connections between clock inputs and BUFGMUX elements. The I0-input provides the best input path to a clock buffer. The I1-input provides the secondary input for the clock multiplexer function.

The four BUFGMUX elements on the top edge are paired together and share inputs from the eight global clock inputs along the top edge. Each BUFGMUX pair connects to four of the eight global clock inputs, as shown in Figure 45. This optionally allows differential inputs to the global clock inputs without wasting a BUFGMUX element.

Table 41: **Connections from Clock Inputs to BUFGMUX Elements and Associated Quadrant Clock**

Quadrant Clock Line[1]	Left-Half BUFGMUX			Top or Bottom BUFGMUX			Right-Half BUFGMUX		
	Location[2]	I0 Input	I1 Input	Location[2]	I0 Input	I1 Input	Location[2]	I0 Input	I1 Input
H	*X0Y9*	LHCLK7	LHCLK6	*X1Y10*	GCLK7 or GCLK11	GCLK6 or GCLK10	*X3Y9*	RHCLK3	RHCLK2
G	*X0Y8*	LHCLK6	LHCLK7	*X1Y11*	GCLK6 or GCLK10	GCLK7 or GCLK11	*X3Y8*	RHCLK2	RHCLK3
F	*X0Y7*	LHCLK5	LHCLK4	*X2Y10*	GCLK5 or GCLK9	GCLK4 or GCLK8	*X3Y7*	RHCLK1	RHCLK0
E	*X0Y6*	LHCLK4	LHCLK5	*X2Y11*	GCLK4 or GCLK8	GCLK5 or GCLK9	*X3Y6*	RHCLK0	RHCLK1
D	*X0Y5*	LHCLK3	LHCLK2	*X1Y0*	GCLK3 or GCLK15	GCLK2 or GCLK14	*X3Y5*	RHCLK7	RHCLK6
C	*X0Y4*	LHCLK2	LHCLK3	*X1Y1*	GCLK2 or GCLK14	GCLK3 or GCLK15	*X3Y4*	RHCLK6	RHCLK7
B	*X0Y3*	LHCLK1	LHCLK0	*X2Y0*	GCLK1 or GCLK13	GCLK0 or GCLK12	*X3Y3*	RHCLK5	RHCLK4
A	*X0Y2*	LHCLK0	LHCLK1	*X2Y1*	GCLK0 or GCLK12	GCLK1 or GCLK13	*X3Y2*	RHCLK4	RHCLK5

Notes:

1. See Quadrant Clock Routing for connectivity details for the eight quadrant clocks.
2. See Figure 45 for specific BUFGMUX locations, and Figure 47 for information on how BUFGMUX elements drive onto a specific clock line within a quadrant.

Direct Connections

Direct connect lines route signals to neighboring tiles: vertically, horizontally, and diagonally. These lines most often drive a signal from a “source” tile to a double, hex, or long line and conversely from the longer interconnect back to a direct line accessing a “destination” tile.

Global Controls (STARTUP_SPARTAN3E)

In addition to the general-purpose interconnect, Spartan-3E FPGAs have two global logic control signals, as described in Table 43. These signals are available to the FPGA application via the STARTUP_SPARTAN3E primitive.

Table 43: **Spartan-3E Global Logic Control Signals**

Global Control Input	Description
GSR	**Global Set/Reset:** When High, asynchronously places all registers and flip-flops in their initial state (see Initialization, page 31). Asserted automatically during the FPGA configuration process (see Start-Up, page 105).
GTS	**Global Three-State:** When High, asynchronously forces all I/O pins to a high-impedance state (Hi-Z, three-state).

The Global Set/Reset (GSR) signal replaces the global reset signal included in many ASIC-style designs. Use the GSR control instead of a separate global reset signal in the design to free up CLB inputs, resulting in a smaller, more efficient design. Similarly, the GSR signal is asserted automatically during the FPGA configuration process, guaranteeing that the FPGA starts-up in a known state.

The STARTUP_SPARTAN3E primitive also includes two other signals used specifically during configuration. The MBT signals are for Dynamically Loading Multiple Configuration Images Using MultiBoot Option, page 91. The CLK input is an alternate clock for configuration Start-Up, page 105.

Daisy-Chaining

If the application requires multiple FPGAs with different configurations, then configure the FPGAs using a daisy chain, as shown in Figure 57. Daisy-chaining from a single SPI serial Flash PROM is supported in Stepping 1 devices. It is not supported in Stepping 0 devices. Use SPI Flash mode (M[2:0] = <0:0:1>) for the FPGA connected to the Platform Flash PROM and Slave Serial mode (M[2:0] = <1:1:1>) for all other FPGAs in the daisy-chain. After the master FPGA—the FPGA on the left in the diagram—finishes loading its configuration data from the SPI Flash PROM, the master device uses its DOUT output pin to supply data to the next device in the daisy-chain, on the falling CCLK edge.

Design Note

SPI mode daisy chains are supported only in Stepping 1 silicon versions.

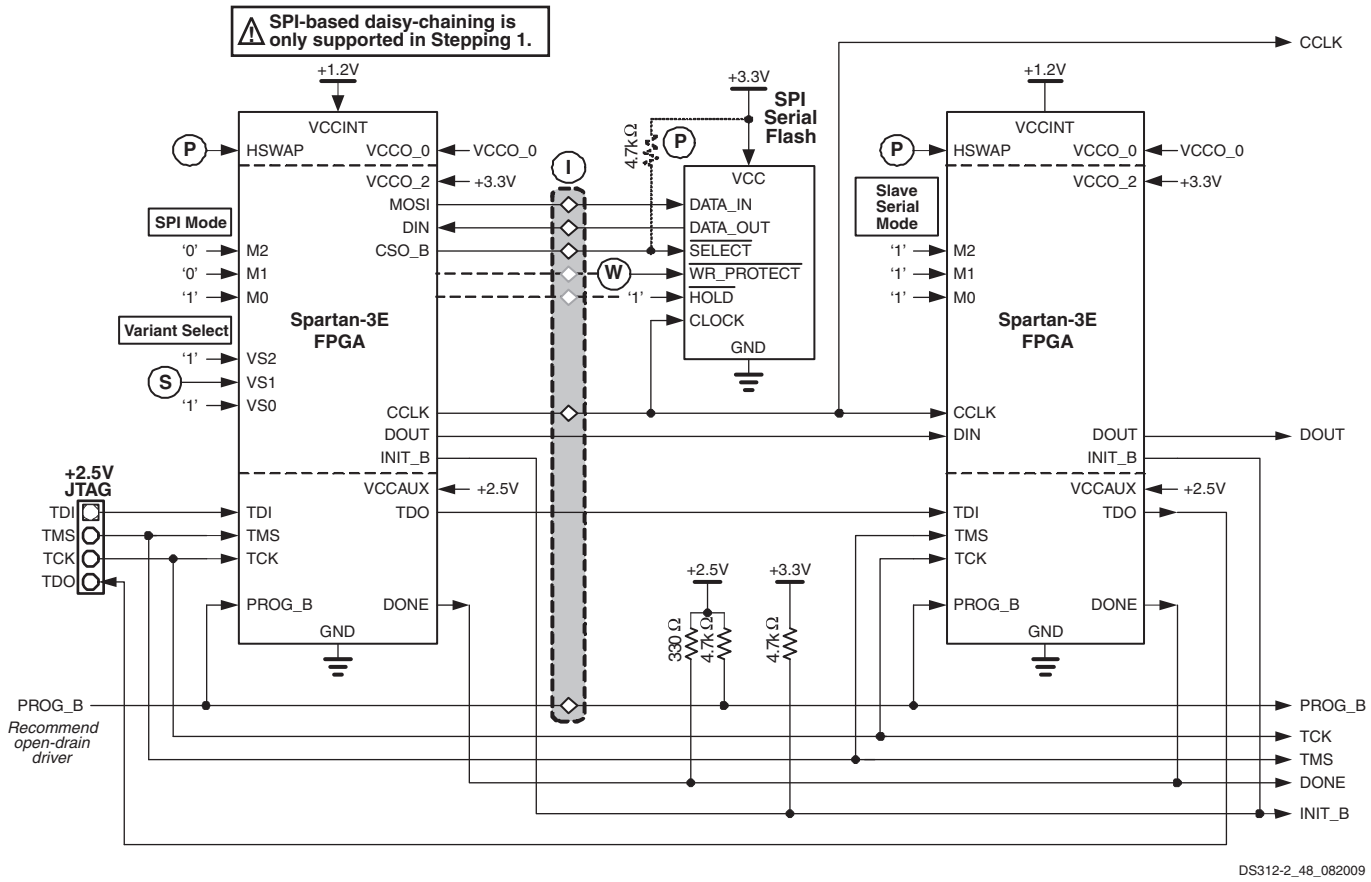

Figure 57: **Daisy-Chaining from SPI Flash Mode (Stepping 1)**

Programming Support

For successful daisy-chaining, the ***DONE_cycle*** configuration option must be set to cycle 5 or sooner. The default cycle is 4. See Table 69 and the Start-Up section for additional information.

(I) In production applications, the SPI Flash PROM is usually pre-programmed before it is mounted on the printed circuit board. The Xilinx ISE development software produces industry-standard programming files that can be used with third-party gang programmers. Consult your specific SPI Flash vendor for recommended production programming solutions.

In-system programming support is available from some third-party PROM programmers using a socket adapter with attached wires. To gain access to the SPI Flash signals, drive the FPGA's PROG_B input Low with an open-drain driver. This action places all FPGA I/O pins, including those attached to the SPI Flash, in high-impedance (Hi-Z). If the HSWAP input is Low, the I/Os have pull-up resistors to the V_{CCO} input on their respective I/O bank. The external programming hardware then has direct access to the SPI Flash pins. The programming access points are highlighted in the gray box in Figure 53, Figure 54, and Figure 57.

Beginning with the Xilinx ISE 8.2i software release, the iMPACT programming utility provides direct, in-system prototype programming support for STMicro M25P-series

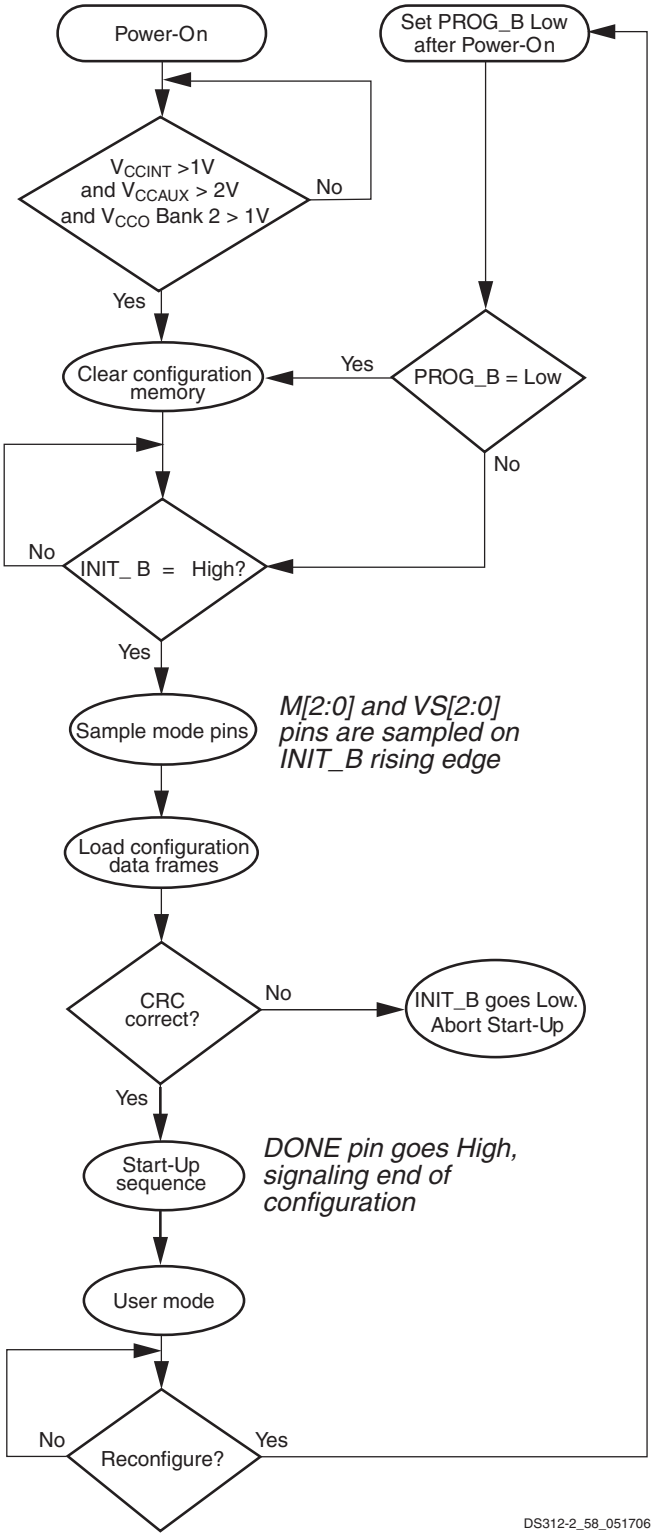

Figure 66: **General Configuration Process**

DC Electrical Characteristics

In this section, specifications may be designated as Advance, Preliminary, or Production. These terms are defined as follows:

Advance: Initial estimates are based on simulation, early characterization, and/or extrapolation from the characteristics of other families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on characterization. Further changes are not expected.

Production: These specifications are approved once the silicon has been characterized over numerous production lots. Parameter values are considered stable with no future changes expected.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all Spartan®-3E devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.**

Absolute Maximum Ratings

Stresses beyond those listed under Table 73, Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to absolute maximum conditions for extended periods of time adversely affects device reliability.

Table 73: **Absolute Maximum Ratings**

Symbol	Description	Conditions		Min	Max	Units
V_{CCINT}	Internal supply voltage			–0.5	1.32	V
V_{CCAUX}	Auxiliary supply voltage			–0.5	3.00	V
V_{CCO}	Output driver supply voltage			–0.5	3.75	V
V_{REF}	Input reference voltage			–0.5	V_{CCO} + 0.5 (1)	V
V_{IN} (1,2,3,4)	Voltage applied to all User I/O pins and Dual-Purpose pins	Driver in a high-impedance state	Commercial	–0.95	4.4	V
			Industrial	–0.85	4.3	V
	Voltage applied to all Dedicated pins		All temp. ranges	–0.5	V_{CCAUX} + 0.5 (3)	V
I_{IK}	Input clamp current per I/O pin	–0.5 V < V_{IN} < (V_{CCO} + 0.5 V)		–	±100	mA
V_{ESD}	Electrostatic Discharge Voltage	Human body model		–	±2000	V
		Charged device model		–	±500	V
		Machine model		–	±200	V
T_J	Junction temperature			–	125	°C
T_{STG}	Storage temperature			–65	150	°C

Notes:

1. Each of the User I/O and Dual-Purpose pins is associated with one of the four banks' V_{CCO} rails. Keeping V_{IN} within 500 mV of the associated V_{CCO} rails or ground rail ensures that the internal diode junctions do not turn on. Table 77 specifies the V_{CCO} range used to evaluate the maximum V_{IN} voltage.
2. Input voltages outside the -0.5V to V_{CCO} + 0.5V (or V_{CCAUX} + 0.5V) voltage range are require the I_{IK} input diode clamp diode rating is met and no more than 100 pins exceed the range simultaneously. Prolonged exposure to such current may compromise device reliability. A sustained current of 10 mA will not compromise device reliability. See XAPP459: *Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins on Spartan-3 Families* for more details.
3. All Dedicated pins (PROG_B, DONE, TCK, TDI, TDO, and TMS) draw power from the V_{CCAUX} rail (2.5V). Meeting the V_{IN} max limit ensures that the internal diode junctions that exist between each of these pins and the V_{CCAUX} rail do not turn on. Table 77 specifies the V_{CCAUX} range used to evaluate the maximum V_{IN} voltage. As long as the V_{IN} max specification is met, oxide stress is not possible.
4. See XAPP459: *Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins on Spartan-3 Families*.
5. For soldering guidelines, see UG112: *Device Packaging and Thermal Characteristics* and XAPP427: *Implementation and Solder Reflow Guidelines for Pb-Free Packages*.

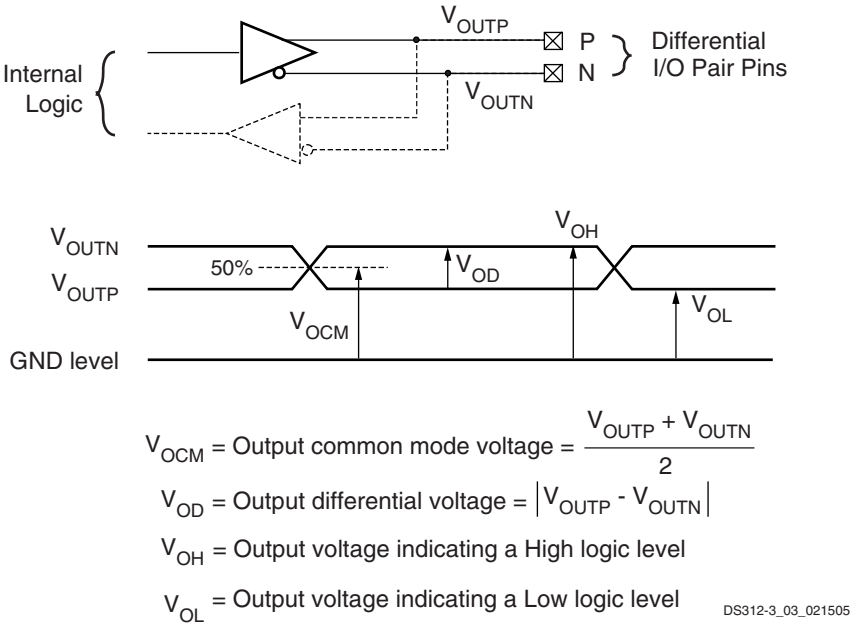

Figure 70: **Differential Output Voltages**

Table 83: **DC Characteristics of User I/Os Using Differential Signal Standards**

IOSTANDARD Attribute	V_{OD}			ΔV_{OD}		V_{OCM}			ΔV_{OCM}		V_{OH}	V_{OL}
	Min (mV)	Typ (mV)	Max (mV)	Min (mV)	Max (mV)	Min (V)	Typ (V)	Max (V)	Min (mV)	Max (mV)	Min (V)	Max (V)
LVDS_25	250	350	450	–	–	1.125	–	1.375	–	–	–	–
BLVDS_25	250	350	450	–	–	–	1.20	–	–	–	–	–
MINI_LVDS_25	300	–	600	–	50	1.0	–	1.4	–	50	–	–
RSDS_25	100	–	400	–	–	1.1	–	1.4	–	–	–	–
DIFF_HSTL_I_18	–	–	–	–	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_III_18	–	–	–	–	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_SSTL18_I	–	–	–	–	–	–	–	–	–	–	V_{TT} + 0.475	V_{TT} – 0.475
DIFF_SSTL2_I	–	–	–	–	–	–	–	–	–	–	V_{TT} + 0.61	V_{TT} – 0.61

Notes:

1. The numbers in this table are based on the conditions set forth in Table 77 and Table 82.
2. Output voltage measurements for all differential standards are made with a termination resistor (R_T) of 100Ω across the N and P pins of the differential signal pair. The exception is for BLVDS, shown in Figure 71.
3. At any given time, no more than two of the following differential output standards may be assigned to an I/O bank: LVDS_25, RSDS_25, MINI_LVDS_25

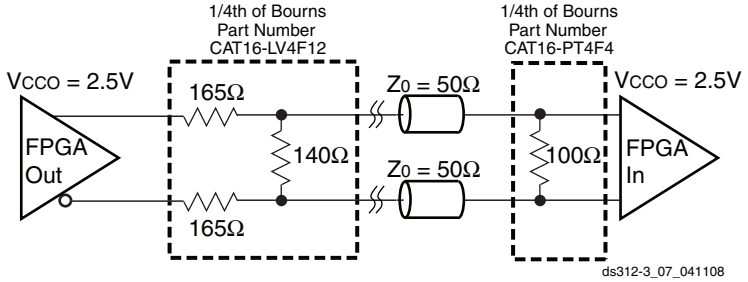

Figure 71: **External Termination Resistors for BLVDS Transmitter and BLVDS Receiver**

Switching Characteristics

All Spartan-3E FPGAs ship in two speed grades: -4 and the higher performance -5. Switching characteristics in this document may be designated as Advance, Preliminary, or Production, as shown in Table 84. Each category is defined as follows:

Advance: These specifications are based on simulations only and are typically available soon after establishing FPGA specifications. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These specifications are based on complete early silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting preliminary delays is greatly reduced compared to Advance data.

Production: These specifications are approved once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Software Version Requirements

Production-quality systems must use FPGA designs compiled using a speed file designated as PRODUCTION status. FPGAs designs using a less mature speed file designation should only be used during system prototyping or pre-production qualification. FPGA designs with speed files designated as Advance or Preliminary should not be used in a production-quality system.

Whenever a speed file designation changes, as a device matures toward Production status, rerun the latest Xilinx ISE software on the FPGA design to ensure that the FPGA design incorporates the latest timing information and software updates.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all Spartan-3E devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.**

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Timing parameters and their representative values are selected for inclusion below either because they are important as general design requirements or they indicate fundamental device performance characteristics. The Spartan-3E speed files (v1.27), part of the Xilinx Development Software, are the original source for many but not all of the values. The speed grade designations for these files are shown in Table 84. For more complete, more precise, and worst-case data, use the values reported by the Xilinx static timing analyzer (TRACE in the Xilinx development software) and back-annotated to the simulation netlist.

Table 84: **Spartan-3E v1.27 Speed Grade Designations**

Device	Advance	Preliminary	Production
XC3S100E			-MIN, -4, -5
XC3S250E			-MIN, -4, -5
XC3S500E			-MIN, -4, -5
XC3S1200E			-MIN, -4, -5
XC3S1600E			-MIN, -4, -5

Table 85 provides the history of the Spartan-3E speed files since all devices reached Production status.

Table 85: **Spartan-3E Speed File Version History**

Version	ISE Release	Description
1.27	9.2.03i	Added XA Automotive.
1.26	8.2.02i	Added -0/-MIN speed grade, which includes minimum values.
1.25	8.2.01i	Added XA Automotive devices to speed file. Improved model for left and right DCMs.
1.23	8.2i	Updated input setup/hold values based on default IFD_DELAY_VALUE settings.
1.21	8.1.03i	All Spartan-3E FPGAs and all speed grades elevated to Production status.

Simultaneously Switching Output Guidelines

This section provides guidelines for the recommended maximum allowable number of Simultaneous Switching Outputs (SSOs). These guidelines describe the maximum number of user I/O pins of a given output signal standard that should simultaneously switch in the same direction, while maintaining a safe level of switching noise. Meeting these guidelines for the stated test conditions ensures that the FPGA operates free from the adverse effects of ground and power bounce.

Ground or power bounce occurs when a large number of outputs simultaneously switch in the same direction. The output drive transistors all conduct current to a common voltage rail. Low-to-High transitions conduct to the V_{CCO} rail; High-to-Low transitions conduct to the GND rail. The resulting cumulative current transient induces a voltage difference across the inductance that exists between the die pad and the power supply or ground return. The inductance is associated with bonding wires, the package lead frame, and any other signal routing inside the package. Other variables contribute to SSO noise levels, including stray inductance on the PCB as well as capacitive loading at receivers. Any SSO-induced voltage consequently affects internal switching noise margins and ultimately signal quality.

Table 96 and Table 97 provide the essential SSO guidelines. For each device/package combination, Table 96 provides the number of equivalent V_{CCO}/GND pairs. The equivalent number of pairs is based on characterization and might not match the physical number of pairs. For each output signal standard and drive strength, Table 97 recommends the maximum number of SSOs, switching in the same direction, allowed per V_{CCO}/GND pair within an I/O bank. The guidelines in Table 97 are categorized by package style. Multiply the appropriate numbers from Table 96 and Table 97 to calculate the maximum number of SSOs allowed within an I/O bank. Exceeding these SSO guidelines might result in increased power or ground bounce, degraded signal integrity, or increased system jitter.

SSO_{MAX}/IO Bank = Table 96 x Table 97

The recommended maximum SSO values assumes that the FPGA is soldered on the printed circuit board and that the board uses sound design practices. The SSO values do not apply for FPGAs mounted in sockets, due to the lead inductance introduced by the socket.

The number of SSOs allowed for quad-flat packages (VQ, TQ, PQ) is lower than for ball grid array packages (FG) due to the larger lead inductance of the quad-flat packages. The results for chip-scale packaging (CP132) are better than quad-flat packaging but not as high as for ball grid array packaging. Ball grid array packages are recommended for applications with a large number of simultaneously switching outputs.

Table 96: **Equivalent V_{CCO}/GND Pairs per Bank**

Device	Package Style *(including Pb-free)*							
	VQ100	CP132	TQ144	PQ208	FT256	FG320	FG400	FG484
XC3S100E	2	2	2	-	-	-	-	-
XC3S250E	2	2	2	3	4	-	-	-
XC3S500E	2	2	-	3	4	5	-	-
XC3S1200E	-	-	-	-	4	5	6	-
XC3S1600E	-	-	-	-	-	5	6	7

Table 97: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}/GND Pair**

Signal Standard (IOSTANDARD)			Package Type				
			VQ 100	TQ 144	PQ 208	CP 132	FT256 FG320 FG400 FG484
Single-Ended Standards							
LVTTL	Slow	2	34	20	19	52	60
		4	17	10	10	26	41
		6	17	10	7	26	29
		8	8	6	6	13	22
		12	8	6	5	13	13
		16	5	5	5	6	11
	Fast	2	17	17	17	26	34
		4	9	9	9	13	20
		6	7	7	7	13	15
		8	6	6	6	6	12
		12	5	5	5	6	10
		16	5	5	5	5	9
LVCMOS33	Slow	2	34	20	20	52	76
		4	17	10	10	26	46
		6	17	10	7	26	27
		8	8	6	6	13	20
		12	8	6	5	13	13
		16	5	5	5	6	10
	Fast	2	17	17	17	26	44
		4	8	8	8	13	26
		6	8	6	6	13	16
		8	6	6	6	6	12
		12	5	5	5	6	10
		16	8	8	5	5	8
LVCMOS25	Slow	2	28	16	16	42	76
		4	13	10	10	19	46
		6	13	7	7	19	33
		8	6	6	6	9	24
		12	6	6	6	9	18
	Fast	2	17	16	16	26	42
		4	9	9	9	13	20
		6	9	7	7	13	15
		8	6	6	6	6	13
		12	5	5	5	6	11
LVCMOS18	Slow	2	19	11	8	29	64
		4	13	7	6	19	34
		6	6	5	5	9	22
		8	6	4	4	9	18
	Fast	2	13	8	8	19	36
		4	8	5	5	13	21
		6	4	4	4	6	13
		8	4	4	4	6	10

Table 97: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}/GND Pair *(Cont'd)***

Signal Standard (IOSTANDARD)			Package Type				
			VQ 100	TQ 144	PQ 208	CP 132	FT256 FG320 FG400 FG484
LVCMOS15	Slow	2	16	10	10	19	55
		4	8	7	7	9	31
		6	6	5	5	9	18
	Fast	2	9	9	9	13	25
		4	7	7	7	7	16
		6	5	5	5	5	13
LVCMOS12	Slow	2	17	11	11	16	55
	Fast	2	10	10	10	10	31
PCI33_3			8	8	8	16	16
PCI66_3			8	8	8	13	13
PCIX			7	7	7	11	11
HSTL_I_18			10	10	10	16	17
HSTL_III_18			10	10	10	16	16
SSTL18_I			9	9	9	15	15
SSTL2_I			12	12	12	18	18
Differential Standards (Number of I/O Pairs or Channels)							
LVDS_25			6	6	6	12	20
BLVDS_25			4	4	4	4	4
MINI_LVDS_25			6	6	6	12	20
LVPECL_25			Input Only				
RSDS_25			6	6	6	12	20
DIFF_HSTL_I_18			5	5	5	8	8
DIFF_HSTL_IIII_18			5	5	5	8	8
DIFF_SSTL18_I			4	4	4	7	7
DIFF_SSTL2_I			6	6	6	9	8

Notes:

1. The numbers in this table are recommendations that assume sound board layout practice. This table assumes the following parasitic factors: combined PCB trace and land inductance per VCCO and GND pin of 1.0 nH, receiver capacitive load of 15 pF. Test limits are the VIL/VIH voltage limits for the respective I/O standard.
2. The PQ208 results are based on physical measurements of a PQ208 package soldered to a typical printed circuit board. All other results are based on worst-case simulation and an interpolation of the PQ208 physical results.
3. If more than one signal standard is assigned to the I/Os of a given bank, refer to XAPP689: Managing Ground Bounce in Large FPGAs for information on how to perform weighted average SSO calculations.

18 x 18 Embedded Multiplier Timing

Table 102: **18 x 18 Embedded Multiplier Timing**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Combinatorial Delay						
T_{MULT}	Combinatorial multiplier propagation delay from the A and B inputs to the P outputs, assuming 18-bit inputs and a 36-bit product (AREG, BREG, and PREG registers unused)	-	4.34(1)	-	4.88(1)	ns
Clock-to-Output Times						
T_{MSCKP_P}	Clock-to-output delay from the active transition of the CLK input to valid data appearing on the P outputs when using the PREG register(2)	-	0.98	-	1.10	ns
T_{MSCKP_A} T_{MSCKP_B}	Clock-to-output delay from the active transition of the CLK input to valid data appearing on the P outputs when using either the AREG or BREG register(3)	-	4.42	-	4.97	ns
Setup Times						
T_{MSDCK_P}	Data setup time at the A or B input before the active transition at the CLK when using only the PREG output register (AREG, BREG registers unused)(2)	3.54	-	3.98	-	ns
T_{MSDCK_A}	Data setup time at the A input before the active transition at the CLK when using the AREG input register(3)	0.20	-	0.23	-	ns
T_{MSDCK_B}	Data setup time at the B input before the active transition at the CLK when using the BREG input register(3)	0.35	-	0.39	-	ns
Hold Times						
T_{MSCKD_P}	Data hold time at the A or B input after the active transition at the CLK when using only the PREG output register (AREG, BREG registers unused)(2)	–0.97	-	–0.97	-	ns
T_{MSCKD_A}	Data hold time at the A input after the active transition at the CLK when using the AREG input register(3)	0.03	-	0.04	-	ns
T_{MSCKD_B}	Data hold time at the B input after the active transition at the CLK when using the BREG input register(3)	0.04	-	0.05	-	ns
Clock Frequency						
F_{MULT}	Internal operating frequency for a two-stage 18x18 multiplier using the AREG and BREG input registers and the PREG output register(1)	0	270	0	240	MHz

Notes:

1. Combinatorial delay is less and pipelined performance is higher when multiplying input data with less than 18 bits.
2. The PREG register is typically used in both single-stage and two-stage pipelined multiplier implementations.
3. Input registers AREG or BREG are typically used when inferring a two-stage multiplier.

Table 105: **Switching Characteristics for the DLL *(Cont'd)***

Symbol	Description		Device	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Phase Alignment(4)								
CLKIN_CLKFB_PHASE	Phase offset between the CLKIN and CLKFB inputs		All	-	±200	-	±200	ps
CLKOUT_PHASE_DLL	Phase offset between DLL outputs	CLK0 to CLK2X (not CLK2X180)		-	±[1% of CLKIN period + 100]	-	±[1% of CLKIN period + 100]	ps
		All others		-	±[1% of CLKIN period + 200]	-	±[1% of CLKIN period + 200]	ps
Lock Time								
LOCK_DLL(3)	When using the DLL alone: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase	5 MHz ≤ F_{CLKIN} ≤ 15 MHz	All	-	5	-	5	ms
		F_{CLKIN} > 15 MHz		-	600	-	600	µs
Delay Lines								
DCM_DELAY_STEP	Finest delay resolution		All	20	40	20	40	ps

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 77 and Table 104.
2. Indicates the maximum amount of output jitter that the DCM adds to the jitter on the CLKIN input.
3. For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
4. Some jitter and duty-cycle specifications include 1% of input clock period or 0.01 UI.
   Example: The data sheet specifies a maximum jitter of ±[1% of CLKIN period + 150]. Assume the CLKIN frequency is 100 MHz. The equivalent CLKIN period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 150 ps] = ±250 ps.

Digital Frequency Synthesizer (DFS)

Table 106: **Recommended Operating Conditions for the DFS**

Symbol		Description		Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Input Frequency Ranges(2)								
F_{CLKIN}	CLKIN_FREQ_FX	Frequency for the CLKIN input		0.200	333(4)	0.200	333(4)	MHz
Input Clock Jitter Tolerance(3)								
CLKIN_CYC_JITT_FX_LF		Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency	F_{CLKFX} ≤ 150 MHz	-	±300	-	±300	ps
CLKIN_CYC_JITT_FX_HF			F_{CLKFX} > 150 MHz	-	±150	-	±150	ps
CLKIN_PER_JITT_FX		Period jitter at the CLKIN input		-	±1	-	±1	ns

Notes:

1. DFS specifications apply when either of the DFS outputs (CLKFX or CLKFX180) are used.
2. If both DFS and DLL outputs are used on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 104.
3. CLKIN input jitter beyond these limits may cause the DCM to lose lock.
4. To support double the maximum effective FCLKIN limit, set the CLKIN_DIVIDE_BY_2 attribute to TRUE. This attribute divides the incoming clock frequency by two as it enters the DCM.

Table 119: **Configuration Timing Requirements for Attached SPI Serial Flash**

Symbol	Description	Requirement	Units
T_{CCS}	SPI serial Flash PROM chip-select time	$T_{CCS} \leq T_{MCCL1} - T_{CCO}$	ns
T_{DSU}	SPI serial Flash PROM data input setup time	$T_{DSU} \leq T_{MCCL1} - T_{CCO}$	ns
T_{DH}	SPI serial Flash PROM data input hold time	$T_{DH} \leq T_{MCCH1}$	ns
T_V	SPI serial Flash PROM data clock-to-output time	$T_V \leq T_{MCCLn} - T_{DCC}$	ns
f_C or f_R	Maximum SPI serial Flash PROM clock frequency (also depends on specific read command used)	$f_C \geq \frac{1}{T_{CCLKn(min)}}$	MHz

Notes:

1. These requirements are for successful FPGA configuration in SPI mode, where the FPGA provides the CCLK frequency. The post configuration timing can be different to support the specific needs of the application loaded into the FPGA and the resulting clock source.
2. Subtract additional printed circuit board routing delay as required by the application.

Package Overview

Table 125 shows the eight low-cost, space-saving production package styles for the Spartan-3E family. Each package style is available as a standard and an environmentally friendly lead-free (Pb-free) option. The Pb-free packages include an extra 'G' in the package style name. For example, the standard "VQ100" package becomes "VQG100" when ordered as the Pb-free option. The mechanical dimensions of the standard and Pb-free packages are similar, as shown in the mechanical drawings provided in Table 127.

Not all Spartan-3E densities are available in all packages. For a specific package, however, there is a common footprint that supports all the devices available in that package. See the footprint diagrams that follow.

For additional package information, see UG112: *Device Package User Guide*.

Table 125: **Spartan-3E Family Package Options**

Package	Leads	Type	Maximum I/O	Lead Pitch (mm)	Footprint Area (mm)	Height (mm)	Mass[1] (g)
VQ100 / VQG100	100	Very-thin Quad Flat Pack (VQFP)	66	0.5	16 x 16	1.20	0.6
CP132 / CPG132	132	Chip-Scale Package (CSP)	92	0.5	8.1 x 8.1	1.10	0.1
TQ144 / TQG144	144	Thin Quad Flat Pack (TQFP)	108	0.5	22 x 22	1.60	1.4
PQ208 / PQG208	208	Plastic Quad Flat Pack (PQFP)	158	0.5	30.6 x 30.6	4.10	5.3
FT256 / FTG256	256	Fine-pitch, Thin Ball Grid Array (FBGA)	190	1.0	17 x 17	1.55	0.9
FG320 / FGG320	320	Fine-pitch Ball Grid Array (FBGA)	250	1.0	19 x 19	2.00	1.4
FG400 / FGG400	400	Fine-pitch Ball Grid Array (FBGA)	304	1.0	21 x 21	2.43	2.2
FG484 / FGG484	484	Fine-pitch Ball Grid Array (FBGA)	376	1.0	23 x 23	2.60	2.2

Notes:

1. Package mass is ±10%.

Selecting the Right Package Option

Spartan-3E FPGAs are available in both quad-flat pack (QFP) and ball grid array (BGA) packaging options. While QFP packaging offers the lowest absolute cost, the BGA packages are superior in almost every other aspect, as summarized in Table 126. Consequently, Xilinx recommends using BGA packaging whenever possible.

Table 126: **QFP and BGA Comparison**

Characteristic	Quad Flat Pack (QFP)	Ball Grid Array (BGA)
Maximum User I/O	158	376
Packing Density (Logic/Area)	Good	Better
Signal Integrity	Fair	Better
Simultaneous Switching Output (SSO) Support	Fair	Better
Thermal Dissipation	Fair	Better
Minimum Printed Circuit Board (PCB) Layers	4	4-6
Hand Assembly/Rework	Possible	Difficult

Footprint Migration Differences

Table 136 summarizes any footprint and functionality differences between the XC3S100E, the XC3S250E, and the XC3S500E FPGAs that may affect easy migration between devices in the CP132 package. There are 14 such balls. All other pins not listed in Table 136 unconditionally migrate between Spartan-3E devices available in the CP132 package.

The XC3S100E is duplicated on both the left and right sides of the table to show migrations to and from the XC3S250E and the XC3S500E. The arrows indicate the direction for easy migration. A double-ended arrow (←→) indicates that the two pins have identical functionality. A left-facing arrow (←) indicates that the pin on the device on the right unconditionally migrates to the pin on the device on the left. It may be possible to migrate the opposite direction depending on the I/O configuration. For example, an I/O pin (Type = I/O) can migrate to an input-only pin (Type = INPUT) if the I/O pin is configured as an input.

The XC3S100E FPGA in the CP132 package has four fewer BPI-mode address lines than the XC3S250E and XC3S500E.

Table 136: **CP132 Footprint Migration Differences**

CP132 Ball	Bank	XC3S100E Type	Migration	XC3S250E Type	Migration	XC3S500E Type	Migration	XC3S100E Type
A12	0	N.C.	→	I/O	←→	I/O	←	N.C.
B4	0	INPUT	→	I/O	←→	I/O	←	INPUT
B11	0	N.C.	→	I/O	←→	I/O	←	N.C.
B12	0	N.C.	→	I/O	←→	I/O	←	N.C.
C4	0	N.C.	→	I/O	←→	I/O	←	N.C.
C11	0	INPUT	→	I/O	←→	I/O	←	INPUT
D1	3	N.C.	→	I/O	←→	I/O	←	N.C.
D2	3	I/O	→	I/O (Diff)	←→	I/O (Diff)	←	I/O
K3	3	VREF(INPUT)	→	VREF(I/O)	←→	VREF(I/O)	←	VREF(INPUT)
M9	2	N.C.	→	DUAL	←→	DUAL	←	N.C.
M10	2	N.C.	→	DUAL	←→	DUAL	←	N.C.
N9	2	N.C.	→	DUAL	←→	DUAL	←	N.C.
N10	2	N.C.	→	DUAL	←→	DUAL	←	N.C.
P11	2	VREF(INPUT)	→	VREF(I/O)	←→	VREF(I/O)	←	VREF(INPUT)
DIFFERENCES			**14**		**0**		**14**	

Legend:

←→ This pin is identical on the device on the left and the right.

→ This pin can unconditionally migrate from the device on the left to the device on the right. Migration in the other direction may be possible depending on how the pin is configured for the device on the right.

← This pin can unconditionally migrate from the device on the right to the device on the left. Migration in the other direction may be possible depending on how the pin is configured for the device on the left.

Table 137: **TQ144 Package Pinout *(Cont'd)***

Bank	XC3S100E Pin Name	XC3S250E Pin Name	TQ144 Pin	Type
2	IP	IP	P38	INPUT
2	IP	IP	P41	INPUT
2	IP	IP	P69	INPUT
2	IP_L03N_2/VREF_2	IP_L03N_2/VREF_2	P48	VREF
2	IP_L03P_2	IP_L03P_2	P47	INPUT
2	IP_L06N_2/M2/GCLK1	IP_L06N_2/M2/GCLK1	P57	DUAL/GCLK
2	IP_L06P_2/RDWR_B/GCLK0	IP_L06P_2/RDWR_B/GCLK0	P56	DUAL/GCLK
2	VCCO_2	VCCO_2	P42	VCCO
2	VCCO_2	VCCO_2	P49	VCCO
2	VCCO_2	VCCO_2	P64	VCCO
3	IP/VREF_3	IO/VREF_3	P31	***100E:*** VREF(INPUT) ***250E:*** VREF(I/O)
3	IO_L01N_3	IO_L01N_3	P3	I/O
3	IO_L01P_3	IO_L01P_3	P2	I/O
3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	P5	VREF
3	IO_L02P_3	IO_L02P_3	P4	I/O
3	IO_L03N_3	IO_L03N_3	P8	I/O
3	IO_L03P_3	IO_L03P_3	P7	I/O
3	IO_L04N_3/LHCLK1	IO_L04N_3/LHCLK1	P15	LHCLK
3	IO_L04P_3/LHCLK0	IO_L04P_3/LHCLK0	P14	LHCLK
3	IO_L05N_3/LHCLK3/IRDY2	IO_L05N_3/LHCLK3	P17	LHCLK
3	IO_L05P_3/LHCLK2	IO_L05P_3/LHCLK2	P16	LHCLK
3	IO_L06N_3/LHCLK5	IO_L06N_3/LHCLK5	P21	LHCLK
3	IO_L06P_3/LHCLK4/TRDY2	IO_L06P_3/LHCLK4	P20	LHCLK
3	IO_L07N_3/LHCLK7	IO_L07N_3/LHCLK7	P23	LHCLK
3	IO_L07P_3/LHCLK6	IO_L07P_3/LHCLK6	P22	LHCLK
3	IO_L08N_3	IO_L08N_3	P26	I/O
3	IO_L08P_3	IO_L08P_3	P25	I/O
3	IO_L09N_3	IO_L09N_3	P33	I/O
3	IO_L09P_3	IO_L09P_3	P32	I/O
3	IO_L10N_3	IO_L10N_3	P35	I/O
3	IO_L10P_3	IO_L10P_3	P34	I/O
3	IP	IP	P6	INPUT
3	IO	IP	P10	***100E:*** I/O ***250E:*** INPUT
3	IP	IP	P18	INPUT
3	IP	IP	P24	INPUT
3	IO	IP	P29	***100E:*** I/O ***250E:*** INPUT
3	IP	IP	P36	INPUT
3	IP/VREF_3	IP/VREF_3	P12	VREF
3	VCCO_3	VCCO_3	P13	VCCO
3	VCCO_3	VCCO_3	P28	VCCO
GND	GND	GND	P11	GND
GND	GND	GND	P19	GND

User I/Os by Bank

Table 138 and Table 139 indicate how the 108 available user-I/O pins are distributed between the four I/O banks on the TQ144 package.

Table 138: **User I/Os Per Bank for the XC3S100E in the TQ144 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF[1]	CLK[2]
Top	0	26	9	6	1	2	8
Right	1	28	0	5	21	2	0[2]
Bottom	2	26	0	4	20	2	0[2]
Left	3	28	13	4	0	3	8
TOTAL		**108**	**22**	**19**	**42**	**9**	**16**

Notes:
1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

Table 139: **User I/Os Per Bank for the XC3S250E in TQ144 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF[1]	CLK[2]
Top	0	26	9	6	1	2	8
Right	1	28	0	5	21	2	0[2]
Bottom	2	26	0	4	20	2	0[2]
Left	3	28	11	6	0	3	8
TOTAL		**108**	**20**	**21**	**42**	**9**	**16**

Notes:
1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

Footprint Migration Differences

Table 140 summarizes any footprint and functionality differences between the XC3S100E and the XC3S250E FPGAs that may affect easy migration between devices. There are four such pins. All other pins not listed in Table 140 unconditionally migrate between Spartan-3E devices available in the TQ144 package.

The arrows indicate the direction for easy migration. For example, a left-facing arrow indicates that the pin on the XC3S250E unconditionally migrates to the pin on the XC3S100E. It may be possible to migrate the opposite direction depending on the I/O configuration. For example, an I/O pin (Type = I/O) can migrate to an input-only pin (Type = INPUT) if the I/O pin is configured as an input.

Table 140: **TQ144 Footprint Migration Differences**

TQ144 Pin	Bank	XC3S100E Type	Migration	XC3S250E Type
P10	3	I/O	←	INPUT
P29	3	I/O	←	INPUT
P31	3	VREF(INPUT)	→	VREF(I/O)
P66	2	VREF(INPUT)	→	VREF(I/O)
DIFFERENCES			**4**	

Legend:

→ This pin can unconditionally migrate from the device on the left to the device on the right. Migration in the other direction may be possible depending on how the pin is configured for the device on the right.

← This pin can unconditionally migrate from the device on the right to the device on the left. Migration in the other direction may be possible depending on how the pin is configured for the device on the left.