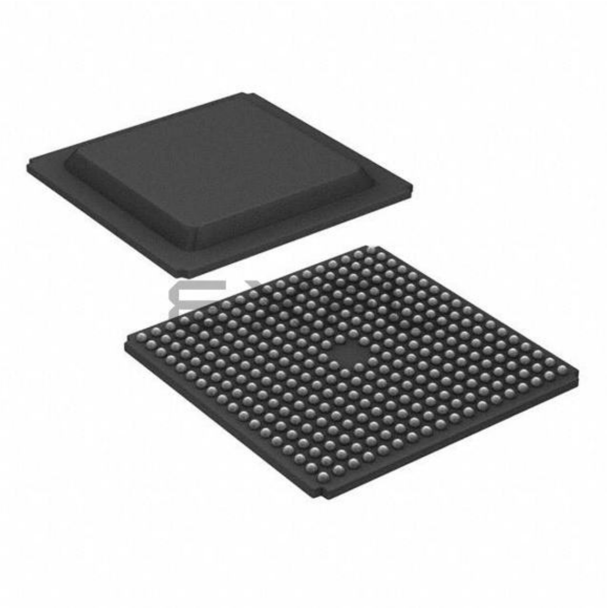
AMD Xilinx - XC3S1600E-4FG320I Datasheet



Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	3688
Number of Logic Elements/Cells	33192
Total RAM Bits	663552
Number of I/O	250
Number of Gates	1600000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	320-BGA
Supplier Device Package	320-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s1600e-4fg320i

IOBs Organized into Banks

The Spartan-3E architecture organizes IOBs into four I/O banks as shown in Figure 13. Each bank maintains separate V_{CCO} and V_{REF} supplies. The separate supplies allow each bank to independently set V_{CCO}. Similarly, the V_{REF} supplies can be set for each bank. Refer to Table 6 and Table 7 for V_{CCO} and V_{REF} requirements.

When working with Spartan-3E devices, most of the differential I/O standards are compatible and can be combined within any given bank. Each bank can support any two of the following differential standards: LVDS_25 outputs, MINI_LVDS_25 outputs, and RSDS_25 outputs. As an example, LVDS_25 outputs, RSDS_25 outputs, and any other differential inputs while using on-chip differential termination are a valid combination. A combination not allowed is a single bank with LVDS_25 outputs, RSDS_25 outputs, and MINI_LVDS_25 outputs.

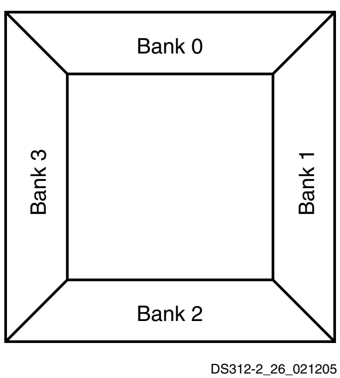


Figure 13: **Spartan-3E I/O Banks (top view)**

I/O Banking Rules

When assigning I/Os to banks, these V_{CCO} rules must be followed:

1. All V_{CCO} pins on the FPGA must be connected even if a bank is unused.
2. All V_{CCO} lines associated within a bank must be set to the same voltage level.
3. The V_{CCO} levels used by all standards assigned to the I/Os of any given bank must agree. The Xilinx development software checks for this. Table 6 and Table 7 describe how different standards use the V_{CCO} supply.
4. If a bank does not have any V_{CCO} requirements, connect V_{CCO} to an available voltage, such as 2.5V or 3.3V. Some configuration modes might place additional V_{CCO} requirements. Refer to Configuration for more information.

If any of the standards assigned to the Inputs of the bank use V_{REF}, then the following additional rules must be observed:

1. All V_{REF} pins must be connected within a bank.
2. All V_{REF} lines associated with the bank must be set to the same voltage level.
3. The V_{REF} levels used by all standards assigned to the Inputs of the bank must agree. The Xilinx development software checks for this. Table 6 describes how different standards use the V_{REF} supply.

If V_{REF} is not required to bias the input switching thresholds, all associated V_{REF} pins within the bank can be used as user I/Os or input pins.

Package Footprint Compatibility

Sometimes, applications outgrow the logic capacity of a specific Spartan-3E FPGA. Fortunately, the Spartan-3E family is designed so that multiple part types are available in pin-compatible package footprints, as described in Module 4, Pinout Descriptions. In some cases, there are subtle differences between devices available in the same footprint. These differences are outlined for each package, such as pins that are unconnected on one device but connected on another in the same package or pins that are dedicated inputs on one package but full I/O on another. When designing the printed circuit board (PCB), plan for potential future upgrades and package migration.

The Spartan-3E family is not pin-compatible with any previous Xilinx FPGA family.

Dedicated Inputs

Dedicated Inputs are IOBs used only as inputs. Pin names designate a Dedicated Input if the name starts with *IP*, for example, IP or IP_Lxxx_x. Dedicated inputs retain the full functionality of the IOB for input functions with a single exception for differential inputs (IP_Lxxx_x). For the differential Dedicated Inputs, the on-chip differential termination is not available. To replace the on-chip differential termination, choose a differential pair that supports outputs (IO_Lxxx_x) or use an external 100Ω termination resistor on the board.

ESD Protection

Clamp diodes protect all device pads against damage from Electro-Static Discharge (ESD) as well as excessive voltage transients. Each I/O has two clamp diodes: one diode extends P-to-N from the pad to V_{CCO} and a second diode extends N-to-P from the pad to GND. During operation, these diodes are normally biased in the off state. These clamp diodes are always connected to the pad, regardless of the signal standard selected. The presence of diodes limits the ability of Spartan-3E I/Os to tolerate high signal voltages. The V_{IN} absolute maximum rating in Table 73 of Module 3, DC and Switching Characteristics specifies the voltage range that I/Os can tolerate.

Carry and Arithmetic Logic

For additional information, refer to the “Using Carry and Arithmetic Logic” chapter in UG331.

The carry chain, together with various dedicated arithmetic logic gates, support fast and efficient implementations of math operations. The carry logic is automatically used for most arithmetic functions in a design. The gates and multiplexers of the carry and arithmetic logic can also be used for general-purpose logic, including simple wide Boolean functions.

The carry chain enters the slice as CIN and exits as COUT, controlled by several multiplexers. The carry chain connects directly from one CLB to the CLB above. The carry chain can be initialized at any point from the BX (or BY) inputs.

The dedicated arithmetic logic includes the exclusive-OR gates XORF and XORG (upper and lower portions of the slice, respectively) as well as the AND gates GAND and FAND (upper and lower portions, respectively). These gates work in conjunction with the LUTs to implement efficient arithmetic functions, including counters and multipliers, typically at two bits per slice. See Figure 22 and Table 14.

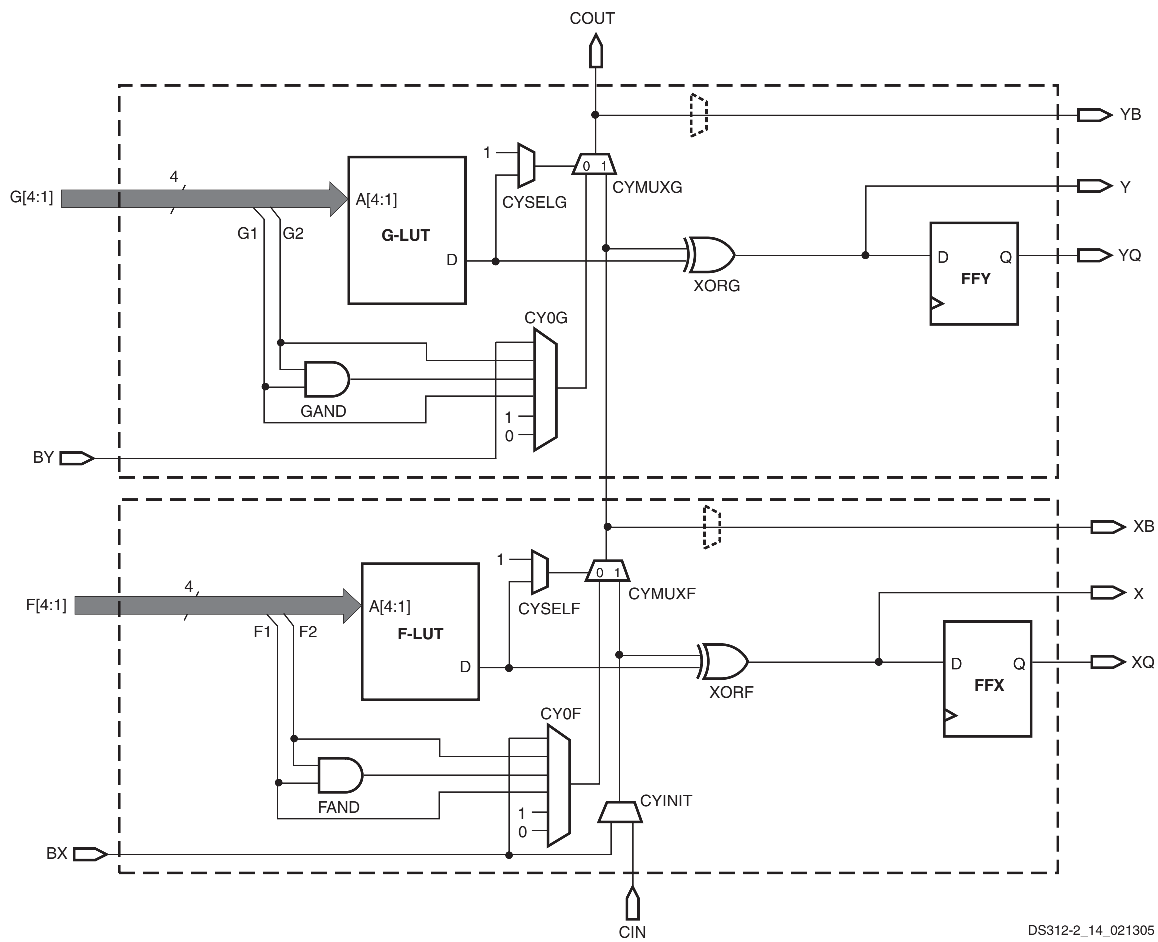


Figure 22: **Carry Logic**

Table 14: **Carry Logic Functions**

Function	Description
CYINIT	Initializes carry chain for a slice. Fixed selection of: · CIN carry input from the slice below · BX input
CY0F	Carry generation for bottom half of slice. Fixed selection of: · F1 or F2 inputs to the LUT (both equal 1 when a carry is to be generated) · FAND gate for multiplication · BX input for carry initialization · Fixed 1 or 0 input for use as a simple Boolean function

Table 14: **Carry Logic Functions *(Cont'd)***

Function	Description
CY0G	Carry generation for top half of slice. Fixed selection of: · G1 or G2 inputs to the LUT (both equal 1 when a carry is to be generated) · GAND gate for multiplication · BY input for carry initialization · Fixed 1 or 0 input for use as a simple Boolean function
CYMUXF	Carry generation or propagation mux for bottom half of slice. Dynamic selection via CYSELF of: · CYINIT carry propagation (CYSELF = 1) · CY0F carry generation (CYSELF = 0)
CYMUXG	Carry generation or propagation mux for top half of slice. Dynamic selection via CYSELF of: · CYMUXF carry propagation (CYSELG = 1) · CY0G carry generation (CYSELG = 0)
CYSELF	Carry generation or propagation select for bottom half of slice. Fixed selection of: · F-LUT output (typically XOR result) · Fixed 1 to always propagate
CYSELG	Carry generation or propagation select for top half of slice. Fixed selection of: · G-LUT output (typically XOR result) · Fixed 1 to always propagate
XORF	Sum generation for bottom half of slice. Inputs from: · F-LUT · CYINIT carry signal from previous stage Result is sent to either the combinatorial or registered output for the top of the slice.
XORG	Sum generation for top half of slice. Inputs from: · G-LUT · CYMUXF carry signal from previous stage Result is sent to either the combinatorial or registered output for the top of the slice.
FAND	Multiplier partial product for bottom half of slice. Inputs: · F-LUT F1 input · F-LUT F2 input Result is sent through CY0F to become the carry generate signal into CYMUXF
GAND	Multiplier partial product for top half of slice. Inputs: · G-LUT G1 input · G-LUT G2 input Result is sent through CY0G to become the carry generate signal into CYMUXG

The basic usage of the carry logic is to generate a half-sum in the LUT via an XOR function, which generates or propagates a carry out COUT via the carry mux CYMUXF (or CYMUXG), and then complete the sum with the dedicated XORF (or XORG) gate and the carry input CIN. This structure allows two bits of an arithmetic function in each slice. The CYMUXF (or CYMUXG) can be instantiated using the MUXCY element, and the XORF (or XORG) can be instantiated using the XORCY element.

The FAND (or GAND) gate is used for partial product multiplication and can be instantiated using the MULT_AND component. Partial products are generated by two-input AND gates and then added. The carry logic is efficient for the adder, but one of the inputs must be outside the LUT as shown in Figure 23.

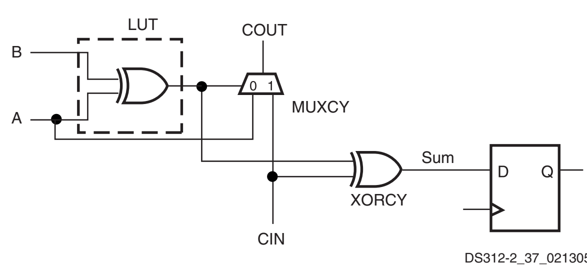


Figure 23: **Using the MUXCY and XORCY in the Carry Logic**

The FAND (or GAND) gate is used to duplicate one of the partial products, while the LUT generates both partial products and the XOR function, as shown in Figure 24.

Initialization

The CLB storage elements are initialized at power-up, during configuration, by the global GSR signal, and by the individual SR or REV inputs to the CLB. The storage elements can also be re-initialized using the GSR input on the STARTUP_SPARTAN3E primitive. See Global Controls (STARTUP_SPARTAN3E).

Table 17: **Slice Storage Element Initialization**

Signal	Description
SR	Set/Reset input. Forces the storage element into the state specified by the attribute SRHIGH or SRLOW. SRHIGH forces a logic 1 when SR is asserted. SRLOW forces a logic 0. For each slice, set and reset can be set to be synchronous or asynchronous.
REV	Reverse of Set/Reset input. A second input (BY) forces the storage element into the opposite state. The reset condition is predominant over the set condition if both are active. Same synchronous/asynchronous setting as for SR.
GSR	Global Set/Reset. GSR defaults to active High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_SPARTAN3E element. The initial state after configuration or GSR is defined by a separate INIT0 and INIT1 attribute. By default, setting the SRLOW attribute sets INIT0, and setting the SRHIGH attribute sets INIT1.

Distributed RAM

For additional information, refer to the “Using Look-Up Tables as Distributed RAM” chapter in UG331.

The LUTs in the SLICEM can be programmed as distributed RAM. This type of memory affords moderate amounts of data buffering anywhere along a data path. One SLICEM LUT stores 16 bits (RAM16). The four LUT inputs F[4:1] or G[4:1] become the address lines labeled A[4:1] in the device model and A[3:0] in the design components, providing a 16x1 configuration in one LUT. Multiple SLICEM LUTs can be combined in various ways to store larger amounts of data, including 16x4, 32x2, or 64x1 configurations in one CLB. The fifth and sixth address lines required for the 32-deep and 64-deep configurations, respectively, are implemented using the BX and BY inputs, which connect to the write enable logic for writing and the F5MUX and F6MUX for reading.

Writing to distributed RAM is always synchronous to the SLICEM clock (WCLK for distributed RAM) and enabled by the SLICEM SR input which functions as the active-High Write Enable (WE). The read operation is asynchronous, and, therefore, during a write, the output initially reflects the old data at the address being written.

The distributed RAM outputs can be captured using the flip-flops within the SLICEM element. The WE write-enable control for the RAM and the CE clock-enable control for the flip-flop are independent, but the WCLK and CLK clock inputs are shared. Because the RAM read operation is asynchronous, the output data always reflects the currently addressed RAM location.

A dual-port option combines two LUTs so that memory access is possible from two independent data lines. The same data is written to both 16x1 memories but they have independent read address lines and outputs. The dual-port function is implemented by cascading the G-LUT address lines, which are used for both read and write, to the F-LUT write address lines (WF[4:1] in Figure 15), and by cascading the G-LUT data input D1 through the DIF_MUX in Figure 15 and to the D1 input on the F-LUT. One CLB provides a 16x1 dual-port memory as shown in Figure 26.

Any write operation on the D input and any read operation on the SPO output can occur simultaneously with and independently from a read operation on the second read-only port, DPO.

Multiplier/Block RAM Interaction

Each multiplier is located adjacent to an 18 Kbit block RAM and shares some interconnect resources. Configuring an 18 Kbit block RAM for 36-bit wide data (512 x 36 mode) prevents use of the associated dedicated multiplier.

The upper 16 bits of the 'A' multiplicand input are shared with the upper 16 bits of the block RAM's Port A Data input. Similarly, the upper 16 bits of the 'B' multiplicand input are shared with Port B's data input. See also Figure 48, page 62.

Table 27 defines each port of the MULT18X18SIO primitive.

Table 27: **MULT18X18SIO Embedded Multiplier Primitives Description**

Signal Name	Direction	Function
A[17:0]	Input	The primary 18-bit two's complement value for multiplication. The block multiplies by this value asynchronously if the optional AREG and PREG registers are omitted. When AREG and/or PREG are used, the value provided on this port is qualified by the rising edge of CLK, subject to the appropriate register controls.
B[17:0]	Input	The second 18-bit two's complement value for multiplication if the B_INPUT attribute is set to DIRECT. The block multiplies by this value asynchronously if the optional BREG and PREG registers are omitted. When BREG and/or PREG are used, the value provided on this port is qualified by the rising edge of CLK, subject to the appropriate register controls.
BCIN[17:0]	Input	The second 18-bit two's complement value for multiplication if the B_INPUT attribute is set to CASCADE. The block multiplies by this value asynchronously if the optional BREG and PREG registers are omitted. When BREG and/or PREG are used, the value provided on this port is qualified by the rising edge of CLK, subject to the appropriate register controls.
P[35:0]	Output	The 36-bit two's complement product resulting from the multiplication of the two input values applied to the multiplier. If the optional AREG, BREG and PREG registers are omitted, the output operates asynchronously. Use of PREG causes this output to respond to the rising edge of CLK with the value qualified by CEP and RSTP. If PREG is omitted, but AREG and BREG are used, this output responds to the rising edge of CLK with the value qualified by CEA, RSTA, CEB, and RSTB. If PREG is omitted and only one of AREG or BREG is used, this output responds to both asynchronous and synchronous events.
BCOUT[17:0]	Output	The value being applied to the second input of the multiplier. When the optional BREG register is omitted, this output responds asynchronously in response to changes at the B[17:0] or BCIN[17:0] ports according to the setting of the B_INPUT attribute. If BREG is used, this output responds to the rising edge of CLK with the value qualified by CEB and RSTB.
CEA	Input	Clock enable qualifier for the optional AREG register. The value provided on the A[17:0] port is captured by AREG in response to a rising edge of CLK when this signal is High, provided that RSTA is Low.
RSTA	Input	Synchronous reset for the optional AREG register. AREG content is forced to the value zero in response to a rising edge of CLK when this signal is High.
CEB	Input	Clock enable qualifier for the optional BREG register. The value provided on the B[17:0] or BCIN[17:0] port is captured by BREG in response to a rising edge of CLK when this signal is High, provided that RSTB is Low.
RSTB	Input	Synchronous reset for the optional BREG register. BREG content is forced to the value zero in response to a rising edge of CLK when this signal is High.
CEP	Input	Clock enable qualifier for the optional PREG register. The value provided on the output of the multiplier port is captured by PREG in response to a rising edge of CLK when this signal is High, provided that RSTP is Low.
RSTP	Input	Synchronous reset for the optional PREG register. PREG content is forced to the value zero in response to a rising edge of CLK when this signal is High.

Notes:

1. The control signals CLK, CEA, RSTA, CEB, RSTB, CEP, and RSTP have the option of inverted polarity.

Digital Clock Managers (DCMs)

For additional information, refer to the “Using Digital Clock Managers (DCMs)” chapter in UG331.

Differences from the Spartan-3 Architecture

- Spartan-3E FPGAs have two, four, or eight DCMs, depending on device size.
- The variable phase shifting feature functions differently on Spartan-3E FPGAs than from Spartan-3 FPGAs.
- The Spartan-3E DLLs support lower input frequencies, down to 5 MHz. Spartan-3 DLLs support down to 18 MHz.

Overview

Spartan-3E FPGA Digital Clock Managers (DCMs) provide flexible, complete control over clock frequency, phase shift and skew. To accomplish this, the DCM employs a Delay-Locked Loop (DLL), a fully digital control system that uses feedback to maintain clock signal characteristics with a high degree of precision despite normal variations in operating temperature and voltage. This section provides a fundamental description of the DCM.

The XC3S100E FPGA has two DCMs, one at the top and one at the bottom of the device. The XC3S250E and XC3S500E FPGAs each include four DCMs, two at the top and two at the bottom. The XC3S1200E and XC3S1600E FPGAs contain eight DCMs with two on each edge (see also Figure 45). The DCM in Spartan-3E FPGAs is surrounded by CLBs within the logic array and is no longer located at the top and bottom of a column of block RAM as in the Spartan-3 architecture. The Digital Clock Manager is instantiated within a design using a “DCM” primitive.

The DCM supports three major functions:

- **Clock-skew Elimination:** Clock skew within a system occurs due to the different arrival times of a clock signal at different points on the die, typically caused by the clock signal distribution network. Clock skew increases setup and hold time requirements and increases clock-to-out times, all of which are undesirable in high frequency applications. The DCM eliminates clock skew by phase-aligning the output clock signal that it generates with the incoming clock signal. This mechanism effectively cancels out the clock distribution delays.
- **Frequency Synthesis:** The DCM can generate a wide range of different output clock frequencies derived from the incoming clock signal. This is accomplished by either multiplying and/or dividing the frequency of the input clock signal by any of several different factors.
- **Phase Shifting:** The DCM provides the ability to shift the phase of all its output clock signals with respect to the input clock signal.

Although a single design primitive, the DCM consists of four interrelated functional units: the Delay-Locked Loop (DLL), the Digital Frequency Synthesizer (DFS), the Phase Shifter (PS), and the Status Logic. Each component has its associated signals, as shown in Figure 40.

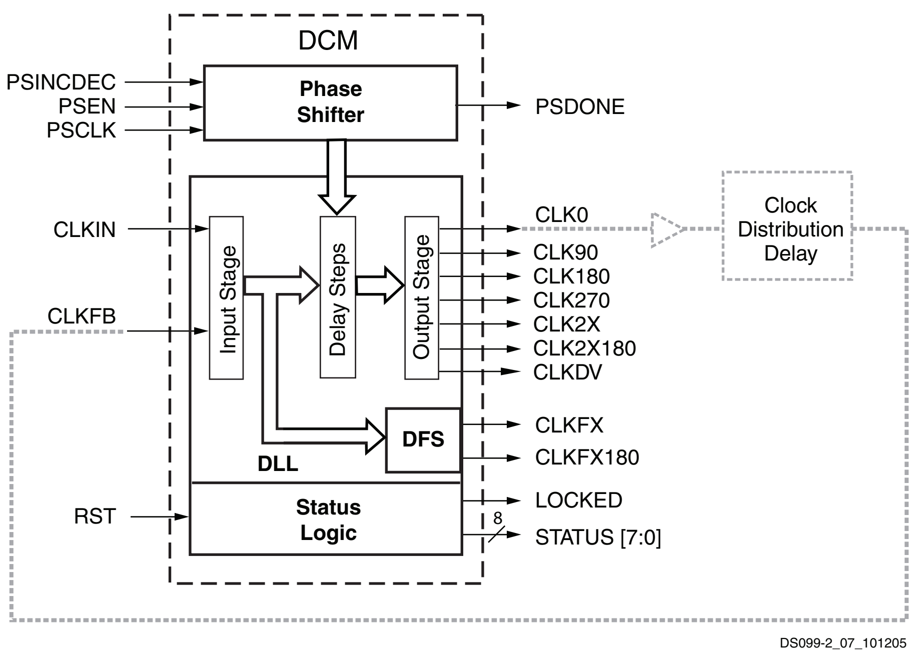


Figure 40: **DCM Functional Blocks and Associated Signals**

Clocking Infrastructure

For additional information, refer to the “Using Global Clock Resources” chapter in UG331.

The Spartan-3E clocking infrastructure, shown in Figure 45, provides a series of low-capacitance, low-skew interconnect lines well-suited to carrying high-frequency signals throughout the FPGA. The infrastructure also includes the clock inputs and BUFGMUX clock buffers/multiplexers. The Xilinx Place-and-Route (PAR) software automatically routes high-fanout clock signals using these resources.

Clock Inputs

Clock pins accept external clock signals and connect directly to DCMs and BUFGMUX elements. Each Spartan-3E FPGA has:

- 16 Global Clock inputs (GCLK0 through GCLK15) located along the top and bottom edges of the FPGA
- 8 Right-Half Clock inputs (RHCLK0 through RHCLK7) located along the right edge
- 8 Left-Half Clock inputs (LHCLK0 through LHCLK7) located along the left edge

Clock inputs optionally connect directly to DCMs using dedicated connections. Table 30, Table 31, and Table 32 show the clock inputs that best feed a specific DCM within a given Spartan-3E part number. Different Spartan-3E FPGA densities have different numbers of DCMs. The XC3S1200E and XC3S1600E are the only two densities with the left- and right-edge DCMs.

Each clock input is also optionally a user-I/O pin and connects to internal interconnect. Some clock pad pins are input-only pins as indicated in Module 4, Pinout Descriptions.

Design Note

Avoid using global clock input GCLK1 as it is always shared with the M2 mode select pin. Global clock inputs GCLK0, GCLK2, GCLK3, GCLK12, GCLK13, GCLK14, and GCLK15 have shared functionality in some configuration modes.

Clock Buffers/Multiplexers

Clock Buffers/Multiplexers either drive clock input signals directly onto a clock line (BUFG) or optionally provide a multiplexer to switch between two unrelated, possibly asynchronous clock signals (BUFGMUX).

Each BUFGMUX element, shown in Figure 46, is a 2-to-1 multiplexer. The select line, S, chooses which of the two inputs, I0 or I1, drives the BUFGMUX’s output signal, O, as described in Table 40. The switching from one clock to the other is glitch-less, and done in such a way that the output High and Low times are never shorter than the shortest High or Low time of either input clock. The two clock inputs can be asynchronous with regard to each other, and the S input can change at any time, except for a short setup time prior to the rising edge of the presently selected clock (I0 or I1). This setup time is specified as TGSI in Table 101, page 136. Violating this setup time requirement possibly results in an undefined runt pulse output.

Table 40: **BUFGMUX Select Mechanism**

S Input	O Output
0	I0 Input
1	I1 Input

The BUFG clock buffer primitive drives a single clock signal onto the clock network and is essentially the same element as a BUFGMUX, just without the clock select mechanism. Similarly, the BUFGCE primitive creates an enabled clock buffer using the BUFGMUX select mechanism.

The I0 and I1 inputs to an BUFGMUX element originate from clock input pins, DCMs, or Double-Line interconnect, as shown in Figure 46. As shown in Figure 45, there are 24 BUFGMUX elements distributed around the four edges of the device. Clock signals from the four BUFGMUX elements at the top edge and the four at the bottom edge are truly global and connect to all clocking quadrants. The eight left-edge BUFGMUX elements only connect to the two clock quadrants in the left half of the device. Similarly, the eight right-edge BUFGMUX elements only connect to the right half of the device.

BUFGMUX elements are organized in pairs and share I0 and I1 connections with adjacent BUFGMUX elements from a common clock switch matrix as shown in Figure 46. For example, the input on I0 of one BUFGMUX is also a shared input to I1 of the adjacent BUFGMUX.

The clock switch matrix for the left- and right-edge BUFGMUX elements receive signals from any of the three following sources: an LHCLK or RHCLK pin as appropriate, a Double-Line interconnect, or a DCM in the XC3S1200E and XC3S1600E devices.

W Table 54 shows the connections between the SPI Flash PROM and the FPGA's SPI configuration interface. Each SPI Flash PROM vendor uses slightly different signal naming. The SPI Flash PROM's write protect and hold controls are not used by the FPGA during configuration. However, the $\overline{\text{HOLD}}$ pin must be High during the configuration process. The PROM's write protect input must be High in order to write or program the Flash memory.

Table 54: **Example SPI Flash PROM Connections and Pin Naming**

SPI Flash Pin	FPGA Connection	STMicro	NexFlash	Silicon Storage Technology	Atmel DataFlash
DATA_IN	MOSI	D	DI	SI	SI
DATA_OUT	DIN	Q	DO	SO	SO
$\overline{\text{SELECT}}$	CSO_B	$\overline{\text{S}}$	$\overline{\text{CS}}$	CE#	$\overline{\text{CS}}$
CLOCK	CCLK	C	CLK	SCK	SCK
$\overline{\text{WR\_PROTECT}}$ W	Not required for FPGA configuration. Must be High to program SPI Flash. Optional connection to FPGA user I/O after configuration.	$\overline{\text{W}}$	$\overline{\text{WP}}$	WP#	$\overline{\text{WP}}$
$\overline{\text{HOLD}}$ (see Figure 53)	Not required for FPGA configuration but must be High during configuration. Optional connection to FPGA user I/O after configuration. Not applicable to Atmel DataFlash.	$\overline{\text{HOLD}}$	$\overline{\text{HOLD}}$	HOLD#	N/A
$\overline{\text{RESET}}$ (see Figure 54)	Only applicable to Atmel DataFlash. Not required for FPGA configuration but must be High during configuration. Optional connection to FPGA user I/O after configuration. Do not connect to FPGA's PROG_B as this will prevent direct programming of the DataFlash.	N/A	N/A	N/A	$\overline{\text{RESET}}$
RDY/$\overline{\text{BUSY}}$ (see Figure 54)	Only applicable to Atmel DataFlash and only available on certain packages. Not required for FPGA configuration. Output from DataFlash PROM. Optional connection to FPGA user I/O after configuration.	N/A	N/A	N/A	RDY/$\overline{\text{BUSY}}$

The mode select pins, M[2:0], and the variant select pins, VS[2:0] are sampled when the FPGA's INIT_B output goes High and must be at defined logic levels during this time. After configuration, when the FPGA's DONE output goes High, these pins are all available as full-featured user-I/O pins.

P Similarly, the FPGA's HSWAP pin must be Low to enable pull-up resistors on all user-I/O pins or High to disable the pull-up resistors. The HSWAP control must remain at a constant logic level throughout FPGA configuration. After configuration, when the FPGA's DONE output goes High, the HSWAP pin is available as full-featured user-I/O pin and is powered by the VCCO_0 supply.

In a single-FPGA application, the FPGA's DOUT pin is not used but is actively driving during the configuration process.

Table 55: **Serial Peripheral Interface (SPI) Connections**

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
HSWAP P	Input	**User I/O Pull-Up Control**. When Low during configuration, enables pull-up resistors in all I/O pins to respective I/O bank V_{CCO} input. 0: Pull-ups during configuration 1: No pull-ups	Drive at valid logic level throughout configuration.	User I/O
M[2:0]	Input	**Mode Select**. Selects the FPGA configuration mode. See Design Considerations for the HSWAP, M[2:0], and VS[2:0] Pins.	M2 = 0, M1 = 0, M0 = 1. Sampled when INIT_B goes High.	User I/O

support byte-wide data. However, after configuration, the FPGA supports either x8 or x16 modes. In x16 mode, up to eight additional user I/O pins are required for the upper data bits, D[15:8].

Connecting a Spartan-3E FPGA to a x8/x16 Flash PROM is simple, but does require a precaution. Various Flash PROM vendors use slightly different interfaces to support both x8 and x16 modes. Some vendors (Intel, Micron, some STMicroelectronics devices) use a straightforward interface with pin naming that matches the FPGA connections. However, the PROM's A0 pin is wasted in x16 applications and a separate FPGA user-I/O pin is required for the D15 data line. Fortunately, the FPGA A0 pin is still available as a user I/O after configuration, even though it connects to the Flash PROM.

Other vendors (AMD, Atmel, Silicon Storage Technology, some STMicroelectronics devices) use a pin-efficient interface but change the function of one pin, called IO15/A-1, depending if the PROM is in x8 or x16 mode. In x8 mode, BYTE# = 0, this pin is the least-significant address line. The A0 address line selects the halfword location. The A-1 address line selects the byte location. When in x16 mode, BYTE# = 1, the IO15/A-1 pin becomes the most-significant data bit, D15 because byte addressing is not required in this mode. Check to see if the Flash PROM has a pin named "IO15/A-1" or "DQ15/A-1". If so, be careful to connect x8/x16 Flash PROMs correctly, as shown in Table 63. Also, remember that the D[14:8] data connections require FPGA user I/O pins but that the D15 data is already connected for the FPGA's A0 pin.

Table 63: **FPGA Connections to Flash PROM with IO15/A-1 Pin**

FPGA Pin	Connection to Flash PROM with IO15/A-1 Pin	x8 Flash PROM Interface After FPGA Configuration	x16 Flash PROM Interface After FPGA Configuration
LDC2	BYTE#	Drive LDC2 Low or leave unconnected and tie PROM BYTE# input to GND	Drive LCD2 High
LDC1	OE#	Active-Low Flash PROM output-enable control	Active-Low Flash PROM output-enable control
LDC0	CS#	Active-Low Flash PROM chip-select control	Active-Low Flash PROM chip-select control
HDC	WE#	Flash PROM write-enable control	Flash PROM write-enable control
A[23:1]	A[n:0]	A[n:0]	A[n:0]
A0	IO15/A-1	IO15/A-1 is the least-significant address input	IO15/A-1 is the most-significant data line, IO15
D[7:0]	IO[7:0]	IO[7:0]	IO[7:0]
User I/O	Upper data lines IO[14:8] not required unless used as x16 Flash interface after configuration	Upper data lines IO[14:8] not required	IO[14:8]

Some x8/x16 Flash PROMs have a long setup time requirement on the BYTE# signal. For the FPGA to configure correctly, the PROM must be in x8 mode with BYTE# = 0 at power-on or when the FPGA's PROG_B pin is pulsed Low. If required, extend the BYTE# setup time for a 3.3V PROM using an external 680 Ω pull-down resistor on the FPGA's LDC2 pin or by delaying assertion of the CSI_B select input to the FPGA.

Daisy-Chaining

If the application requires multiple FPGAs with different configurations, then configure the FPGAs using a daisy chain, as shown in Figure 59. Use BPI mode (M[2:0] = <0:1:0> or <0:1:1>) for the FPGA connected to the parallel NOR Flash PROM and Slave Parallel mode (M[2:0] = <1:1:0>) for all downstream FPGAs in the daisy-chain. If there are more than two FPGAs in the chain, then last FPGA in the chain can be from any Xilinx FPGA family. However, all intermediate FPGAs located in the chain between the first and last FPGAs must from either the Spartan-3E or Virtex®-5 FPGA families.

After the master FPGA—the FPGA on the left in the diagram—finishes loading its configuration data from the parallel Flash PROM, the master device continues generating addresses to the Flash PROM and asserts its CSO_B output Low, enabling the next FPGA in the daisy-chain. The next FPGA then receives parallel configuration data from the Flash PROM. The master FPGA's CCLK output synchronizes data capture.

If HSWAP = 1, an external 4.7kΩ pull-up resistor must be added on the CSO_B pin. If HSWAP = 0, no external pull-up is necessary.

Design Note

BPI mode daisy chain software support is available starting in ISE 8.2i.

http://www.xilinx.com/support/answers/23061.htm

Table 65: **Slave Parallel Mode Connections *(Cont'd)***

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
INIT_B	Open-drain bidirectional I/O	**Initialization Indicator**. Active Low. Goes Low at the start of configuration during the Initialization memory clearing process. Released at the end of memory clearing, when mode select pins are sampled. In daisy-chain applications, this signal requires an external 4.7 kΩ pull-up resistor to VCCO_2.	Active during configuration. If CRC error detected during configuration, FPGA drives INIT_B Low.	User I/O. If unused in the application, drive INIT_B High.
DONE	Open-drain bidirectional I/O	**FPGA Configuration Done**. Low during configuration. Goes High when FPGA successfully completes configuration. Requires external 330 Ω pull-up resistor to 2.5V.	Low indicates that the FPGA is not yet configured.	Pulled High via external pull-up. When High, indicates that the FPGA successfully configured.
PROG_B	Input	**Program FPGA**. Active Low. When asserted Low for 500 ns or longer, forces the FPGA to restart its configuration process by clearing configuration memory and resetting the DONE and INIT_B pins once PROG_B returns High. Recommend external 4.7 kΩ pull-up resistor to 2.5V. Internal pull-up value may be weaker (see Table 78). If driving externally with a 3.3V output, use an open-drain or open-collector driver or use a current limiting series resistor.	Must be High to allow configuration to start.	Drive PROG_B Low and release to reprogram FPGA.

Voltage Compatibility

(V) Most Slave Parallel interface signals are within the FPGA's I/O Bank 2, supplied by the VCCO_2 supply input. The VCCO_2 voltage can be 1.8V, 2.5V, or 3.3V to match the requirements of the external host, ideally 2.5V. Using 1.8V or 3.3V requires additional design considerations as the DONE and PROG_B pins are powered by the FPGA's 2.5V V_{CCAUX} supply. See XAPP453: *The 3.3V Configuration of Spartan-3 FPGAs* for additional information.

Daisy-Chaining

If the application requires multiple FPGAs with different configurations, then configure the FPGAs using a daisy chain. Use Slave Parallel mode (M[2:0] = <1:1:0>) for all FPGAs in the daisy-chain. The schematic in Figure 62 is optimized for FPGA downloading and does not support the SelectMAP read interface. The FPGA's RDWR_B pin must be Low during configuration.

After the lead FPGA is filled with its configuration data, the lead FPGA enables the next FPGA in the daisy-chain by asserting is chip-select output, CSO_B.

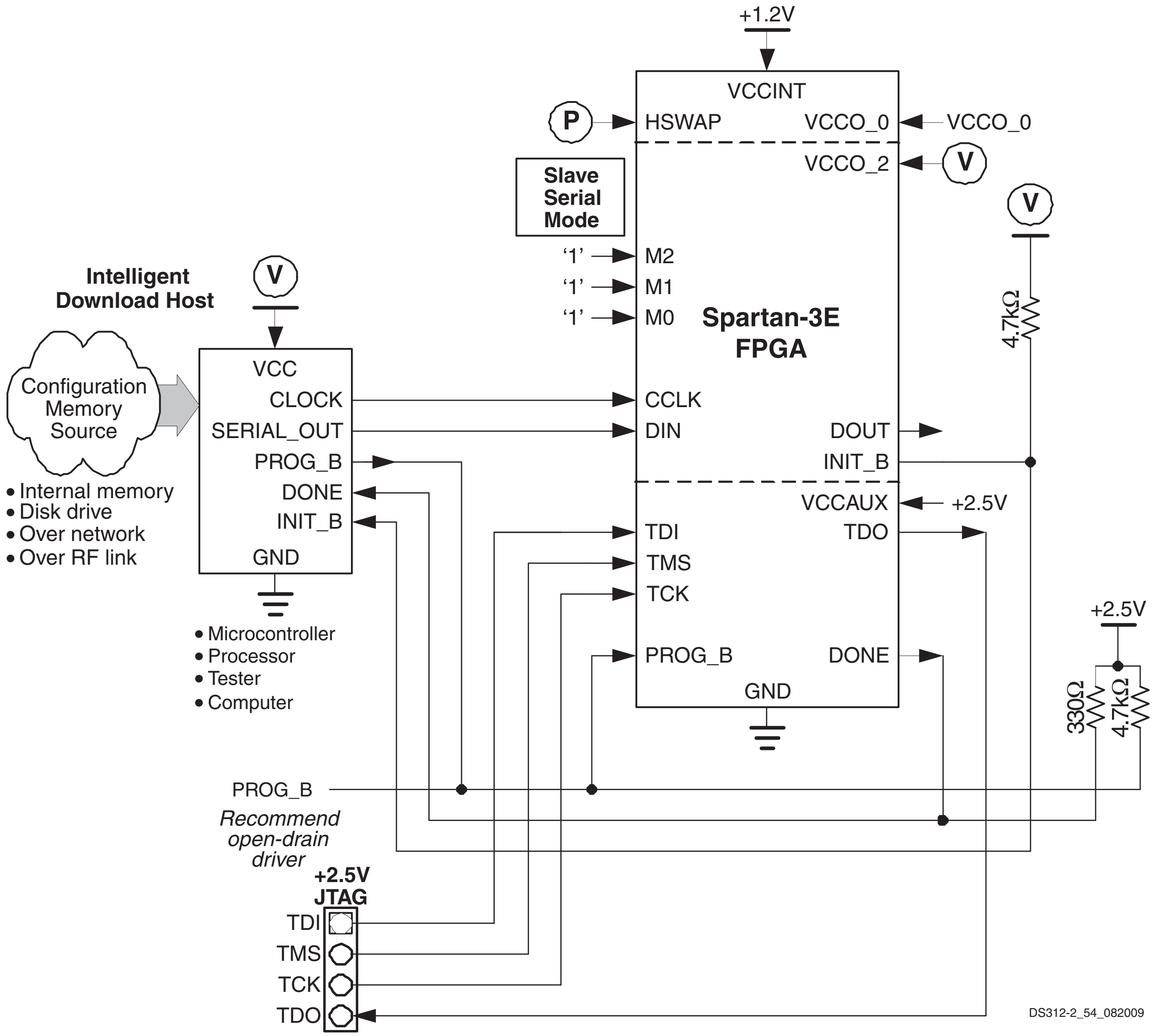


Figure 63: **Slave Serial Configuration**

The mode select pins, M[2:0], are sampled when the FPGA's INIT_B output goes High and must be at defined logic levels during this time. After configuration, when the FPGA's DONE output goes High, the mode pins are available as full-featured user-I/O pins.

(P) Similarly, the FPGA's HSWAP pin must be Low to enable pull-up resistors on all user-I/O pins or High to disable the pull-up resistors. The HSWAP control must remain at a constant logic level throughout FPGA configuration. After configuration, when the FPGA's DONE output goes High, the HSWAP pin is available as full-featured user-I/O pin and is powered by the VCCO_0 supply.

Voltage Compatibility

(V) Most Slave Serial interface signals are within the FPGA's I/O Bank 2, supplied by the VCCO_2 supply input. The VCCO_2 voltage can be 3.3V, 2.5V, or 1.8V to match the requirements of the external host, ideally 2.5V. Using 3.3V or 1.8V requires additional design considerations as the DONE and PROG_B pins are powered by the FPGA's 2.5V V_{CCAUX} supply. See XAPP453: *The 3.3V Configuration of Spartan-3 FPGAs* for additional information.

Daisy-Chaining

If the application requires multiple FPGAs with different configurations, then configure the FPGAs using a daisy chain, as shown in Figure 64. Use Slave Serial mode (M[2:0] = <1:1:1>) for all FPGAs in the daisy-chain. After the lead FPGA is filled with its configuration data, the lead

Table 95: **Test Methods for Timing Measurement at I/Os *(Cont'd)***

Signal Standard (IOSTANDARD)	Inputs			Outputs		Inputs and Outputs
	V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
DIFF_HSTL_I_18	-	$V_{REF} - 0.5$	$V_{REF} + 0.5$	50	0.9	V_{ICM}
DIFF_HSTL_III_18	-	$V_{REF} - 0.5$	$V_{REF} + 0.5$	50	1.8	V_{ICM}
DIFF_SSTL18_I	-	$V_{REF} - 0.5$	$V_{REF} + 0.5$	50	0.9	V_{ICM}
DIFF_SSTL2_I	-	$V_{REF} - 0.5$	$V_{REF} + 0.5$	50	1.25	V_{ICM}

Notes:

1. Descriptions of the relevant symbols are as follows:
   V_{REF} – The reference voltage for setting the input switching threshold
   V_{ICM} – The common mode input voltage
   V_M – Voltage of measurement point on signal transition
   V_L – Low-level test voltage at Input pin
   V_H – High-level test voltage at Input pin
   R_T – Effective termination resistance, which takes on a value of 1MΩ when no parallel termination is required
   V_T – Termination voltage
2. The load capacitance (C_L) at the Output pin is 0 pF for all signal standards.
3. According to the PCI specification.

The capacitive load (C_L) is connected between the output and GND. *The Output timing for all standards, as published in the speed files and the data sheet, is always based on a C_L value of zero.* High-impedance probes (less than 1 pF) are used for all measurements. Any delay that the test fixture might contribute to test measurements is subtracted from those measurements to produce the final timing numbers as published in the speed files and data sheet.

Using IBIS Models to Simulate Load Conditions in Application

IBIS models permit the most accurate prediction of timing delays for a given application. The parameters found in the IBIS model (V_{REF}, R_{REF}, and V_{MEAS}) correspond directly with the parameters used in Table 95 (V_T, R_T, and V_M). Do not confuse V_{REF} (the termination voltage) from the IBIS model with V_{REF} (the input-switching threshold) from the table. A fourth parameter, C_{REF}, is always zero. The four parameters describe all relevant output test conditions. IBIS models are found in the Xilinx development software as well as at the following link:

http://www.xilinx.com/support/download/index.htm

Delays for a given application are simulated according to its specific load conditions as follows:

1. Simulate the desired signal standard with the output driver connected to the test setup shown in Figure 72. Use parameter values V_T, R_T, and V_M from Table 95. C_{REF} is zero.
2. Record the time to V_M.
3. Simulate the same signal standard with the output driver connected to the PCB trace with load. Use the appropriate IBIS model (including V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} values) or capacitive value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. Add (or subtract) the increase (or decrease) in delay to (or from) the appropriate Output standard adjustment (Table 94) to yield the worst-case delay of the PCB trace.

Phase Shifter (PS)

Table 108: **Recommended Operating Conditions for the PS in Variable Phase Mode**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Operating Frequency Ranges						
PSCLK_FREQ (F_{PSCLK})	Frequency for the PSCLK input	1	167	1	167	MHz
Input Pulse Requirements						
PSCLK_PULSE	PSCLK pulse width as a percentage of the PSCLK period	40%	60%	40%	60%	-

Table 109: **Switching Characteristics for the PS in Variable Phase Mode**

Symbol	Description	Equation		Units
Phase Shifting Range				
MAX_STEPS(2)	Maximum allowed number of DCM_DELAY_STEP steps for a given CLKIN clock period, where T = CLKIN clock period in ns. If using CLKIN_DIVIDE_BY_2 = TRUE, double the effective clock period.(3)	CLKIN < 60 MHz	±[INTEGER(10 • (T_{CLKIN} – 3 ns))]	steps
		CLKIN ≥ 60 MHz	±[INTEGER(15 • (T_{CLKIN} – 3 ns))]	steps
FINE_SHIFT_RANGE_MIN	Minimum guaranteed delay for variable phase shifting	±[MAX_STEPS • DCM_DELAY_STEP_MIN]		ns
FINE_SHIFT_RANGE_MAX	Maximum guaranteed delay for variable phase shifting	±[MAX_STEPS • DCM_DELAY_STEP_MAX]		ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 77 and Table 108.
2. The maximum variable phase shift range, MAX_STEPS, is only valid when the DCM is has no initial fixed phase shifting, i.e., the PHASE_SHIFT attribute is set to 0.
3. The DCM_DELAY_STEP values are provided at the bottom of Table 105.

Miscellaneous DCM Timing

Table 110: **Miscellaneous DCM Timing**

Symbol	Description	Min	Max	Units
DCM_RST_PW_MIN(1)	Minimum duration of a RST pulse width	3	-	CLKIN cycles
DCM_RST_PW_MAX(2)	Maximum duration of a RST pulse width	N/A	N/A	seconds
DCM_CONFIG_LAG_TIME(3)	Maximum duration from V_{CCINT} applied to FPGA configuration successfully completed (DONE pin goes High) and clocks applied to DCM DLL	N/A	N/A	minutes

Notes:

1. This limit only applies to applications that use the DCM DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV). The DCM DFS outputs (CLKFX, CLKFX180) are unaffected.
2. This specification is equivalent to the Virtex-4 DCM_RESET specfication.This specification does not apply for Spartan-3E FPGAs.
3. This specification is equivalent to the Virtex-4 TCONFIG specification. This specification does not apply for Spartan-3E FPGAs.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/01/05	1.0	Initial Xilinx release.
11/23/05	2.0	Added AC timing information and additional DC specifications.
03/22/06	3.0	Upgraded data sheet status to Preliminary. Finalized production timing parameters. All speed grades for all Spartan-3E FPGAs are now Production status using the v1.21 speed files, as shown in Table 84. Expanded description in Note 2, Table 78. Updated pin-to-pin and clock-to-output timing based on final characterization, shown in Table 86. Updated system-synchronous input setup and hold times based on final characterization, shown in Table 87 and Table 88. Updated other I/O timing in Table 90. Provided input and output adjustments for LVPECL_25, DIFF_SSTL and DIFF_HSTL I/O standards that supersede the v1.21 speed file values, in Table 91 and Table 94. Reduced I/O three-state and set/reset delays in Table 93. Added XC3S100E FPGA in CP132 package to Table 96. Increased T_{AS} slice flip-flop timing by 100 ps in Table 98. Updated distributed RAM timing in Table 99 and SRL16 timing in Table 100. Updated global clock timing, removed left/right clock buffer limits in Table 101. Updated block RAM timing in Table 103. Added DCM parameters for remainder of Step 0 device; added improved Step 1 DCM performance to Table 104, Table 105, Table 106, and Table 107. Added minimum INIT_B pulse width specification, T_{INIT}, in Table 111. Increased data hold time for Slave Parallel mode to 1.0 ns (T_{SMCCD}) in Table 117. Improved the DCM performance for the XC3S1200E, Stepping 0 in Table 104, Table 105, Table 106, and Table 107. Corrected links in Table 118 and Table 120. Added MultiBoot timing specifications to Table 122.
04/07/06	3.1	Improved SSO limits for LVDS_25, MINI_LVDS_25, and RSDS_25 I/O standards in the QFP packages (Table 97). Removed potentially confusing Note 2 from Table 78.
05/19/06	3.2	Clarified that 100 mV of hysteresis applies to LVCMOS33 and LVCMOS25 I/O standards (Note 4, Table 80). Other minor edits.
05/30/06	3.2.1	Corrected various typos and incorrect links.
11/09/06	3.4	Improved absolute maximum voltage specifications in Table 73, providing additional overshoot allowance. Widened the recommended voltage range for PCI and PCI-X standards in Table 80. Clarified Note 2, Table 83. Improved various timing specifications for v1.26 speed file. Added Table 85 to summarize the history of speed file releases after which time all devices became Production status. Added absolute minimum values for Table 86, Table 92, and Table 93. Updated pin-to-pin setup and hold timing based on default IFD_DELAY_VALUE settings in Table 87, Table 88, and Table 90. Added Table 89 about source-synchronous input capture sample window. Promoted Module 3 to Production status. Synchronized all modules to v3.4.
03/16/07	3.5	Based on extensive 90 nm production data, improved (reduced) the maximum quiescent current limits for the I_{CCINTQ}, I_{CCAUXQ}, and I_{CCOQ} specifications in Table 79 by an average of 50%.
05/29/07	3.6	Added note to Table 74 and Table 75 regarding HSWAP in step 0 devices. Updated t_{RPW_CLB} in Table 98 to match value in speed file. Improved CLKOUT_FREQ_CLK90 to 200 MHz for Stepping 1 in Table 105.
04/18/08	3.7	Clarified that Stepping 0 was offered only for -4C and removed Stepping 0 -5 specifications. Added reference to XAPP459 in Table 73 and Table 77. Improved recommended max V_{CCO} to 3.465V (3.3V + 5%) in Table 77. Removed minimum input capacitance from Table 78. Updated Recommended Operating Conditions for LVCMOS and PCI I/O standards in Table 80. Removed Absolute Minimums from Table 86, Table 92 and Table 93 and added footnote recommending use of Timing Analyzer for minimum values. Updated T_{PSFD} and T_{PHFD} in Table 87 to match current speed file. Update T_{RPW_IOB} in Table 88 to match current speed file and CLB equivalent spec. Added XC3S500E VQG100 to Table 96. Replaced $T_{MULCKID}$ with T_{MSCKD} for A, B, and P registers in Table 102. Updated CLKOUT_PER_JITT_FX in Table 107. Updated MAX_STEPS equation in Table 109. Updated Figure 77 and Table 120 to correct CCLK active edge. Updated links.

VQ100: 100-lead Very-thin Quad Flat Package

The XC3S100E, XC3S250E, and the XC3S500E devices are available in the 100-lead very-thin quad flat package, VQ100. All devices share a common footprint for this package as shown in Table 131 and Figure 80.

Table 131 lists all the package pins. They are sorted by bank number and then by pin name. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The VQ100 package does not support the Byte-wide Peripheral Interface (BPI) configuration mode. Consequently, the VQ100 footprint has fewer DUAL-type pins than other packages.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx web site at:

http://www.xilinx.com/support/documentation/data_sheets/s3e_pin.zip

Pinout Table

Table 131 shows the pinout for production Spartan-3E FPGAs in the VQ100 package.

Table 131: **VQ100 Package Pinout**

Bank	XC3S100E XC3S250E XC3S500E Pin Name	VQ100 Pin Number	Type
0	IO	P92	I/O
0	IO_L01N_0	P79	I/O
0	IO_L01P_0	P78	I/O
0	IO_L02N_0/GCLK5	P84	GCLK
0	IO_L02P_0/GCLK4	P83	GCLK
0	IO_L03N_0/GCLK7	P86	GCLK
0	IO_L03P_0/GCLK6	P85	GCLK
0	IO_L05N_0/GCLK11	P91	GCLK
0	IO_L05P_0/GCLK10	P90	GCLK
0	IO_L06N_0/VREF_0	P95	VREF
0	IO_L06P_0	P94	I/O
0	IO_L07N_0/HSWAP	P99	DUAL
0	IO_L07P_0	P98	I/O
0	IP_L04N_0/GCLK9	P89	GCLK
0	IP_L04P_0/GCLK8	P88	GCLK
0	VCCO_0	P82	VCCO
0	VCCO_0	P97	VCCO
1	IO_L01N_1	P54	I/O
1	IO_L01P_1	P53	I/O
1	IO_L02N_1	P58	I/O

Table 131: **VQ100 Package Pinout *(Cont'd)***

Bank	XC3S100E XC3S250E XC3S500E Pin Name	VQ100 Pin Number	Type
1	IO_L02P_1	P57	I/O
1	IO_L03N_1/RHCLK1	P61	RHCLK
1	IO_L03P_1/RHCLK0	P60	RHCLK
1	IO_L04N_1/RHCLK3	P63	RHCLK
1	IO_L04P_1/RHCLK2	P62	RHCLK
1	IO_L05N_1/RHCLK5	P66	RHCLK
1	IO_L05P_1/RHCLK4	P65	RHCLK
1	IO_L06N_1/RHCLK7	P68	RHCLK
1	IO_L06P_1/RHCLK6	P67	RHCLK
1	IO_L07N_1	P71	I/O
1	IO_L07P_1	P70	I/O
1	IP/VREF_1	P69	VREF
1	VCCO_1	P55	VCCO
1	VCCO_1	P73	VCCO
2	IO/D5	P34	DUAL
2	IO/M1	P42	DUAL
2	IO_L01N_2/INIT_B	P25	DUAL
2	IO_L01P_2/CSO_B	P24	DUAL
2	IO_L02N_2/MOSI/CSI_B	P27	DUAL
2	IO_L02P_2/DOUT/BUSY	P26	DUAL
2	IO_L03N_2/D6/GCLK13	P33	DUAL/GCLK
2	IO_L03P_2/D7/GCLK12	P32	DUAL/GCLK
2	IO_L04N_2/D3/GCLK15	P36	DUAL/GCLK
2	IO_L04P_2/D4/GCLK14	P35	DUAL/GCLK
2	IO_L06N_2/D1/GCLK3	P41	DUAL/GCLK
2	IO_L06P_2/D2/GCLK2	P40	DUAL/GCLK
2	IO_L07N_2/DIN/D0	P44	DUAL
2	IO_L07P_2/M0	P43	DUAL
2	IO_L08N_2/VS1	P48	DUAL
2	IO_L08P_2/VS2	P47	DUAL
2	IO_L09N_2/CCLK	P50	DUAL
2	IO_L09P_2/VS0	P49	DUAL
2	IP/VREF_2	P30	VREF
2	IP_L05N_2/M2/GCLK1	P39	DUAL/GCLK
2	IP_L05P_2/RDWR_B/ GCLK0	P38	DUAL/GCLK
2	VCCO_2	P31	VCCO
2	VCCO_2	P45	VCCO
3	IO_L01N_3	P3	I/O
3	IO_L01P_3	P2	I/O
3	IO_L02N_3/VREF_3	P5	VREF

Table 133: **CP132 Package Pinout *(Cont'd)***

Bank	XC3S100E Pin Name	XC3S250E XC3S500E Pin Name	CP132 Ball	Type
GND	GND	GND	C10	GND
GND	GND	GND	E3	GND
GND	GND	GND	E14	GND
GND	GND	GND	G2	GND
GND	GND	GND	H14	GND
GND	GND	GND	J1	GND
GND	GND	GND	K12	GND
GND	GND	GND	M3	GND
GND	GND	GND	M7	GND
GND	GND	GND	P5	GND
GND	N.C. (GND)	GND	P10	GND
GND	GND	GND	P14	GND
VCCAUX	DONE	DONE	P13	CONFIG
VCCAUX	PROG_B	PROG_B	A1	CONFIG
VCCAUX	TCK	TCK	B13	JTAG
VCCAUX	TDI	TDI	A2	JTAG
VCCAUX	TDO	TDO	A14	JTAG
VCCAUX	TMS	TMS	B14	JTAG
VCCAUX	VCCAUX	VCCAUX	A5	VCCAUX
VCCAUX	VCCAUX	VCCAUX	E12	VCCAUX
VCCAUX	VCCAUX	VCCAUX	K1	VCCAUX
VCCAUX	VCCAUX	VCCAUX	P9	VCCAUX
VCCINT	VCCINT	VCCINT	A11	VCCINT
VCCINT	VCCINT	VCCINT	D3	VCCINT
VCCINT	N.C. (VCCINT)	VCCINT	D14	VCCINT
VCCINT	N.C. (VCCINT)	VCCINT	K2	VCCINT
VCCINT	VCCINT	VCCINT	L12	VCCINT
VCCINT	VCCINT	VCCINT	P2	VCCINT

CP132 Footprint

Bank 0

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	PROG_B	TDI	I/O L11P_0	GND	VCCAUX	VCCO_0	I/O L07P_0 GCLK10	GND	I/O L05N_0 GCLK7	I/O L04P_0 GCLK4	VCCINT	I/O L02N_0 ◆	I/O L01P_0	TDO
B	I/O L01N_3	I/O L01P_3	I/O L11N_0 HSWAP	I/O L10P_0 ←→	I/O L09P_0	I/O L08P_0	I/O L07N_0 GCLK11	INPUT L06P_0 GCLK8	I/O L05P_0 GCLK6	VCCO_0	I/O L03N_0 VREF_0 ◆	I/O L02P_0 ◆	TCK	TMS
C	GND	I/O L02N_3	I/O L02P_3	I/O L10N_0 ◆	I/O L09N_0	I/O L08N_0 VREF_0	GND	INPUT L06N_0 GCLK9	I/O L04N_0 GCLK5	GND	I/O L03P_0 ←→	I/O L01N_0	I/O L10N_1 LDC2	I/O L10P_1 LDC1
D	I/O L03N_3 ◆	I/O L03P_3 ←→	VCCINT									I/O L09N_1 LDC0	I/O L09P_1 HDC	VCCINT
E	VCCO_3	INPUT VREF_3	GND									VCCAUX	VCCO_1	GND
F	I/O L05P_3 LHCLK2	I/O L04N_3 LHCLK1	I/O L04P_3 LHCLK0									I/O A0	I/O L08N_1 A1	I/O L08P_1 A2
G	I/O L05N_3 LHCLK3 IRDY2	GND	I/O L06P_3 LHCLK4 TRDY2									INPUT VREF_1	I/O L07N_1 A3 RHCLK7	I/O L07P_1 A4 RHCLK6
H	I/O L06N_3 LHCLK5	I/O L07P_3 LHCLK6	I/O L07N_3 LHCLK7									I/O L06N_1 A5 RHCLK5	I/O L06P_1 A6 RHCLK4 IRDY1	GND
J	GND	VCCO_3	I/O									I/O L04N_1 A9 RHCLK1	I/O L05P_1 A8 RHCLK2	I/O L05N_1 A7 RHCLK3 TRDY1
K	VCCAUX	VCCINT	I/O VREF_3 ←→									GND	I/O VREF_1	I/O L04P_1 A10 RHCLK0
L	I/O L08P_3	I/O L08N_3	I/O L09P_3									VCCINT	I/O L03P_1 A12	I/O L03N_1 A11
M	I/O L09N_3	I/O L01P_2 CSO_B	GND	I/O L03P_2 D7 GCLK12	I/O L04P_2 D4 GCLK14	INPUT L05P_2 RDWR_B GCLK0	GND	VCCO_2	I/O L08N_2 A22 ◆	I/O L09N_2 A20 ◆	I/O L10N_2 VS1 A18	I/O L02P_1 A14	I/O L02N_1 A13	VCCO_1
N	I/O L01N_2 INIT_B	I/O L02N_2 MOSI CSI_B	INPUT VREF_2	I/O L03N_2 D6 GCLK13	I/O L04N_2 D3 GCLK15	INPUT L05N_2 M2 GCLK1	I/O M1	I/O L07N_2 DIN D0	I/O L08P_2 A23 ◆	I/O L09P_2 A21 ◆	I/O L10P_2 VS2 A19	I/O L11N_2 CCLK	I/O L01P_1 A16	I/O L01N_1 A15
P	I/O L02P_2 DOUT BUSY	VCCINT	VCCO_2	I/O D5	GND	I/O L06P_2 D2 GCLK2	I/O L06N_2 D1 GCLK3	I/O L07P_2 M0	VCCAUX	GND	I/O VREF_2 ←→	I/O L11P_2 VS0 A17	DONE	GND

Bank 3 | Bank 1

Bank 2

DS312-4_07_030206

Figure 81: **CP132 Package Footprint (top view)**

16-22	**I/O:** Unrestricted, general-purpose user I/O	42-46	**DUAL:** Configuration pin, then possible user I/O	7-8	**VREF:** User I/O or input voltage reference for bank
0-2	**INPUT:** Unrestricted, general-purpose input pin	16	**CLK:** User I/O, input, or global buffer input	8	**VCCO:** Output voltage supply for bank
2	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	6	**VCCINT:** Internal core supply voltage (+1.2V)
9	**N.C.:** Unconnected balls on the XC3S100E FPGA (◆)	16	**GND:** Ground	4	**VCCAUX:** Auxiliary supply voltage (+2.5V)

PQ208 Footprint (Right)

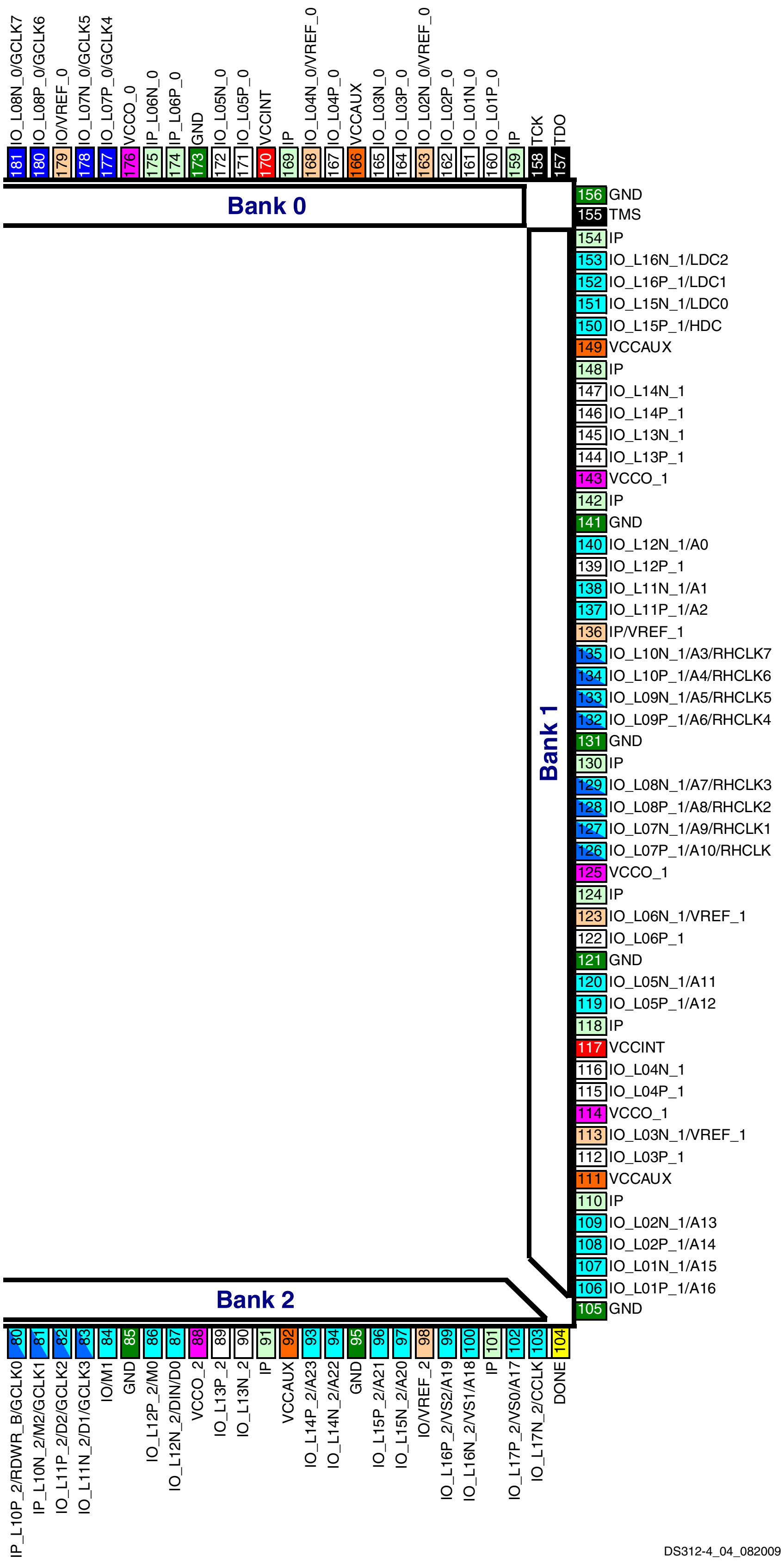


Figure 84: **PQ208 Footprint (Right)**

Table 155: **User I/Os Per Bank for the XC3S1600E in the FG484 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF[(1)]	CLK[(2)]
Top	0	94	56	22	1	7	8
Right	1	94	50	16	21	7	0[(2)]
Bottom	2	94	45	18	24	7	0[(2)]
Left	3	94	63	16	0	7	8
TOTAL		**376**	**214**	**72**	**46**	**28**	**16**

Notes:
1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

Footprint Migration Differences

The XC3S1600E FPGA is the only Spartan-3E device offered in the FG484 package.

FG484 Footprint

Left Half of Package (top view)

214	**I/O:** Unrestricted, general-purpose user I/O
72	**INPUT:** User I/O or reference resistor input for bank
46	**DUAL:** Configuration pin, then possible user I/O
28	**VREF:** User I/O or input voltage reference for bank
16	**CLK:** User I/O, input, or clock buffer input
2	**CONFIG:** Dedicated configuration pins
4	**JTAG:** Dedicated JTAG port pins
48	**GND:** Ground
28	**VCCO:** Output voltage supply for bank
16	**VCCINT:** Internal core supply voltage (+1.2V)
10	**VCCAUX:** Auxiliary supply voltage (+2.5V)
0	**N.C.:** Not connected

Bank 0

	1	2	3	4	5	6	7	8	9	10	11
A	GND	INPUT L37P_0	INPUT L37N_0	I/O L35N_0	I/O L35P_0	I/O L33N_0	I/O L33P_0	I/O L30P_0	I/O L24N_0	I/O L24P_0	GND
B	PROG_B	TDI	I/O L39P_0	I/O L39N_0	VCCO_0	I/O	GND	I/O L30N_0	I/O L28P_0	VCCO_0	I/O L21N_0 GCLK11
C	I/O L01N_3	I/O L01P_3	GND	I/O L40P_0	I/O	INPUT L34P_0	INPUT L34N_0	INPUT L31N_0	I/O L28N_0	I/O L25P_0	I/O L21P_0 GCLK10
D	I/O L04P_3	I/O L02N_3 VREF_3	I/O L02P_3	I/O L40N_0 HSWAP	I/O L38P_0	I/O L38N_0 VREF_0	I/O L36P_0	INPUT L31P_0	I/O L29P_0	I/O L25N_0 VREF_0	I/O L22N_0
E	I/O L04N_3	VCCO_3	I/O L03N_3	I/O L03P_3	VCCAUX	INPUT	I/O L36N_0	VCCO_0	I/O L29N_0	GND	I/O L22P_0
F	I/O L07N_3	INPUT	I/O L05P_3	I/O L05N_3	INPUT	GND	I/O L32N_0 VREF_0	I/O L32P_0	I/O	INPUT L23N_0	INPUT L23P_0
G	I/O L07P_3	GND	INPUT	I/O L06P_3	I/O L06N_3	I/O L08N_3 VREF_3	I/O L08P_3	I/O	INPUT L26N_0	INPUT L26P_0	VCCO_0
H	I/O L11N_3	I/O L10N_3	I/O L10P_3	I/O L09N_3	I/O L09P_3	VCCO_3	INPUT	I/O L27N_0	I/O L27P_0	I/O	INPUT L20N_0 GCLK9
J	I/O L11P_3	VCCO_3	I/O L13N_3 VREF_3	GND	I/O L12P_3	I/O L12N_3	INPUT	I/O L14N_3	GND	VCCINT	I/O
K	I/O L16N_3	INPUT	I/O L13P_3	I/O L15N_3	I/O L15P_3	INPUT	I/O L17P_3	I/O L14P_3	VCCINT	GND	VCCINT
L	I/O L16P_3	GND	INPUT VREF_3	VCCAUX	I/O L18N_3 LHCLK1	GND	I/O L17N_3	I/O L19P_3 LHCLK2	GND	VCCINT	VCCINT
M	I/O L20P_3 LHCLK4 TRDY2	INPUT	I/O L21P_3 LHCLK6	I/O L21N_3 LHCLK7	I/O L18P_3 LHCLK0	INPUT	VCCO_3	I/O L19N_3 LHCLK3 IRDY2	VCCINT	GND	VCCINT
N	I/O L20N_3 LHCLK5	VCCO_3	INPUT	I/O L24N_3 VREF_3	I/O L24P_3	I/O L22N_3	I/O L22P_3	I/O L23P_3	VCCAUX	VCCINT	GND
P	I/O L25P_3	I/O L25N_3	INPUT	GND	I/O L27P_3	I/O L27N_3	I/O L26P_3	I/O L23N_3	GND	I/O L17P_2	GND
R	I/O L28P_3	I/O L28N_3	I/O L29N_3	I/O L29P_3	VCCO_3	I/O L30P_3	I/O L26N_3	INPUT	I/O L13N_2 VREF_2	I/O L17N_2	I/O L20P_2 D4 GCLK14
T	INPUT	GND	INPUT VREF_3	I/O L32N_3	I/O L32P_3	I/O L30N_3	INPUT	I/O L10N_2	I/O L13P_2	I/O L16P_2	I/O L20N_2 D3 GCLK15
U	I/O L31P_3	I/O L31N_3	I/O L34P_3	I/O L34N_3	INPUT	GND	I/O L07N_2	I/O L10P_2	VCCO_2	I/O L16N_2	I/O L19N_2 D6 GCLK13
V	I/O L33P_3	VCCO_3	I/O L35P_3	I/O L35N_3	VCCAUX	I/O L04P_2	I/O L07P_2	I/O L09N_2 VREF_2	I/O L12P_2	GND	I/O L19P_2 D7 GCLK12
W	I/O L33N_3	I/O L36P_3	I/O L36N_3 VREF_3	INPUT	I/O L03P_2 DOUT BUSY	I/O L04N_2	I/O L06N_2	I/O L09P_2	I/O L12N_2	INPUT L15P_2	VCCAUX
Y	I/O L37P_3	I/O L37N_3	GND	INPUT L02P_2	I/O L03N_2 MOSI CSI_B	INPUT L05N_2	I/O L06P_2	I/O	I/O	INPUT L15N_2	INPUT L18P_2
AA	I/O L38N_3	I/O L38P_3	I/O L01P_2 CSO_B	INPUT L02N_2	VCCO_2	INPUT L05P_2	GND	I/O L11P_2	VCCO_2	I/O	INPUT L18N_2 VREF_2
AB	GND	INPUT	I/O L01N_2 INIT_B	I/O VREF_2	I/O	INPUT L08P_2	INPUT L08N_2	I/O L11N_2	I/O L14N_2	I/O L14P_2	I/O D5

Bank 3

Bank 2

DS312_10_101905

Figure 88: **FG484 Package Footprint (top view)**