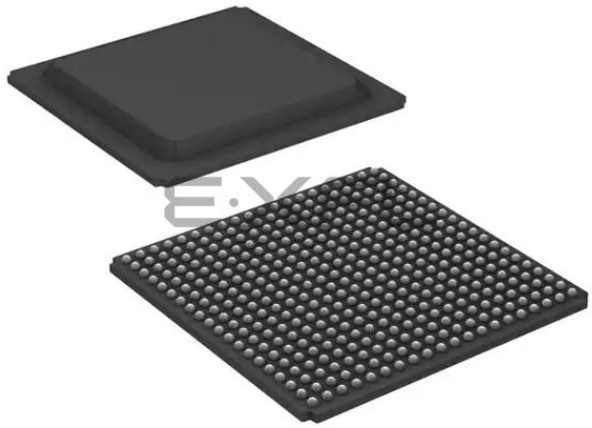
AMD Xilinx - XC3S1600E-4FG400I Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	3688
Number of Logic Elements/Cells	33192
Total RAM Bits	663552
Number of I/O	304
Number of Gates	1600000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	400-BGA
Supplier Device Package	400-FBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s1600e-4fg400i

Supply Voltages for the IOBs

The IOBs are powered by three supplies:

1. The V_{CCO} supplies, one for each of the FPGA's I/O banks, power the output drivers. The voltage on the V_{CCO} pins determines the voltage swing of the output signal.
2. V_{CCINT} is the main power supply for the FPGA's internal logic.
3. V_{CCAUX} is an auxiliary source of power, primarily to optimize the performance of various FPGA functions such as I/O switching.

I/O and Input-Only Pin Behavior During Power-On, Configuration, and User Mode

In this section, all behavior described for I/O pins also applies to input-only pins and dual-purpose I/O pins that are not actively involved in the currently-selected configuration mode.

All I/O pins have ESD clamp diodes to their respective V_{CCO} supply and from GND, as shown in Figure 5. The V_{CCINT} (1.2V), V_{CCAUX} (2.5V), and V_{CCO} supplies can be applied in any order. Before the FPGA can start its configuration process, V_{CCINT}, V_{CCO} Bank 2, and V_{CCAUX} must have reached their respective minimum recommended operating levels indicated in Table 74. At this time, all output drivers are in a high-impedance state. V_{CCO} Bank 2, V_{CCINT}, and V_{CCAUX} serve as inputs to the internal Power-On Reset circuit (POR).

A Low level applied to the HSWAP input enables pull-up resistors on user-I/O and input-only pins from power-on throughout configuration. A High level on HSWAP disables the pull-up resistors, allowing the I/Os to float. HSWAP contains an internal pull-up resistor and defaults to High if left floating. As soon as power is applied, the FPGA begins initializing its configuration memory. At the same time, the FPGA internally asserts the Global Set-Reset (GSR), which asynchronously resets all IOB storage elements to a default Low state. Also see Pin Behavior During Configuration.

Upon the completion of initialization and the beginning of configuration, INIT_B goes High, sampling the M0, M1, and M2 inputs to determine the configuration mode. Configuration data is then loaded into the FPGA. The I/O drivers remain in a high-impedance state (with or without pull-up resistors, as determined by the HSWAP input) throughout configuration.

At the end of configuration, the GSR net is released, placing the IOB registers in a Low state by default, unless the loaded design reverses the polarity of their respective SR inputs.

The Global Three State (GTS) net is released during Start-Up, marking the end of configuration and the beginning of design operation in the User mode. After the GTS net is released, all user I/Os go active while all unused I/Os are pulled down (PULLDOWN). The designer can control how the unused I/Os are terminated after GTS is released by setting the Bitstream Generator (BitGen) option UnusedPin to PULLUP, PULLDOWN, or FLOAT.

One clock cycle later (default), the Global Write Enable (GWE) net is released allowing the RAM and registers to change states. Once in User mode, any pull-up resistors enabled by HSWAP revert to the user settings and HSWAP is available as a general-purpose I/O. For more information on PULLUP and PULLDOWN, see Pull-Up and Pull-Down Resistors.

Behavior of Unused I/O Pins After Configuration

By default, the Xilinx ISE development software automatically configures all unused I/O pins as input pins with individual internal pull-down resistors to GND.

This default behavior is controlled by the ***UnusedPin*** bitstream generator (BitGen) option, as described in Table 69.

JTAG Boundary-Scan Capability

All Spartan-3E IOBs support boundary-scan testing compatible with IEEE 1149.1/1532 standards. During boundary-scan operations such as EXTEST and HIGHZ the pull-down resistor is active. See JTAG Mode for more information on programming via JTAG.

Block RAM

For additional information, refer to the “Using Block RAM” chapter in UG331.

Spartan-3E devices incorporate 4 to 36 dedicated block RAMs, which are organized as dual-port configurable 18 Kbit blocks. Functionally, the block RAM is identical to the Spartan-3 architecture block RAM. Block RAM synchronously stores large amounts of data while distributed RAM, previously described, is better suited for buffering small amounts of data anywhere along signal paths. This section describes basic block RAM functions.

Each block RAM is configurable by setting the content’s initial values, default signal value of the output registers, port aspect ratios, and write modes. Block RAM can be used in single-port or dual-port modes.

Arrangement of RAM Blocks on Die

The block RAMs are located together with the multipliers on the die in one or two columns depending on the size of the device. The XC3S100E has one column of block RAM. The Spartan-3E devices ranging from the XC3S250E to XC3S1600E have two columns of block RAM. Table 21 shows the number of RAM blocks, the data storage capacity, and the number of columns for each device. Row(s) of CLBs are located above and below each block RAM column.

Table 21: **Number of RAM Blocks by Device**

Device	Total Number of RAM Blocks	Total Addressable Locations (bits)	Number of Columns
XC3S100E	4	73,728	1
XC3S250E	12	221,184	2
XC3S500E	20	368,640	2
XC3S1200E	28	516,096	2
XC3S1600E	36	663,552	2

Immediately adjacent to each block RAM is an embedded 18x18 hardware multiplier. The upper 16 bits of the block RAM's Port A Data input bus are shared with the upper 16 bits of the A multiplicand input bus of the multiplier. Similarly, the upper 16 bits of Port B's data input bus are shared with the B multiplicand input bus of the multiplier.

The Internal Structure of the Block RAM

The block RAM has a dual port structure. The two identical data ports called A and B permit independent access to the common block RAM, which has a maximum capacity of 18,432 bits, or 16,384 bits with no parity bits (see parity bits description in Table 22). Each port has its own dedicated set of data, control, and clock lines for synchronous read and write operations. There are four basic data paths, as shown in Figure 30:

1. Write to and read from Port A
2. Write to and read from Port B
3. Data transfer from Port A to Port B
4. Data transfer from Port B to Port A

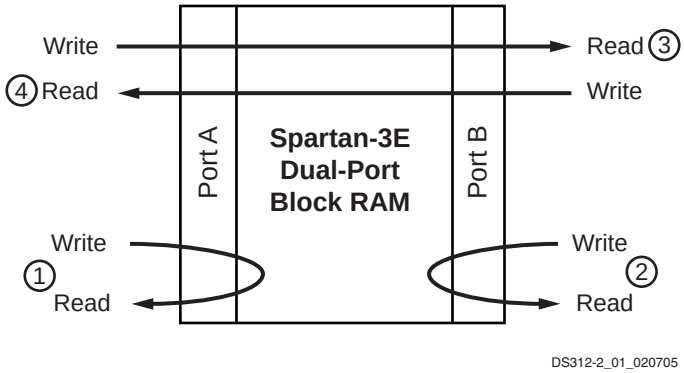

Figure 30: **Block RAM Data Paths**

Number of Ports

A choice among primitives determines whether the block RAM functions as dual- or single-port memory. A name of the form RAMB16_S[w_A]_S[w_B] calls out the dual-port primitive, where the integers w_A and w_B specify the total data path width at ports A and B, respectively. Thus, a RAMB16_S9_S18 is a dual-port RAM with a 9-bit Port A and an 18-bit Port B. A name of the form RAMB16_S[w] identifies the single-port primitive, where the integer w specifies the total data path width of the lone port A. A RAMB16_S18 is a single-port RAM with an 18-bit port.

Port Aspect Ratios

Each port of the block RAM can be configured independently to select a number of different possible widths for the data input (DI) and data output (DO) signals as shown in Table 22.

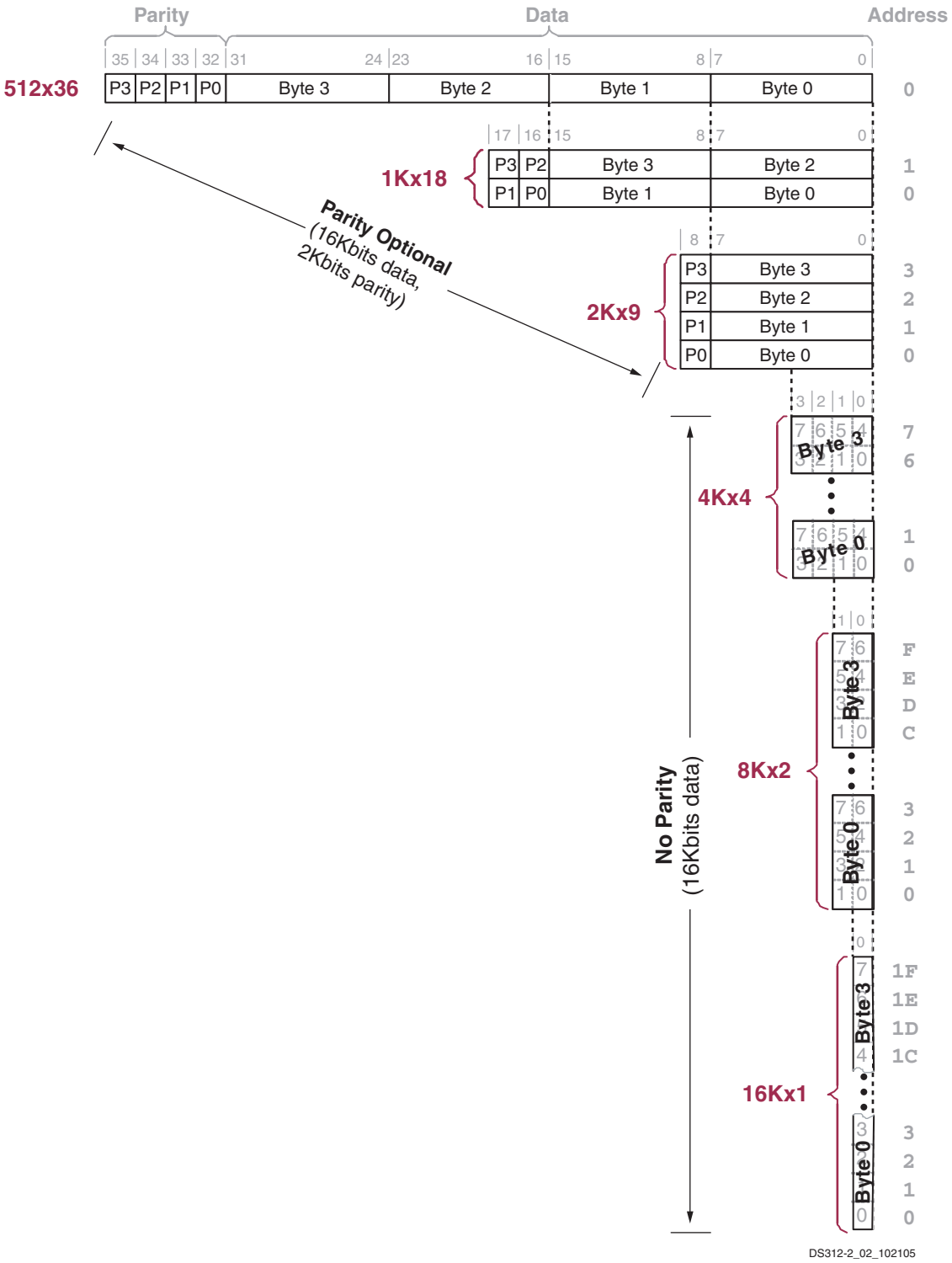

Figure 31: **Data Organization and Bus-matching Operation with Different Port Widths on Port A and Port B**

The BCIN and BCOUT ports have associated dedicated routing that connects adjacent multipliers within the same column. Via the cascade connection, the BCOUT port of one multiplier block drives the BCIN port of the multiplier block directly above it. There is no connection to the BCIN port of the bottom-most multiplier block in a column or a connection from the BCOUT port of the top-most block in a column. As an example, Figure 39 shows the multiplier cascade capability within the XC3S100E FPGA, which has a single column of multiplier, four blocks tall. For clarity, the figure omits the register control inputs.

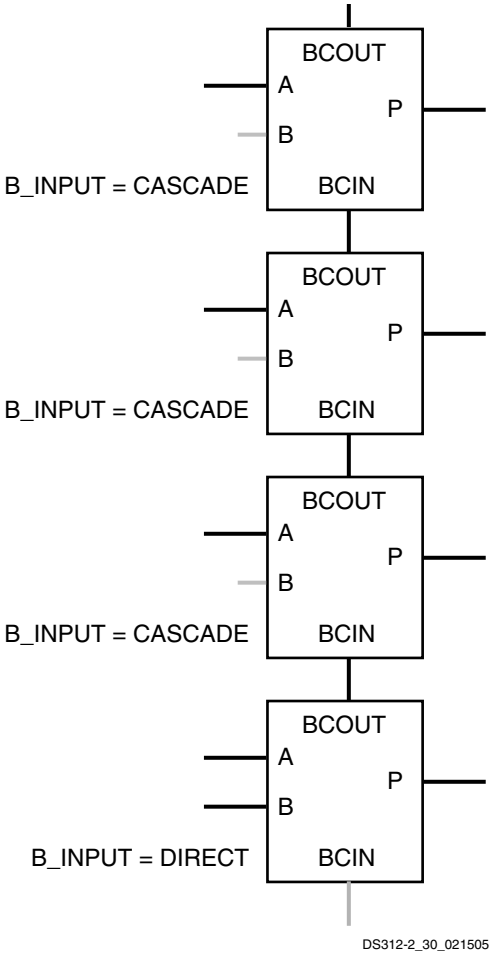

Figure 39: **Multiplier Cascade Connection**

When using the BREG register, the cascade connection forms a shift register structure typically used in DSP algorithms such as direct-form FIR filters. When the BREG register is omitted, the cascade structure essentially feeds the same input value to more than one multiplier. This parallel connection serves to create wide-input multipliers, implement transpose FIR filters, and is used in any application that requires that several multipliers have the same input value.

Configuration

For additional information on configuration, refer to UG332: *Spartan-3 Generation Configuration User Guide*.

Differences from Spartan-3 FPGAs

In general, Spartan-3E FPGA configuration modes are a superset to those available in Spartan-3 FPGAs. Two new modes added in Spartan-3E FPGAs provide a glueless configuration interface to industry-standard parallel NOR Flash and SPI serial Flash memories.

Configuration Process

The function of a Spartan-3E FPGA is defined by loading application-specific configuration data into the FPGA's internal, reprogrammable CMOS configuration latches (CCLs), similar to the way a microprocessor's function is defined by its application program. For FPGAs, this configuration process uses a subset of the device pins, some of which are dedicated to configuration; other pins are merely borrowed and returned to the application as general-purpose user I/Os after configuration completes.

Spartan-3E FPGAs offer several configuration options to minimize the impact of configuration on the overall system design. In some configuration modes, the FPGA generates a clock and loads itself from an external memory source, either serially or via a byte-wide data path. Alternatively, an external host such as a microprocessor downloads the FPGA's configuration data using a simple synchronous serial interface or via a byte-wide peripheral-style interface. Furthermore, multiple-FPGA designs share a single configuration memory source, creating a structure called a daisy chain.

Three FPGA pins—M2, M1, and M0—select the desired configuration mode. The mode pin settings appear in Table 44. The mode pin values are sampled during the start of configuration when the FPGA's INIT_B output goes High. After the FPGA completes configuration, the mode pins are available as user I/Os.

Table 44: **Spartan-3E Configuration Mode Options and Pin Settings**

	Master Serial	SPI	BPI	Slave Parallel	Slave Serial	JTAG
M[2:0] mode pin settings	<0:0:0>	<0:0:1>	<0:1:0>=Up <0:1:1>=Down	<1:1:0>	<1:1:1>	<1:0:1>
Data width	Serial	Serial	Byte-wide	Byte-wide	Serial	Serial
Configuration memory source	Xilinx Platform Flash	Industry-standard SPI serial Flash	Industry-standard parallel NOR Flash or Xilinx parallel Platform Flash	Any source via microcontroller, CPU, Xilinx parallel Platform Flash, etc.	Any source via microcontroller, CPU, Xilinx Platform Flash, etc.	Any source via microcontroller, CPU, System ACE™ CF, etc.
Clock source	Internal oscillator	Internal oscillator	Internal oscillator	External clock on CCLK pin	External clock on CCLK pin	External clock on TCK pin
Total I/O pins borrowed during configuration	8	13	46	21	8	0
Configuration mode for downstream daisy-chained FPGAs	Slave Serial	Slave Serial	Slave Parallel	Slave Parallel or Memory Mapped	Slave Serial	JTAG
Stand-alone FPGA applications (no external download host)	✓	✓	✓	Possible using XCFxxP Platform Flash, which optionally generates CCLK	Possible using XCFxxP Platform Flash, which optionally generates CCLK	
Uses low-cost, industry-standard Flash		✓	✓			
Supports optional MultiBoot, multi-configuration mode			✓			

Table 46: **Pin Behavior during Configuration *(Cont'd)***

Pin Name	Master Serial	SPI (Serial Flash)	BPI (Parallel NOR Flash)	JTAG	Slave Parallel	Slave Serial	I/O Bank[3]
D0/DIN	DIN	DIN	D0		D0	DIN	2
RDWR_B			RDWR_B		RDWR_B		2
A23			A23				2
A22			A22				2
A21			A21				2
A20			A20				2
A19/VS2		VS2	A19				2
A18/VS1		VS1	A18				2
A17/VS0		VS0	A17				2
A16			A16				1
A15			A15				1
A14			A14				1
A13			A13				1
A12			A12				1
A11			A11				1
A10			A10				1
A9			A9				1
A8			A8				1
A7			A7				1
A6			A6				1
A5			A5				1
A4			A4				1
A3			A3				1
A2			A2				1
A1			A1				1
A0			A0				1
LDC0			LDC0				1
LDC1			LDC1				1
LDC2			LDC2				1
HDC			HDC				1

Notes:
1. Gray shaded cells represent pins that are in a high-impedance state (Hi-Z, floating) during configuration. These pins have an optional internal pull-up resistor to their respective V_{CCO} supply pin that is active throughout configuration if the HSWAP input is Low.
2. Yellow shaded cells represent pins with an internal pull-up resistor to its respective voltage supply rail that is active during configuration, regardless of the HSWAP pin.
3. Note that dual-purpose outputs are supplied by V_{CCO}, and configuration inputs are supplied by V_{CCAUX}.

The HSWAP pin itself has a pull-up resistor enabled during configuration. However, the VCCO_0 supply voltage must be applied before the pull-up resistor becomes active. If the VCCO_0 supply ramps after the VCCO_2 power supply, do not let HSWAP float; tie HSWAP to the desired logic level externally.

Spartan-3E FPGAs have only six dedicated configuration pins, including the DONE and PROG_B pins, and the four JTAG boundary-scan pins: TDI, TDO, TMS, and TCK. All other configuration pins are dual-purpose I/O pins and are available to the FPGA application after the DONE pin goes High. See Start-Up for additional information.

Table 47 shows the default I/O standard setting for the various configuration pins during the configuration process. The configuration interface is designed primarily for 2.5V operation when the VCCO_2 (and VCCO_1 in BPI mode) connects to 2.5V.

Table 47: **Default I/O Standard Setting During Configuration (VCCO_2 = 2.5V)**

Pin(s)	I/O Standard	Output Drive	Slew Rate
All, including CCLK	LVCMOS25	8 mA	Slow

Table 55: **Serial Peripheral Interface (SPI) Connections *(Cont'd)***

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
VS[2:0] Ⓢ	Input	**Variant Select**. Instructs the FPGA how to communicate with the attached SPI Flash PROM. See Design Considerations for the HSWAP, M[2:0], and VS[2:0] Pins.	Must be at the logic levels shown in Table 53. Sampled when INIT_B goes High.	User I/O
MOSI	Output	**Serial Data Output**.	FPGA sends SPI Flash memory read commands and starting address to the PROM's serial data input.	User I/O
DIN	Input	**Serial Data Input**.	FPGA receives serial data from PROM's serial data output.	User I/O
CSO_B	Output	**Chip Select Output**. Active Low.	Connects to the SPI Flash PROM's chip-select input. If HSWAP = 1, connect this signal to a 4.7 kΩ pull-up resistor to 3.3V.	Drive CSO_B High after configuration to disable the SPI Flash and reclaim the MOSI, DIN, and CCLK pins. Optionally, re-use this pin and MOSI, DIN, and CCLK to continue communicating with SPI Flash.
CCLK	Output	**Configuration Clock**. Generated by FPGA internal oscillator. Frequency controlled by ***ConfigRate*** bitstream generator option. If CCLK PCB trace is long or has multiple connections, terminate this output to maintain signal integrity. See CCLK Design Considerations.	Drives PROM's clock input.	User I/O
DOUT	Output	**Serial Data Output**.	Actively drives. Not used in single-FPGA designs. In a daisy-chain configuration, this pin connects to DIN input of the next FPGA in the chain.	User I/O
INIT_B	Open-drain bidirectional I/O	**Initialization Indicator**. Active Low. Goes Low at start of configuration during Initialization memory clearing process. Released at end of memory clearing, when mode select pins are sampled. In daisy-chain applications, this signal requires an external 4.7 kΩ pull-up resistor to VCCO_2.	Active during configuration. If SPI Flash PROM requires > 2 ms to awake after powering on, hold INIT_B Low until PROM is ready. If CRC error detected during configuration, FPGA drives INIT_B Low.	User I/O. If unused in the application, drive INIT_B High.
DONE	Open-drain bidirectional I/O	**FPGA Configuration Done**. Low during configuration. Goes High when FPGA successfully completes configuration. Requires external 330 Ω pull-up resistor to 2.5V.	Low indicates that the FPGA is not yet configured.	Pulled High via external pull-up. When High, indicates that the FPGA successfully configured.
PROG_B	Input	**Program FPGA**. Active Low. When asserted Low for 500 ns or longer, forces the FPGA to restart its configuration process by clearing configuration memory and resetting the DONE and INIT_B pins once PROG_B returns High. Recommend external 4.7 kΩ pull-up resistor to 2.5V. Internal pull-up value may be weaker (see Table 78). If driving externally with a 3.3V output, use an open-drain or open-collector driver or use a current limiting series resistor.	Must be High to allow configuration to start.	Drive PROG_B Low and release to reprogram FPGA. Hold PROG_B to force FPGA I/O pins into Hi-Z, allowing direct programming access to SPI Flash PROM pins.

Table 65: **Slave Parallel Mode Connections *(Cont'd)***

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
INIT_B	Open-drain bidirectional I/O	**Initialization Indicator**. Active Low. Goes Low at the start of configuration during the Initialization memory clearing process. Released at the end of memory clearing, when mode select pins are sampled. In daisy-chain applications, this signal requires an external 4.7 kΩ pull-up resistor to VCCO_2.	Active during configuration. If CRC error detected during configuration, FPGA drives INIT_B Low.	User I/O. If unused in the application, drive INIT_B High.
DONE	Open-drain bidirectional I/O	**FPGA Configuration Done**. Low during configuration. Goes High when FPGA successfully completes configuration. Requires external 330 Ω pull-up resistor to 2.5V.	Low indicates that the FPGA is not yet configured.	Pulled High via external pull-up. When High, indicates that the FPGA successfully configured.
PROG_B	Input	**Program FPGA**. Active Low. When asserted Low for 500 ns or longer, forces the FPGA to restart its configuration process by clearing configuration memory and resetting the DONE and INIT_B pins once PROG_B returns High. Recommend external 4.7 kΩ pull-up resistor to 2.5V. Internal pull-up value may be weaker (see Table 78). If driving externally with a 3.3V output, use an open-drain or open-collector driver or use a current limiting series resistor.	Must be High to allow configuration to start.	Drive PROG_B Low and release to reprogram FPGA.

Voltage Compatibility

Ⓥ Most Slave Parallel interface signals are within the FPGA's I/O Bank 2, supplied by the VCCO_2 supply input. The VCCO_2 voltage can be 1.8V, 2.5V, or 3.3V to match the requirements of the external host, ideally 2.5V. Using 1.8V or 3.3V requires additional design considerations as the DONE and PROG_B pins are powered by the FPGA's 2.5V V_{CCAUX} supply. See XAPP453: *The 3.3V Configuration of Spartan-3 FPGAs* for additional information.

Daisy-Chaining

If the application requires multiple FPGAs with different configurations, then configure the FPGAs using a daisy chain. Use Slave Parallel mode (M[2:0] = <1:1:0>) for all FPGAs in the daisy-chain. The schematic in Figure 62 is optimized for FPGA downloading and does not support the SelectMAP read interface. The FPGA's RDWR_B pin must be Low during configuration.

After the lead FPGA is filled with its configuration data, the lead FPGA enables the next FPGA in the daisy-chain by asserting is chip-select output, CSO_B.

Switching Characteristics

All Spartan-3E FPGAs ship in two speed grades: -4 and the higher performance -5. Switching characteristics in this document may be designated as Advance, Preliminary, or Production, as shown in Table 84. Each category is defined as follows:

Advance: These specifications are based on simulations only and are typically available soon after establishing FPGA specifications. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These specifications are based on complete early silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting preliminary delays is greatly reduced compared to Advance data.

Production: These specifications are approved once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Software Version Requirements

Production-quality systems must use FPGA designs compiled using a speed file designated as PRODUCTION status. FPGAs designs using a less mature speed file designation should only be used during system prototyping or pre-production qualification. FPGA designs with speed files designated as Advance or Preliminary should not be used in a production-quality system.

Whenever a speed file designation changes, as a device matures toward Production status, rerun the latest Xilinx ISE software on the FPGA design to ensure that the FPGA design incorporates the latest timing information and software updates.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all Spartan-3E devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.**

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Timing parameters and their representative values are selected for inclusion below either because they are important as general design requirements or they indicate fundamental device performance characteristics. The Spartan-3E speed files (v1.27), part of the Xilinx Development Software, are the original source for many but not all of the values. The speed grade designations for these files are shown in Table 84. For more complete, more precise, and worst-case data, use the values reported by the Xilinx static timing analyzer (TRACE in the Xilinx development software) and back-annotated to the simulation netlist.

Table 84: **Spartan-3E v1.27 Speed Grade Designations**

Device	Advance	Preliminary	Production
XC3S100E			-MIN, -4, -5
XC3S250E			-MIN, -4, -5
XC3S500E			-MIN, -4, -5
XC3S1200E			-MIN, -4, -5
XC3S1600E			-MIN, -4, -5

Table 85 provides the history of the Spartan-3E speed files since all devices reached Production status.

Table 85: **Spartan-3E Speed File Version History**

Version	ISE Release	Description
1.27	9.2.03i	Added XA Automotive.
1.26	8.2.02i	Added -0/-MIN speed grade, which includes minimum values.
1.25	8.2.01i	Added XA Automotive devices to speed file. Improved model for left and right DCMs.
1.23	8.2i	Updated input setup/hold values based on default IFD_DELAY_VALUE settings.
1.21	8.1.03i	All Spartan-3E FPGAs and all speed grades elevated to Production status.

Table 97: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}/GND Pair**

Signal Standard (IOSTANDARD)			Package Type				
			VQ 100	TQ 144	PQ 208	CP 132	FT256 FG320 FG400 FG484
Single-Ended Standards							
LVTTL	Slow	2	34	20	19	52	60
		4	17	10	10	26	41
		6	17	10	7	26	29
		8	8	6	6	13	22
		12	8	6	5	13	13
		16	5	5	5	6	11
	Fast	2	17	17	17	26	34
		4	9	9	9	13	20
		6	7	7	7	13	15
		8	6	6	6	6	12
		12	5	5	5	6	10
		16	5	5	5	5	9
LVCMOS33	Slow	2	34	20	20	52	76
		4	17	10	10	26	46
		6	17	10	7	26	27
		8	8	6	6	13	20
		12	8	6	5	13	13
		16	5	5	5	6	10
	Fast	2	17	17	17	26	44
		4	8	8	8	13	26
		6	8	6	6	13	16
		8	6	6	6	6	12
		12	5	5	5	6	10
		16	8	8	5	5	8
LVCMOS25	Slow	2	28	16	16	42	76
		4	13	10	10	19	46
		6	13	7	7	19	33
		8	6	6	6	9	24
		12	6	6	6	9	18
	Fast	2	17	16	16	26	42
		4	9	9	9	13	20
		6	9	7	7	13	15
		8	6	6	6	6	13
		12	5	5	5	6	11
LVCMOS18	Slow	2	19	11	8	29	64
		4	13	7	6	19	34
		6	6	5	5	9	22
		8	6	4	4	9	18
	Fast	2	13	8	8	19	36
		4	8	5	5	13	21
		6	4	4	4	6	13
		8	4	4	4	6	10

Table 97: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}/GND Pair *(Cont'd)***

Signal Standard (IOSTANDARD)			Package Type				
			VQ 100	TQ 144	PQ 208	CP 132	FT256 FG320 FG400 FG484
LVCMOS15	Slow	2	16	10	10	19	55
		4	8	7	7	9	31
		6	6	5	5	9	18
	Fast	2	9	9	9	13	25
		4	7	7	7	7	16
		6	5	5	5	5	13
LVCMOS12	Slow	2	17	11	11	16	55
	Fast	2	10	10	10	10	31
PCI33_3			8	8	8	16	16
PCI66_3			8	8	8	13	13
PCIX			7	7	7	11	11
HSTL_I_18			10	10	10	16	17
HSTL_III_18			10	10	10	16	16
SSTL18_I			9	9	9	15	15
SSTL2_I			12	12	12	18	18
Differential Standards (Number of I/O Pairs or Channels)							
LVDS_25			6	6	6	12	20
BLVDS_25			4	4	4	4	4
MINI_LVDS_25			6	6	6	12	20
LVPECL_25			Input Only				
RSDS_25			6	6	6	12	20
DIFF_HSTL_I_18			5	5	5	8	8
DIFF_HSTL_IIII_18			5	5	5	8	8
DIFF_SSTL18_I			4	4	4	7	7
DIFF_SSTL2_I			6	6	6	9	8

Notes:

1. The numbers in this table are recommendations that assume sound board layout practice. This table assumes the following parasitic factors: combined PCB trace and land inductance per VCCO and GND pin of 1.0 nH, receiver capacitive load of 15 pF. Test limits are the VIL/VIH voltage limits for the respective I/O standard.
2. The PQ208 results are based on physical measurements of a PQ208 package soldered to a typical printed circuit board. All other results are based on worst-case simulation and an interpolation of the PQ208 physical results.
3. If more than one signal standard is assigned to the I/Os of a given bank, refer to XAPP689: Managing Ground Bounce in Large FPGAs for information on how to perform weighted average SSO calculations.

Configurable Logic Block (CLB) Timing

Table 98: **CLB (SLICEM) Timing**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{CKO}	When reading from the FFX (FFY) Flip-Flop, the time from the active transition at the CLK input to data appearing at the XQ (YQ) output	-	0.52	-	0.60	ns
Setup Times						
T_{AS}	Time from the setup of data at the F or G input to the active transition at the CLK input of the CLB	0.46	-	0.52	-	ns
T_{DICK}	Time from the setup of data at the BX or BY input to the active transition at the CLK input of the CLB	1.58	-	1.81	-	ns
Hold Times						
T_{AH}	Time from the active transition at the CLK input to the point where data is last held at the F or G input	0	-	0	-	ns
T_{CKDI}	Time from the active transition at the CLK input to the point where data is last held at the BX or BY input	0	-	0	-	ns
Clock Timing						
T_{CH}	The High pulse width of the CLB's CLK signal	0.70	-	0.80	-	ns
T_{CL}	The Low pulse width of the CLK signal	0.70	-	0.80	-	ns
F_{TOG}	Toggle frequency (for export control)	0	657	0	572	MHz
Propagation Times						
T_{ILO}	The time it takes for data to travel from the CLB's F (G) input to the X (Y) output	-	0.66	-	0.76	ns
Set/Reset Pulse Width						
T_{RPW_CLB}	The minimum allowable pulse width, High or Low, to the CLB's SR input	1.57	-	1.80	-	ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 77.

Phase Shifter (PS)

Table 108: **Recommended Operating Conditions for the PS in Variable Phase Mode**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Operating Frequency Ranges						
PSCLK_FREQ (F_{PSCLK})	Frequency for the PSCLK input	1	167	1	167	MHz
Input Pulse Requirements						
PSCLK_PULSE	PSCLK pulse width as a percentage of the PSCLK period	40%	60%	40%	60%	-

Table 109: **Switching Characteristics for the PS in Variable Phase Mode**

Symbol	Description	Equation		Units
Phase Shifting Range				
MAX_STEPS(2)	Maximum allowed number of DCM_DELAY_STEP steps for a given CLKIN clock period, where T = CLKIN clock period in ns. If using CLKIN_DIVIDE_BY_2 = TRUE, double the effective clock period.(3)	CLKIN < 60 MHz	±[INTEGER(10 • (T_{CLKIN} – 3 ns))]	steps
		CLKIN ≥ 60 MHz	±[INTEGER(15 • (T_{CLKIN} – 3 ns))]	steps
FINE_SHIFT_RANGE_MIN	Minimum guaranteed delay for variable phase shifting	±[MAX_STEPS • DCM_DELAY_STEP_MIN]		ns
FINE_SHIFT_RANGE_MAX	Maximum guaranteed delay for variable phase shifting	±[MAX_STEPS • DCM_DELAY_STEP_MAX]		ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 77 and Table 108.
2. The maximum variable phase shift range, MAX_STEPS, is only valid when the DCM is has no initial fixed phase shifting, i.e., the PHASE_SHIFT attribute is set to 0.
3. The DCM_DELAY_STEP values are provided at the bottom of Table 105.

Miscellaneous DCM Timing

Table 110: **Miscellaneous DCM Timing**

Symbol	Description	Min	Max	Units
DCM_RST_PW_MIN(1)	Minimum duration of a RST pulse width	3	-	CLKIN cycles
DCM_RST_PW_MAX(2)	Maximum duration of a RST pulse width	N/A	N/A	seconds
DCM_CONFIG_LAG_TIME(3)	Maximum duration from V_{CCINT} applied to FPGA configuration successfully completed (DONE pin goes High) and clocks applied to DCM DLL	N/A	N/A	minutes

Notes:

1. This limit only applies to applications that use the DCM DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV). The DCM DFS outputs (CLKFX, CLKFX180) are unaffected.
2. This specification is equivalent to the Virtex-4 DCM_RESET specfication.This specification does not apply for Spartan-3E FPGAs.
3. This specification is equivalent to the Virtex-4 TCONFIG specification. This specification does not apply for Spartan-3E FPGAs.

Configuration Clock (CCLK) Characteristics

Table 112: **Master Mode CCLK Output Period by *ConfigRate* Option Setting**

Symbol	Description	*ConfigRate* Setting	Temperature Range	Minimum	Maximum	Units
T_{CCLK1}	CCLK clock period by ***ConfigRate*** setting	1 *(power-on value and default value)*	Commercial	570	1,250	ns
			Industrial	485		ns
T_{CCLK3}		3	Commercial	285	625	ns
			Industrial	242		ns
T_{CCLK6}		6	Commercial	142	313	ns
			Industrial	121		ns
T_{CCLK12}		12	Commercial	71.2	157	ns
			Industrial	60.6		ns
T_{CCLK25}		25	Commercial	35.5	78.2	ns
			Industrial	30.3		ns
T_{CCLK50}		50	Commercial	17.8	39.1	ns
			Industrial	15.1		ns

Notes:

1. Set the ***ConfigRate*** option value when generating a configuration bitstream. See Bitstream Generator (BitGen) Options in Module 2.

Table 113: **Master Mode CCLK Output Frequency by *ConfigRate* Option Setting**

Symbol	Description	*ConfigRate* Setting	Temperature Range	Minimum	Maximum	Units
F_{CCLK1}	Equivalent CCLK clock frequency by ***ConfigRate*** setting	1 *(power-on value and default value)*	Commercial	0.8	1.8	MHz
			Industrial		2.1	MHz
F_{CCLK3}		3	Commercial	1.6	3.6	MHz
			Industrial		4.2	MHz
F_{CCLK6}		6	Commercial	3.2	7.1	MHz
			Industrial		8.3	MHz
F_{CCLK12}		12	Commercial	6.4	14.1	MHz
			Industrial		16.5	MHz
F_{CCLK25}		25	Commercial	12.8	28.1	MHz
			Industrial		33.0	MHz
F_{CCLK50}		50	Commercial	25.6	56.2	MHz
			Industrial		66.0	MHz

Table 114: **Master Mode CCLK Output Minimum Low and High Time**

Symbol	Description		*ConfigRate* Setting						Units
			1	3	6	12	25	50	
T_{MCCL}, T_{MCCH}	Master mode CCLK minimum Low and High time	Commercial	276	138	69	34.5	17.1	8.5	ns
		Industrial	235	117	58	29.3	14.5	7.3	ns

Table 115: **Slave Mode CCLK Input Low and High Time**

Symbol	Description	Min	Max	Units
T_{SCCL}, T_{SCCH}	CCLK Low and High time	5	∞	ns

Table 117: **Timing for the Slave Parallel Configuration Mode *(Cont'd)***

Symbol	Description			All Speed Grades		Units
				Min	Max	
Clock Timing						
T_{CCH}	The High pulse width at the CCLK input pin			5	-	ns
T_{CCL}	The Low pulse width at the CCLK input pin			5	-	ns
F_{CCPAR}	Frequency of the clock signal at the CCLK input pin	No bitstream compression	Not using the BUSY pin(2)	0	50	MHz
			Using the BUSY pin	0	66	MHz
		With bitstream compression		0	20	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 77.
2. In the Slave Parallel mode, it is necessary to use the BUSY pin when the CCLK frequency exceeds this maximum specification.
3. Some Xilinx documents refer to Parallel modes as "SelectMAP" modes.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/01/05	1.0	Initial Xilinx release.
11/23/05	2.0	Added AC timing information and additional DC specifications.
03/22/06	3.0	Upgraded data sheet status to Preliminary. Finalized production timing parameters. All speed grades for all Spartan-3E FPGAs are now Production status using the v1.21 speed files, as shown in Table 84. Expanded description in Note 2, Table 78. Updated pin-to-pin and clock-to-output timing based on final characterization, shown in Table 86. Updated system-synchronous input setup and hold times based on final characterization, shown in Table 87 and Table 88. Updated other I/O timing in Table 90. Provided input and output adjustments for LVPECL_25, DIFF_SSTL and DIFF_HSTL I/O standards that supersede the v1.21 speed file values, in Table 91 and Table 94. Reduced I/O three-state and set/reset delays in Table 93. Added XC3S100E FPGA in CP132 package to Table 96. Increased T_{AS} slice flip-flop timing by 100 ps in Table 98. Updated distributed RAM timing in Table 99 and SRL16 timing in Table 100. Updated global clock timing, removed left/right clock buffer limits in Table 101. Updated block RAM timing in Table 103. Added DCM parameters for remainder of Step 0 device; added improved Step 1 DCM performance to Table 104, Table 105, Table 106, and Table 107. Added minimum INIT_B pulse width specification, T_{INIT}, in Table 111. Increased data hold time for Slave Parallel mode to 1.0 ns (T_{SMCCD}) in Table 117. Improved the DCM performance for the XC3S1200E, Stepping 0 in Table 104, Table 105, Table 106, and Table 107. Corrected links in Table 118 and Table 120. Added MultiBoot timing specifications to Table 122.
04/07/06	3.1	Improved SSO limits for LVDS_25, MINI_LVDS_25, and RSDS_25 I/O standards in the QFP packages (Table 97). Removed potentially confusing Note 2 from Table 78.
05/19/06	3.2	Clarified that 100 mV of hysteresis applies to LVCMOS33 and LVCMOS25 I/O standards (Note 4, Table 80). Other minor edits.
05/30/06	3.2.1	Corrected various typos and incorrect links.
11/09/06	3.4	Improved absolute maximum voltage specifications in Table 73, providing additional overshoot allowance. Widened the recommended voltage range for PCI and PCI-X standards in Table 80. Clarified Note 2, Table 83. Improved various timing specifications for v1.26 speed file. Added Table 85 to summarize the history of speed file releases after which time all devices became Production status. Added absolute minimum values for Table 86, Table 92, and Table 93. Updated pin-to-pin setup and hold timing based on default IFD_DELAY_VALUE settings in Table 87, Table 88, and Table 90. Added Table 89 about source-synchronous input capture sample window. Promoted Module 3 to Production status. Synchronized all modules to v3.4.
03/16/07	3.5	Based on extensive 90 nm production data, improved (reduced) the maximum quiescent current limits for the I_{CCINTQ}, I_{CCAUXQ}, and I_{CCOQ} specifications in Table 79 by an average of 50%.
05/29/07	3.6	Added note to Table 74 and Table 75 regarding HSWAP in step 0 devices. Updated t_{RPW_CLB} in Table 98 to match value in speed file. Improved CLKOUT_FREQ_CLK90 to 200 MHz for Stepping 1 in Table 105.
04/18/08	3.7	Clarified that Stepping 0 was offered only for -4C and removed Stepping 0 -5 specifications. Added reference to XAPP459 in Table 73 and Table 77. Improved recommended max V_{CCO} to 3.465V (3.3V + 5%) in Table 77. Removed minimum input capacitance from Table 78. Updated Recommended Operating Conditions for LVCMOS and PCI I/O standards in Table 80. Removed Absolute Minimums from Table 86, Table 92 and Table 93 and added footnote recommending use of Timing Analyzer for minimum values. Updated T_{PSFD} and T_{PHFD} in Table 87 to match current speed file. Update T_{RPW_IOB} in Table 88 to match current speed file and CLB equivalent spec. Added XC3S500E VQG100 to Table 96. Replaced $T_{MULCKID}$ with T_{MSCKD} for A, B, and P registers in Table 102. Updated CLKOUT_PER_JITT_FX in Table 107. Updated MAX_STEPS equation in Table 109. Updated Figure 77 and Table 120 to correct CCLK active edge. Updated links.

Spartan-3 FPGA Family: Pinout Descriptions

DS312 (4.0) October 29, 2012 **Product Specification**

Introduction

This section describes the various pins on a Spartan®-3E FPGA and how they connect within the supported component packages.

Pin Types

Most pins on a Spartan-3E FPGA are general-purpose, user-defined I/O pins. There are, however, up to 11 different functional types of pins on Spartan-3E packages, as outlined in Table 124. In the package footprint drawings that follow, the individual pins are color-coded according to pin type as in the table.

Table 124: **Types of Pins on Spartan-3E FPGAs**

Type / Color Code	Description	Pin Name(s) in Type[1]
I/O	Unrestricted, general-purpose user-I/O pin. Most pins can be paired together to form differential I/Os.	IO IO_Lxxy_#
INPUT	Unrestricted, general-purpose input-only pin. This pin does not have an output structure, differential termination resistor, or PCI clamp diode.	IP IP_Lxxy_#
DUAL	Dual-purpose pin used in some configuration modes during the configuration process and then usually available as a user I/O after configuration. If the pin is not used during configuration, this pin behaves as an I/O-type pin. Some of the dual-purpose pins are also shared with bottom-edge global (GCLK) or right-half (RHCLK) clock inputs. See the Configuration section in Module 2 for additional information on these signals.	M[2:0] HSWAP CCLK MOSI/CSI_B D[7:1] D0/DIN CSO_B RDWR_B BUSY/DOUT INIT_B A[23:20] A19/VS2 A18/VS1 A17/VS0 A[16:0] LDC[2:0] HDC
VREF	Dual-purpose pin that is either a user-I/O pin or Input-only pin, or, along with all other VREF pins in the same bank, provides a reference voltage input for certain I/O standards. If used for a reference voltage within a bank, all VREF pins within the bank must be connected.	IP/VREF_# IP_Lxxy_#/VREF_# IO/VREF_# IO_Lxxy_#/VREF_#
CLK	Either a user-I/O pin or Input-only pin, or an input to a specific clock buffer driver. Every package has 16 global clock inputs that optionally clock the entire device. The RHCLK inputs optionally clock the right-half of the device. The LHCLK inputs optionally clock the left-half of the device. Some of the clock pins are shared with the dual-purpose configuration pins and are considered DUAL-type. See the Clocking Infrastructure section in Module 2 for additional information on these signals.	IO_Lxxy_#/GCLK[15:10, 7:2] IP_Lxxy_#/GCLK[9:8, 1:0] IO_Lxxy_#/LHCLK[7:0] IO_Lxxy_#/RHCLK[7:0]
CONFIG	Dedicated configuration pin. Not available as a user-I/O pin. Every package has two dedicated configuration pins. These pins are powered by VCCAUX. See the Configuration section in Module 2 for details.	DONE, PROG_B
JTAG	Dedicated JTAG pin. Not available as a user-I/O pin. Every package has four dedicated JTAG pins. These pins are powered by VCCAUX.	TDI, TMS, TCK, TDO
GND	Dedicated ground pin. The number of GND pins depends on the package used. All must be connected.	GND

Package Overview

Table 125 shows the eight low-cost, space-saving production package styles for the Spartan-3E family. Each package style is available as a standard and an environmentally friendly lead-free (Pb-free) option. The Pb-free packages include an extra 'G' in the package style name. For example, the standard "VQ100" package becomes "VQG100" when ordered as the Pb-free option. The mechanical dimensions of the standard and Pb-free packages are similar, as shown in the mechanical drawings provided in Table 127.

Not all Spartan-3E densities are available in all packages. For a specific package, however, there is a common footprint that supports all the devices available in that package. See the footprint diagrams that follow.

For additional package information, see UG112: *Device Package User Guide*.

Table 125: **Spartan-3E Family Package Options**

Package	Leads	Type	Maximum I/O	Lead Pitch (mm)	Footprint Area (mm)	Height (mm)	Mass[1] (g)
VQ100 / VQG100	100	Very-thin Quad Flat Pack (VQFP)	66	0.5	16 x 16	1.20	0.6
CP132 / CPG132	132	Chip-Scale Package (CSP)	92	0.5	8.1 x 8.1	1.10	0.1
TQ144 / TQG144	144	Thin Quad Flat Pack (TQFP)	108	0.5	22 x 22	1.60	1.4
PQ208 / PQG208	208	Plastic Quad Flat Pack (PQFP)	158	0.5	30.6 x 30.6	4.10	5.3
FT256 / FTG256	256	Fine-pitch, Thin Ball Grid Array (FBGA)	190	1.0	17 x 17	1.55	0.9
FG320 / FGG320	320	Fine-pitch Ball Grid Array (FBGA)	250	1.0	19 x 19	2.00	1.4
FG400 / FGG400	400	Fine-pitch Ball Grid Array (FBGA)	304	1.0	21 x 21	2.43	2.2
FG484 / FGG484	484	Fine-pitch Ball Grid Array (FBGA)	376	1.0	23 x 23	2.60	2.2

Notes:

1. Package mass is ±10%.

Selecting the Right Package Option

Spartan-3E FPGAs are available in both quad-flat pack (QFP) and ball grid array (BGA) packaging options. While QFP packaging offers the lowest absolute cost, the BGA packages are superior in almost every other aspect, as summarized in Table 126. Consequently, Xilinx recommends using BGA packaging whenever possible.

Table 126: **QFP and BGA Comparison**

Characteristic	Quad Flat Pack (QFP)	Ball Grid Array (BGA)
Maximum User I/O	158	376
Packing Density (Logic/Area)	Good	Better
Signal Integrity	Fair	Better
Simultaneous Switching Output (SSO) Support	Fair	Better
Thermal Dissipation	Fair	Better
Minimum Printed Circuit Board (PCB) Layers	4	4-6
Hand Assembly/Rework	Possible	Difficult

Table 129: **Maximum User I/O by Package**

Device	Package	Maximum User I/Os and Input-Only	Maximum Input-Only	Maximum Differential Pairs	All Possible I/Os by Type					
					I/O	INPUT	DUAL	VREF[1]	CLK[2]	N.C.
XC3S100E	VQ100	66	7	30	16	1	21	4	24	0
XC3S250E		66	7	30	16	1	21	4	24	0
XC3S500E		66	7	30	16	1	21	4	24	0
XC3S100E	CP132	83	11	35	16	2	42	7	16	9
XC3S250E		92	7	41	22	0	46	8	16	0
XC3S500E		92	7	41	22	0	46	8	16	0
XC3S100E	TQ144	108	28	40	22	19	42	9	16	0
XC3S250E		108	28	40	20	21	42	9	16	0
XC3S250E	PQ208	158	32	65	58	25	46	13	16	0
XC3S500E		158	32	65	58	25	46	13	16	0
XC3S250E	FT256	172	40	68	62	33	46	15	16	18
XC3S500E		190	41	77	76	33	46	19	16	0
XC3S1200E		190	40	77	78	31	46	19	16	0
XC3S500E	FG320	232	56	92	102	48	46	20	16	18
XC3S1200E		250	56	99	120	47	46	21	16	0
XC3S1600E		250	56	99	120	47	46	21	16	0
XC3S1200E	FG400	304	72	124	156	62	46	24	16	0
XC3S1600E		304	72	124	156	62	46	24	16	0
XC3S1600E	FG484	376	82	156	214	72	46	28	16	0

Notes:

1. Some VREF pins are on INPUT pins. See pinout tables for details.
2. All devices have 24 possible global clock and right- and left-half side clock inputs. The right-half and bottom-edge clock pins have shared functionality in some FPGA configuration modes. Consequently, some clock pins are counted in the DUAL column. 4 GCLK pins, including 2 DUAL pins, are on INPUT pins.

Electronic versions of the package pinout tables and footprints are available for download from the Xilinx website. Download the files from the following location:

http://www.xilinx.com/support/documentation/data_sheets/s3e_pin.zip

Using a spreadsheet program, the data can be sorted and reformatted according to any specific needs. Similarly, the ASCII-text file is easily parsed by most scripting programs.

Table 148: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S500E Pin Name	XC3S1200E Pin Name	XC3S1600E Pin Name	FG320 Ball	Type
GND	GND	GND	GND	K8	GND
GND	GND	GND	GND	K11	GND
GND	GND	GND	GND	K16	GND
GND	GND	GND	GND	L8	GND
GND	GND	GND	GND	L9	GND
GND	GND	GND	GND	L10	GND
GND	GND	GND	GND	L11	GND
GND	GND	GND	GND	M7	GND
GND	GND	GND	GND	M12	GND
GND	GND	GND	GND	T9	GND
GND	GND	GND	GND	U2	GND
GND	GND	GND	GND	U17	GND
GND	GND	GND	GND	V1	GND
GND	GND	GND	GND	V18	GND
VCCAUX	DONE	DONE	DONE	V17	CONFIG
VCCAUX	PROG_B	PROG_B	PROG_B	B1	CONFIG
VCCAUX	TCK	TCK	TCK	A17	JTAG
VCCAUX	TDI	TDI	TDI	A2	JTAG
VCCAUX	TDO	TDO	TDO	C16	JTAG
VCCAUX	TMS	TMS	TMS	D15	JTAG
VCCAUX	VCCAUX	VCCAUX	VCCAUX	B7	VCCAUX
VCCAUX	VCCAUX	VCCAUX	VCCAUX	B12	VCCAUX
VCCAUX	VCCAUX	VCCAUX	VCCAUX	G2	VCCAUX
VCCAUX	VCCAUX	VCCAUX	VCCAUX	G17	VCCAUX
VCCAUX	VCCAUX	VCCAUX	VCCAUX	M2	VCCAUX
VCCAUX	VCCAUX	VCCAUX	VCCAUX	M17	VCCAUX
VCCAUX	VCCAUX	VCCAUX	VCCAUX	U7	VCCAUX
VCCAUX	VCCAUX	VCCAUX	VCCAUX	U12	VCCAUX
VCCINT	VCCINT	VCCINT	VCCINT	E5	VCCINT
VCCINT	VCCINT	VCCINT	VCCINT	E14	VCCINT
VCCINT	VCCINT	VCCINT	VCCINT	F6	VCCINT
VCCINT	VCCINT	VCCINT	VCCINT	F13	VCCINT
VCCINT	VCCINT	VCCINT	VCCINT	N6	VCCINT
VCCINT	VCCINT	VCCINT	VCCINT	N13	VCCINT
VCCINT	VCCINT	VCCINT	VCCINT	P5	VCCINT
VCCINT	VCCINT	VCCINT	VCCINT	P14	VCCINT

User I/Os by Bank

Table 149 and Table 150 indicate how the available user-I/O pins are distributed between the four I/O banks on the FG320 package.

Table 149: **User I/Os Per Bank for XC3S500E in the FG320 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF(1)	CLK(2)
Top	0	58	29	14	1	6	8
Right	1	58	22	10	21	5	0(2)
Bottom	2	58	17	13	24	4	0(2)
Left	3	58	34	11	0	5	8
TOTAL		**232**	**102**	**48**	**46**	**20**	**16**

Notes:

1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

Table 150: **User I/Os Per Bank for XC3S1200E and XC3S1600E in the FG320 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF(1)	CLK(2)
Top	0	61	34	12	1	6	8
Right	1	63	25	12	21	5	0(2)
Bottom	2	63	23	11	24	5	0(2)
Left	3	63	38	12	0	5	8
TOTAL		**250**	**120**	**47**	**46**	**21**	**16**

Notes:

1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.