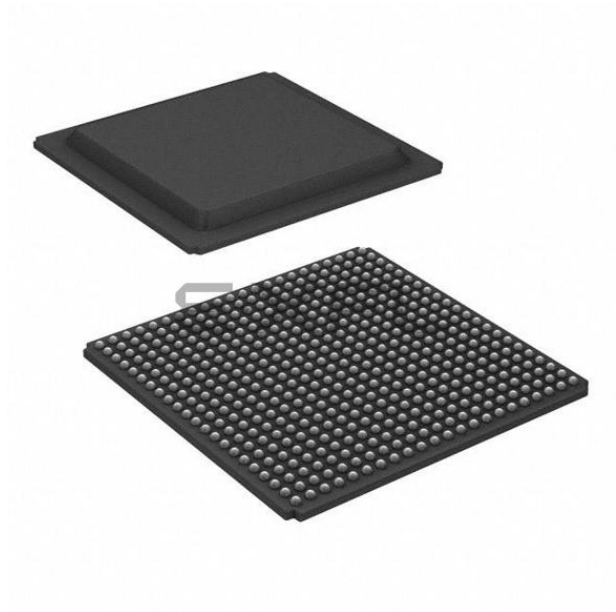
AMD Xilinx - XC3S1600E-4FG484C Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	3688
Number of Logic Elements/Cells	33192
Total RAM Bits	663552
Number of I/O	376
Number of Gates	1600000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s1600e-4fg484c

Configurable Logic Block (CLB) and Slice Resources

For additional information, refer to the “Using Configurable Logic Blocks (CLBs)” chapter in UG331.

CLB Overview

The Configurable Logic Blocks (CLBs) constitute the main logic resource for implementing synchronous as well as combinatorial circuits. Each CLB contains four slices, and each slice contains two Look-Up Tables (LUTs) to implement logic and two dedicated storage elements that can be used as flip-flops or latches. The LUTs can be used as a 16x1 memory (RAM16) or as a 16-bit shift register (SRL16), and additional multiplexers and carry logic simplify wide logic and arithmetic functions. Most general-purpose logic in a design is automatically mapped to the slice resources in the CLBs. Each CLB is identical, and the Spartan-3E family CLB structure is identical to that for the Spartan-3 family.

CLB Array

The CLBs are arranged in a regular array of rows and columns as shown in Figure 14.

Each density varies by the number of rows and columns of CLBs (see Table 9).

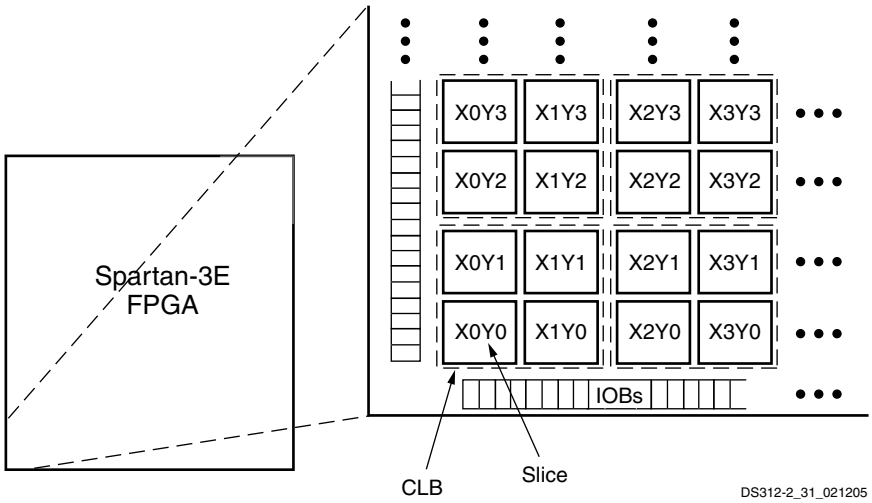

Figure 14: **CLB Locations**

Table 9: **Spartan-3E CLB Resources**

Device	CLB Rows	CLB Columns	CLB Total(1)	Slices	LUTs / Flip-Flops	Equivalent Logic Cells	RAM16 / SRL16	Distributed RAM Bits
XC3S100E	22	16	240	960	1,920	2,160	960	15,360
XC3S250E	34	26	612	2,448	4,896	5,508	2,448	39,168
XC3S500E	46	34	1,164	4,656	9,312	10,476	4,656	74,496
XC3S1200E	60	46	2,168	8,672	17,344	19,512	8,672	138,752
XC3S1600E	76	58	3,688	14,752	29,504	33,192	14,752	236,032

Notes:

1. The number of CLBs is less than the multiple of the rows and columns because the block RAM/multiplier blocks and the DCMs are embedded in the array (see Figure 1 in Module 1).

Slices

Each CLB comprises four interconnected slices, as shown in Figure 16. These slices are grouped in pairs. Each pair is organized as a column with an independent carry chain. The left pair supports both logic and memory functions and its slices are called SLICEM. The right pair supports logic only and its slices are called SLICEL. Therefore half the LUTs support both logic and memory (including both RAM16 and SRL16 shift registers) while half support logic only, and the two types alternate throughout the array columns. The SLICEL reduces the size of the CLB and lowers the cost of the device, and can also provide a performance advantage over the SLICEM.

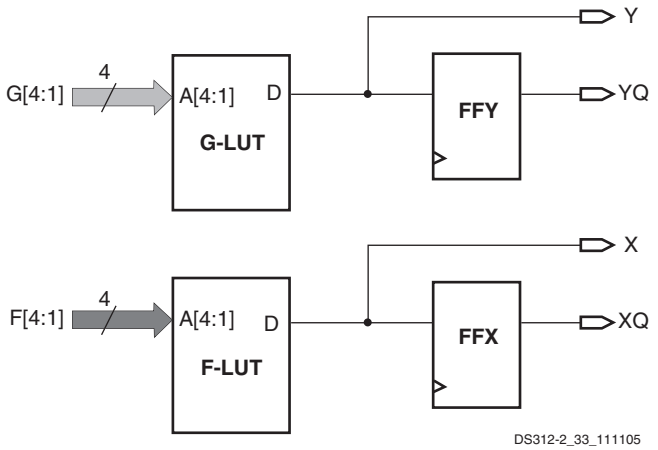

Figure 18: **LUT Resources in a Slice**

Wide Multiplexers

For additional information, refer to the “Using Dedicated Multiplexers” chapter in UG331.

Wide-function multiplexers effectively combine LUTs in order to permit more complex logic operations. Each slice has two of these multiplexers with F5MUX in the bottom portion of the slice and FiMUX in the top portion. The F5MUX multiplexes the two LUTs in a slice. The FiMUX multiplexes two CLB inputs which connect directly to the F5MUX and FiMUX results from the same slice or from other slices. See Figure 19.

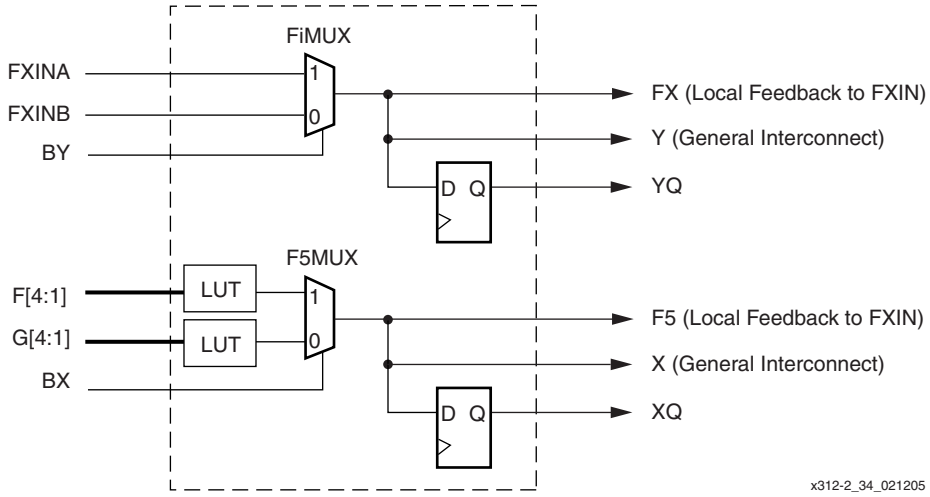

Figure 19: **Dedicated Multiplexers in Spartan-3E CLB**

Depending on the slice, FiMUX takes on the name F6MUX, F7MUX, or F8MUX. The designation indicates the number of inputs possible without restriction on the function. For example, an F7MUX can generate any function of seven inputs. Figure 20 shows the names of the multiplexers in each position in the Spartan-3E CLB. The figure also includes the direct connections within the CLB, along with the F7MUX connection to the CLB below.

Each mux can create logic functions of more inputs than indicated by its name. The F5MUX, for example, can generate any function of five inputs, with four inputs duplicated to two LUTs and the fifth input controlling the mux. Because each LUT can implement independent 2:1 muxes, the F5MUX can combine them to create a 4:1 mux, which is a six-input function. If the two LUTs have completely independent sets of inputs, some functions of all nine inputs can be implemented. Table 11 shows the connections for each multiplexer and the number of inputs possible for different types of functions.

Block RAM

For additional information, refer to the “Using Block RAM” chapter in UG331.

Spartan-3E devices incorporate 4 to 36 dedicated block RAMs, which are organized as dual-port configurable 18 Kbit blocks. Functionally, the block RAM is identical to the Spartan-3 architecture block RAM. Block RAM synchronously stores large amounts of data while distributed RAM, previously described, is better suited for buffering small amounts of data anywhere along signal paths. This section describes basic block RAM functions.

Each block RAM is configurable by setting the content’s initial values, default signal value of the output registers, port aspect ratios, and write modes. Block RAM can be used in single-port or dual-port modes.

Arrangement of RAM Blocks on Die

The block RAMs are located together with the multipliers on the die in one or two columns depending on the size of the device. The XC3S100E has one column of block RAM. The Spartan-3E devices ranging from the XC3S250E to XC3S1600E have two columns of block RAM. Table 21 shows the number of RAM blocks, the data storage capacity, and the number of columns for each device. Row(s) of CLBs are located above and below each block RAM column.

Table 21: **Number of RAM Blocks by Device**

Device	Total Number of RAM Blocks	Total Addressable Locations (bits)	Number of Columns
XC3S100E	4	73,728	1
XC3S250E	12	221,184	2
XC3S500E	20	368,640	2
XC3S1200E	28	516,096	2
XC3S1600E	36	663,552	2

Immediately adjacent to each block RAM is an embedded 18x18 hardware multiplier. The upper 16 bits of the block RAM's Port A Data input bus are shared with the upper 16 bits of the A multiplicand input bus of the multiplier. Similarly, the upper 16 bits of Port B's data input bus are shared with the B multiplicand input bus of the multiplier.

The Internal Structure of the Block RAM

The block RAM has a dual port structure. The two identical data ports called A and B permit independent access to the common block RAM, which has a maximum capacity of 18,432 bits, or 16,384 bits with no parity bits (see parity bits description in Table 22). Each port has its own dedicated set of data, control, and clock lines for synchronous read and write operations. There are four basic data paths, as shown in Figure 30:

1. Write to and read from Port A
2. Write to and read from Port B
3. Data transfer from Port A to Port B
4. Data transfer from Port B to Port A

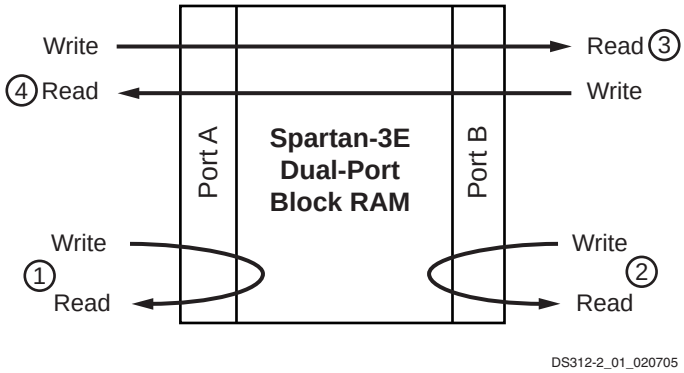

Figure 30: **Block RAM Data Paths**

Number of Ports

A choice among primitives determines whether the block RAM functions as dual- or single-port memory. A name of the form RAMB16_S[w_A]_S[w_B] calls out the dual-port primitive, where the integers w_A and w_B specify the total data path width at ports A and B, respectively. Thus, a RAMB16_S9_S18 is a dual-port RAM with a 9-bit Port A and an 18-bit Port B. A name of the form RAMB16_S[w] identifies the single-port primitive, where the integer w specifies the total data path width of the lone port A. A RAMB16_S18 is a single-port RAM with an 18-bit port.

Port Aspect Ratios

Each port of the block RAM can be configured independently to select a number of different possible widths for the data input (DI) and data output (DO) signals as shown in Table 22.

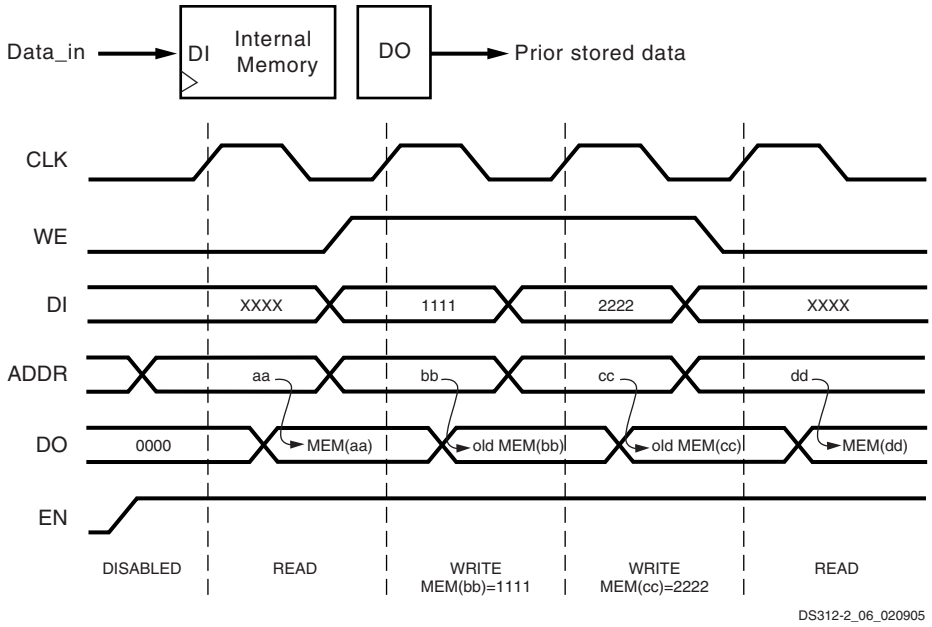

Figure 34: **Waveforms of Block RAM Data Operations with READ_FIRST Selected**

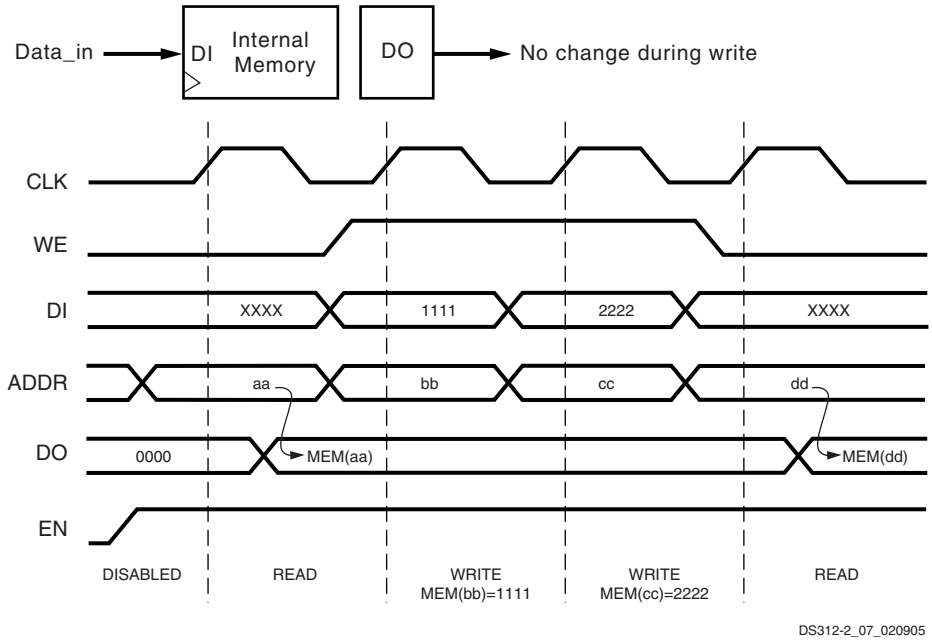

Figure 35: **Waveforms of Block RAM Data Operations with NO_CHANGE Selected**

Setting the WRITE_MODE attribute to a value of NO_CHANGE, puts the DO outputs in a latched state when asserting WE. Under this condition, the DO outputs retain the data driven just before WE is asserted. NO_CHANGE timing is shown in the portion of Figure 35 during which WE is High.

Interconnect

For additional information, refer to the “Using Interconnect” chapter in UG331.

Interconnect is the programmable network of signal pathways between the inputs and outputs of functional elements within the FPGA, such as IOBs, CLBs, DCMs, and block RAM.

Overview

Interconnect, also called routing, is segmented for optimal connectivity. Functionally, interconnect resources are identical to that of the Spartan-3 architecture. There are four kinds of interconnects: long lines, hex lines, double lines, and direct lines. The Xilinx Place and Route (PAR) software exploits the rich interconnect array to deliver optimal system performance and the fastest compile times.

Switch Matrix

The switch matrix connects to the different kinds of interconnects across the device. An interconnect tile, shown in Figure 48, is defined as a single switch matrix connected to a functional element, such as a CLB, IOB, or DCM. If a functional element spans across multiple switch matrices such as the block RAM or multipliers, then an interconnect tile is defined by the number of switch matrices connected to that functional element. A Spartan-3E device can be represented as an array of interconnect tiles where interconnect resources are for the channel between any two adjacent interconnect tile rows or columns as shown in Figure 49.

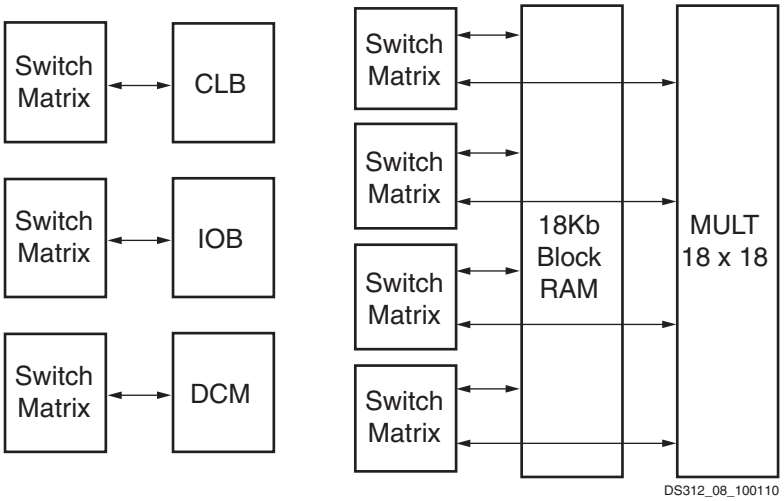

Figure 48: **Four Types of Interconnect Tiles (CLBs, IOBs, DCMs, and Block RAM/Multiplier)**

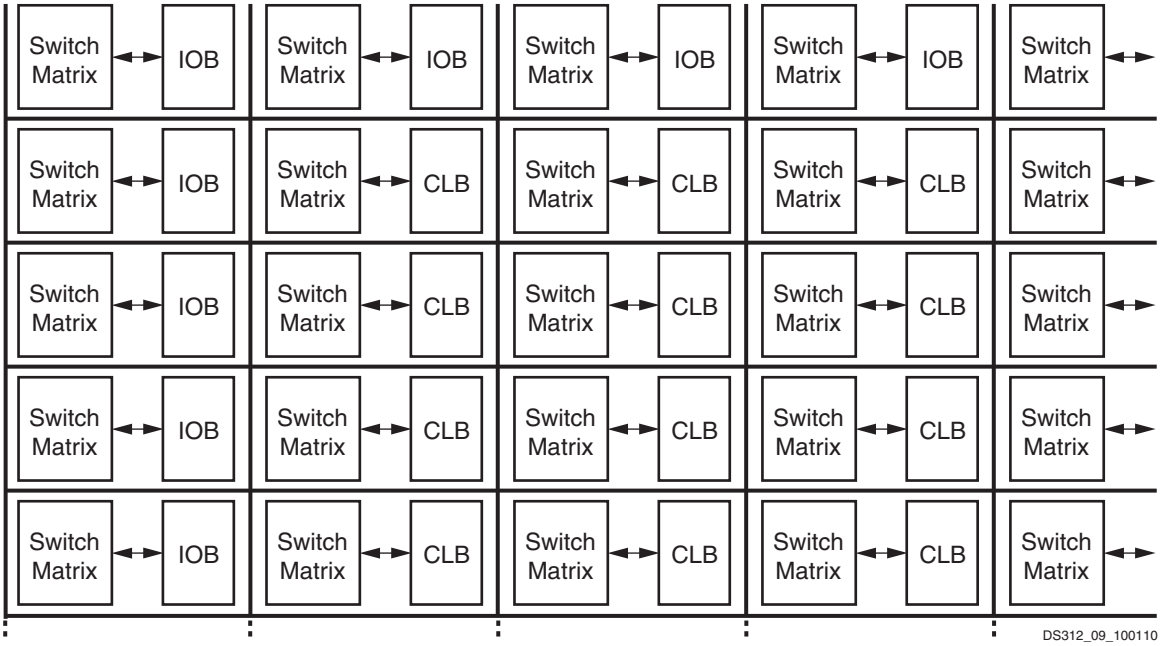

Figure 49: **Array of Interconnect Tiles in Spartan-3E FPGA**

SPI Serial Flash Mode

For additional information, refer to the “Master SPI Mode” chapter in UG332.

In SPI Serial Flash mode (M[2:0] = <0:0:1>), the Spartan-3E FPGA configures itself from an attached industry-standard SPI serial Flash PROM, as illustrated in Figure 53 and Figure 54. The FPGA supplies the CCLK output clock from its internal oscillator to the clock input of the attached SPI Flash PROM.

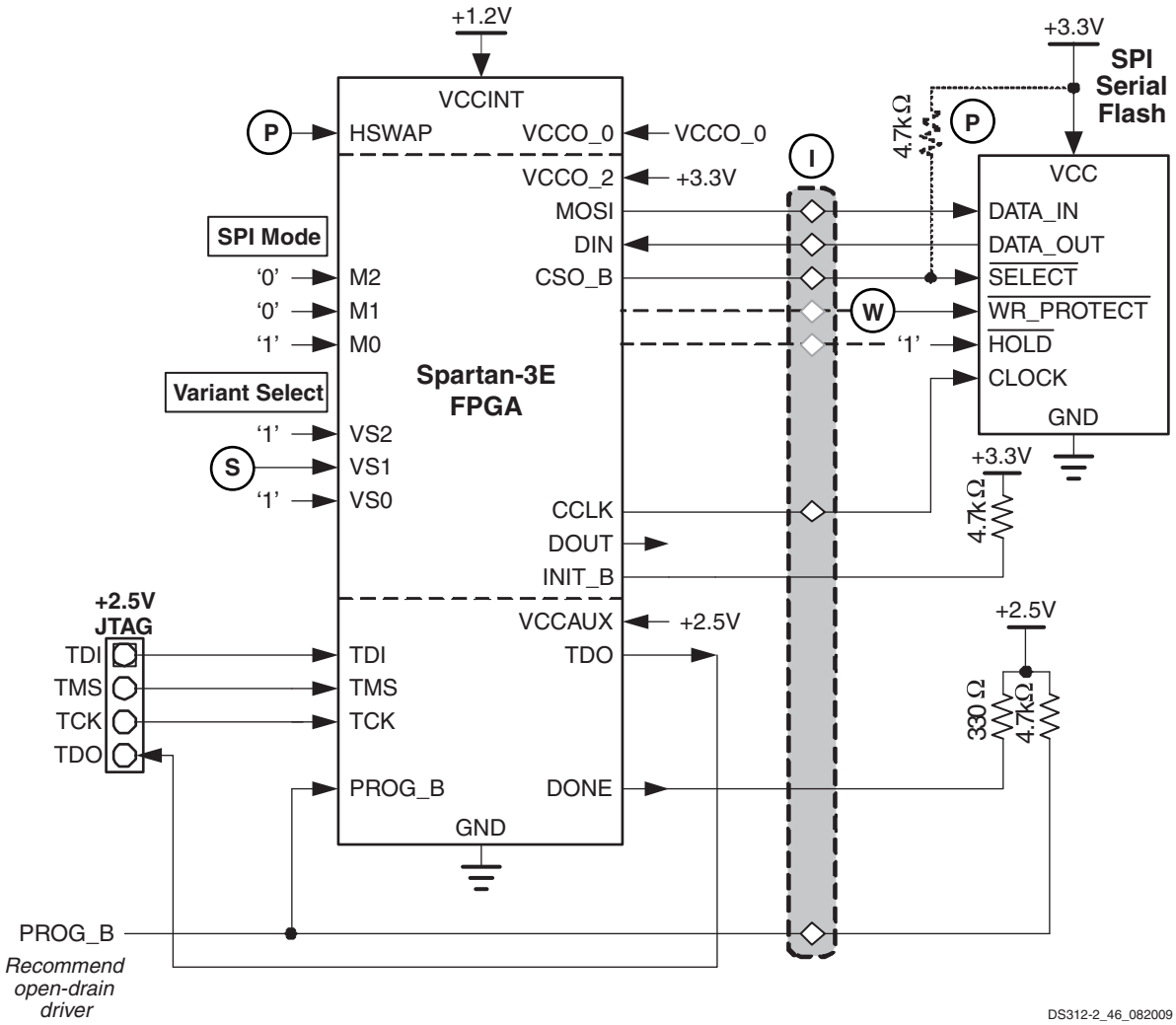

Figure 53: **SPI Flash PROM Interface for PROMs Supporting READ (0x03) and FAST_READ (0x0B) Commands**

S Although SPI is a standard four-wire interface, various available SPI Flash PROMs use different command protocols. The FPGA’s variant select pins, VS[2:0], define how the FPGA communicates with the SPI Flash, including which SPI Flash command the FPGA issues to start the read operation and the number of dummy bytes inserted before the FPGA expects to receive valid data from the SPI Flash. Table 53 shows the available SPI Flash PROMs expected to operate with Spartan-3E FPGAs. Other compatible devices might work but have not been tested for suitability with Spartan-3E FPGAs. All other VS[2:0] values are reserved for future use. Consult the data sheet for the desired SPI Flash device to determine its suitability. The basic timing requirements and waveforms are provided in Serial Peripheral Interface (SPI) Configuration Timing in Module 3.

Figure 53 shows the general connection diagram for those SPI Flash PROMs that support the 0x03 READ command or the 0x0B FAST READ commands.

Figure 54 shows the connection diagram for Atmel DataFlash serial PROMs, which also use an SPI-based protocol. ‘B’-series DataFlash devices are limited to FPGA applications operating over the commercial temperature range. Industrial temperature range applications must use ‘C’- or ‘D’-series DataFlash devices, which have a shorter DataFlash select setup time, because of the faster FPGA CCLK frequency at cold temperatures.

read operations at this time. Spartan-3E FPGAs issue the read command just once. If the SPI Flash is not ready, then the FPGA does not properly configure.

If the 3.3V supply is last in the sequence and does not ramp fast enough, or if the SPI Flash PROM cannot be ready when required by the FPGA, delay the FPGA configuration process by holding either the FPGA's PROG_B input or INIT_B input Low, as highlighted in Figure 54. Release the FPGA when the SPI Flash PROM is ready. For example, a simple R-C delay circuit attached to the INIT_B pin forces the FPGA to wait for a preselected amount of time. Alternately, a Power Good signal from the 3.3V supply or a system reset signal accomplishes the same purpose. Use an open-drain or open-collector output when driving PROG_B or INIT_B.

SPI Flash PROM Density Requirements

Table 57 shows the smallest usable SPI Flash PROM to program a single Spartan-3E FPGA. Commercially available SPI Flash PROMs range in density from 1 Mbit to 128 Mbits. A multiple-FPGA daisy-chained application requires a SPI Flash PROM large enough to contain the sum of the FPGA file sizes. An application can also use a larger-density SPI Flash PROM to hold additional data beyond just FPGA configuration data. For example, the SPI Flash PROM can also store application code for a MicroBlaze™ RISC processor core integrated in the Spartan-3E FPGA. See Using the SPI Flash Interface after Configuration.

Table 57: **Number of Bits to Program a Spartan-3E FPGA and Smallest SPI Flash PROM**

Device	Number of Configuration Bits	Smallest Usable SPI Flash PROM
XC3S100E	581,344	1 Mbit
XC3S250E	1,353,728	2 Mbit
XC3S500E	2,270,208	4 Mbit
XC3S1200E	3,841,184	4 Mbit
XC3S1600E	5,969,696	8 Mbit

CCLK Frequency

In SPI Flash mode, the FPGA's internal oscillator generates the configuration clock frequency. The FPGA provides this clock on its CCLK output pin, driving the PROM's clock input pin. The FPGA starts configuration at its lowest frequency and increases its frequency for the remainder of the configuration process if so specified in the configuration bitstream. The maximum frequency is specified using the ***ConfigRate*** bitstream generator option. The maximum frequency supported by the FPGA configuration logic depends on the timing for the SPI Flash device. Without examining the timing for a specific SPI Flash PROM, use ***ConfigRate*** = 12 or lower. SPI Flash PROMs that support the FAST READ command support higher data rates. Some such PROMs support up to ***ConfigRate*** = 25 and beyond but require careful data sheet analysis. See Serial Peripheral Interface (SPI) Configuration Timing for more detailed timing analysis.

Using the SPI Flash Interface after Configuration

After the FPGA successfully completes configuration, all of the pins connected to the SPI Flash PROM are available as user-I/O pins.

If not using the SPI Flash PROM after configuration, drive CSO_B High to disable the PROM. The MOSI, DIN, and CCLK pins are then available to the FPGA application.

Because all the interface pins are user I/O after configuration, the FPGA application can continue to use the SPI Flash interface pins to communicate with the SPI Flash PROM, as shown in Figure 56. SPI Flash PROMs offer random-accessible, byte-addressable, read/write, non-volatile storage to the FPGA application.

SPI Flash PROMs are available in densities ranging from 1 Mbit up to 128 Mbits. However, a single Spartan-3E FPGA requires less than 6 Mbits. If desired, use a larger SPI Flash PROM to contain additional non-volatile application data, such as MicroBlaze processor code, or other user data such as serial numbers and Ethernet MAC IDs. In the example shown in Figure 56, the FPGA configures from SPI Flash PROM. Then using FPGA logic after configuration, the FPGA copies MicroBlaze code from SPI Flash into external DDR SDRAM for code execution. Similarly, the FPGA application can store non-volatile application data within the SPI Flash PROM.

The FPGA configuration data is stored starting at location 0. Store any additional data beginning in the next available SPI Flash PROM sector or page. Do not mix configuration data and user data in the same sector or page.

Similarly, the SPI bus can be expanded to additional SPI peripherals. Because SPI is a common industry-standard interface, various SPI-based peripherals are available, such as analog-to-digital (A/D) converters, digital-to-analog (D/A) converters, CAN controllers, and temperature sensors. However, if sufficient I/O pins are available in the application, Xilinx recommends creating a separate SPI bus to control peripherals. Creating a second port reduces the loading on the CCLK and DIN pins, which are crucial for configuration.

The MOSI, DIN, and CCLK pins are common to all SPI peripherals. Connect the select input on each additional SPI peripheral to one of the FPGA user I/O pins. If HSWAP = 0 during configuration, the FPGA holds the select line High. If HSWAP = 1, connect the select line to +3.3V via an external 4.7 kΩ pull-up resistor to avoid spurious read or write operations. After configuration, drive the select line Low to select the desired SPI peripheral.

Table 65: **Slave Parallel Mode Connections *(Cont'd)***

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
INIT_B	Open-drain bidirectional I/O	**Initialization Indicator**. Active Low. Goes Low at the start of configuration during the Initialization memory clearing process. Released at the end of memory clearing, when mode select pins are sampled. In daisy-chain applications, this signal requires an external 4.7 kΩ pull-up resistor to VCCO_2.	Active during configuration. If CRC error detected during configuration, FPGA drives INIT_B Low.	User I/O. If unused in the application, drive INIT_B High.
DONE	Open-drain bidirectional I/O	**FPGA Configuration Done**. Low during configuration. Goes High when FPGA successfully completes configuration. Requires external 330 Ω pull-up resistor to 2.5V.	Low indicates that the FPGA is not yet configured.	Pulled High via external pull-up. When High, indicates that the FPGA successfully configured.
PROG_B	Input	**Program FPGA**. Active Low. When asserted Low for 500 ns or longer, forces the FPGA to restart its configuration process by clearing configuration memory and resetting the DONE and INIT_B pins once PROG_B returns High. Recommend external 4.7 kΩ pull-up resistor to 2.5V. Internal pull-up value may be weaker (see Table 78). If driving externally with a 3.3V output, use an open-drain or open-collector driver or use a current limiting series resistor.	Must be High to allow configuration to start.	Drive PROG_B Low and release to reprogram FPGA.

Voltage Compatibility

Ⓥ Most Slave Parallel interface signals are within the FPGA's I/O Bank 2, supplied by the VCCO_2 supply input. The VCCO_2 voltage can be 1.8V, 2.5V, or 3.3V to match the requirements of the external host, ideally 2.5V. Using 1.8V or 3.3V requires additional design considerations as the DONE and PROG_B pins are powered by the FPGA's 2.5V V_{CCAUX} supply. See XAPP453: *The 3.3V Configuration of Spartan-3 FPGAs* for additional information.

Daisy-Chaining

If the application requires multiple FPGAs with different configurations, then configure the FPGAs using a daisy chain. Use Slave Parallel mode (M[2:0] = <1:1:0>) for all FPGAs in the daisy-chain. The schematic in Figure 62 is optimized for FPGA downloading and does not support the SelectMAP read interface. The FPGA's RDWR_B pin must be Low during configuration.

After the lead FPGA is filled with its configuration data, the lead FPGA enables the next FPGA in the daisy-chain by asserting is chip-select output, CSO_B.

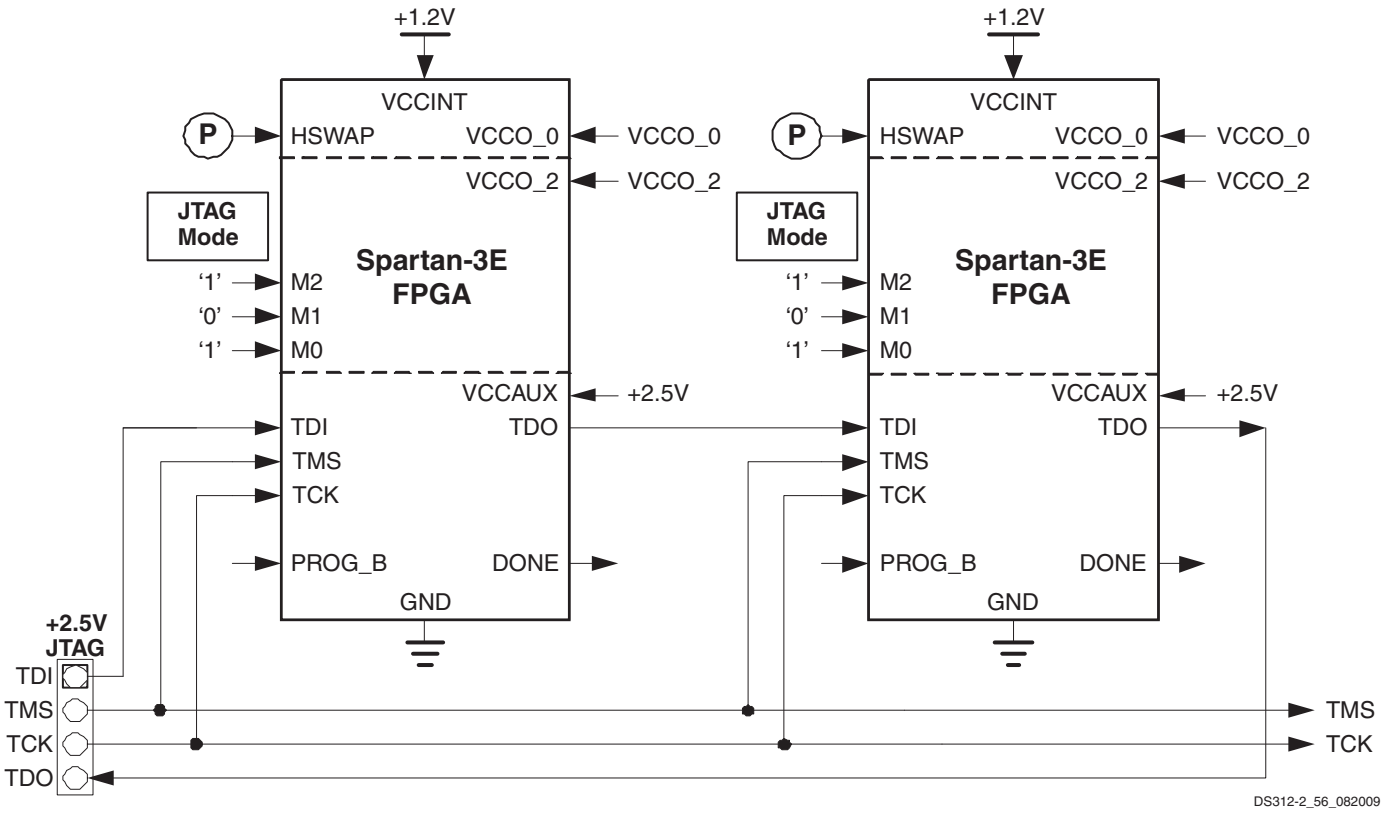

Figure 65: **JTAG Configuration Mode**

Voltage Compatibility

The 2.5V V_{CCAUX} supply powers the JTAG interface. All of the user I/Os are separately powered by their respective VCCO_# supplies.

When connecting the Spartan-3E JTAG port to a 3.3V interface, the JTAG input pins must be current-limited to 10 mA or less using series resistors. Similarly, the TDO pin is a CMOS output powered from +2.5V. The TDO output can directly drive a 3.3V input but with reduced noise immunity. See XAPP453: *The 3.3V Configuration of Spartan-3 FPGAs* for additional information.

Table 67: **Spartan-3E JTAG Device Identifiers**

Spartan-3E FPGA	4-Bit Revision Code		28-Bit Vendor/Device Identifier
	Step 0	Step 1	
XC3S100E	0x0	0x1	0x1C 10 093
XC3S250E	0x0	0x1	0x1C 1A 093
XC3S500E	0x0 0x2	0x4	0x1C 22 093
XC3S1200E	0x0 0x1	0x2	0x1C 2E 093
XC3S1600E	0x0 0x1	0x2	0x1C 3A 093

JTAG Device ID

Each Spartan-3E FPGA array type has a 32-bit device-specific JTAG device identifier as shown in Table 67. The lower 28 bits represent the device vendor (Xilinx) and device identifer. The upper four bits, ignored by most tools, represent the revision level of the silicon mounted on the printed circuit board. Table 67 associates the revision code with a specific stepping level.

JTAG User ID

The Spartan-3E JTAG interface also provides the option to store a 32-bit User ID, loaded during configuration. The User ID value is specified via the ***UserID*** configuration bitstream option, shown in Table 69, page 107.

Using JTAG Interface to Communicate to a Configured FPGA Design

After the FPGA is configured, using any of the available modes, the JTAG interface offers a possible communications channel to internal FPGA logic. The BSCAN_SPARTAN3 design primitive provides two private JTAG instructions to create an internal boundary scan chain.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/01/05	1.0	Initial Xilinx release.
03/21/05	1.1	Updated Figure 45. Modified title on Table 39 and Table 45.
11/23/05	2.0	Updated values of On-Chip Differential Termination resistors. Updated Table 7. Updated configuration bitstream sizes for XC3S250E through XC3S1600E in Table 45, Table 51, Table 57, and Table 60. Added DLL Performance Differences Between Steppings. Added Stepping 0 Limitations when Reprogramming via JTAG if FPGA Set for BPI Configuration. Added Stepping 0 limitations when Daisy-Chaining in SPI configuration mode. Added Multiplier/Block RAM Interaction section. Updated Digital Clock Managers (DCMs) section, especially Phase Shifter (PS) portion. Corrected and enhanced the clock infrastructure diagram in Figure 45 and Table 41. Added CCLK Design Considerations section. Added Design Considerations for the HSWAP, M[2:0], and VS[2:0] Pins section. Added Spansion, Winbond, and Macronix to list of SPI Flash vendors in Table 53 and Table 56. Clarified that SPI mode configuration supports Atmel 'C'- and 'D'-series DataFlash. Updated the Programming Support section for SPI Flash PROMs. Added Power-On Precautions if PROM Supply is Last in Sequence, Compatible Flash Families, and BPI Mode Interaction with Right and Bottom Edge Global Clock Inputs sections to BPI configuration mode topic. Updated and amplified Powering Spartan-3E FPGAs section. Added Production Stepping section.
03/22/06	3.0	Upgraded data sheet status to Preliminary. Updated Input Delay Functions and Figure 6. Added clarification that Input-only pins also have Pull-Up and Pull-Down Resistors. Added design note about address setup and hold requirements to Block RAM. Added warning message about software differences between ISE 8.1i, Service Pack 3 and earlier software to FIXED Phase Shift Mode and VARIABLE Phase Shift Mode. Added message about using GCLK1 in DLL Clock Input Connections and Clock Inputs. Updated Figure 45. Added additional information on HSWAP behavior to Pin Behavior During Configuration. Highlighted which pins have configuration pull-up resistors unaffected by HSWAP in Table 46. Updated bitstream image sizes for the XC3S1200E and XC3S1600E in Table 45, Table 51, Table 57, and Table 60. Clarified that 'B'-series Atmel DataFlash SPI PROMs can be used in Commercial temperature range applications in Table 53 and Figure 54. Updated Figure 56. Updated Dynamically Loading Multiple Configuration Images Using MultiBoot Option section. Added design note about BPI daisy-chaining software support to BPI Daisy-Chaining section. Updated JTAG revision codes in Table 67. Added No Internal Charge Pumps or Free-Running Oscillators. Updated information on production stepping differences in Table 71. Updated Software Version Requirements.
04/10/06	3.1	Updated JTAG User ID information. Clarified Note 1, Figure 5. Clarified that Figure 45 shows electrical connectivity and corrected left- and right-edge DCM coordinates. Updated Table 30, Table 31, and Table 32 to show the specific clock line driven by the associated BUFGMUX primitive. Corrected the coordinate locations for the associated BUFGMUX primitives in Table 31 and Table 32. Updated Table 41 to show that the I0-input is the preferred connection to a BUFGMUX.
05/19/06	3.2	Made further clarifying changes to Figure 46, showing both direct inputs to BUFGMUX primitives and to DCMs. Added Atmel AT45DBxxxD-series DataFlash serial PROMs to Table 53. Added details that intermediate FPGAs in a BPI-mode, multi-FPGA configuration daisy-chain must be from either the Spartan-3E or the Virtex-5 FPGA families (see BPI Daisy-Chaining). Added Using JTAG Interface to Communicate to a Configured FPGA Design. Minor updates to Figure 66 and Figure 67. Clarified which Spartan-3E FPGA product options support the Readback feature, shown in Table 68.
05/30/06	3.2.1	Corrected various typos and incorrect links.
10/02/06	3.3	Clarified that the block RAM Readback feature is available either on the -5 speed grade or the Industrial temperature range.
11/09/06	3.4	Updated the description of the Input Delay Functions. The ODDR2 flip-flop with C0 or C1 Alignment is no longer supported. Updated Figure 5. Updated Table 6 for improved PCI input voltage tolerance. Replaced missing text in Clock Buffers/Multiplexers. Updated SPI Flash devices in Table 53. Updated parallel NOR Flash devices in Table 61. Direct, SPI Flash in-system Programming Support was added beginning with ISE 8.1i iMPACT software for STMicro and Atmel SPI PROMs. Updated Table 71 and Table 72 as Stepping 1 is in full production. Freshened various hyper links. Promoted Module 2 to Production status.

Block RAM Timing

Table 103: **Block RAM Timing**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{BCKO}	When reading from block RAM, the delay from the active transition at the CLK input to data appearing at the DOUT output	-	2.45	-	2.82	ns
Setup Times						
T_{BACK}	Setup time for the ADDR inputs before the active transition at the CLK input of the block RAM	0.33	-	0.38	-	ns
T_{BDCK}	Setup time for data at the DIN inputs before the active transition at the CLK input of the block RAM	0.23	-	0.23	-	ns
T_{BECK}	Setup time for the EN input before the active transition at the CLK input of the block RAM	0.67	-	0.77	-	ns
T_{BWCK}	Setup time for the WE input before the active transition at the CLK input of the block RAM	1.09	-	1.26	-	ns
Hold Times						
T_{BCKA}	Hold time on the ADDR inputs after the active transition at the CLK input	0.12	-	0.14	-	ns
T_{BCKD}	Hold time on the DIN inputs after the active transition at the CLK input	0.12	-	0.13	-	ns
T_{BCKE}	Hold time on the EN input after the active transition at the CLK input	0	-	0	-	ns
T_{BCKW}	Hold time on the WE input after the active transition at the CLK input	0	-	0	-	ns
Clock Timing						
T_{BPWH}	High pulse width of the CLK signal	1.39	-	1.59	-	ns
T_{BPWL}	Low pulse width of the CLK signal	1.39	-	1.59	-	ns
Clock Frequency						
F_{BRAM}	Block RAM clock frequency. RAM read output value written back into RAM, for shift-registers and circular buffers. Write-only or read-only performance is faster.	0	270	0	230	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 77.

Phase Shifter (PS)

Table 108: **Recommended Operating Conditions for the PS in Variable Phase Mode**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Operating Frequency Ranges						
PSCLK_FREQ (F_{PSCLK})	Frequency for the PSCLK input	1	167	1	167	MHz
Input Pulse Requirements						
PSCLK_PULSE	PSCLK pulse width as a percentage of the PSCLK period	40%	60%	40%	60%	-

Table 109: **Switching Characteristics for the PS in Variable Phase Mode**

Symbol	Description	Equation		Units
Phase Shifting Range				
MAX_STEPS(2)	Maximum allowed number of DCM_DELAY_STEP steps for a given CLKIN clock period, where T = CLKIN clock period in ns. If using CLKIN_DIVIDE_BY_2 = TRUE, double the effective clock period.(3)	CLKIN < 60 MHz	±[INTEGER(10 • (T_{CLKIN} – 3 ns))]	steps
		CLKIN ≥ 60 MHz	±[INTEGER(15 • (T_{CLKIN} – 3 ns))]	steps
FINE_SHIFT_RANGE_MIN	Minimum guaranteed delay for variable phase shifting	±[MAX_STEPS • DCM_DELAY_STEP_MIN]		ns
FINE_SHIFT_RANGE_MAX	Maximum guaranteed delay for variable phase shifting	±[MAX_STEPS • DCM_DELAY_STEP_MAX]		ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 77 and Table 108.
2. The maximum variable phase shift range, MAX_STEPS, is only valid when the DCM is has no initial fixed phase shifting, i.e., the PHASE_SHIFT attribute is set to 0.
3. The DCM_DELAY_STEP values are provided at the bottom of Table 105.

Miscellaneous DCM Timing

Table 110: **Miscellaneous DCM Timing**

Symbol	Description	Min	Max	Units
DCM_RST_PW_MIN(1)	Minimum duration of a RST pulse width	3	-	CLKIN cycles
DCM_RST_PW_MAX(2)	Maximum duration of a RST pulse width	N/A	N/A	seconds
DCM_CONFIG_LAG_TIME(3)	Maximum duration from V_{CCINT} applied to FPGA configuration successfully completed (DONE pin goes High) and clocks applied to DCM DLL	N/A	N/A	minutes

Notes:

1. This limit only applies to applications that use the DCM DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV). The DCM DFS outputs (CLKFX, CLKFX180) are unaffected.
2. This specification is equivalent to the Virtex-4 DCM_RESET specfication.This specification does not apply for Spartan-3E FPGAs.
3. This specification is equivalent to the Virtex-4 TCONFIG specification. This specification does not apply for Spartan-3E FPGAs.

VQ100 Footprint

In Figure 80, note pin 1 indicator in top-left corner and logo orientation.

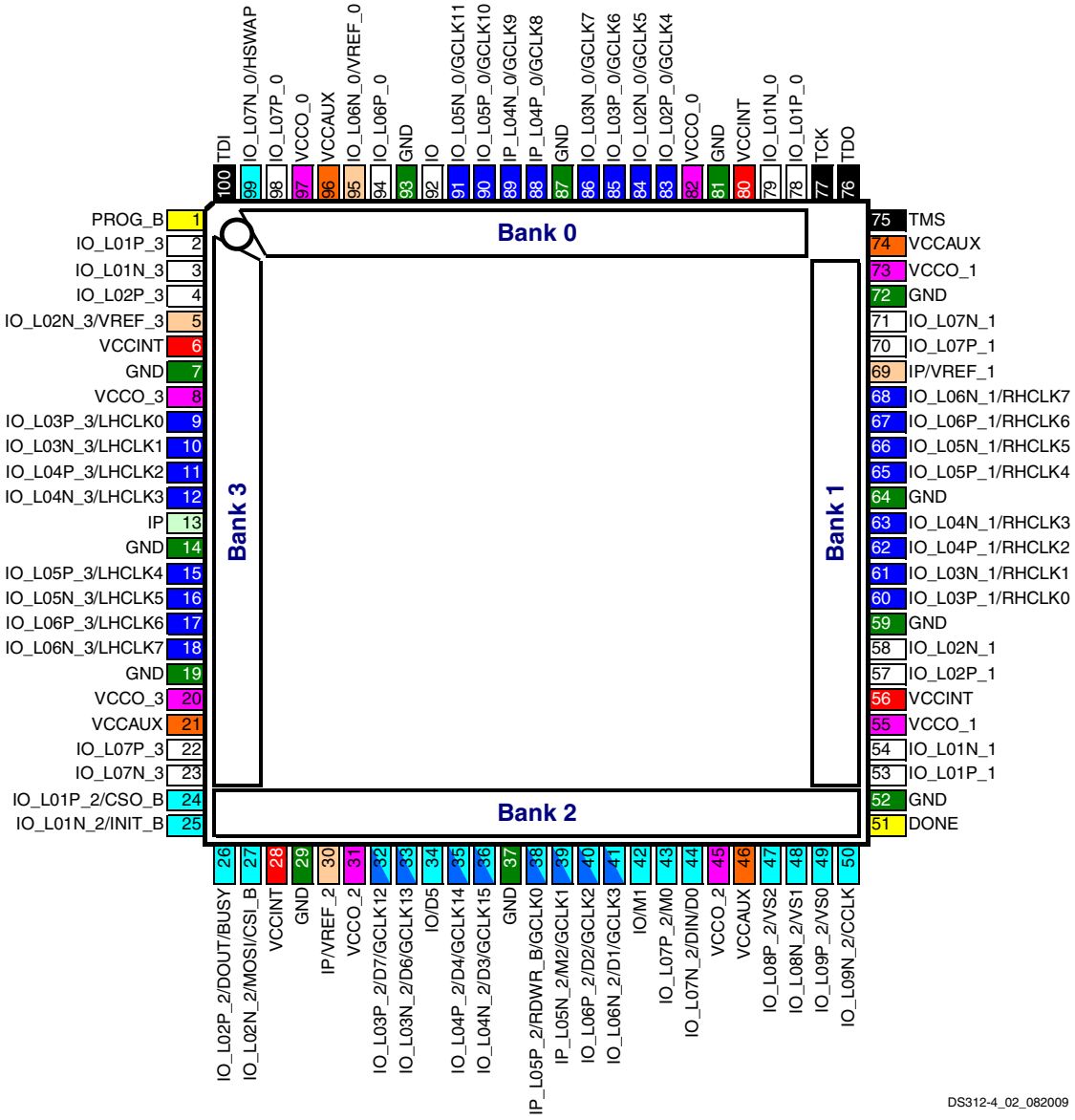

Figure 80: **VQ100 Package Footprint (top view)**

16	**I/O:** Unrestricted, general-purpose user I/O	21	**DUAL:** Configuration pin, then possible user-I/O	4	**VREF:** User I/O or input voltage reference for bank
1	**INPUT:** Unrestricted, general-purpose input pin	24	**CLK:** User I/O, input, or global buffer input	8	**VCCO:** Output voltage supply for bank
2	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	4	**VCCINT:** Internal core supply voltage (+1.2V)
0	**N.C.:** Not connected	12	**GND:** Ground	4	**VCCAUX:** Auxiliary supply voltage (+2.5V)

CP132: 132-ball Chip-scale Package

The XC3S100E, XC3S250E and the XC3S500E FPGAs are available in the 132-ball chip-scale package, CP132. The devices share a common footprint for this package as shown in Table 133 and Figure 81.

Table 133 lists all the CP132 package pins. They are sorted by bank number and then by pin name. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

Physically, the D14 and K2 balls on the XC3S100E and XC3S250E FPGAs are not connected but should be connected to VCCINT to maintain density migration compatibility.

Similarly, the A4, C1, and P10 balls on the XC3S100E FPGA are not connected but should be connected to GND to maintain density migration compatibility.

The XC3S100E FPGA has four fewer BPI address pins, A[19:0], whereas the XC3S250E and XC3S500E support A[23:0].

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx web site at:

http://www.xilinx.com/support/documentation/data_sheets/s3e_pin.zip

Pinout Table

Table 133: **CP132 Package Pinout**

Bank	XC3S100E Pin Name	XC3S250E XC3S500E Pin Name	CP132 Ball	Type
0	IO_L01N_0	IO_L01N_0	C12	I/O
0	IO_L01P_0	IO_L01P_0	A13	I/O
0	N.C. (◆)	IO_L02N_0	A12	***100E:*** N.C. ***Others:*** I/O
0	N.C. (◆)	IO_L02P_0	B12	***100E:*** N.C. ***Others:*** I/O
0	N.C. (◆)	IO_L03N_0/VREF_0	B11	***100E:*** N.C. ***Others:*** VREF (I/O)
0	IP	IO_L03P_0	C11	***100E:*** INPUT ***Others:*** I/O
0	IO_L04N_0/GCLK5	IO_L04N_0/GCLK5	C9	GCLK
0	IO_L04P_0/GCLK4	IO_L04P_0/GCLK4	A10	GCLK
0	IO_L05N_0/GCLK7	IO_L05N_0/GCLK7	A9	GCLK
0	IO_L05P_0/GCLK6	IO_L05P_0/GCLK6	B9	GCLK
0	IO_L07N_0/GCLK11	IO_L07N_0/GCLK11	B7	GCLK
0	IO_L07P_0/GCLK10	IO_L07P_0/GCLK10	A7	GCLK
0	IO_L08N_0/VREF_0	IO_L08N_0/VREF_0	C6	VREF
0	IO_L08P_0	IO_L08P_0	B6	I/O
0	IO_L09N_0	IO_L09N_0	C5	I/O
0	IO_L09P_0	IO_L09P_0	B5	I/O
0	N.C. (◆)	IO_L10N_0	C4	***100E:*** N.C. ***Others:*** I/O
0	IP	IO_L10P_0	B4	***100E:*** INPUT ***Others:*** I/O
0	IO_L11N_0/HSWAP	IO_L11N_0/HSWAP	B3	DUAL
0	IO_L11P_0	IO_L11P_0	A3	I/O
0	IP_L06N_0/GCLK9	IP_L06N_0/GCLK9	C8	GCLK
0	IP_L06P_0/GCLK8	IP_L06P_0/GCLK8	B8	GCLK
0	VCCO_0	VCCO_0	A6	VCCO

Table 133: **CP132 Package Pinout *(Cont'd)***

Bank	XC3S100E Pin Name	XC3S250E XC3S500E Pin Name	CP132 Ball	Type
GND	GND	GND	C10	GND
GND	GND	GND	E3	GND
GND	GND	GND	E14	GND
GND	GND	GND	G2	GND
GND	GND	GND	H14	GND
GND	GND	GND	J1	GND
GND	GND	GND	K12	GND
GND	GND	GND	M3	GND
GND	GND	GND	M7	GND
GND	GND	GND	P5	GND
GND	N.C. (GND)	GND	P10	GND
GND	GND	GND	P14	GND
VCCAUX	DONE	DONE	P13	CONFIG
VCCAUX	PROG_B	PROG_B	A1	CONFIG
VCCAUX	TCK	TCK	B13	JTAG
VCCAUX	TDI	TDI	A2	JTAG
VCCAUX	TDO	TDO	A14	JTAG
VCCAUX	TMS	TMS	B14	JTAG
VCCAUX	VCCAUX	VCCAUX	A5	VCCAUX
VCCAUX	VCCAUX	VCCAUX	E12	VCCAUX
VCCAUX	VCCAUX	VCCAUX	K1	VCCAUX
VCCAUX	VCCAUX	VCCAUX	P9	VCCAUX
VCCINT	VCCINT	VCCINT	A11	VCCINT
VCCINT	VCCINT	VCCINT	D3	VCCINT
VCCINT	N.C. (VCCINT)	VCCINT	D14	VCCINT
VCCINT	N.C. (VCCINT)	VCCINT	K2	VCCINT
VCCINT	VCCINT	VCCINT	L12	VCCINT
VCCINT	VCCINT	VCCINT	P2	VCCINT

Table 137: **TQ144 Package Pinout *(Cont'd)***

Bank	XC3S100E Pin Name	XC3S250E Pin Name	TQ144 Pin	Type
1	IO_L02P_1/A14	IO_L02P_1/A14	P76	DUAL
1	IO_L03N_1/A11	IO_L03N_1/A11	P82	DUAL
1	IO_L03P_1/A12	IO_L03P_1/A12	P81	DUAL
1	IO_L04N_1/A9/RHCLK1	IO_L04N_1/A9/RHCLK1	P86	RHCLK/DUAL
1	IO_L04P_1/A10/RHCLK0	IO_L04P_1/A10/RHCLK0	P85	RHCLK/DUAL
1	IO_L05N_1/A7/RHCLK3/TRDY1	IO_L05N_1/A7/RHCLK3	P88	RHCLK/DUAL
1	IO_L05P_1/A8/RHCLK2	IO_L05P_1/A8/RHCLK2	P87	RHCLK/DUAL
1	IO_L06N_1/A5/RHCLK5	IO_L06N_1/A5/RHCLK5	P92	RHCLK/DUAL
1	IO_L06P_1/A6/RHCLK4/IRDY1	IO_L06P_1/A6/RHCLK4	P91	RHCLK/DUAL
1	IO_L07N_1/A3/RHCLK7	IO_L07N_1/A3/RHCLK7	P94	RHCLK/DUAL
1	IO_L07P_1/A4/RHCLK6	IO_L07P_1/A4/RHCLK6	P93	RHCLK/DUAL
1	IO_L08N_1/A1	IO_L08N_1/A1	P97	DUAL
1	IO_L08P_1/A2	IO_L08P_1/A2	P96	DUAL
1	IO_L09N_1/LDC0	IO_L09N_1/LDC0	P104	DUAL
1	IO_L09P_1/HDC	IO_L09P_1/HDC	P103	DUAL
1	IO_L10N_1/LDC2	IO_L10N_1/LDC2	P106	DUAL
1	IO_L10P_1/LDC1	IO_L10P_1/LDC1	P105	DUAL
1	IP	IP	P78	INPUT
1	IP	IP	P84	INPUT
1	IP	IP	P89	INPUT
1	IP	IP	P101	INPUT
1	IP	IP	P107	INPUT
1	IP/VREF_1	IP/VREF_1	P95	VREF
1	VCCO_1	VCCO_1	P79	VCCO
1	VCCO_1	VCCO_1	P100	VCCO
2	IO/D5	IO/D5	P52	DUAL
2	IO/M1	IO/M1	P60	DUAL
2	IP/VREF_2	IO/VREF_2	P66	***100E:*** VREF(INPUT) ***250E:*** VREF(I/O)
2	IO_L01N_2/INIT_B	IO_L01N_2/INIT_B	P40	DUAL
2	IO_L01P_2/CSO_B	IO_L01P_2/CSO_B	P39	DUAL
2	IO_L02N_2/MOSI/CSI_B	IO_L02N_2/MOSI/CSI_B	P44	DUAL
2	IO_L02P_2/DOUT/BUSY	IO_L02P_2/DOUT/BUSY	P43	DUAL
2	IO_L04N_2/D6/GCLK13	IO_L04N_2/D6/GCLK13	P51	DUAL/GCLK
2	IO_L04P_2/D7/GCLK12	IO_L04P_2/D7/GCLK12	P50	DUAL/GCLK
2	IO_L05N_2/D3/GCLK15	IO_L05N_2/D3/GCLK15	P54	DUAL/GCLK
2	IO_L05P_2/D4/GCLK14	IO_L05P_2/D4/GCLK14	P53	DUAL/GCLK
2	IO_L07N_2/D1/GCLK3	IO_L07N_2/D1/GCLK3	P59	DUAL/GCLK
2	IO_L07P_2/D2/GCLK2	IO_L07P_2/D2/GCLK2	P58	DUAL/GCLK
2	IO_L08N_2/DIN/D0	IO_L08N_2/DIN/D0	P63	DUAL
2	IO_L08P_2/M0	IO_L08P_2/M0	P62	DUAL
2	IO_L09N_2/VS1/A18	IO_L09N_2/VS1/A18	P68	DUAL
2	IO_L09P_2/VS2/A19	IO_L09P_2/VS2/A19	P67	DUAL
2	IO_L10N_2/CCLK	IO_L10N_2/CCLK	P71	DUAL
2	IO_L10P_2/VS0/A17	IO_L10P_2/VS0/A17	P70	DUAL

TQ144 Footprint

Note pin 1 indicator in top-left corner and logo orientation.
Double arrows (↔) indicates a pinout migration difference between the XC3S100E and XC3S250E.

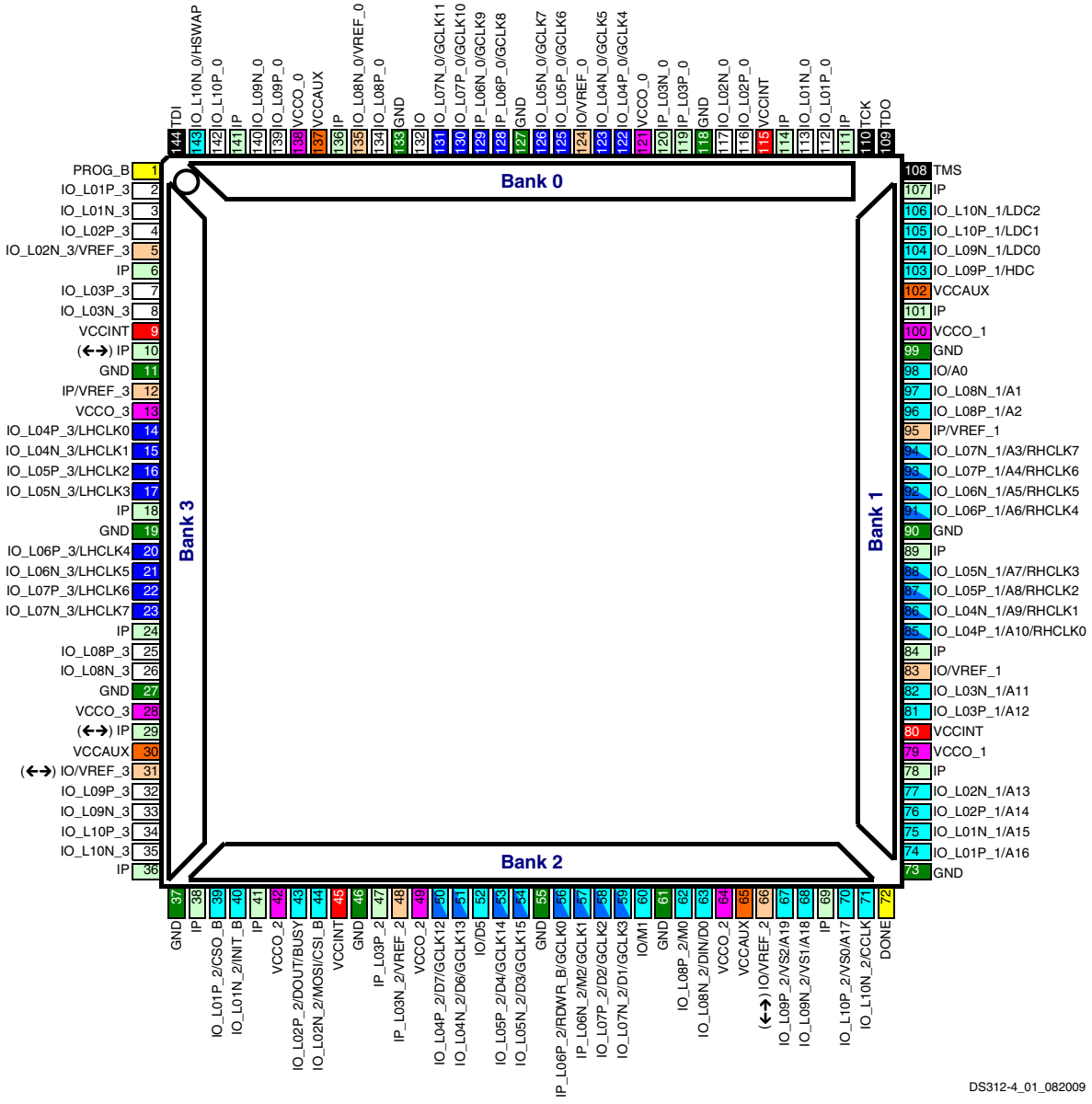

Figure 82: **TQ144 Package Footprint (top view)**

20	**I/O:** Unrestricted, general-purpose user I/O	42	**DUAL:** Configuration pin, then possible user I/O	9	**VREF:** User I/O or input voltage reference for bank
21	**INPUT:** Unrestricted, general-purpose input pin	16	**CLK:** User I/O, input, or global buffer input	9	**VCCO:** Output voltage supply for bank
2	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	4	**VCCINT:** Internal core supply voltage (+1.2V)
0	**N.C.:** Not connected	13	**GND:** Ground	4	**VCCAUX:** Auxiliary supply voltage (+2.5V)

Table 148: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S500E Pin Name	XC3S1200E Pin Name	XC3S1600E Pin Name	FG320 Ball	Type
2	IO_L20P_2	IO_L20P_2	IO_L20P_2	T12	I/O
2	N.C. (◆)	IO_L21N_2	IO_L21N_2	P12	**500E:** N.C. **1200E:** I/O **1600E:** I/O
2	N.C. (◆)	IO_L21P_2	IO_L21P_2	N12	**500E:** N.C. **1200E:** I/O **1600E:** I/O
2	IO_L22N_2/A22	IO_L22N_2/A22	IO_L22N_2/A22	R13	DUAL
2	IO_L22P_2/A23	IO_L22P_2/A23	IO_L22P_2/A23	P13	DUAL
2	IO_L24N_2/A20	IO_L24N_2/A20	IO_L24N_2/A20	R14	DUAL
2	IO_L24P_2/A21	IO_L24P_2/A21	IO_L24P_2/A21	T14	DUAL
2	IO_L25N_2/VS1/A18	IO_L25N_2/VS1/A18	IO_L25N_2/VS1/A18	U15	DUAL
2	IO_L25P_2/VS2/A19	IO_L25P_2/VS2/A19	IO_L25P_2/VS2/A19	V15	DUAL
2	IO_L26N_2/CCLK	IO_L26N_2/CCLK	IO_L26N_2/CCLK	U16	DUAL
2	IO_L26P_2/VS0/A17	IO_L26P_2/VS0/A17	IO_L26P_2/VS0/A17	T16	DUAL
2	IP	IP	IP	V2	INPUT
2	IP	IP	IP	V16	INPUT
2	IP_L02N_2	IP_L02N_2	IP_L02N_2	V3	INPUT
2	IP_L02P_2	IP_L02P_2	IP_L02P_2	V4	INPUT
2	IP_L08N_2	IP_L08N_2	IP_L08N_2	R7	INPUT
2	IP_L08P_2	IP_L08P_2	IP_L08P_2	T7	INPUT
2	IP_L11N_2/VREF_2	IP_L11N_2/VREF_2	IP_L11N_2/VREF_2	V8	VREF
2	IP_L11P_2	IP_L11P_2	IP_L11P_2	U8	INPUT
2	IP_L14N_2/M2/GCLK1	IP_L14N_2/M2/GCLK1	IP_L14N_2/M2/GCLK1	T10	DUAL/GCLK
2	IP_L14P_2/RDWR_B/ GCLK0	IP_L14P_2/RDWR_B/ GCLK0	IP_L14P_2/RDWR_B/ GCLK0	U10	DUAL/GCLK
2	IP_L17N_2	IP_L17N_2	IP_L17N_2	U11	INPUT
2	IP_L17P_2	IP_L17P_2	IP_L17P_2	T11	INPUT
2	IP_L23N_2	IP_L23N_2	IP_L23N_2	U14	INPUT
2	IP_L23P_2	IP_L23P_2	IP_L23P_2	V14	INPUT
2	VCCO_2	VCCO_2	VCCO_2	M8	VCCO
2	VCCO_2	VCCO_2	VCCO_2	M11	VCCO
2	VCCO_2	VCCO_2	VCCO_2	T6	VCCO
2	VCCO_2	VCCO_2	VCCO_2	T13	VCCO
2	VCCO_2	VCCO_2	VCCO_2	V10	VCCO
3	N.C. (◆)	IO	IO	D4	**500E:** N.C. **1200E:** I/O **1600E:** I/O
3	IO_L01N_3	IO_L01N_3	IO_L01N_3	C2	I/O
3	IO_L01P_3	IO_L01P_3	IO_L01P_3	C1	I/O
3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	D2	VREF
3	IO_L02P_3	IO_L02P_3	IO_L02P_3	D1	I/O
3	IO_L03N_3	IO_L03N_3	IO_L03N_3	E1	I/O
3	IO_L03P_3	IO_L03P_3	IO_L03P_3	E2	I/O

User I/Os by Bank

Table 153 indicates how the 304 available user-I/O pins are distributed between the four I/O banks on the FG400 package.

Table 153: **User I/Os Per Bank for the XC3S1200E and XC3S1600E in the FG400 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF[1]	CLK[2]
Top	0	78	43	20	1	6	8
Right	1	74	35	12	21	6	0[2]
Bottom	2	78	30	18	24	6	0[2]
Left	3	74	48	12	0	6	8
TOTAL		**304**	**156**	**62**	**46**	**24**	**16**

Notes:

1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

Footprint Migration Differences

The XC3S1200E and XC3S1600E FPGAs have identical footprints in the FG400 package. Designs can migrate between the XC3S1200E and XC3S1600E FPGAs without further consideration.

FG484 Footprint

Left Half of Package (top view)

214 **I/O:** Unrestricted, general-purpose user I/O

72 **INPUT:** User I/O or reference resistor input for bank

46 **DUAL:** Configuration pin, then possible user I/O

28 **VREF:** User I/O or input voltage reference for bank

16 **CLK:** User I/O, input, or clock buffer input

2 **CONFIG:** Dedicated configuration pins

4 **JTAG:** Dedicated JTAG port pins

48 **GND:** Ground

28 **VCCO:** Output voltage supply for bank

16 **VCCINT:** Internal core supply voltage (+1.2V)

10 **VCCAUX:** Auxiliary supply voltage (+2.5V)

0 **N.C.:** Not connected

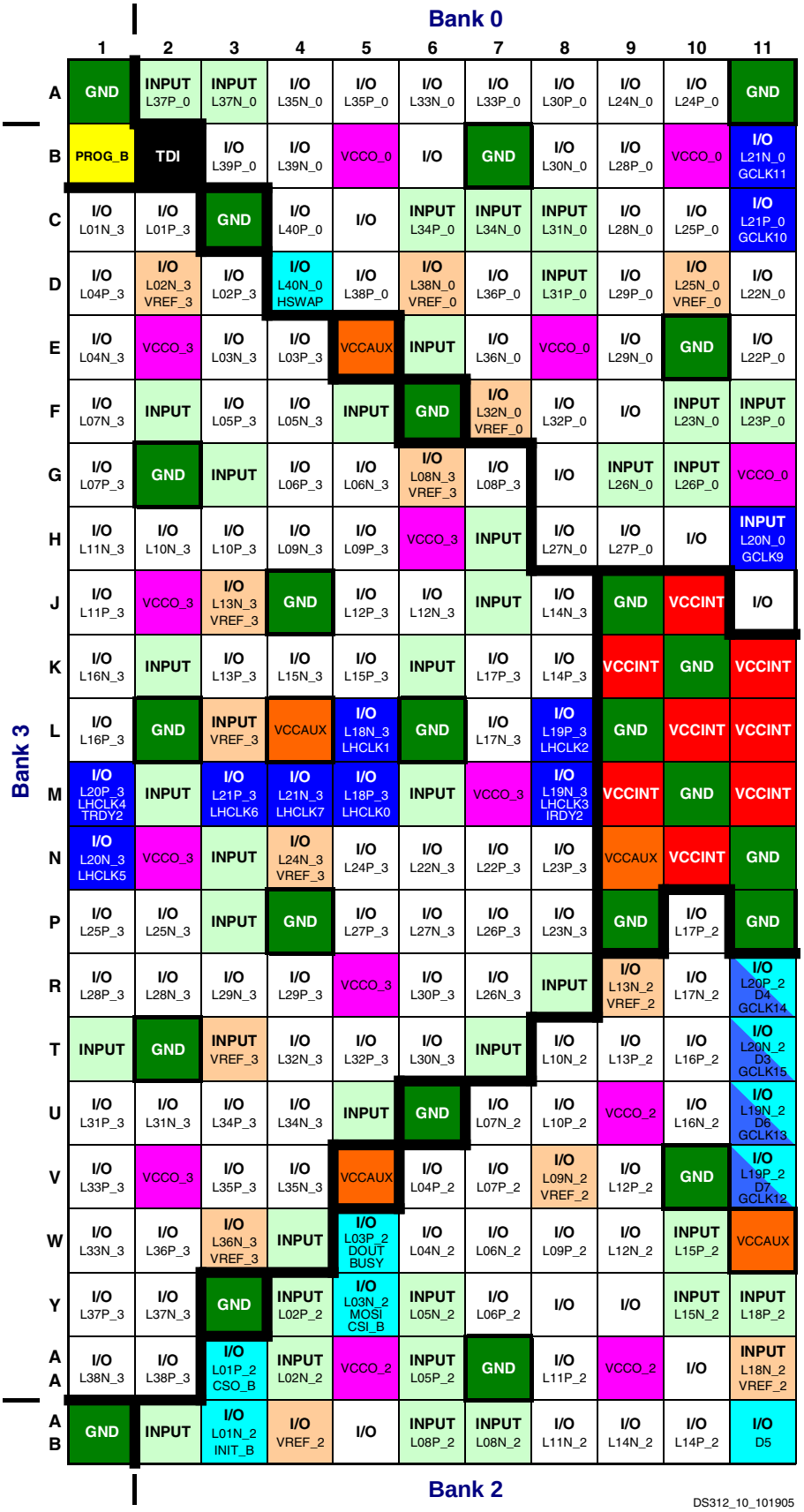

Figure 88: **FG484 Package Footprint (top view)**