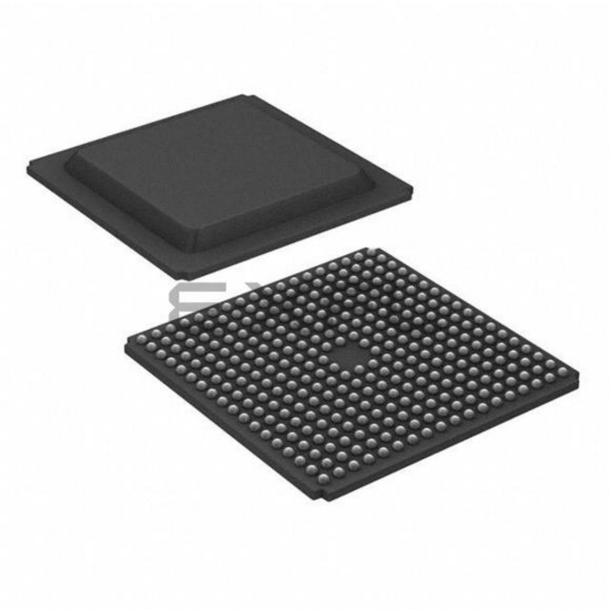

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	3688
Number of Logic Elements/Cells	33192
Total RAM Bits	663552
Number of I/O	250
Number of Gates	1600000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	320-BGA
Supplier Device Package	320-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s1600e-4fgg320c

Package Marking

Figure 2 provides a top marking example for Spartan-3E FPGAs in the quad-flat packages. Figure 3 shows the top marking for Spartan-3E FPGAs in BGA packages except the 132-ball chip-scale package (CP132 and CPG132). The markings for the BGA packages are nearly identical to those for the quad-flat packages, except that the marking is rotated with respect to the ball A1 indicator. Figure 4 shows the top marking for Spartan-3E FPGAs in the CP132 and CPG132 packages.

On the QFP and BGA packages, the optional numerical Stepping Code follows the Lot Code.

The "5C" and "4I" part combinations can have a dual mark of "5C/4I". Devices with a single mark are only guaranteed for the marked speed grade and temperature range. All "5C" and "4I" part combinations use the Stepping 1 production silicon.

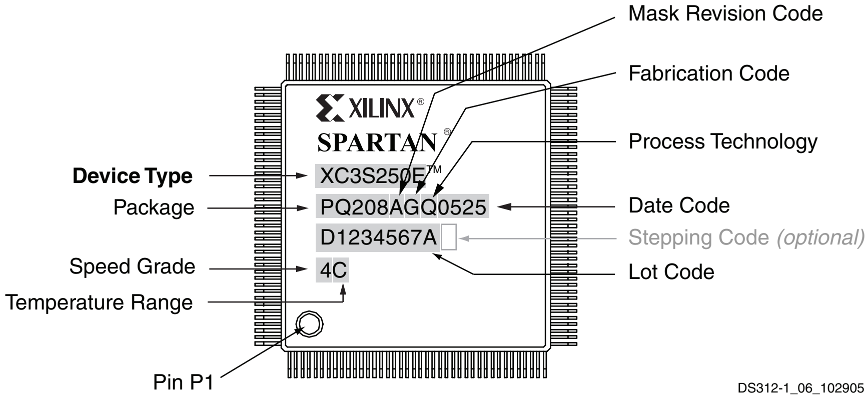

Figure 2: **Spartan-3E QFP Package Marking Example**

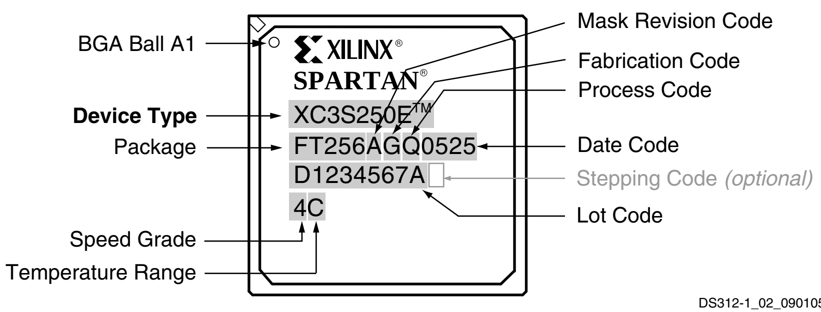

Figure 3: **Spartan-3E BGA Package Marking Example**

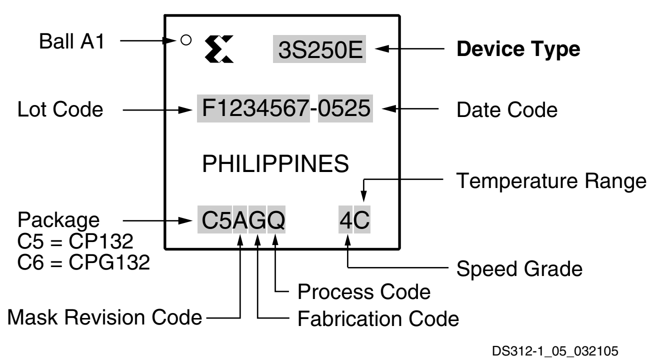

Figure 4: **Spartan-3E CP132 and CPG132 Package Marking Example**

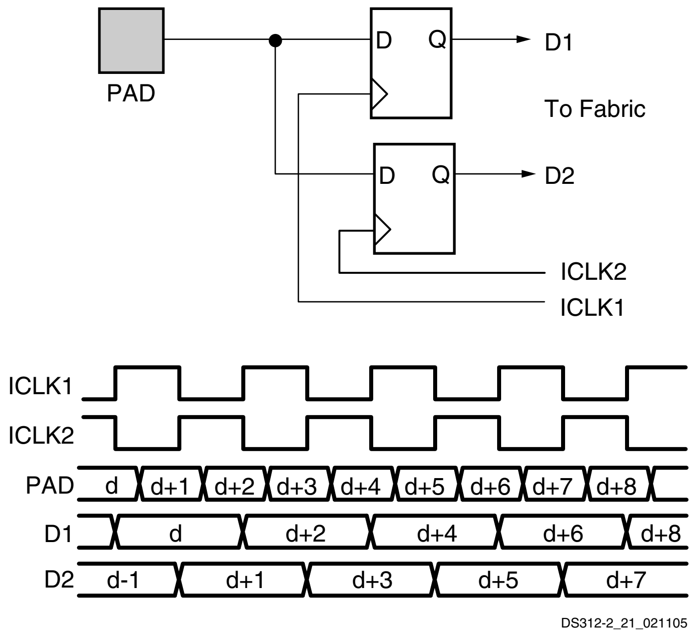

Figure 8: **Input DDR (without Cascade Feature)**

In the Spartan-3E device, the signal D2 can be cascaded into the storage element of the adjacent slave IOB. There it is re-registered to ICLK1, and only then fed to the FPGA fabric where it is now already in the same time domain as D1. Here, the FPGA fabric uses only the clock ICLK1 to process the received data. See Figure 9 for a graphical illustration of this function.

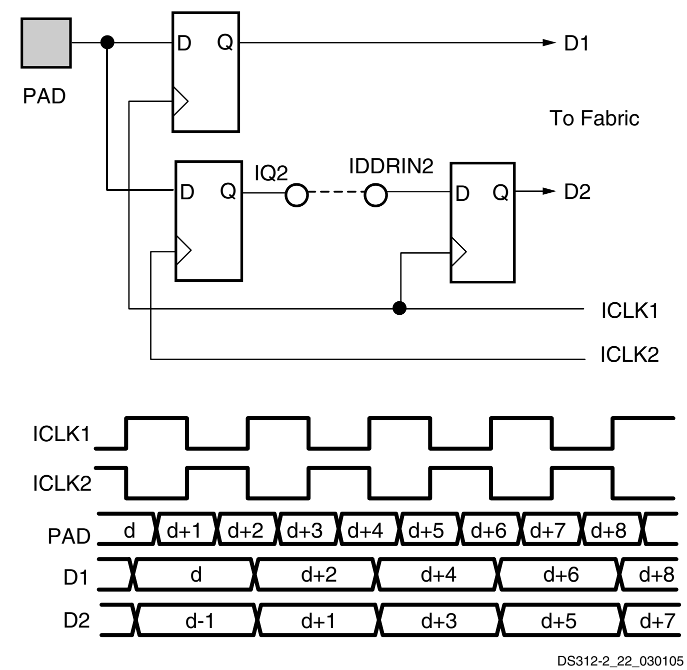

Figure 9: **Input DDR Using Spartan-3E Cascade Feature**

ODDR2

As a DDR output pair, the master IOB registers data coming from the FPGA fabric on the rising edge of OCLK1 (= D1) and the rising edge of OCLK2 (= D2), which is typically the same as the falling edge of OCLK1. These two bits of data are multiplexed by the DDR mux and forwarded to the output pin. The D2 data signal must be re-synchronized from the OCLK1 clock domain to the OCLK2 domain using FPGA slice flip-flops. Placement is critical at high frequencies, because the time available is only one half a clock cycle. See Figure 10 for a graphical illustration of this function.

The C0 or C1 alignment feature of the ODDR2 flip-flop, originally introduced in the Spartan-3E FPGA family, is not recommended or supported in the ISE development software. The ODDR2 flip-flop without the alignment feature remains fully supported. Without the alignment feature, the ODDR2 feature behaves equivalent to the ODDR flip-flop on previous Xilinx FPGA families.

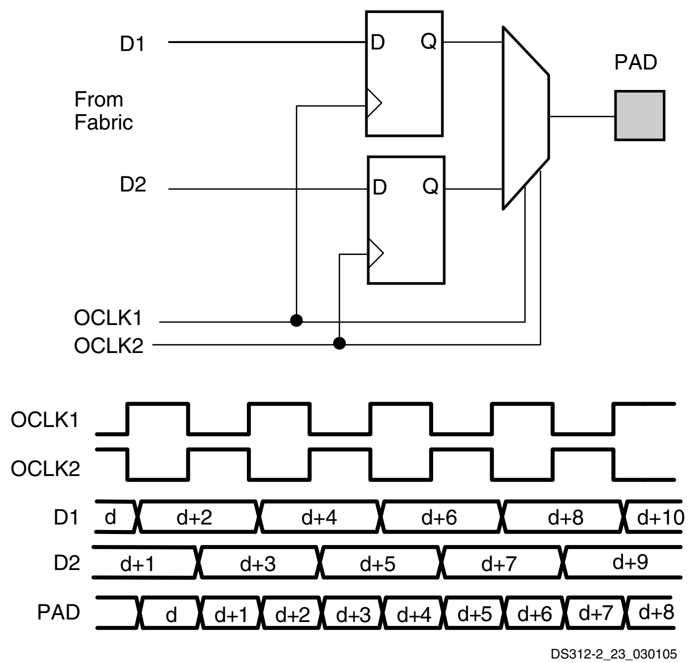

Figure 10: **Output DDR**

SelectIO Signal Standards

The Spartan-3E I/Os feature inputs and outputs that support a wide range of I/O signaling standards (Table 6 and Table 7). The majority of the I/Os also can be used to form differential pairs to support any of the differential signaling standards (Table 7).

To define the I/O signaling standard in a design, set the IOSTANDARD attribute to the appropriate setting. Xilinx provides a variety of different methods for applying the IOSTANDARD for maximum flexibility. For a full description of different methods of applying attributes to control IOSTANDARD, refer to the Xilinx Software Manuals and Help.

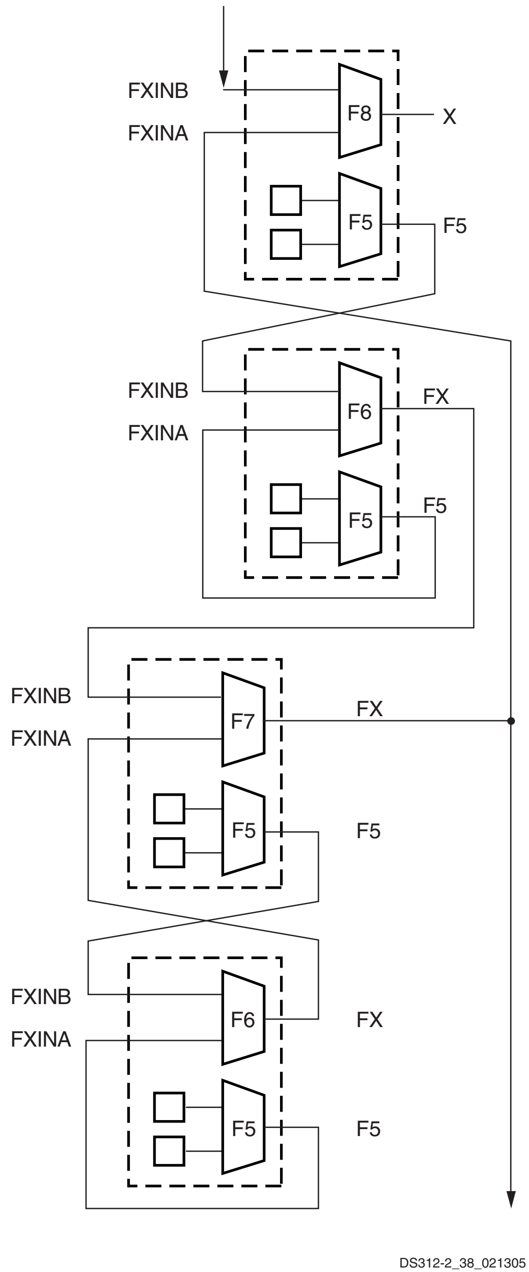

Figure 20: **MUXes and Dedicated Feedback in Spartan-3E CLB**

Table 11: **MUX Capabilities**

MUX	Usage	Input Source	Total Number of Inputs per Function		
			For Any Function	For MUX	For Limited Functions
F5MUX	F5MUX	LUTs	5	6 (4:1 MUX)	9
FiMUX	F6MUX	F5MUX	6	11 (8:1 MUX)	19
	F7MUX	F6MUX	7	20 (16:1 MUX)	39
	F8MUX	F7MUX	8	37 (32:1 MUX)	79

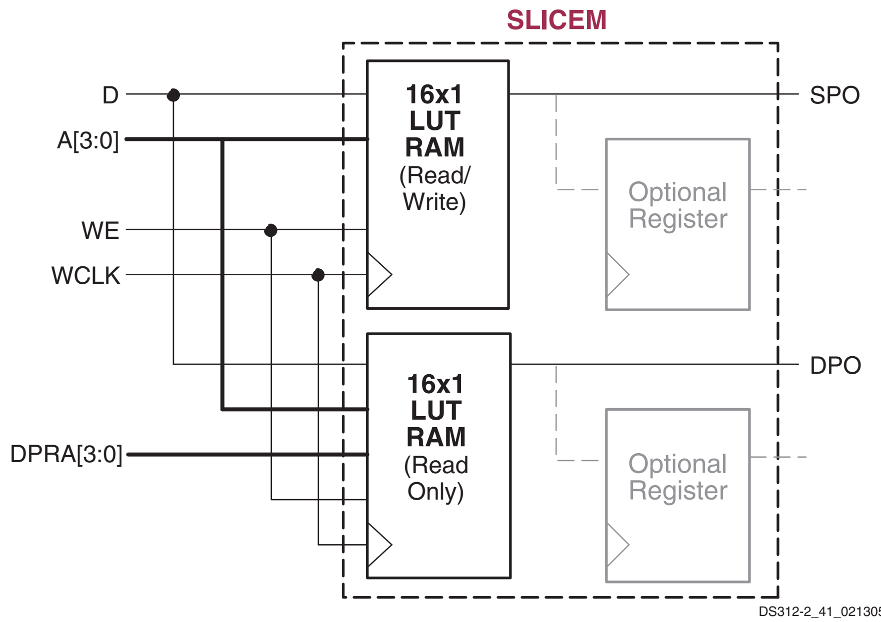

Figure 26: **RAM16X1D Dual-Port Usage**

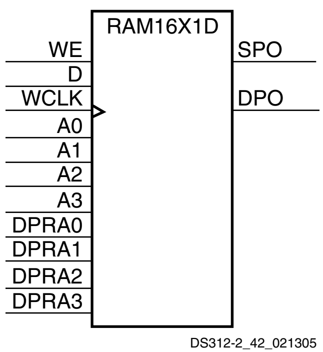

Figure 27: **Dual-Port RAM Component**

Table 18: **Dual-Port RAM Function**

Inputs			Outputs	
WE (mode)	**WCLK**	**D**	**SPO**	**DPO**
0 (read)	X	X	data_a	data_d
1 (read)	0	X	data_a	data_d
1 (read)	1	X	data_a	data_d
1 (write)	↑	D	D	data_d
1 (read)	↓	X	data_a	data_d

Notes:
1. data_a = word addressed by bits A3-A0.
2. data_d = word addressed by bits DPRA3-DPRA0.

Table 19: **Distributed RAM Signals**

Signal	Description
WCLK	The clock is used for synchronous writes. The data and the address input pins have setup times referenced to the WCLK pin. Active on the positive edge by default with built-in programmable polarity.
WE	The enable pin affects the write functionality of the port. An inactive Write Enable prevents any writing to memory cells. An active Write Enable causes the clock edge to write the data input signal to the memory location pointed to by the address inputs. Active High by default with built-in programmable polarity.
A0, A1, A2, A3 (A4, A5)	The address inputs select the memory cells for read or write. The width of the port determines the required address inputs.
D	The data input provides the new data value to be written into the RAM.
O, SPO, and DPO	The data output O on single-port RAM or the SPO and DPO outputs on dual-port RAM reflects the contents of the memory cells referenced by the address inputs. Following an active write clock edge, the data out (O or SPO) reflects the newly written data.

The INIT attribute can be used to preload the memory with data during FPGA configuration. The default initial contents for RAM is all zeros. If the WE is held Low, the element can be considered a ROM. The ROM function is possible even in the SLICEL.

The global write enable signal, GWE, is asserted automatically at the end of device configuration to enable all writable elements. The GWE signal guarantees that the initialized distributed RAM contents are not disturbed during the configuration process.

The distributed RAM is useful for smaller amounts of memory. Larger memory requirements can use the dedicated 18Kbit RAM blocks (see Block RAM).

Shift Registers

For additional information, refer to the "Using Look-Up Tables as Shift Registers (SRL16)" chapter in UG331.

It is possible to program each SLICEM LUT as a 16-bit shift register (see Figure 28). Used in this way, each LUT can delay serial data anywhere from 1 to 16 clock cycles without using any of the dedicated flip-flops. The resulting programmable delays can be used to balance the timing of data pipelines.

The SLICEM LUTs cascade from the G-LUT to the F-LUT through the DIFMUX (see Figure 15). SHIFTIN and SHIFTOUT lines cascade a SLICEM to the SLICEM below to form larger shift registers. The four SLICEM LUTs of a single CLB can be combined to produce delays up to 64 clock cycles. It is also possible to combine shift registers across more than one CLB.

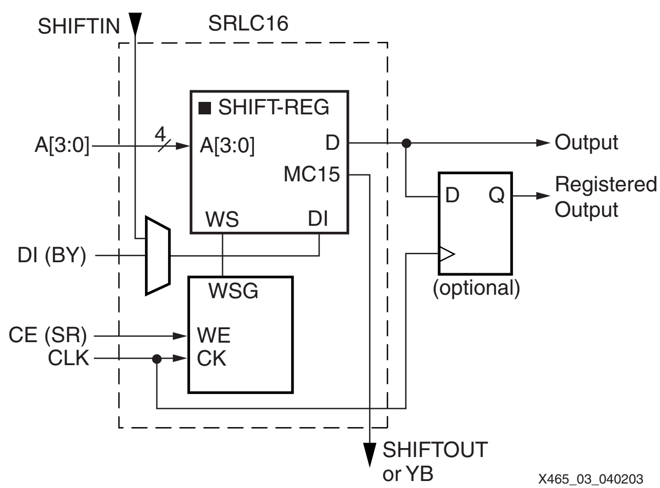

Figure 28: **Logic Cell SRL16 Structure**

Each shift register provides a shift output MC15 for the last bit in each LUT, in addition to providing addressable access to any bit in the shift register through the normal D output. The address inputs A[3:0] are the same as the distributed RAM address lines, which come from the LUT inputs F[4:1] or G[4:1]. At the end of the shift register, the CLB flip-flop can be used to provide one more shift delay for the addressable bit.

The shift register element is known as the SRL16 (Shift Register LUT 16-bit), with a 'C' added to signify a cascade ability (Q15 output) and 'E' to indicate a Clock Enable. See Figure 29 for an example of the SRLC16E component.

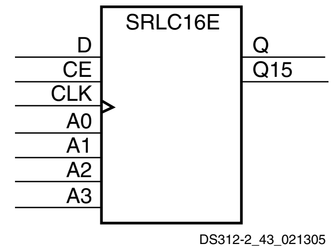

Figure 29: **SRL16 Shift Register Component with Cascade and Clock Enable**

The functionality of the shift register is shown in Table 20. The SRL16 shifts on the rising edge of the clock input when the Clock Enable control is High. This shift register cannot be initialized either during configuration or during operation except by shifting data into it. The clock enable and clock inputs are shared between the two LUTs in a SLICEM. The clock enable input is automatically kept active if unused.

Table 20: **SRL16 Shift Register Function**

Inputs				Outputs	
Am	**CLK**	**CE**	**D**	**Q**	**Q15**
Am	X	0	X	Q[Am]	Q[15]
Am	↑	1	D	Q[Am-1]	Q[15]

Notes:

1. m = 0, 1, 2, 3.

Table 31: **Direct Clock Input and Optional External Feedback to Left-Edge DCMs (XC3S1200E and XC3S1600E)**

Diff. Clock		Single-Ended Pin Number by Package Type									Left Edge			
		VQ100	CP132	TQ144	PQ208	FT256	FG320	FG400	FG484		LHCLK	DCM/BUFGMUX		
												BUFGMUX_X0Y5	→	D
												BUFGMUX_X0Y4	→	C
Pair	P	P9	F3	P14	P22	H5	J5	K3	M5	→	LHCLK0	DCM_X0Y2		Clock Lines
	N	P10	F2	P15	P23	H6	J4	K2	L5	→	LHCLK1			
Pair	P	P11	F1	P16	P24	H3	J1	K7	L8	→	LHCLK2			
	N	P12	G1	P17	P25	H4	J2	L7	M8	→	LHCLK3			
												BUFGMUX_X0Y3	→	B
												BUFGMUX_X0Y2	→	A
												BUFGMUX_X0Y9	→	H
												BUFGMUX_X0Y8	→	G
Pair	P	P15	G3	P20	P28	J2	K3	M1	M1	→	LHCLK4	DCM_X0Y1		Clock Lines
	N	P16	H1	P21	P29	J3	K4	L1	N1	→	LHCLK5			
Pair	P	P17	H2	P22	P30	J5	K6	M3	M3	→	LHCLK6			
	N	P18	H3	P23	P31	J4	K5	L3	M4	→	LHCLK7			
												BUFGMUX_X0Y7	→	F
												BUFGMUX_X0Y6	→	E

Table 32: **Direct Clock Input and Optional External Feedback to Right-Edge DCMs (XC3S1200E and XC3S1600E)**

		Right Edge			Single-Ended Pin Number by Package Type								Diff. Clock	
		DCM/BUFGMUX	RHCLK		VQ100	CP132	TQ144	PQ208	FT256	FG320	FG400	FG484		
D	←	BUFGMUX_X3Y5												
C	←	BUFGMUX_X3Y4												
Clock Lines		DCM_X3Y2	RHCLK7	←	P68	G13	P94	P135	H11	J14	J20	L19	N	Pair
			RHCLK6	←	P67	G14	P93	P134	H12	J15	K20	L18	P	
			RHCLK5	←	P66	H12	P92	P133	H14	J16	K14	L21	N	Pair
			RHCLK4	←	P65	H13	P91	P132	H15	J17	K13	L20	P	
B	←	BUFGMUX_X3Y3												
A	←	BUFGMUX_X3Y2												
H	←	BUFGMUX_X3Y9												
G	←	BUFGMUX_X3Y8												
Clock Lines		DCM_X3Y1	RHCLK3	←	P63	J14	P88	P129	J13	K14	L14	M16	N	Pair
			RHCLK2	←	P62	J13	P87	P128	J14	K15	L15	M15	P	
			RHCLK1	←	P61	J12	P86	P127	J16	K12	L16	M22	N	Pair
			RHCLK0	←	P60	K14	P85	P126	K16	K13	M16	N22	P	
F	←	BUFGMUX_X3Y7												
E	←	BUFGMUX_X3Y6												

Every FPGA input provides a possible DCM clock input, but the path is not temperature and voltage compensated like the GCLKs. Alternatively, clock signals within the FPGA optionally provide a DCM clock input via a Global Clock Multiplexer Buffer (BUFGMUX). The global clock net connects directly to the CLKIN input. The internal and external connections are shown in Figure 42a and Figure 42c, respectively.

VARIABLE Phase Shift Mode

In VARIABLE phase shift mode, the FPGA application dynamically adjusts the fine phase shift value using three inputs to the PS unit (PSEN, PSCLK, and PSINCDEC), as defined in Table 36 and shown in Figure 40.

Table 36: **Signals for Variable Phase Mode**

Signal	Direction	Description
PSEN(1)	Input	Enables the Phase Shift unit for variable phase adjustment.
PSCLK(1)	Input	Clock to synchronize phase shift adjustment.
PSINCDEC(1)	Input	When High, increments the current phase shift value. When Low, decrements the current phase shift value. This signal is synchronized to the PSCLK signal.
PSDONE	Output	Goes High to indicate that the present phase adjustment is complete and PS unit is ready for next phase adjustment request. This signal is synchronized to the PSCLK signal.

Notes:
1. This input supports either a true or inverted polarity.

The FPGA application uses the three PS inputs on the Phase Shift unit to dynamically and incrementally increase or decrease the phase shift amount on all nine DCM clock outputs.

To adjust the current phase shift value, the PSEN enable signal must be High to enable the PS unit. Coincidently, PSINCDEC must be High to increment the current phase shift amount or Low to decrement the current amount. All VARIABLE phase shift operations are controlled by the PSCLK input, which can be the CLKIN signal or any other clock signal.

Design Note

The VARIABLE phase shift feature operates differently from the Spartan-3 DCM; use the DCM_SP primitive, not the DCM primitive.

DCM_DELAY_STEP

DCM_DELAY_STEP is the finest delay resolution available in the PS unit. Its value is provided at the bottom of Table 105 in Module 3. For each enabled PSCLK cycle that PSINCDEC is High, the PS unit adds one DCM_ DELAY_STEP of phase shift to all nine DCM outputs. Similarly, for each enabled PSCLK cycle that PSINCDEC is Low, the PS unit subtracts one DCM_ DELAY_STEP of phase shift from all nine DCM outputs.

Because each DCM_DELAY_STEP has a minimum and maximum value, the actual phase shift delay for the present phase increment/decrement value (VALUE) falls within the minimum and maximum values according to Equation 4 and Equation 5.

$$T_{PS}(Max) = VALUE \bullet \text{DCM\_DELAY\_STEP\_MAX} \qquad \text{Eq 4}$$

$$T_{PS}(Min) = VALUE \bullet \text{DCM\_DELAY\_STEP\_MIN} \qquad \text{Eq 5}$$

The maximum variable phase shift steps, MAX_STEPS, is described in Equation 6 or Equation 7, for a given CLKIN input period, T_{CLKIN}, in nanoseconds. To convert this to a phase shift range measured in time and not steps, use MAX_STEPS derived in Equation 6 and Equation 7 for VALUE in Equation 4 and Equation 5.

If CLKIN < 60 MHz:

$$\text{MAX\_STEPS} = \pm[INTEGER(10 \bullet (T_{CLKIN} - 3))] \qquad \text{Eq 6}$$

If CLKIN ≥ 60 MHz:

$$\text{MAX\_STEPS} = \pm[INTEGER(15 \bullet (T_{CLKIN} - 3))] \qquad \text{Eq 7}$$

The phase adjustment might require as many as 100 CLKIN cycles plus 3 PSCLK cycles to take effect, at which point the DCM's PSDONE output goes High for one PSCLK cycle. This pulse indicates that the PS unit completed the previous adjustment and is now ready for the next request.

Asserting the Reset (RST) input returns the phase shift to zero.

(P) Similarly, the FPGA's HSWAP pin must be Low to enable pull-up resistors on all user-I/O pins during configuration or High to disable the pull-up resistors. The HSWAP control must remain at a constant logic level throughout FPGA configuration. After configuration, when the FPGA's DONE output goes High, the HSWAP pin is available as full-featured user-I/O pin and is powered by the VCCO_0 supply.

The FPGA's DOUT pin is used in daisy-chain applications, described later. In a single-FPGA application, the FPGA's DOUT pin is not used but is actively driving during the configuration process.

Table 50: **Serial Master Mode Connections**

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
HSWAP (P)	Input	**User I/O Pull-Up Control**. When Low during configuration, enables pull-up resistors in all I/O pins to respective I/O bank V_{CCO} input. 0: Pull-ups during configuration 1: No pull-ups	Drive at valid logic level throughout configuration.	User I/O
M[2:0]	Input	**Mode Select**. Selects the FPGA configuration mode. See Design Considerations for the HSWAP, M[2:0], and VS[2:0] Pins.	M2 = 0, M1 = 0, M0 = 0. Sampled when INIT_B goes High.	User I/O
DIN	Input	**Serial Data Input**.	Receives serial data from PROM's D0 output.	User I/O
CCLK	Output	**Configuration Clock**. Generated by FPGA internal oscillator. Frequency controlled by ***ConfigRate*** bitstream generator option. If CCLK PCB trace is long or has multiple connections, terminate this output to maintain signal integrity. See CCLK Design Considerations.	Drives PROM's CLK clock input.	User I/O
DOUT	Output	**Serial Data Output**.	Actively drives. Not used in single-FPGA designs. In a daisy-chain configuration, this pin connects to DIN input of the next FPGA in the chain.	User I/O
INIT_B	Open-drain bidirectional I/O	**Initialization Indicator**. Active Low. Goes Low at start of configuration during Initialization memory clearing process. Released at end of memory clearing, when mode select pins are sampled. Requires external 4.7 kΩ pull-up resistor to VCCO_2.	Connects to PROM's OE/RESET input. FPGA clears PROM's address counter at start of configuration, enables outputs during configuration. PROM also holds FPGA in Initialization state until PROM reaches Power-On Reset (POR) state. If CRC error detected during configuration, FPGA drives INIT_B Low.	User I/O. If unused in the application, drive INIT_B High.
DONE	Open-drain bidirectional I/O	**FPGA Configuration Done**. Low during configuration. Goes High when FPGA successfully completes configuration. Requires external 330 Ω pull-up resistor to 2.5V.	Connects to PROM's chip-enable (CE) input. Enables PROM during configuration. Disables PROM after configuration.	Pulled High via external pull-up. When High, indicates that the FPGA successfully configured.
PROG_B	Input	**Program FPGA**. Active Low. When asserted Low for 500 ns or longer, forces the FPGA to restart its configuration process by clearing configuration memory and resetting the DONE and INIT_B pins once PROG_B returns High. Recommend external 4.7 kΩ pull-up resistor to 2.5V. Internal pull-up value may be weaker (see Table 78). If driving externally with a 3.3V output, use an open-drain or open-collector driver or use a current limiting series resistor.	Must be High during configuration to allow configuration to start. Connects to PROM's CF pin, allowing JTAG PROM programming algorithm to reprogram the FPGA.	Drive PROG_B Low and release to reprogram FPGA.

Table 59: **Byte-Wide Peripheral Interface (BPI) Connections *(Cont'd)***

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
HDC	Output	PROM Write Enable	Connect to PROM write-enable input (WE#). FPGA drives this signal High throughout configuration.	User I/O
LDC2 (D)	Output	PROM Byte Mode	This signal is not used for x8 PROMs. For PROMs with a x8/x16 data width control, connect to PROM byte-mode input (BYTE#). See Precautions Using x8/x16 Flash PROMs. FPGA drives this signal Low throughout configuration.	User I/O. Drive this pin High after configuration to use a x8/x16 PROM in x16 mode.
A[23:0]	Output	Address	Connect to PROM address inputs. High-order address lines may not be available in all packages and not all may be required. Number of address lines required depends on the size of the attached Flash PROM. FPGA address generation controlled by M0 mode pin. Addresses presented on falling CCLK edge. Only 20 address lines are available in TQ144 package.	User I/O
D[7:0]	Input	Data Input	FPGA receives byte-wide data on these pins in response the address presented on A[23:0]. Data captured by FPGA on rising edge of CCLK.	User I/O. If bitstream option ***Persist=Yes***, becomes part of SelectMap parallel peripheral interface.
CSO_B	Output	**Chip Select Output**. Active Low.	Not used in single FPGA applications. In a daisy-chain configuration, this pin connects to the CSI_B pin of the next FPGA in the chain. If HSWAP = 1 in a multi-FPGA daisy-chain application, connect this signal to a 4.7 kΩ pull-up resistor to VCCO_2. Actively drives Low when selecting a downstream device in the chain.	User I/O
BUSY	Output	**Busy Indicator**. Typically only used after configuration, if bitstream option ***Persist=Yes***.	Not used during configuration but actively drives.	User I/O. If bitstream option ***Persist=Yes***, becomes part of SelectMap parallel peripheral interface.
CCLK	Output	**Configuration Clock**. Generated by FPGA internal oscillator. Frequency controlled by ***ConfigRate*** bitstream generator option. If CCLK PCB trace is long or has multiple connections, terminate this output to maintain signal integrity. See CCLK Design Considerations.	Not used in single FPGA applications but actively drives. In a daisy-chain configuration, drives the CCLK inputs of all other FPGAs in the daisy-chain.	User I/O. If bitstream option ***Persist=Yes***, becomes part of SelectMap parallel peripheral interface.
INIT_B	Open-drain bidirectional I/O	**Initialization Indicator**. Active Low. Goes Low at start of configuration during the Initialization memory clearing process. Released at the end of memory clearing, when the mode select pins are sampled. In daisy-chain applications, this signal requires an external 4.7 kΩ pull-up resistor to VCCO_2.	Active during configuration. If CRC error detected during configuration, FPGA drives INIT_B Low.	User I/O. If unused in the application, drive INIT_B High.

Table 65: **Slave Parallel Mode Connections *(Cont'd)***

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
INIT_B	Open-drain bidirectional I/O	**Initialization Indicator**. Active Low. Goes Low at the start of configuration during the Initialization memory clearing process. Released at the end of memory clearing, when mode select pins are sampled. In daisy-chain applications, this signal requires an external 4.7 kΩ pull-up resistor to VCCO_2.	Active during configuration. If CRC error detected during configuration, FPGA drives INIT_B Low.	User I/O. If unused in the application, drive INIT_B High.
DONE	Open-drain bidirectional I/O	**FPGA Configuration Done**. Low during configuration. Goes High when FPGA successfully completes configuration. Requires external 330 Ω pull-up resistor to 2.5V.	Low indicates that the FPGA is not yet configured.	Pulled High via external pull-up. When High, indicates that the FPGA successfully configured.
PROG_B	Input	**Program FPGA**. Active Low. When asserted Low for 500 ns or longer, forces the FPGA to restart its configuration process by clearing configuration memory and resetting the DONE and INIT_B pins once PROG_B returns High. Recommend external 4.7 kΩ pull-up resistor to 2.5V. Internal pull-up value may be weaker (see Table 78). If driving externally with a 3.3V output, use an open-drain or open-collector driver or use a current limiting series resistor.	Must be High to allow configuration to start.	Drive PROG_B Low and release to reprogram FPGA.

Voltage Compatibility

(V) Most Slave Parallel interface signals are within the FPGA's I/O Bank 2, supplied by the VCCO_2 supply input. The VCCO_2 voltage can be 1.8V, 2.5V, or 3.3V to match the requirements of the external host, ideally 2.5V. Using 1.8V or 3.3V requires additional design considerations as the DONE and PROG_B pins are powered by the FPGA's 2.5V V_{CCAUX} supply. See XAPP453: *The 3.3V Configuration of Spartan-3 FPGAs* for additional information.

Daisy-Chaining

If the application requires multiple FPGAs with different configurations, then configure the FPGAs using a daisy chain. Use Slave Parallel mode (M[2:0] = <1:1:0>) for all FPGAs in the daisy-chain. The schematic in Figure 62 is optimized for FPGA downloading and does not support the SelectMAP read interface. The FPGA's RDWR_B pin must be Low during configuration.

After the lead FPGA is filled with its configuration data, the lead FPGA enables the next FPGA in the daisy-chain by asserting is chip-select output, CSO_B.

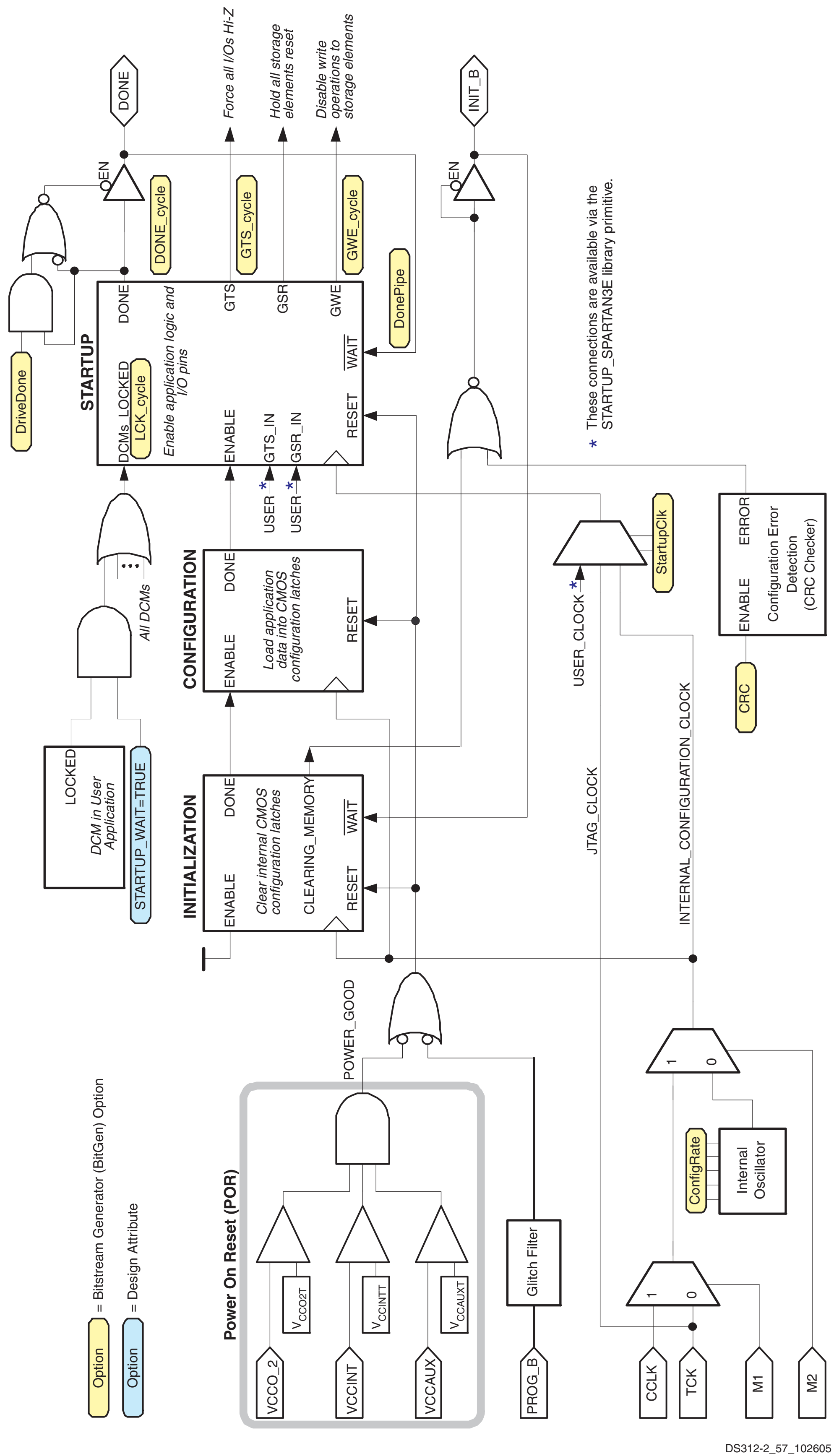

Figure 66: **Generalized Spartan-3E FPGA Configuration Logic Block Diagram**

Table 88: **Setup and Hold Times for the IOB Input Path**

Symbol	Description	Conditions	IFD_ DELAY_ VALUE=	Device	Speed Grade -5 Min	Speed Grade -4 Min	Units
Setup Times							
T_{IOPICK}	Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). No Input Delay is programmed.	LVCMOS25[(2)], IFD_DELAY_VALUE = 0	0	All	1.84	2.12	ns
$T_{IOPICKD}$	Time from the setup of data at the Input pin to the active transition at the IFF's ICLK input. The Input Delay is programmed.	LVCMOS25[(2)], IFD_DELAY_VALUE = default software setting	2	XC3S100E	6.12	7.01	ns
			3	All Others	6.76	7.72	
Hold Times							
T_{IOICKP}	Time from the active transition at the IFF's ICLK input to the point where data must be held at the Input pin. No Input Delay is programmed.	LVCMOS25[(3)], IFD_DELAY_VALUE = 0	0	All	–0.76	–0.76	ns
$T_{IOICKPD}$	Time from the active transition at the IFF's ICLK input to the point where data must be held at the Input pin. The Input Delay is programmed.	LVCMOS25[(3)], IFD_DELAY_VALUE = default software setting	2	XC3S100E	–3.93	–3.93	ns
			3	All Others	–3.50	–3.50	
Set/Reset Pulse Width							
T_{RPW_IOB}	Minimum pulse width to SR control input on IOB			All	1.57	1.80	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 95 and are based on the operating conditions set forth in Table 77 and Table 80.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, add the appropriate Input adjustment from Table 91.
3. These hold times require adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, subtract the appropriate Input adjustment from Table 91. When the hold time is negative, it is possible to change the data before the clock's active edge.

Table 89: **Sample Window (Source Synchronous)**

Symbol	Description	Max	Units
T_{SAMP}	Setup and hold capture window of an IOB input flip-flop	The input capture sample window value is highly specific to a particular application, device, package, I/O standard, I/O placement, DCM usage, and clock buffer. Please consult the appropriate Xilinx application note for application-specific values. • XAPP485: *1:7 Deserialization in Spartan-3E FPGAs at Speeds Up to 666 Mbps*	ps

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/01/05	1.0	Initial Xilinx release.
11/23/05	2.0	Added AC timing information and additional DC specifications.
03/22/06	3.0	Upgraded data sheet status to Preliminary. Finalized production timing parameters. All speed grades for all Spartan-3E FPGAs are now Production status using the v1.21 speed files, as shown in Table 84. Expanded description in Note 2, Table 78. Updated pin-to-pin and clock-to-output timing based on final characterization, shown in Table 86. Updated system-synchronous input setup and hold times based on final characterization, shown in Table 87 and Table 88. Updated other I/O timing in Table 90. Provided input and output adjustments for LVPECL_25, DIFF_SSTL and DIFF_HSTL I/O standards that supersede the v1.21 speed file values, in Table 91 and Table 94. Reduced I/O three-state and set/reset delays in Table 93. Added XC3S100E FPGA in CP132 package to Table 96. Increased T_{AS} slice flip-flop timing by 100 ps in Table 98. Updated distributed RAM timing in Table 99 and SRL16 timing in Table 100. Updated global clock timing, removed left/right clock buffer limits in Table 101. Updated block RAM timing in Table 103. Added DCM parameters for remainder of Step 0 device; added improved Step 1 DCM performance to Table 104, Table 105, Table 106, and Table 107. Added minimum INIT_B pulse width specification, T_{INIT}, in Table 111. Increased data hold time for Slave Parallel mode to 1.0 ns (T_{SMCCD}) in Table 117. Improved the DCM performance for the XC3S1200E, Stepping 0 in Table 104, Table 105, Table 106, and Table 107. Corrected links in Table 118 and Table 120. Added MultiBoot timing specifications to Table 122.
04/07/06	3.1	Improved SSO limits for LVDS_25, MINI_LVDS_25, and RSDS_25 I/O standards in the QFP packages (Table 97). Removed potentially confusing Note 2 from Table 78.
05/19/06	3.2	Clarified that 100 mV of hysteresis applies to LVCMOS33 and LVCMOS25 I/O standards (Note 4, Table 80). Other minor edits.
05/30/06	3.2.1	Corrected various typos and incorrect links.
11/09/06	3.4	Improved absolute maximum voltage specifications in Table 73, providing additional overshoot allowance. Widened the recommended voltage range for PCI and PCI-X standards in Table 80. Clarified Note 2, Table 83. Improved various timing specifications for v1.26 speed file. Added Table 85 to summarize the history of speed file releases after which time all devices became Production status. Added absolute minimum values for Table 86, Table 92, and Table 93. Updated pin-to-pin setup and hold timing based on default IFD_DELAY_VALUE settings in Table 87, Table 88, and Table 90. Added Table 89 about source-synchronous input capture sample window. Promoted Module 3 to Production status. Synchronized all modules to v3.4.
03/16/07	3.5	Based on extensive 90 nm production data, improved (reduced) the maximum quiescent current limits for the I_{CCINTQ}, I_{CCAUXQ}, and I_{CCOQ} specifications in Table 79 by an average of 50%.
05/29/07	3.6	Added note to Table 74 and Table 75 regarding HSWAP in step 0 devices. Updated t_{RPW_CLB} in Table 98 to match value in speed file. Improved CLKOUT_FREQ_CLK90 to 200 MHz for Stepping 1 in Table 105.
04/18/08	3.7	Clarified that Stepping 0 was offered only for -4C and removed Stepping 0 -5 specifications. Added reference to XAPP459 in Table 73 and Table 77. Improved recommended max V_{CCO} to 3.465V (3.3V + 5%) in Table 77. Removed minimum input capacitance from Table 78. Updated Recommended Operating Conditions for LVCMOS and PCI I/O standards in Table 80. Removed Absolute Minimums from Table 86, Table 92 and Table 93 and added footnote recommending use of Timing Analyzer for minimum values. Updated T_{PSFD} and T_{PHFD} in Table 87 to match current speed file. Update T_{RPW_IOB} in Table 88 to match current speed file and CLB equivalent spec. Added XC3S500E VQG100 to Table 96. Replaced $T_{MULCKID}$ with T_{MSCKD} for A, B, and P registers in Table 102. Updated CLKOUT_PER_JITT_FX in Table 107. Updated MAX_STEPS equation in Table 109. Updated Figure 77 and Table 120 to correct CCLK active edge. Updated links.

Package Thermal Characteristics

The power dissipated by an FPGA application has implications on package selection and system design. The power consumed by a Spartan-3E FPGA is reported using either the XPower Estimator or the XPower Analyzer calculator integrated in the Xilinx ISE® development software. Table 130 provides the thermal characteristics for the various Spartan-3E package offerings.

The junction-to-case thermal resistance (θ_{JC}) indicates the difference between the temperature measured on the package body (case) and the die junction temperature per watt of power consumption. The junction-to-board (θ_{JB}) value similarly reports the difference between the board and junction temperature. The junction-to-ambient (θ_{JA}) value reports the temperature difference per watt between the ambient environment and the junction temperature. The θ_{JA} value is reported at different air velocities, measured in linear feet per minute (LFM). The Still Air (0 LFM) column shows the θ_{JA} value in a system without a fan. The thermal resistance drops with increasing air flow.

Table 130: **Spartan-3E Package Thermal Characteristics**

Device	Package	Junction-to-Case (θ_{JC})	Junction-to-Board (θ_{JB})	Junction-to-Ambient (θ_{JA}) at Different Air Flows				Units
				Still Air (0 LFM)	250 LFM	500 LFM	750 LFM	
XC3S100E	VQ100	13.0	30.9	49.0	40.7	37.9	37.0	°C/Watt
XC3S250E		11.0	25.9	43.3	36.0	33.6	32.7	°C/Watt
XC3S500E		9.8		40.0	33.3	31.0	30.2	°C/Watt
XC3S100E	CP132	19.3	42.0	62.1	55.3	52.8	51.2	°C/Watt
XC3S250E		11.8	28.1	48.3	41.8	39.5	38.0	°C/Watt
XC3S500E		8.5	21.3	41.5	35.2	32.9	31.5	°C/Watt
XC3S100E	TQ144	8.2	31.9	52.1	40.5	34.6	32.5	°C/Watt
XC3S250E		7.2	25.7	37.6	29.2	25.0	23.4	°C/Watt
XC3S250E	PQ208	9.8	29.0	37.0	27.3	24.1	22.4	°C/Watt
XC3S500E		8.5	26.8	36.1	26.6	23.6	21.8	°C/Watt
XC3S250E	FT256	12.4	27.7	35.8	29.3	28.4	28.1	°C/Watt
XC3S500E		9.6	22.2	31.1	25.0	24.0	23.6	°C/Watt
XC3S1200E		6.5	16.4	26.2	20.5	19.3	18.9	°C/Watt
XC3S500E	FG320	9.8	15.6	26.1	20.6	19.4	18.6	°C/Watt
XC3S1200E		8.2	12.5	23.0	17.7	16.4	15.7	°C/Watt
XC3S1600E		7.1	10.6	21.1	15.9	14.6	13.8	°C/Watt
XC3S1200E	FG400	7.5	12.4	22.3	17.2	16.0	15.3	°C/Watt
XC3S1600E		6.0	10.4	20.3	15.2	14.0	13.3	°C/Watt
XC3S1600E	FG484	5.7	9.4	18.8	12.5	11.3	10.8	°C/Watt

Table 137: **TQ144 Package Pinout *(Cont'd)***

Bank	XC3S100E Pin Name	XC3S250E Pin Name	TQ144 Pin	Type
1	IO_L02P_1/A14	IO_L02P_1/A14	P76	DUAL
1	IO_L03N_1/A11	IO_L03N_1/A11	P82	DUAL
1	IO_L03P_1/A12	IO_L03P_1/A12	P81	DUAL
1	IO_L04N_1/A9/RHCLK1	IO_L04N_1/A9/RHCLK1	P86	RHCLK/DUAL
1	IO_L04P_1/A10/RHCLK0	IO_L04P_1/A10/RHCLK0	P85	RHCLK/DUAL
1	IO_L05N_1/A7/RHCLK3/TRDY1	IO_L05N_1/A7/RHCLK3	P88	RHCLK/DUAL
1	IO_L05P_1/A8/RHCLK2	IO_L05P_1/A8/RHCLK2	P87	RHCLK/DUAL
1	IO_L06N_1/A5/RHCLK5	IO_L06N_1/A5/RHCLK5	P92	RHCLK/DUAL
1	IO_L06P_1/A6/RHCLK4/IRDY1	IO_L06P_1/A6/RHCLK4	P91	RHCLK/DUAL
1	IO_L07N_1/A3/RHCLK7	IO_L07N_1/A3/RHCLK7	P94	RHCLK/DUAL
1	IO_L07P_1/A4/RHCLK6	IO_L07P_1/A4/RHCLK6	P93	RHCLK/DUAL
1	IO_L08N_1/A1	IO_L08N_1/A1	P97	DUAL
1	IO_L08P_1/A2	IO_L08P_1/A2	P96	DUAL
1	IO_L09N_1/LDC0	IO_L09N_1/LDC0	P104	DUAL
1	IO_L09P_1/HDC	IO_L09P_1/HDC	P103	DUAL
1	IO_L10N_1/LDC2	IO_L10N_1/LDC2	P106	DUAL
1	IO_L10P_1/LDC1	IO_L10P_1/LDC1	P105	DUAL
1	IP	IP	P78	INPUT
1	IP	IP	P84	INPUT
1	IP	IP	P89	INPUT
1	IP	IP	P101	INPUT
1	IP	IP	P107	INPUT
1	IP/VREF_1	IP/VREF_1	P95	VREF
1	VCCO_1	VCCO_1	P79	VCCO
1	VCCO_1	VCCO_1	P100	VCCO
2	IO/D5	IO/D5	P52	DUAL
2	IO/M1	IO/M1	P60	DUAL
2	IP/VREF_2	IO/VREF_2	P66	***100E:*** VREF(INPUT) ***250E:*** VREF(I/O)
2	IO_L01N_2/INIT_B	IO_L01N_2/INIT_B	P40	DUAL
2	IO_L01P_2/CSO_B	IO_L01P_2/CSO_B	P39	DUAL
2	IO_L02N_2/MOSI/CSI_B	IO_L02N_2/MOSI/CSI_B	P44	DUAL
2	IO_L02P_2/DOUT/BUSY	IO_L02P_2/DOUT/BUSY	P43	DUAL
2	IO_L04N_2/D6/GCLK13	IO_L04N_2/D6/GCLK13	P51	DUAL/GCLK
2	IO_L04P_2/D7/GCLK12	IO_L04P_2/D7/GCLK12	P50	DUAL/GCLK
2	IO_L05N_2/D3/GCLK15	IO_L05N_2/D3/GCLK15	P54	DUAL/GCLK
2	IO_L05P_2/D4/GCLK14	IO_L05P_2/D4/GCLK14	P53	DUAL/GCLK
2	IO_L07N_2/D1/GCLK3	IO_L07N_2/D1/GCLK3	P59	DUAL/GCLK
2	IO_L07P_2/D2/GCLK2	IO_L07P_2/D2/GCLK2	P58	DUAL/GCLK
2	IO_L08N_2/DIN/D0	IO_L08N_2/DIN/D0	P63	DUAL
2	IO_L08P_2/M0	IO_L08P_2/M0	P62	DUAL
2	IO_L09N_2/VS1/A18	IO_L09N_2/VS1/A18	P68	DUAL
2	IO_L09P_2/VS2/A19	IO_L09P_2/VS2/A19	P67	DUAL
2	IO_L10N_2/CCLK	IO_L10N_2/CCLK	P71	DUAL
2	IO_L10P_2/VS0/A17	IO_L10P_2/VS0/A17	P70	DUAL

User I/Os by Bank

Table 138 and Table 139 indicate how the 108 available user-I/O pins are distributed between the four I/O banks on the TQ144 package.

Table 138: **User I/Os Per Bank for the XC3S100E in the TQ144 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF(1)	CLK(2)
Top	0	26	9	6	1	2	8
Right	1	28	0	5	21	2	0(2)
Bottom	2	26	0	4	20	2	0(2)
Left	3	28	13	4	0	3	8
TOTAL		**108**	**22**	**19**	**42**	**9**	**16**

Notes:
1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

Table 139: **User I/Os Per Bank for the XC3S250E in TQ144 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF(1)	CLK(2)
Top	0	26	9	6	1	2	8
Right	1	28	0	5	21	2	0(2)
Bottom	2	26	0	4	20	2	0(2)
Left	3	28	11	6	0	3	8
TOTAL		**108**	**20**	**21**	**42**	**9**	**16**

Notes:
1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

Footprint Migration Differences

Table 140 summarizes any footprint and functionality differences between the XC3S100E and the XC3S250E FPGAs that may affect easy migration between devices. There are four such pins. All other pins not listed in Table 140 unconditionally migrate between Spartan-3E devices available in the TQ144 package.

The arrows indicate the direction for easy migration. For example, a left-facing arrow indicates that the pin on the XC3S250E unconditionally migrates to the pin on the XC3S100E. It may be possible to migrate the opposite direction depending on the I/O configuration. For example, an I/O pin (Type = I/O) can migrate to an input-only pin (Type = INPUT) if the I/O pin is configured as an input.

Table 140: **TQ144 Footprint Migration Differences**

TQ144 Pin	Bank	XC3S100E Type	Migration	XC3S250E Type
P10	3	I/O	←	INPUT
P29	3	I/O	←	INPUT
P31	3	VREF(INPUT)	→	VREF(I/O)
P66	2	VREF(INPUT)	→	VREF(I/O)
DIFFERENCES			**4**	

Legend:

→	This pin can unconditionally migrate from the device on the left to the device on the right. Migration in the other direction may be possible depending on how the pin is configured for the device on the right.
←	This pin can unconditionally migrate from the device on the right to the device on the left. Migration in the other direction may be possible depending on how the pin is configured for the device on the left.

TQ144 Footprint

Note pin 1 indicator in top-left corner and logo orientation.
Double arrows (←→) indicates a pinout migration difference between the XC3S100E and XC3S250E.

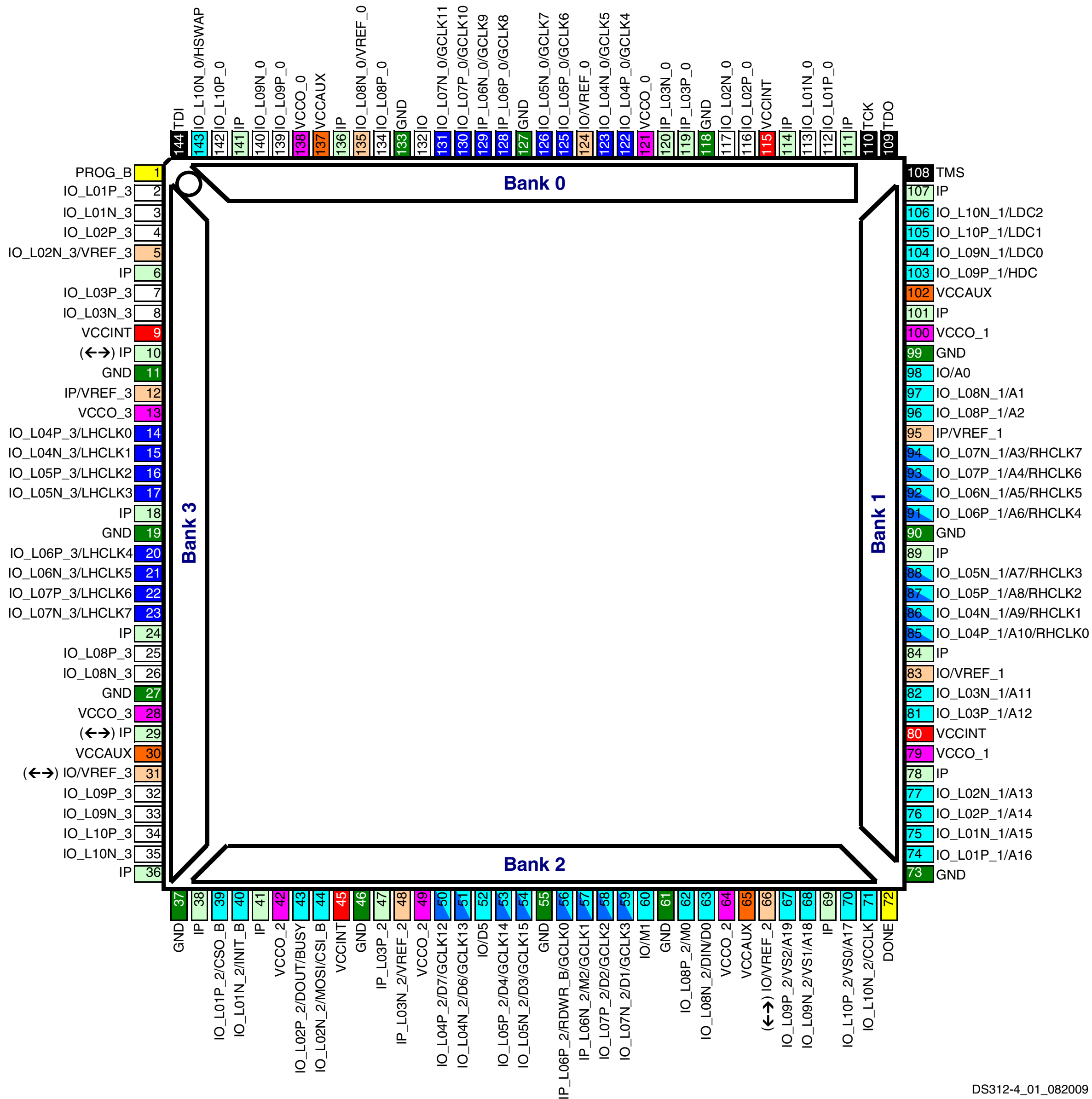

Figure 82: **TQ144 Package Footprint (top view)**

20	**I/O:** Unrestricted, general-purpose user I/O	42	**DUAL:** Configuration pin, then possible user I/O	9	**VREF:** User I/O or input voltage reference for bank
21	**INPUT:** Unrestricted, general-purpose input pin	16	**CLK:** User I/O, input, or global buffer input	9	**VCCO:** Output voltage supply for bank
2	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	4	**VCCINT:** Internal core supply voltage (+1.2V)
0	**N.C.:** Not connected	13	**GND:** Ground	4	**VCCAUX:** Auxiliary supply voltage (+2.5V)

FT256: 256-ball Fine-pitch, Thin Ball Grid Array

The 256-ball fine-pitch, thin ball grid array package, FT256, supports three different Spartan-3E FPGAs, including the XC3S250E, the XC3S500E, and the XC3S1200E.

Table 143 lists all the package pins. They are sorted by bank number and then by pin name of the largest device. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The highlighted rows indicate pinout differences between the XC3S250E, the XC3S500E, and the XC3S1200E FPGAs. The XC3S250E has 18 unconnected balls, indicated as N.C. (No Connection) in Table 143 and with the black diamond character (◆) in Table 143 and Figure 83.

If the table row is highlighted in tan, then this is an instance where an unconnected pin on the XC3S250E FPGA maps to a VREF pin on the XC3S500E and XC3S1200E FPGA. If the FPGA application uses an I/O standard that requires a VREF voltage reference, connect the highlighted pin to the VREF voltage supply, even though this does not actually connect to the XC3S250E FPGA. This VREF connection on the board allows future migration to the larger devices without modifying the printed-circuit board.

All other balls have nearly identical functionality on all three devices. Table 147 summarizes the Spartan-3E footprint migration differences for the FT256 package.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx web site at:

http://www.xilinx.com/support/documentation/data_sheets/s3e_pin.zip

Pinout Table

Table 143: **FT256 Package Pinout**

Bank	XC3S250E Pin Name	XC3S500E Pin Name	XC3S1200E Pin Name	FT256 Ball	Type
0	IO	IO	IO	A7	I/O
0	IO	IO	IO	A12	I/O
0	IO	IO	IO	B4	I/O
0	IP	IP	IO	B6	***250E:*** INPUT ***500E:*** INPUT ***1200E:*** I/O
0	IP	IP	IO	B10	***250E:*** INPUT ***500E:*** INPUT ***1200E:*** I/O
0	IO/VREF_0	IO/VREF_0	IO/VREF_0	D9	VREF
0	IO_L01N_0	IO_L01N_0	IO_L01N_0	A14	I/O
0	IO_L01P_0	IO_L01P_0	IO_L01P_0	B14	I/O
0	IO_L03N_0/VREF_0	IO_L03N_0/VREF_0	IO_L03N_0/VREF_0	A13	VREF
0	IO_L03P_0	IO_L03P_0	IO_L03P_0	B13	I/O
0	IO_L04N_0	IO_L04N_0	IO_L04N_0	E11	I/O
0	IO_L04P_0	IO_L04P_0	IO_L04P_0	D11	I/O
0	IO_L05N_0/VREF_0	IO_L05N_0/VREF_0	IO_L05N_0/VREF_0	B11	VREF
0	IO_L05P_0	IO_L05P_0	IO_L05P_0	C11	I/O
0	IO_L06N_0	IO_L06N_0	IO_L06N_0	E10	I/O
0	IO_L06P_0	IO_L06P_0	IO_L06P_0	D10	I/O
0	IO_L08N_0/GCLK5	IO_L08N_0/GCLK5	IO_L08N_0/GCLK5	F9	GCLK
0	IO_L08P_0/GCLK4	IO_L08P_0/GCLK4	IO_L08P_0/GCLK4	E9	GCLK
0	IO_L09N_0/GCLK7	IO_L09N_0/GCLK7	IO_L09N_0/GCLK7	A9	GCLK
0	IO_L09P_0/GCLK6	IO_L09P_0/GCLK6	IO_L09P_0/GCLK6	A10	GCLK
0	IO_L11N_0/GCLK11	IO_L11N_0/GCLK11	IO_L11N_0/GCLK11	D8	GCLK
0	IO_L11P_0/GCLK10	IO_L11P_0/GCLK10	IO_L11P_0/GCLK10	C8	GCLK
0	IO_L12N_0	IO_L12N_0	IO_L12N_0	F8	I/O

Table 154: **FG484 Package Pinout *(Cont'd)***

Bank	XC3S1600E Pin Name	FG484 Ball	Type
0	IP	E6	INPUT
0	IP_L02N_0	D17	INPUT
0	IP_L02P_0	D18	INPUT
0	IP_L05N_0	C17	INPUT
0	IP_L05P_0	B17	INPUT
0	IP_L08N_0	E15	INPUT
0	IP_L08P_0	D15	INPUT
0	IP_L14N_0	D13	INPUT
0	IP_L14P_0	C13	INPUT
0	IP_L17N_0	A12	INPUT
0	IP_L17P_0	A13	INPUT
0	IP_L20N_0/GCLK9	H11	GCLK
0	IP_L20P_0/GCLK8	H12	GCLK
0	IP_L23N_0	F10	INPUT
0	IP_L23P_0	F11	INPUT
0	IP_L26N_0	G9	INPUT
0	IP_L26P_0	G10	INPUT
0	IP_L31N_0	C8	INPUT
0	IP_L31P_0	D8	INPUT
0	IP_L34N_0	C7	INPUT
0	IP_L34P_0	C6	INPUT
0	IP_L37N_0	A3	INPUT
0	IP_L37P_0	A2	INPUT
0	VCCO_0	B5	VCCO
0	VCCO_0	B10	VCCO
0	VCCO_0	B14	VCCO
0	VCCO_0	B18	VCCO
0	VCCO_0	E8	VCCO
0	VCCO_0	F14	VCCO
0	VCCO_0	G11	VCCO
1	IO_L01N_1/A15	Y22	DUAL
1	IO_L01P_1/A16	AA22	DUAL
1	IO_L02N_1/A13	W21	DUAL
1	IO_L02P_1/A14	Y21	DUAL
1	IO_L03N_1/VREF_1	W20	VREF
1	IO_L03P_1	V20	I/O
1	IO_L04N_1	U19	I/O
1	IO_L04P_1	V19	I/O
1	IO_L05N_1	V22	I/O
1	IO_L05P_1	W22	I/O
1	IO_L06N_1	T19	I/O
1	IO_L06P_1	T18	I/O
1	IO_L07N_1/VREF_1	U20	VREF
1	IO_L07P_1	U21	I/O

Table 154: **FG484 Package Pinout *(Cont'd)***

Bank	XC3S1600E Pin Name	FG484 Ball	Type
1	IO_L08N_1	T22	I/O
1	IO_L08P_1	U22	I/O
1	IO_L09N_1	R19	I/O
1	IO_L09P_1	R18	I/O
1	IO_L10N_1	R16	I/O
1	IO_L10P_1	T16	I/O
1	IO_L11N_1	R21	I/O
1	IO_L11P_1	R20	I/O
1	IO_L12N_1/VREF_1	P18	VREF
1	IO_L12P_1	P17	I/O
1	IO_L13N_1	P22	I/O
1	IO_L13P_1	R22	I/O
1	IO_L14N_1	P15	I/O
1	IO_L14P_1	P16	I/O
1	IO_L15N_1	N18	I/O
1	IO_L15P_1	N19	I/O
1	IO_L16N_1/A11	N16	DUAL
1	IO_L16P_1/A12	N17	DUAL
1	IO_L17N_1/VREF_1	M20	VREF
1	IO_L17P_1	N20	I/O
1	IO_L18N_1/A9/RHCLK1	M22	RHCLK/ DUAL
1	IO_L18P_1/A10/RHCLK0	N22	RHCLK/ DUAL
1	IO_L19N_1/A7/RHCLK3/ TRDY1	M16	RHCLK/ DUAL
1	IO_L19P_1/A8/RHCLK2	M15	RHCLK/ DUAL
1	IO_L20N_1/A5/RHCLK5	L21	RHCLK/ DUAL
1	IO_L20P_1/A6/RHCLK4/ IRDY1	L20	RHCLK/ DUAL
1	IO_L21N_1/A3/RHCLK7	L19	RHCLK/ DUAL
1	IO_L21P_1/A4/RHCLK6	L18	RHCLK/ DUAL
1	IO_L22N_1/A1	K22	DUAL
1	IO_L22P_1/A2	L22	DUAL
1	IO_L23N_1/A0	K17	DUAL
1	IO_L23P_1	K16	I/O
1	IO_L24N_1	K19	I/O
1	IO_L24P_1	K18	I/O
1	IO_L25N_1	K15	I/O
1	IO_L25P_1	J15	I/O
1	IO_L26N_1	J20	I/O
1	IO_L26P_1	J21	I/O

Table 154: **FG484 Package Pinout *(Cont'd)***

Bank	XC3S1600E Pin Name	FG484 Ball	Type
3	IO_L11N_3	H1	I/O
3	IO_L11P_3	J1	I/O
3	IO_L12N_3	J6	I/O
3	IO_L12P_3	J5	I/O
3	IO_L13N_3/VREF_3	J3	VREF
3	IO_L13P_3	K3	I/O
3	IO_L14N_3	J8	I/O
3	IO_L14P_3	K8	I/O
3	IO_L15N_3	K4	I/O
3	IO_L15P_3	K5	I/O
3	IO_L16N_3	K1	I/O
3	IO_L16P_3	L1	I/O
3	IO_L17N_3	L7	I/O
3	IO_L17P_3	K7	I/O
3	IO_L18N_3/LHCLK1	L5	LHCLK
3	IO_L18P_3/LHCLK0	M5	LHCLK
3	IO_L19N_3/LHCLK3/IRDY2	M8	LHCLK
3	IO_L19P_3/LHCLK2	L8	LHCLK
3	IO_L20N_3/LHCLK5	N1	LHCLK
3	IO_L20P_3/LHCLK4/TRDY2	M1	LHCLK
3	IO_L21N_3/LHCLK7	M4	LHCLK
3	IO_L21P_3/LHCLK6	M3	LHCLK
3	IO_L22N_3	N6	I/O
3	IO_L22P_3	N7	I/O
3	IO_L23N_3	P8	I/O
3	IO_L23P_3	N8	I/O
3	IO_L24N_3/VREF_3	N4	VREF
3	IO_L24P_3	N5	I/O
3	IO_L25N_3	P2	I/O
3	IO_L25P_3	P1	I/O
3	IO_L26N_3	R7	I/O
3	IO_L26P_3	P7	I/O
3	IO_L27N_3	P6	I/O
3	IO_L27P_3	P5	I/O
3	IO_L28N_3	R2	I/O
3	IO_L28P_3	R1	I/O
3	IO_L29N_3	R3	I/O
3	IO_L29P_3	R4	I/O
3	IO_L30N_3	T6	I/O
3	IO_L30P_3	R6	I/O
3	IO_L31N_3	U2	I/O
3	IO_L31P_3	U1	I/O
3	IO_L32N_3	T4	I/O
3	IO_L32P_3	T5	I/O

Table 154: **FG484 Package Pinout *(Cont'd)***

Bank	XC3S1600E Pin Name	FG484 Ball	Type
3	IO_L33N_3	W1	I/O
3	IO_L33P_3	V1	I/O
3	IO_L34N_3	U4	I/O
3	IO_L34P_3	U3	I/O
3	IO_L35N_3	V4	I/O
3	IO_L35P_3	V3	I/O
3	IO_L36N_3/VREF_3	W3	VREF
3	IO_L36P_3	W2	I/O
3	IO_L37N_3	Y2	I/O
3	IO_L37P_3	Y1	I/O
3	IO_L38N_3	AA1	I/O
3	IO_L38P_3	AA2	I/O
3	IP	F2	INPUT
3	IP	F5	INPUT
3	IP	G3	INPUT
3	IP	H7	INPUT
3	IP	J7	INPUT
3	IP	K2	INPUT
3	IP	K6	INPUT
3	IP	M2	INPUT
3	IP	M6	INPUT
3	IP	N3	INPUT
3	IP	P3	INPUT
3	IP	R8	INPUT
3	IP	T1	INPUT
3	IP	T7	INPUT
3	IP	U5	INPUT
3	IP	W4	INPUT
3	IP/VREF_3	L3	VREF
3	IP/VREF_3	T3	VREF
3	VCCO_3	E2	VCCO
3	VCCO_3	H6	VCCO
3	VCCO_3	J2	VCCO
3	VCCO_3	M7	VCCO
3	VCCO_3	N2	VCCO
3	VCCO_3	R5	VCCO
3	VCCO_3	V2	VCCO
GND	GND	A1	GND
GND	GND	A11	GND
GND	GND	A22	GND
GND	GND	B7	GND
GND	GND	B16	GND
GND	GND	C3	GND
GND	GND	C20	GND