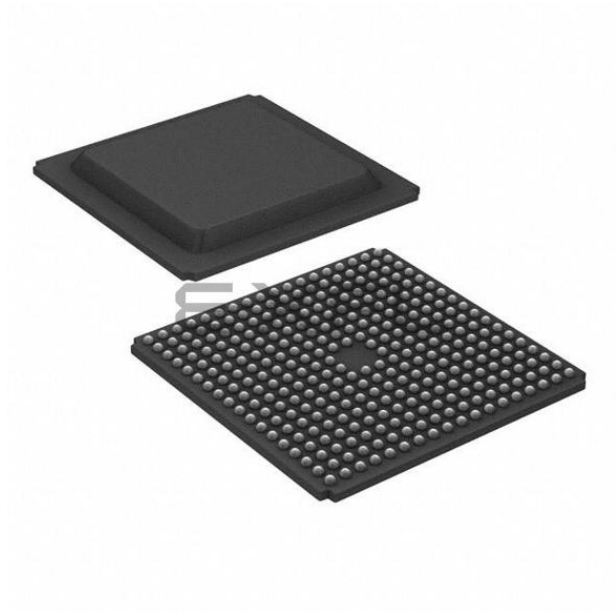
AMD Xilinx - XC3S1600E-4FGG320I Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	3688
Number of Logic Elements/Cells	33192
Total RAM Bits	663552
Number of I/O	250
Number of Gates	1600000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	320-BGA
Supplier Device Package	320-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s1600e-4fgg320i

Package Marking

Figure 2 provides a top marking example for Spartan-3E FPGAs in the quad-flat packages. Figure 3 shows the top marking for Spartan-3E FPGAs in BGA packages except the 132-ball chip-scale package (CP132 and CPG132). The markings for the BGA packages are nearly identical to those for the quad-flat packages, except that the marking is rotated with respect to the ball A1 indicator. Figure 4 shows the top marking for Spartan-3E FPGAs in the CP132 and CPG132 packages.

On the QFP and BGA packages, the optional numerical Stepping Code follows the Lot Code.

The "5C" and "4I" part combinations can have a dual mark of "5C/4I". Devices with a single mark are only guaranteed for the marked speed grade and temperature range. All "5C" and "4I" part combinations use the Stepping 1 production silicon.

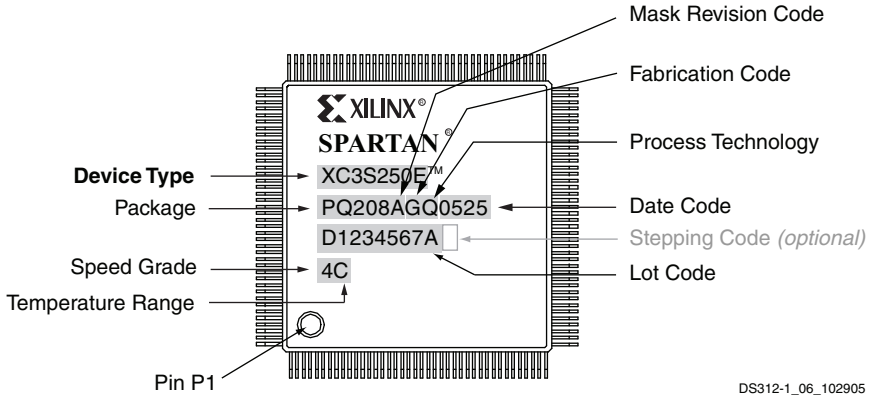


Figure 2: **Spartan-3E QFP Package Marking Example**

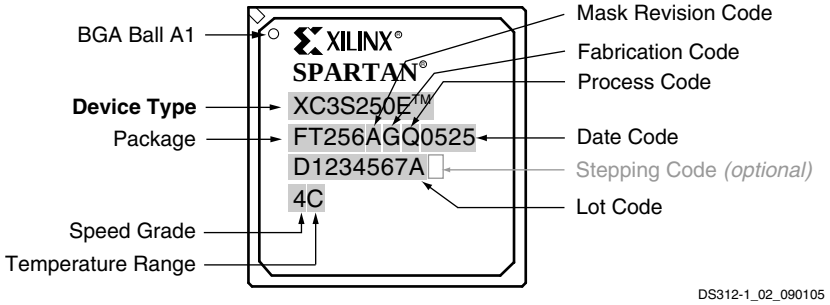


Figure 3: **Spartan-3E BGA Package Marking Example**

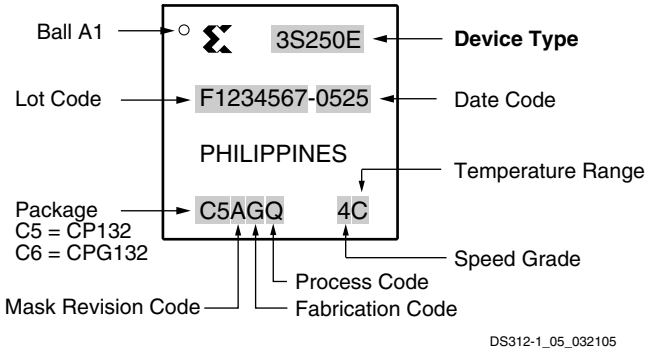


Figure 4: **Spartan-3E CP132 and CPG132 Package Marking Example**

Spartan-3E FPGAs provide additional input flexibility by allowing I/O standards to be mixed in different banks. For a particular V_{CCO} voltage, Table 6 and Table 7 list all of the IOSTANDARDs that can be combined and if the IOSTANDARD is supported as an input only or can be used for both inputs and outputs.

Table 6: **Single-Ended IOSTANDARD Bank Compatibility**

Single-Ended IOSTANDARD	V_{CCO} Supply/Compatibility					Input Requirements	
	1.2V	1.5V	1.8V	2.5V	3.3V	V_{REF}	Board Termination Voltage (V_{TT})
LVTTL	-	-	-	-	Input/ Output	N/R(1)	N/R
LVCMOS33	-	-	-	-	Input/ Output	N/R	N/R
LVCMOS25	-	-	-	Input/ Output	Input	N/R	N/R
LVCMOS18	-	-	Input/ Output	Input	Input	N/R	N/R
LVCMOS15	-	Input/ Output	Input	Input	Input	N/R	N/R
LVCMOS12	Input/ Output	Input	Input	Input	Input	N/R	N/R
PCI33_3	-	-	-	-	Input/ Output	N/R	N/R
PCI66_3	-	-	-	-	Input/ Output	N/R	N/R
HSTL_I_18	-	-	Input/ Output	Input	Input	0.9	0.9
HSTL_III_18	-	-	Input/ Output	Input	Input	1.1	1.8
SSTL18_I	-	-	Input/ Output	Input	Input	0.9	0.9
SSTL2_I	-	-	-	Input/ Output	Input	1.25	1.25

Notes:

1. N/R - Not required for input operation.

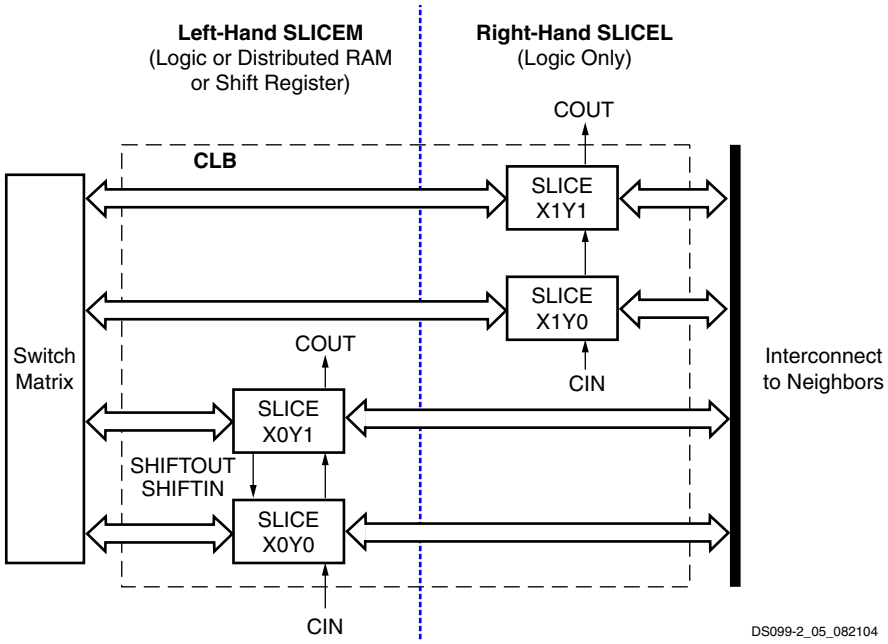


Figure 16: **Arrangement of Slices within the CLB**

Slice Location Designations

The Xilinx development software designates the location of a slice according to its X and Y coordinates, starting in the bottom left corner, as shown in Figure 14. The letter 'X' followed by a number identifies columns of slices, incrementing from the left side of the die to the right. The letter 'Y' followed by a number identifies the position of each slice in a pair as well as indicating the CLB row, incrementing from the bottom of the die. Figure 16 shows the CLB located in the lower left-hand corner of the die. The SLICEM always has an even 'X' number, and the SLICEL always has an odd 'X' number.

Slice Overview

A slice includes two LUT function generators and two storage elements, along with additional logic, as shown in Figure 17.

Both SLICEM and SLICEL have the following elements in common to provide logic, arithmetic, and ROM functions:

- Two 4-input LUT function generators, F and G
- Two storage elements
- Two wide-function multiplexers, F5MUX and FiMUX
- Carry and arithmetic logic

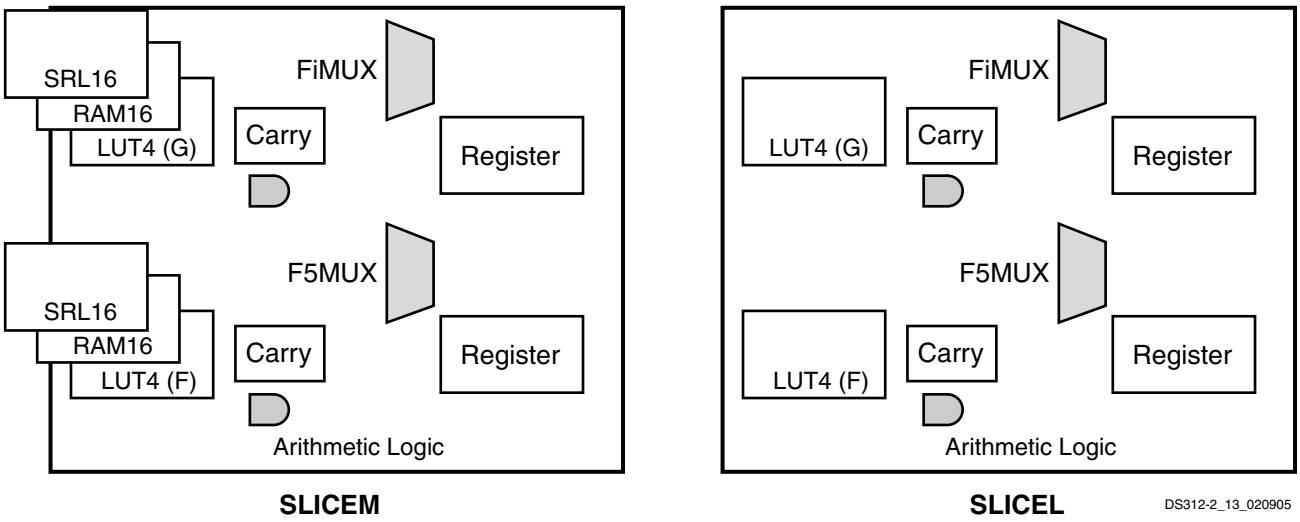


Figure 17: **Resources in a Slice**

Table 14: **Carry Logic Functions *(Cont'd)***

Function	Description
CY0G	Carry generation for top half of slice. Fixed selection of: · G1 or G2 inputs to the LUT (both equal 1 when a carry is to be generated) · GAND gate for multiplication · BY input for carry initialization · Fixed 1 or 0 input for use as a simple Boolean function
CYMUXF	Carry generation or propagation mux for bottom half of slice. Dynamic selection via CYSELF of: · CYINIT carry propagation (CYSELF = 1) · CY0F carry generation (CYSELF = 0)
CYMUXG	Carry generation or propagation mux for top half of slice. Dynamic selection via CYSELF of: · CYMUXF carry propagation (CYSELG = 1) · CY0G carry generation (CYSELG = 0)
CYSELF	Carry generation or propagation select for bottom half of slice. Fixed selection of: · F-LUT output (typically XOR result) · Fixed 1 to always propagate
CYSELG	Carry generation or propagation select for top half of slice. Fixed selection of: · G-LUT output (typically XOR result) · Fixed 1 to always propagate
XORF	Sum generation for bottom half of slice. Inputs from: · F-LUT · CYINIT carry signal from previous stage Result is sent to either the combinatorial or registered output for the top of the slice.
XORG	Sum generation for top half of slice. Inputs from: · G-LUT · CYMUXF carry signal from previous stage Result is sent to either the combinatorial or registered output for the top of the slice.
FAND	Multiplier partial product for bottom half of slice. Inputs: · F-LUT F1 input · F-LUT F2 input Result is sent through CY0F to become the carry generate signal into CYMUXF
GAND	Multiplier partial product for top half of slice. Inputs: · G-LUT G1 input · G-LUT G2 input Result is sent through CY0G to become the carry generate signal into CYMUXG

The basic usage of the carry logic is to generate a half-sum in the LUT via an XOR function, which generates or propagates a carry out COUT via the carry mux CYMUXF (or CYMUXG), and then complete the sum with the dedicated XORF (or XORG) gate and the carry input CIN. This structure allows two bits of an arithmetic function in each slice. The CYMUXF (or CYMUXG) can be instantiated using the MUXCY element, and the XORF (or XORG) can be instantiated using the XORCY element.

The FAND (or GAND) gate is used for partial product multiplication and can be instantiated using the MULT_AND component. Partial products are generated by two-input AND gates and then added. The carry logic is efficient for the adder, but one of the inputs must be outside the LUT as shown in Figure 23.

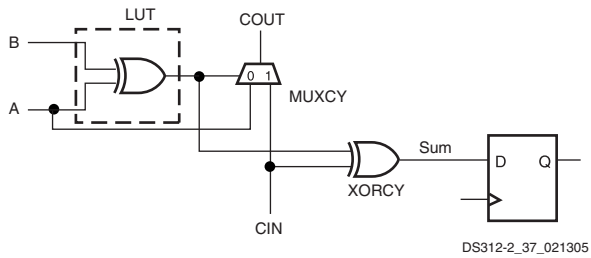
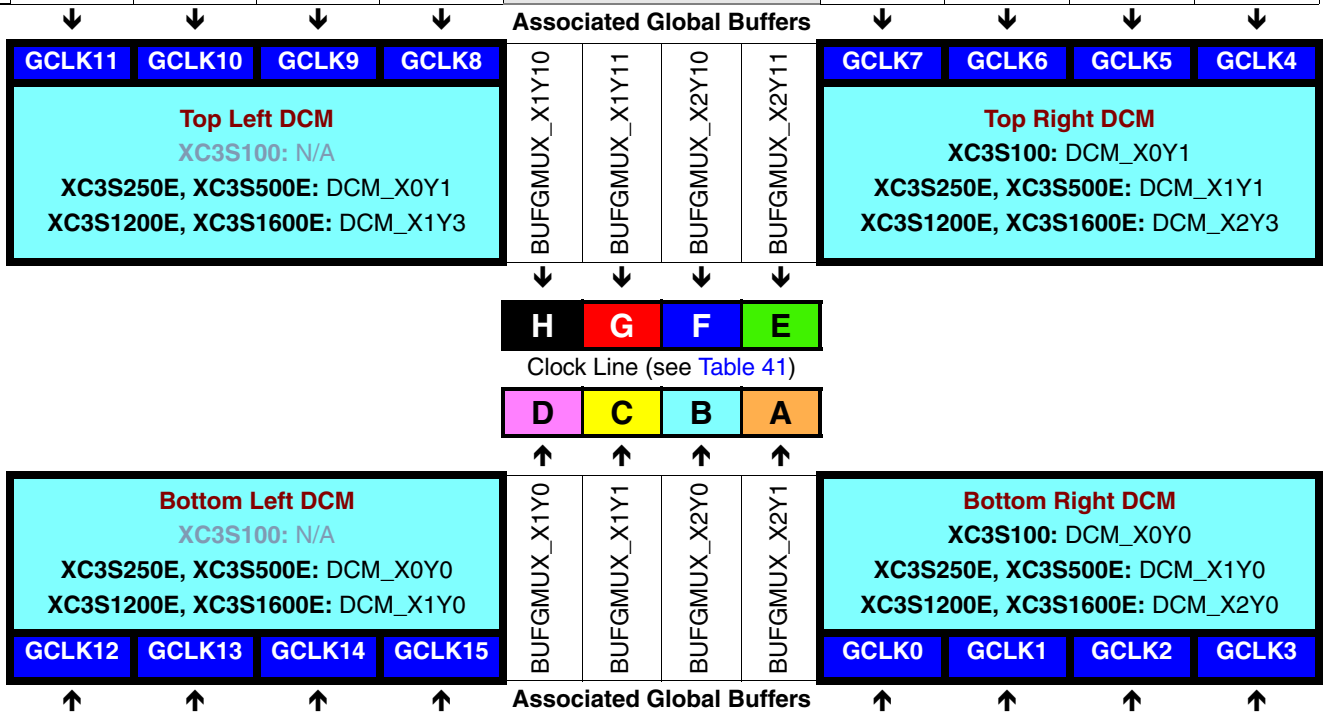


Figure 23: **Using the MUXCY and XORCY in the Carry Logic**

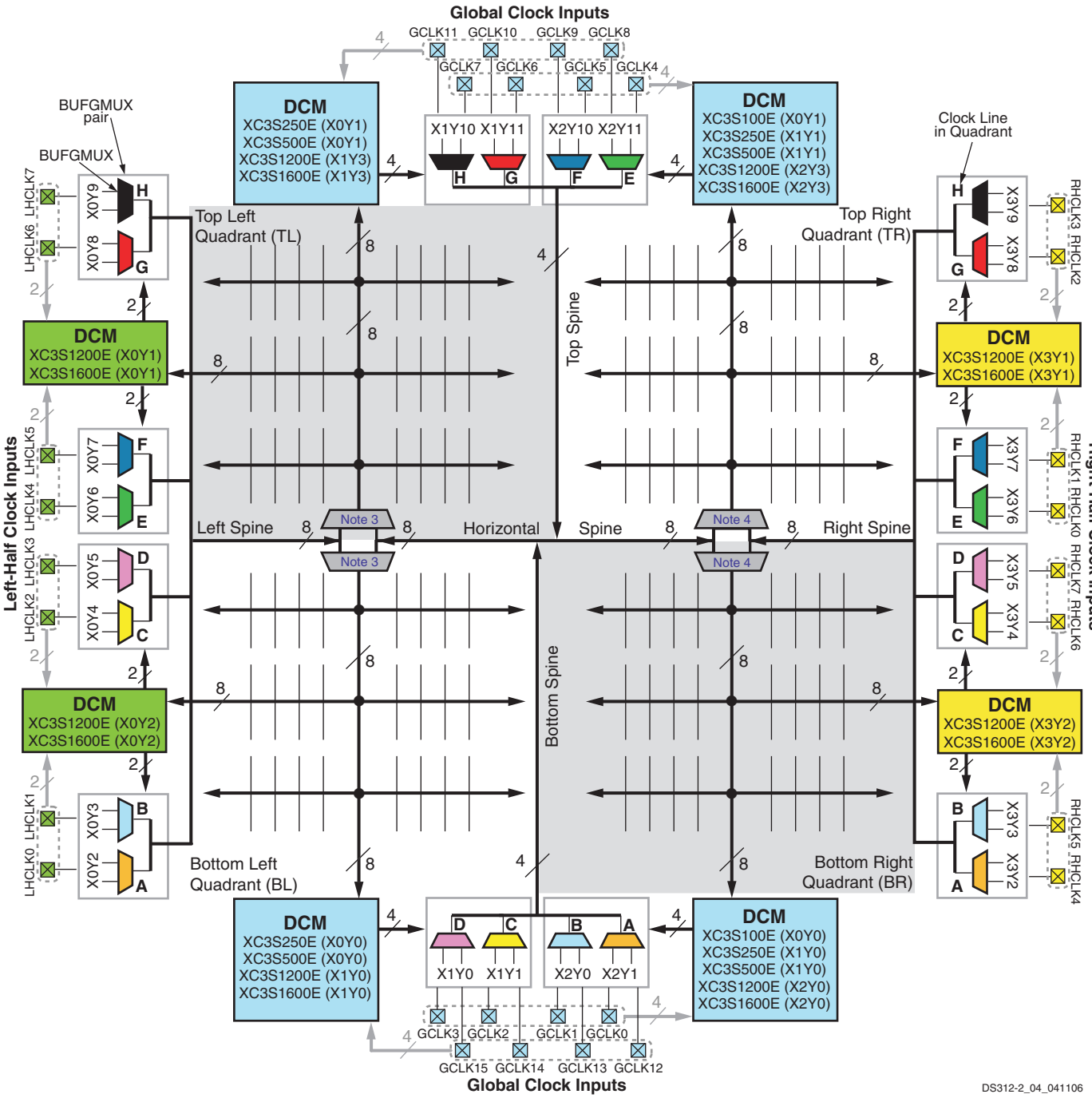
The FAND (or GAND) gate is used to duplicate one of the partial products, while the LUT generates both partial products and the XOR function, as shown in Figure 24.

Table 30: **Direct Clock Input Connections and Optional External Feedback to Associated DCMs**

Package	Differential Pair		Differential Pair			Differential Pair		Differential Pair	
	N	P	N	P		N	P	N	P
	Pin Number for Single-Ended Input					Pin Number for Single-Ended Input			
VQ100	P91	P90	P89	P88		P86	P85	P84	P83
CP132	B7	A7	C8	B8		A9	B9	C9	A10
TQ144	P131	P130	P129	P128		P126	P125	P123	P122
PQ208	P186	P185	P184	P183		P181	P180	P178	P177
FT256	D8	C8	B8	A8		A9	A10	F9	E9
FG320	D9	C9	B9	B8		A10	B10	E10	D10
FG400	A9	A10	G10	H10		E10	E11	G11	F11
FG484	B11	C11	H11	H12		C12	B12	E12	F12



Package	Differential Pair		Differential Pair			Differential Pair		Differential Pair	
	P	N	P	N		P	N	P	N
	Pin Number for Single-Ended Input					Pin Number for Single-Ended Input			
VQ100	P32	P33	P35	P36		P38	P39	P40	P41
CP132	M4	N4	M5	N5		M6	N6	P6	P7
TQ144	P50	P51	P53	P54		P56	P57	P58	P59
PQ208	P74	P75	P77	P78		P80	P81	P82	P83
FT256	M8	L8	N8	P8		T9	R9	P9	N9
FG320	N9	M9	U9	V9		U10	T10	R10	P10
FG400	W9	W10	R10	P10		P11	P12	V10	V11
FG484	V11	U11	R11	T11		R12	P12	Y12	W12



Notes:

1. The diagram presents electrical connectivity. The diagram locations do not necessarily match the physical location on the device, although the coordinate locations shown are correct.
2. Number of DCMs and locations of these DCM varies for different device densities. The left and right DCMs are only in the XC3S1200E and XC3S1600E. The XC3S100E has only two DCMs, one on the top right and one on the bottom right of the die.
3. See Figure 47a, which shows how the eight clock lines are multiplexed on the left-hand side of the device.
4. See Figure 47b, which shows how the eight clock lines are multiplexed on the right-hand side of the device.
5. For best direct clock inputs to a particular clock buffer, not a DCM, see Table 41.
6. For best direct clock inputs to a particular DCM, not a BUFGMUX, see Table 30, Table 31, and Table 32. Direct pin inputs to a DCM are shown in gray.

Figure 45: **Spartan-3E Internal Quadrant-Based Clock Network (Electrical Connectivity View)**

(P) Similarly, the FPGA's HSWAP pin must be Low to enable pull-up resistors on all user-I/O pins during configuration or High to disable the pull-up resistors. The HSWAP control must remain at a constant logic level throughout FPGA configuration. After configuration, when the FPGA's DONE output goes High, the HSWAP pin is available as full-featured user-I/O pin and is powered by the VCCO_0 supply.

The FPGA's DOUT pin is used in daisy-chain applications, described later. In a single-FPGA application, the FPGA's DOUT pin is not used but is actively driving during the configuration process.

Table 50: **Serial Master Mode Connections**

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
HSWAP (P)	Input	**User I/O Pull-Up Control**. When Low during configuration, enables pull-up resistors in all I/O pins to respective I/O bank V_{CCO} input. 0: Pull-ups during configuration 1: No pull-ups	Drive at valid logic level throughout configuration.	User I/O
M[2:0]	Input	**Mode Select**. Selects the FPGA configuration mode. See Design Considerations for the HSWAP, M[2:0], and VS[2:0] Pins.	M2 = 0, M1 = 0, M0 = 0. Sampled when INIT_B goes High.	User I/O
DIN	Input	**Serial Data Input**.	Receives serial data from PROM's D0 output.	User I/O
CCLK	Output	**Configuration Clock**. Generated by FPGA internal oscillator. Frequency controlled by ***ConfigRate*** bitstream generator option. If CCLK PCB trace is long or has multiple connections, terminate this output to maintain signal integrity. See CCLK Design Considerations.	Drives PROM's CLK clock input.	User I/O
DOUT	Output	**Serial Data Output**.	Actively drives. Not used in single-FPGA designs. In a daisy-chain configuration, this pin connects to DIN input of the next FPGA in the chain.	User I/O
INIT_B	Open-drain bidirectional I/O	**Initialization Indicator**. Active Low. Goes Low at start of configuration during Initialization memory clearing process. Released at end of memory clearing, when mode select pins are sampled. Requires external 4.7 kΩ pull-up resistor to VCCO_2.	Connects to PROM's OE/RESET input. FPGA clears PROM's address counter at start of configuration, enables outputs during configuration. PROM also holds FPGA in Initialization state until PROM reaches Power-On Reset (POR) state. If CRC error detected during configuration, FPGA drives INIT_B Low.	User I/O. If unused in the application, drive INIT_B High.
DONE	Open-drain bidirectional I/O	**FPGA Configuration Done**. Low during configuration. Goes High when FPGA successfully completes configuration. Requires external 330 Ω pull-up resistor to 2.5V.	Connects to PROM's chip-enable (CE) input. Enables PROM during configuration. Disables PROM after configuration.	Pulled High via external pull-up. When High, indicates that the FPGA successfully configured.
PROG_B	Input	**Program FPGA**. Active Low. When asserted Low for 500 ns or longer, forces the FPGA to restart its configuration process by clearing configuration memory and resetting the DONE and INIT_B pins once PROG_B returns High. Recommend external 4.7 kΩ pull-up resistor to 2.5V. Internal pull-up value may be weaker (see Table 78). If driving externally with a 3.3V output, use an open-drain or open-collector driver or use a current limiting series resistor.	Must be High during configuration to allow configuration to start. Connects to PROM's CF pin, allowing JTAG PROM programming algorithm to reprogram the FPGA.	Drive PROG_B Low and release to reprogram FPGA.

Voltage Compatibility

Available SPI Flash PROMs use a single 3.3V supply voltage. All of the FPGA's SPI Flash interface signals are within I/O Bank 2. Consequently, the FPGA's VCCO_2 supply voltage must also be 3.3V to match the SPI Flash PROM.

Power-On Precautions if 3.3V Supply is Last in Sequence

Spartan-3E FPGAs have a built-in power-on reset (POR) circuit, as shown in Figure 66, page 102. The FPGA waits for its three power supplies — V_{CCINT}, V_{CCAUX}, and V_{CCO} to I/O Bank 2 (VCCO_2) — to reach their respective power-on thresholds before beginning the configuration process.

The SPI Flash PROM is powered by the same voltage supply feeding the FPGA's VCCO_2 voltage input, typically 3.3V. SPI Flash PROMs specify that they cannot be accessed until their V_{CC} supply reaches its minimum data sheet voltage, followed by an additional delay. For some devices, this additional delay is as little as 10 µs as shown in Table 56. For other vendors, this delay is as much as 20 ms.

Table 56: **Example Minimum Power-On to Select Times for Various SPI Flash PROMs**

Vendor	SPI Flash PROM Part Number	Data Sheet Minimum Time from V_{CC} min to Select = Low		
		Symbol	Value	Units
STMicroelectronics	M25Pxx	T_{VSL}	10	µs
Spansion	S25FLxxxA	t_{PU}	10	ms
NexFlash	NX25xx	T_{VSL}	10	µs
Macronix	MX25Lxxxx	t_{VSL}	10	µs
Silicon Storage Technology	SST25LFxx	$T_{PU-READ}$	10	µs
Programmable Microelectronics Corporation	Pm25LVxxx	T_{VCS}	50	µs
Atmel Corporation	AT45DBxxxD	t_{VCSL}	30	µs
	AT45DBxxxB		20	ms

In many systems, the 3.3V supply feeding the FPGA's VCCO_2 input is valid before the FPGA's other V_{CCINT} and V_{CCAUX} supplies, and consequently, there is no issue. However, if the 3.3V supply feeding the FPGA's VCCO_2 supply is last in the sequence, a potential race occurs between the FPGA and the SPI Flash PROM, as shown in Figure 55.

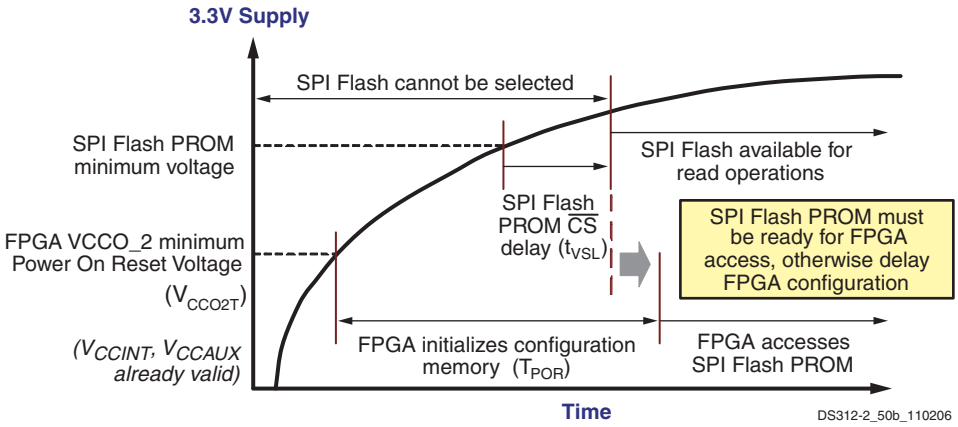


Figure 55: **SPI Flash PROM/FPGA Power-On Timing if 3.3V Supply is Last in Power-On Sequence**

If the FPGA's V_{CCINT} and V_{CCAUX} supplies are already valid, then the FPGA waits for VCCO_2 to reach its minimum threshold voltage before starting configuration. This threshold voltage is labeled as V_{CCO2T} in Table 74 of Module 3 and ranges from approximately 0.4V to 1.0V, substantially lower than the SPI Flash PROM's minimum voltage. Once all three FPGA supplies reach their respective Power On Reset (POR) thresholds, the FPGA starts the configuration process and begins initializing its internal configuration memory. Initialization requires approximately 1 ms (T_{POR}, minimum in Table 111 of Module 3, after which the FPGA de-asserts INIT_B, selects the SPI Flash PROM, and starts sending the appropriate read command. The SPI Flash PROM must be ready for

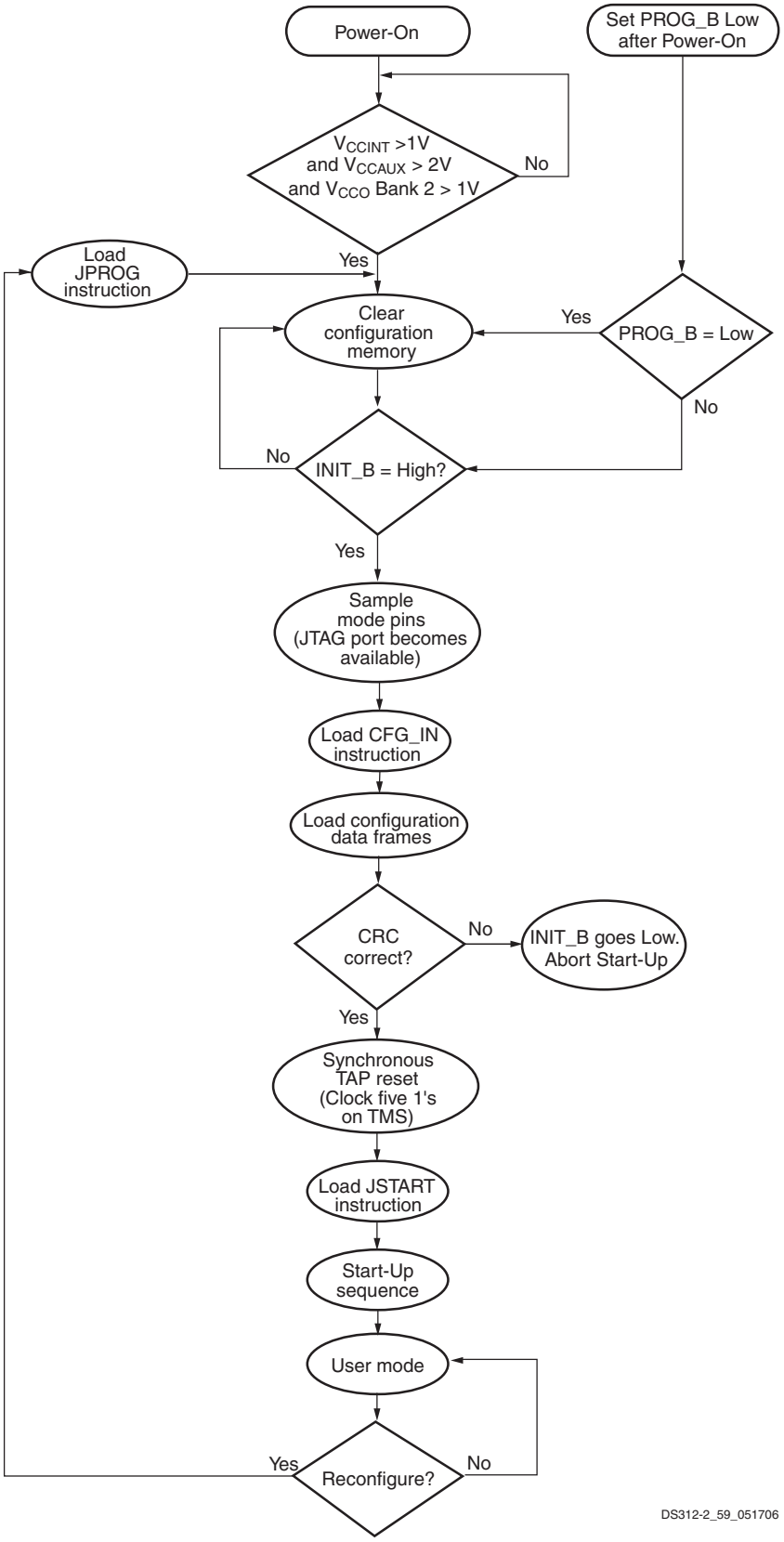


Figure 67: **Boundary-Scan Configuration Flow Diagram**

Table 99: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	-5		-4		Units
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{SHCKO}	Time from the active edge at the CLK input to data appearing on the distributed RAM output	-	2.05	-	2.35	ns
Setup Times						
T_{DS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the distributed RAM	0.40	-	0.46	-	ns
T_{AS}	Setup time of the F/G address inputs before the active transition at the CLK input of the distributed RAM	0.46	-	0.52	-	ns
T_{WS}	Setup time of the write enable input before the active transition at the CLK input of the distributed RAM	0.34	-	0.40	-	ns
Hold Times						
T_{DH}	Hold time of the BX, BY data inputs after the active transition at the CLK input of the distributed RAM	0.13	-	0.15	-	ns
T_{AH}, T_{WH}	Hold time of the F/G address inputs or the write enable input after the active transition at the CLK input of the distributed RAM	0	-	0	-	ns
Clock Pulse Width						
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	0.88	-	1.01	-	ns

Table 100: **CLB Shift Register Switching Characteristics**

Symbol	Description	-5		-4		Units
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{REG}	Time from the active edge at the CLK input to data appearing on the shift register output	-	3.62	-	4.16	ns
Setup Times						
T_{SRLDS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the shift register	0.41	-	0.46	-	ns
Hold Times						
T_{SRLDH}	Hold time of the BX or BY data input after the active transition at the CLK input of the shift register	0.14	-	0.16	-	ns
Clock Pulse Width						
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	0.88	-	1.01	-	ns

Clock Buffer/Multiplexer Switching Characteristics

Table 101: **Clock Distribution Switching Characteristics**

Description	Symbol	Maximum		Units
		Speed Grade		
		-5	-4	
Global clock buffer (BUFG, BUFGMUX, BUFGCE) I input to O-output delay	T_{GIO}	1.46	1.46	ns
Global clock multiplexer (BUFGMUX) select S-input setup to I0 and I1 inputs. Same as BUFGCE enable CE-input	T_{GSI}	0.55	0.63	ns
Frequency of signals distributed on global buffers (all sides)	F_{BUFG}	333	311	MHz

Byte Peripheral Interface (BPI) Configuration Timing

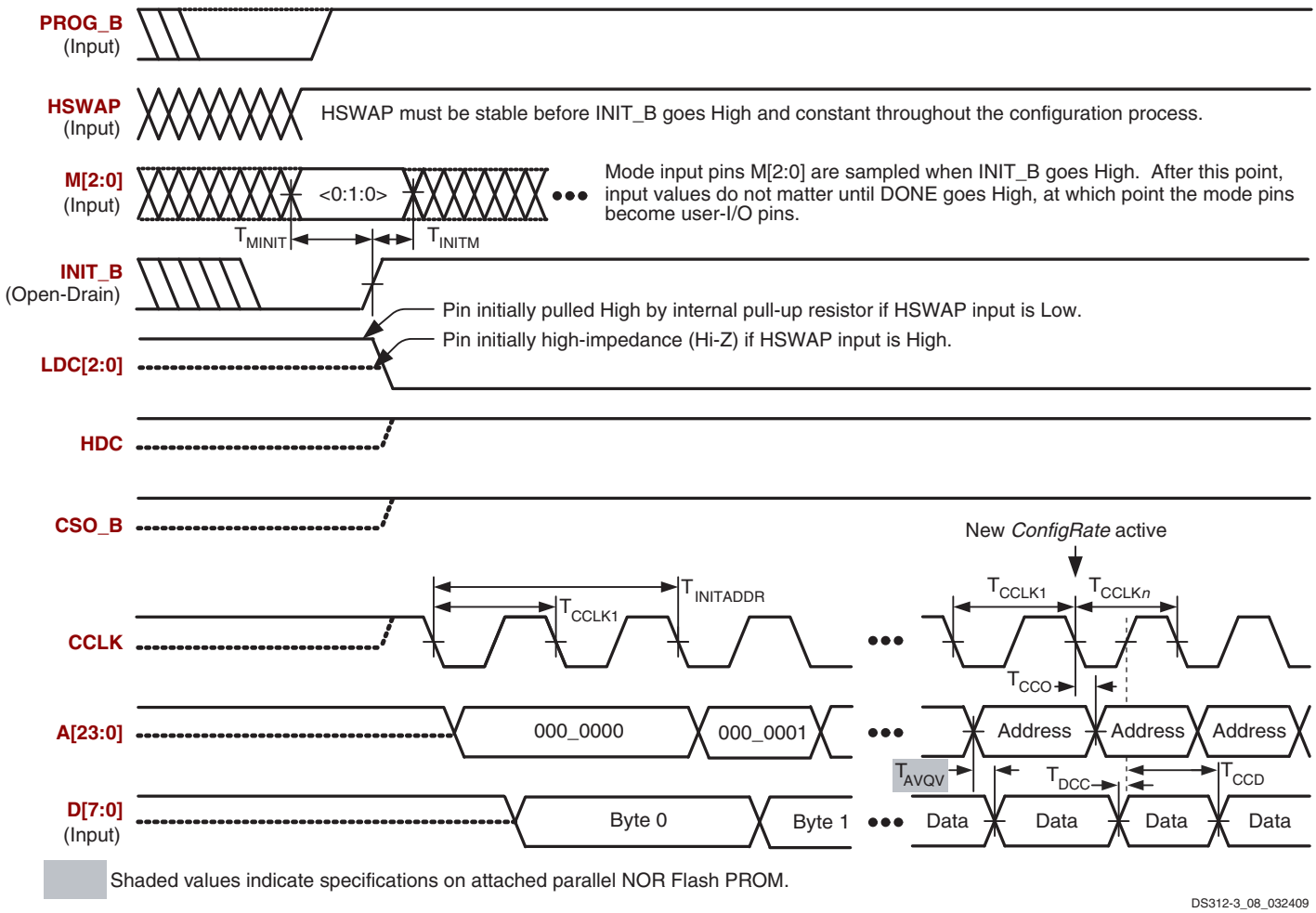


Figure 77: **Waveforms for Byte-wide Peripheral Interface (BPI) Configuration (BPI-DN mode shown)**

Table 120: **Timing for Byte-wide Peripheral Interface (BPI) Configuration Mode**

Symbol	Description		Minimum	Maximum	Units
T_{CCLK1}	Initial CCLK clock period		See Table 112		
T_{CCLKn}	CCLK clock period after FPGA loads ConfigRate setting		See Table 112		
T_{MINIT}	Setup time on CSI_B, RDWR_B, and M[2:0] mode pins before the rising edge of INIT_B		50	-	ns
T_{INITM}	Hold time on CSI_B, RDWR_B, and M[2:0] mode pins after the rising edge of INIT_B		0	-	ns
$T_{INITADDR}$	Minimum period of initial A[23:0] address cycle; LDC[2:0] and HDC are asserted and valid	BPI-UP: (M[2:0] = <0:1:0>)	5	5	T_{CCLK1} cycles
		BPI-DN: (M[2:0] = <0:1:1>)	2	2	
T_{CCO}	Address A[23:0] outputs valid after CCLK falling edge		See Table 116		
T_{DCC}	Setup time on D[7:0] data inputs before CCLK rising edge		See Table 116		
T_{CCD}	Hold time on D[7:0] data inputs after CCLK rising edge		See Table 116		

TQ144 Footprint

Note pin 1 indicator in top-left corner and logo orientation.
Double arrows (↔) indicates a pinout migration difference between the XC3S100E and XC3S250E.

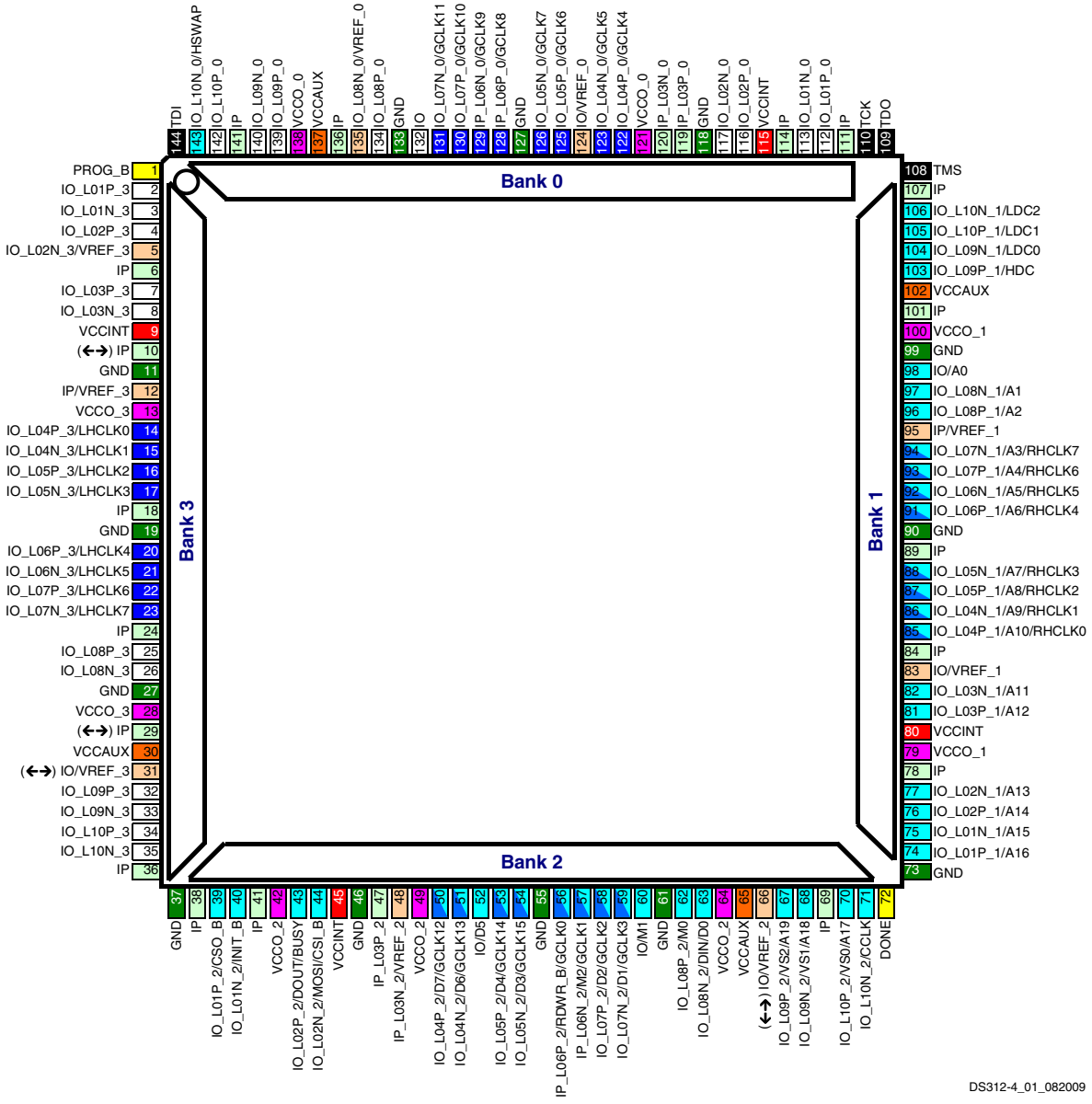


Figure 82: **TQ144 Package Footprint (top view)**

20	**I/O:** Unrestricted, general-purpose user I/O	42	**DUAL:** Configuration pin, then possible user I/O	9	**VREF:** User I/O or input voltage reference for bank
21	**INPUT:** Unrestricted, general-purpose input pin	16	**CLK:** User I/O, input, or global buffer input	9	**VCCO:** Output voltage supply for bank
2	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	4	**VCCINT:** Internal core supply voltage (+1.2V)
0	**N.C.:** Not connected	13	**GND:** Ground	4	**VCCAUX:** Auxiliary supply voltage (+2.5V)

Table 141: **PQ208 Package Pinout *(Cont'd)***

Bank	XC3S250E XC3S500E Pin Name	PQ208 Pin	Type
1	IO_L15N_1/LDC0	P151	DUAL
1	IO_L15P_1/HDC	P150	DUAL
1	IO_L16N_1/LDC2	P153	DUAL
1	IO_L16P_1/LDC1	P152	DUAL
1	IP	P110	INPUT
1	IP	P118	INPUT
1	IP	P124	INPUT
1	IP	P130	INPUT
1	IP	P142	INPUT
1	IP	P148	INPUT
1	IP	P154	INPUT
1	IP/VREF_1	P136	VREF
1	VCCO_1	P114	VCCO
1	VCCO_1	P125	VCCO
1	VCCO_1	P143	VCCO
2	IO/D5	P76	DUAL
2	IO/M1	P84	DUAL
2	IO/VREF_2	P98	VREF
2	IO_L01N_2/INIT_B	P56	DUAL
2	IO_L01P_2/CSO_B	P55	DUAL
2	IO_L03N_2/MOSI/CSI_B	P61	DUAL
2	IO_L03P_2/DOUT/BUSY	P60	DUAL
2	IO_L04N_2	P63	I/O
2	IO_L04P_2	P62	I/O
2	IO_L05N_2	P65	I/O
2	IO_L05P_2	P64	I/O
2	IO_L06N_2	P69	I/O
2	IO_L06P_2	P68	I/O
2	IO_L08N_2/D6/GCLK13	P75	DUAL/GCLK
2	IO_L08P_2/D7/GCLK12	P74	DUAL/GCLK
2	IO_L09N_2/D3/GCLK15	P78	DUAL/GCLK
2	IO_L09P_2/D4/GCLK14	P77	DUAL/GCLK
2	IO_L11N_2/D1/GCLK3	P83	DUAL/GCLK
2	IO_L11P_2/D2/GCLK2	P82	DUAL/GCLK
2	IO_L12N_2/DIN/D0	P87	DUAL
2	IO_L12P_2/M0	P86	DUAL
2	IO_L13N_2	P90	I/O
2	IO_L13P_2	P89	I/O
2	IO_L14N_2/A22	P94	DUAL
2	IO_L14P_2/A23	P93	DUAL
2	IO_L15N_2/A20	P97	DUAL
2	IO_L15P_2/A21	P96	DUAL
2	IO_L16N_2/VS1/A18	P100	DUAL

Table 141: **PQ208 Package Pinout *(Cont'd)***

Bank	XC3S250E XC3S500E Pin Name	PQ208 Pin	Type
2	IO_L16P_2/VS2/A19	P99	DUAL
2	IO_L17N_2/CCLK	P103	DUAL
2	IO_L17P_2/VS0/A17	P102	DUAL
2	IP	P54	INPUT
2	IP	P91	INPUT
2	IP	P101	INPUT
2	IP_L02N_2	P58	INPUT
2	IP_L02P_2	P57	INPUT
2	IP_L07N_2/VREF_2	P72	VREF
2	IP_L07P_2	P71	INPUT
2	IP_L10N_2/M2/GCLK1	P81	DUAL/GCLK
2	IP_L10P_2/RDWR_B/ GCLK0	P80	DUAL/GCLK
2	VCCO_2	P59	VCCO
2	VCCO_2	P73	VCCO
2	VCCO_2	P88	VCCO
3	IO/VREF_3	P45	VREF
3	IO_L01N_3	P3	I/O
3	IO_L01P_3	P2	I/O
3	IO_L02N_3/VREF_3	P5	VREF
3	IO_L02P_3	P4	I/O
3	IO_L03N_3	P9	I/O
3	IO_L03P_3	P8	I/O
3	IO_L04N_3	P12	I/O
3	IO_L04P_3	P11	I/O
3	IO_L05N_3	P16	I/O
3	IO_L05P_3	P15	I/O
3	IO_L06N_3	P19	I/O
3	IO_L06P_3	P18	I/O
3	IO_L07N_3/LHCLK1	P23	LHCLK
3	IO_L07P_3/LHCLK0	P22	LHCLK
3	IO_L08N_3/LHCLK3	P25	LHCLK
3	IO_L08P_3/LHCLK2	P24	LHCLK
3	IO_L09N_3/LHCLK5	P29	LHCLK
3	IO_L09P_3/LHCLK4	P28	LHCLK
3	IO_L10N_3/LHCLK7	P31	LHCLK
3	IO_L10P_3/LHCLK6	P30	LHCLK
3	IO_L11N_3	P34	I/O
3	IO_L11P_3	P33	I/O
3	IO_L12N_3	P36	I/O
3	IO_L12P_3	P35	I/O
3	IO_L13N_3	P40	I/O
3	IO_L13P_3	P39	I/O
3	IO_L14N_3	P42	I/O

Table 143: **FT256 Package Pinout *(Cont'd)***

Bank	XC3S250E Pin Name	XC3S500E Pin Name	XC3S1200E Pin Name	FT256 Ball	Type
1	IO	IO	IP	M14	***250E:*** I/O ***500E:*** I/O ***1200E:*** INPUT
1	IO/VREF_1	IP/VREF_1	IP/VREF_1	D16	***250E:*** VREF(I/O) ***500E:*** VREF(INPUT) ***1200E:*** VREF(INPUT)
1	IP/VREF_1	IP/VREF_1	IP/VREF_1	H13	VREF
1	VCCO_1	VCCO_1	VCCO_1	E15	VCCO
1	VCCO_1	VCCO_1	VCCO_1	G11	VCCO
1	VCCO_1	VCCO_1	VCCO_1	K11	VCCO
1	VCCO_1	VCCO_1	VCCO_1	M15	VCCO
2	IP	IP	IO	M7	***250E:*** INPUT ***500E:*** INPUT ***1200E:*** I/O
2	IP	IP	IO	T12	***250E:*** INPUT ***500E:*** INPUT ***1200E:*** I/O
2	IO/D5	IO/D5	IO/D5	T8	DUAL
2	IO/M1	IO/M1	IO/M1	T10	DUAL
2	IO/VREF_2	IO/VREF_2	IO/VREF_2	P13	VREF
2	IO/VREF_2	IO/VREF_2	IO/VREF_2	R4	VREF
2	IO_L01N_2/INIT_B	IO_L01N_2/INIT_B	IO_L01N_2/INIT_B	P4	DUAL
2	IO_L01P_2/CSO_B	IO_L01P_2/CSO_B	IO_L01P_2/CSO_B	P3	DUAL
2	IO_L03N_2/MOSI/CSI_B	IO_L03N_2/MOSI/CSI_B	IO_L03N_2/MOSI/CSI_B	N5	DUAL
2	IO_L03P_2/DOUT/BUSY	IO_L03P_2/DOUT/BUSY	IO_L03P_2/DOUT/BUSY	P5	DUAL
2	IO_L04N_2	IO_L04N_2	IO_L04N_2	T5	I/O
2	IO_L04P_2	IO_L04P_2	IO_L04P_2	T4	I/O
2	IO_L05N_2	IO_L05N_2	IO_L05N_2	N6	I/O
2	IO_L05P_2	IO_L05P_2	IO_L05P_2	M6	I/O
2	IO_L06N_2	IO_L06N_2	IO_L06N_2	P6	I/O
2	IO_L06P_2	IO_L06P_2	IO_L06P_2	R6	I/O
2	N.C. (◆)	IO_L07N_2	IO_L07N_2	P7	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O
2	N.C. (◆)	IO_L07P_2	IO_L07P_2	N7	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O
2	IO_L09N_2/D6/GCLK13	IO_L09N_2/D6/GCLK13	IO_L09N_2/D6/GCLK13	L8	DUAL/GCLK
2	IO_L09P_2/D7/GCLK12	IO_L09P_2/D7/GCLK12	IO_L09P_2/D7/GCLK12	M8	DUAL/GCLK
2	IO_L10N_2/D3/GCLK15	IO_L10N_2/D3/GCLK15	IO_L10N_2/D3/GCLK15	P8	DUAL/GCLK
2	IO_L10P_2/D4/GCLK14	IO_L10P_2/D4/GCLK14	IO_L10P_2/D4/GCLK14	N8	DUAL/GCLK
2	IO_L12N_2/D1/GCLK3	IO_L12N_2/D1/GCLK3	IO_L12N_2/D1/GCLK3	N9	DUAL/GCLK
2	IO_L12P_2/D2/GCLK2	IO_L12P_2/D2/GCLK2	IO_L12P_2/D2/GCLK2	P9	DUAL/GCLK
2	IO_L13N_2/DIN/D0	IO_L13N_2/DIN/D0	IO_L13N_2/DIN/D0	M9	DUAL
2	IO_L13P_2/M0	IO_L13P_2/M0	IO_L13P_2/M0	L9	DUAL

Table 148: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S500E Pin Name	XC3S1200E Pin Name	XC3S1600E Pin Name	FG320 Ball	Type
0	IO_L08P_0	IO_L08P_0	IO_L08P_0	E11	I/O
0	IO_L09N_0	IO_L09N_0	IO_L09N_0	D11	I/O
0	IO_L09P_0	IO_L09P_0	IO_L09P_0	C11	I/O
0	IO_L11N_0/GCLK5	IO_L11N_0/GCLK5	IO_L11N_0/GCLK5	E10	GCLK
0	IO_L11P_0/GCLK4	IO_L11P_0/GCLK4	IO_L11P_0/GCLK4	D10	GCLK
0	IO_L12N_0/GCLK7	IO_L12N_0/GCLK7	IO_L12N_0/GCLK7	A10	GCLK
0	IO_L12P_0/GCLK6	IO_L12P_0/GCLK6	IO_L12P_0/GCLK6	B10	GCLK
0	IO_L14N_0/GCLK11	IO_L14N_0/GCLK11	IO_L14N_0/GCLK11	D9	GCLK
0	IO_L14P_0/GCLK10	IO_L14P_0/GCLK10	IO_L14P_0/GCLK10	C9	GCLK
0	IO_L15N_0	IO_L15N_0	IO_L15N_0	F9	I/O
0	IO_L15P_0	IO_L15P_0	IO_L15P_0	E9	I/O
0	IO_L17N_0	IO_L17N_0	IO_L17N_0	F8	I/O
0	IO_L17P_0	IO_L17P_0	IO_L17P_0	E8	I/O
0	IO_L18N_0/VREF_0	IO_L18N_0/VREF_0	IO_L18N_0/VREF_0	D7	VREF
0	IO_L18P_0	IO_L18P_0	IO_L18P_0	C7	I/O
0	IO_L19N_0/VREF_0	IO_L19N_0/VREF_0	IO_L19N_0/VREF_0	E7	VREF
0	IO_L19P_0	IO_L19P_0	IO_L19P_0	F7	I/O
0	IO_L20N_0	IO_L20N_0	IO_L20N_0	A6	I/O
0	IO_L20P_0	IO_L20P_0	IO_L20P_0	B6	I/O
0	N.C. (◆)	IO_L21N_0	IO_L21N_0	E6	**500E:** N.C. **1200E:** I/O **1600E:** I/O
0	N.C. (◆)	IO_L21P_0	IO_L21P_0	D6	**500E:** N.C. **1200E:** I/O **1600E:** I/O
0	IO_L23N_0/VREF_0	IO_L23N_0/VREF_0	IO_L23N_0/VREF_0	D5	VREF
0	IO_L23P_0	IO_L23P_0	IO_L23P_0	C5	I/O
0	IO_L24N_0	IO_L24N_0	IO_L24N_0	B4	I/O
0	IO_L24P_0	IO_L24P_0	IO_L24P_0	A4	I/O
0	IO_L25N_0/HSWAP	IO_L25N_0/HSWAP	IO_L25N_0/HSWAP	B3	DUAL
0	IO_L25P_0	IO_L25P_0	IO_L25P_0	C3	I/O
0	IP	IP	IP	A3	INPUT
0	IP	IP	IP	C15	INPUT
0	IP_L02N_0	IP_L02N_0	IP_L02N_0	A15	INPUT
0	IP_L02P_0	IP_L02P_0	IP_L02P_0	B15	INPUT
0	IP_L07N_0	IP_L07N_0	IP_L07N_0	D12	INPUT
0	IP_L07P_0	IP_L07P_0	IP_L07P_0	C12	INPUT
0	IP_L10N_0	IP_L10N_0	IP_L10N_0	G10	INPUT
0	IP_L10P_0	IP_L10P_0	IP_L10P_0	F10	INPUT
0	IP_L13N_0/GCLK9	IP_L13N_0/GCLK9	IP_L13N_0/GCLK9	B9	GCLK
0	IP_L13P_0/GCLK8	IP_L13P_0/GCLK8	IP_L13P_0/GCLK8	B8	GCLK
0	IP_L16N_0	IP_L16N_0	IP_L16N_0	D8	INPUT
0	IP_L16P_0	IP_L16P_0	IP_L16P_0	C8	INPUT
0	IP_L22N_0	IP_L22N_0	IP_L22N_0	B5	INPUT
0	IP_L22P_0	IP_L22P_0	IP_L22P_0	A5	INPUT

Table 148: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S500E Pin Name	XC3S1200E Pin Name	XC3S1600E Pin Name	FG320 Ball	Type
2	IO_L20P_2	IO_L20P_2	IO_L20P_2	T12	I/O
2	N.C. (◆)	IO_L21N_2	IO_L21N_2	P12	**500E:** N.C. **1200E:** I/O **1600E:** I/O
2	N.C. (◆)	IO_L21P_2	IO_L21P_2	N12	**500E:** N.C. **1200E:** I/O **1600E:** I/O
2	IO_L22N_2/A22	IO_L22N_2/A22	IO_L22N_2/A22	R13	DUAL
2	IO_L22P_2/A23	IO_L22P_2/A23	IO_L22P_2/A23	P13	DUAL
2	IO_L24N_2/A20	IO_L24N_2/A20	IO_L24N_2/A20	R14	DUAL
2	IO_L24P_2/A21	IO_L24P_2/A21	IO_L24P_2/A21	T14	DUAL
2	IO_L25N_2/VS1/A18	IO_L25N_2/VS1/A18	IO_L25N_2/VS1/A18	U15	DUAL
2	IO_L25P_2/VS2/A19	IO_L25P_2/VS2/A19	IO_L25P_2/VS2/A19	V15	DUAL
2	IO_L26N_2/CCLK	IO_L26N_2/CCLK	IO_L26N_2/CCLK	U16	DUAL
2	IO_L26P_2/VS0/A17	IO_L26P_2/VS0/A17	IO_L26P_2/VS0/A17	T16	DUAL
2	IP	IP	IP	V2	INPUT
2	IP	IP	IP	V16	INPUT
2	IP_L02N_2	IP_L02N_2	IP_L02N_2	V3	INPUT
2	IP_L02P_2	IP_L02P_2	IP_L02P_2	V4	INPUT
2	IP_L08N_2	IP_L08N_2	IP_L08N_2	R7	INPUT
2	IP_L08P_2	IP_L08P_2	IP_L08P_2	T7	INPUT
2	IP_L11N_2/VREF_2	IP_L11N_2/VREF_2	IP_L11N_2/VREF_2	V8	VREF
2	IP_L11P_2	IP_L11P_2	IP_L11P_2	U8	INPUT
2	IP_L14N_2/M2/GCLK1	IP_L14N_2/M2/GCLK1	IP_L14N_2/M2/GCLK1	T10	DUAL/GCLK
2	IP_L14P_2/RDWR_B/ GCLK0	IP_L14P_2/RDWR_B/ GCLK0	IP_L14P_2/RDWR_B/ GCLK0	U10	DUAL/GCLK
2	IP_L17N_2	IP_L17N_2	IP_L17N_2	U11	INPUT
2	IP_L17P_2	IP_L17P_2	IP_L17P_2	T11	INPUT
2	IP_L23N_2	IP_L23N_2	IP_L23N_2	U14	INPUT
2	IP_L23P_2	IP_L23P_2	IP_L23P_2	V14	INPUT
2	VCCO_2	VCCO_2	VCCO_2	M8	VCCO
2	VCCO_2	VCCO_2	VCCO_2	M11	VCCO
2	VCCO_2	VCCO_2	VCCO_2	T6	VCCO
2	VCCO_2	VCCO_2	VCCO_2	T13	VCCO
2	VCCO_2	VCCO_2	VCCO_2	V10	VCCO
3	N.C. (◆)	IO	IO	D4	**500E:** N.C. **1200E:** I/O **1600E:** I/O
3	IO_L01N_3	IO_L01N_3	IO_L01N_3	C2	I/O
3	IO_L01P_3	IO_L01P_3	IO_L01P_3	C1	I/O
3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	D2	VREF
3	IO_L02P_3	IO_L02P_3	IO_L02P_3	D1	I/O
3	IO_L03N_3	IO_L03N_3	IO_L03N_3	E1	I/O
3	IO_L03P_3	IO_L03P_3	IO_L03P_3	E2	I/O

FG400 Footprint

Left Half of Package (top view)

156 **I/O:** Unrestricted, general-purpose user I/O

62 **INPUT:** Unrestricted, general-purpose input pin

46 **DUAL:** Configuration pin, then possible user I/O

24 **VREF:** User I/O or input voltage reference for bank

16 **CLK:** User I/O, input, or clock buffer input

2 **CONFIG:** Dedicated configuration pins

4 **JTAG:** Dedicated JTAG port pins

42 **GND:** Ground

24 **VCCO:** Output voltage supply for bank

16 **VCCINT:** Internal core supply voltage (+1.2V)

8 **VCCAUX:** Auxiliary supply voltage (+2.5V)

0 **N.C.:** Not connected

Bank 0

	1	2	3	4	5	6	7	8	9	10
A	GND	I/O L31N_0	I/O	INPUT L29N_0	INPUT L29P_0	I/O L25N_0	I/O L25P_0	I/O	I/O L18N_0 GCLK11	I/O L18P_0 GCLK10
B	I/O L03P_3	I/O L31P_0	TDI	VCCO_0	I/O L27N_0	I/O L27P_0	GND	I/O L22N_0 VREF_0	I/O L22P_0	VCCO_0
C	I/O L03N_3	PROG_B	GND	I/O L32P_0	I/O L30N_0 VREF_0	I/O L28P_0	I/O	INPUT L23N_0	I/O L21N_0	I/O
D	I/O L04P_3	I/O L01N_3	I/O L01P_3	I/O L32N_0 HSWAP	I/O L30P_0	I/O L28N_0	VCCO_0	INPUT L23P_0	I/O L21P_0	GND
E	I/O L04N_3	VCCO_3	I/O L02N_3 VREF_3	I/O L02P_3	INPUT	INPUT L26N_0	INPUT L26P_0	I/O	I/O L19P_0	I/O L16N_0 GCLK7
F	I/O L06N_3	I/O L06P_3	I/O L05N_3	I/O L05P_3	INPUT	GND	I/O L24N_0 VREF_0	I/O L24P_0	I/O L19N_0	VCCO_0
G	INPUT	GND	I/O L07P_3	I/O L07N_3	I/O L08N_3	INPUT	I/O	INPUT L20P_0	INPUT L20N_0	INPUT L17N_0 GCLK9
H	INPUT	I/O L09P_3	I/O L09N_3 VREF_3	VCCO_3	I/O L08P_3	I/O L10P_3	I/O L10N_3	GND	VCCINT	INPUT L17P_0 GCLK8
J	I/O L12N_3	I/O L12P_3	I/O L11P_3	I/O L11N_3	INPUT	I/O L13N_3	VCCAUX	VCCINT	GND	VCCINT
K	GND	I/O L14N_3 LHCLK1	I/O L14P_3 LHCLK0	VCCAUX	INPUT VREF_3	I/O L13P_3	I/O L15P_3 LHCLK2	GND	VCCINT	GND
L	I/O L16N_3 LHCLK5	VCCO_3	I/O L17N_3 LHCLK7	GND	INPUT	VCCO_3	I/O L15N_3 LHCLK3 IRDY2	INPUT	GND	VCCINT
M	I/O L16P_3 LHCLK4 TRDY2	INPUT	I/O L17P_3 LHCLK6	I/O L19N_3	I/O L19P_3	I/O L20P_3	I/O L18N_3	I/O L18P_3	VCCINT	GND
N	I/O L21P_3	I/O L21N_3	I/O L23P_3	I/O L23N_3	INPUT	I/O L20N_3 VREF_3	I/O L22P_3	VCCINT	VCCAUX	VCCINT
P	I/O L24P_3	GND	INPUT	VCCO_3	I/O L25P_3	INPUT VREF_3	I/O L22N_3	I/O	GND	I/O L16N_2 D3 GCLK15
R	I/O L24N_3	I/O L26P_3	I/O L27P_3	I/O L27N_3	I/O L25N_3	GND	I/O L09N_2 VREF_2	INPUT L11N_2	I/O	I/O L16P_2 D4 GCLK14
T	I/O L28N_3 VREF_3	I/O L26N_3	I/O L29N_3	INPUT	I/O L06P_2	I/O L06N_2	I/O L09P_2	INPUT L11P_2	INPUT L14P_2	INPUT L14N_2 VREF_2
U	I/O L28P_3	VCCO_3	I/O L29P_3	I/O L01P_2 CSO_B	I/O L03P_2 DOUT BUSY	INPUT L05P_2	I/O L07N_2	VCCO_2	I/O L12N_2	VCCAUX
V	I/O L30N_3	I/O L30P_3	GND	I/O L01N_2 INIT_B	I/O L03N_2 MOSI CSI_B	INPUT L05N_2	I/O L07P_2	I/O L10N_2	I/O L12P_2	I/O L18P_2 D2 GCLK2
W	INPUT	INPUT L02P_2	INPUT	I/O L04P_2	VCCO_2	INPUT L08P_2	GND	I/O L10P_2	I/O L15P_2 D7 GCLK12	I/O L15N_2 D6 GCLK13
Y	GND	INPUT L02N_2	I/O VREF_2	I/O L04N_2	I/O	INPUT L08N_2	I/O	I/O L13N_2	I/O L13P_2	GND

Bank 3

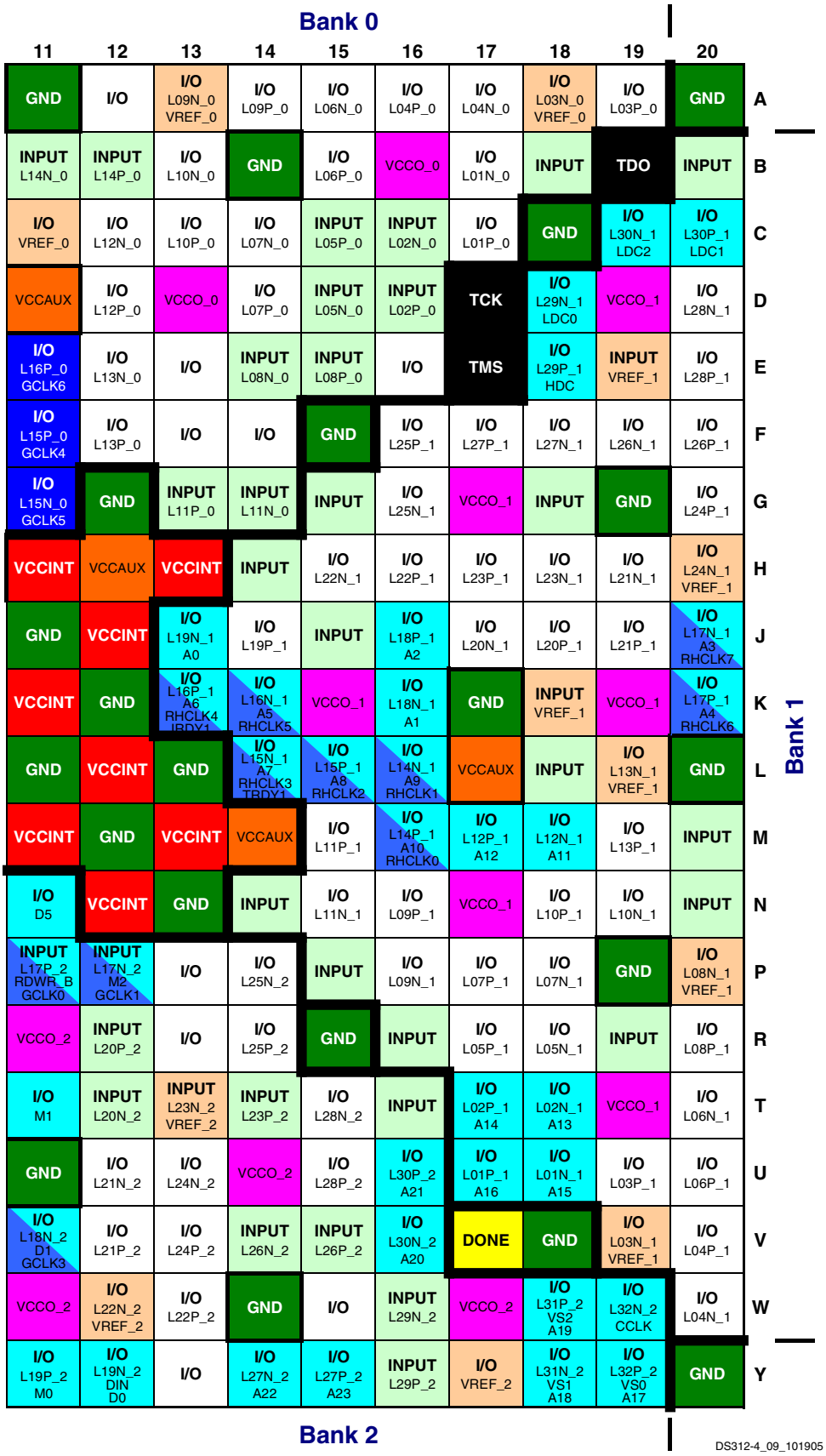
Bank 2

DS312-4_08_101905

Figure 87: **FG400 Package Footprint (top view)**

FG400 Footprint

Right Half of Package (top view)



FG484: 484-ball Fine-pitch Ball Grid Array

The 484-ball fine-pitch ball grid array, FG484, supports the XC3S1600E FPGA.

Table 154 lists all the FG484 package pins. They are sorted by bank number and then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at:

http://www.xilinx.com/support/documentation/data_sheets/s3e_pin.zip

Pinout Table

Table 154: **FG484 Package Pinout**

Bank	XC3S1600E Pin Name	FG484 Ball	Type
0	IO	B6	I/O
0	IO	B13	I/O
0	IO	C5	I/O
0	IO	C14	I/O
0	IO	E16	I/O
0	IO	F9	I/O
0	IO	F16	I/O
0	IO	G8	I/O
0	IO	H10	I/O
0	IO	H15	I/O
0	IO	J11	I/O
0	IO/VREF_0	G12	VREF
0	IO_L01N_0	C18	I/O
0	IO_L01P_0	C19	I/O
0	IO_L03N_0/VREF_0	A20	VREF
0	IO_L03P_0	A21	I/O
0	IO_L04N_0	A19	I/O
0	IO_L04P_0	A18	I/O
0	IO_L06N_0	C16	I/O
0	IO_L06P_0	D16	I/O
0	IO_L07N_0	A16	I/O
0	IO_L07P_0	A17	I/O
0	IO_L09N_0/VREF_0	B15	VREF
0	IO_L09P_0	C15	I/O
0	IO_L10N_0	G15	I/O
0	IO_L10P_0	F15	I/O
0	IO_L11N_0	D14	I/O
0	IO_L11P_0	E14	I/O
0	IO_L12N_0/VREF_0	A14	VREF
0	IO_L12P_0	A15	I/O
0	IO_L13N_0	H14	I/O
0	IO_L13P_0	G14	I/O
0	IO_L15N_0	G13	I/O
0	IO_L15P_0	F13	I/O
0	IO_L16N_0	J13	I/O
0	IO_L16P_0	H13	I/O
0	IO_L18N_0/GCLK5	E12	GCLK
0	IO_L18P_0/GCLK4	F12	GCLK
0	IO_L19N_0/GCLK7	C12	GCLK
0	IO_L19P_0/GCLK6	B12	GCLK
0	IO_L21N_0/GCLK11	B11	GCLK
0	IO_L21P_0/GCLK10	C11	GCLK
0	IO_L22N_0	D11	I/O
0	IO_L22P_0	E11	I/O
0	IO_L24N_0	A9	I/O
0	IO_L24P_0	A10	I/O
0	IO_L25N_0/VREF_0	D10	VREF
0	IO_L25P_0	C10	I/O
0	IO_L27N_0	H8	I/O
0	IO_L27P_0	H9	I/O
0	IO_L28N_0	C9	I/O
0	IO_L28P_0	B9	I/O
0	IO_L29N_0	E9	I/O
0	IO_L29P_0	D9	I/O
0	IO_L30N_0	B8	I/O
0	IO_L30P_0	A8	I/O
0	IO_L32N_0/VREF_0	F7	VREF
0	IO_L32P_0	F8	I/O
0	IO_L33N_0	A6	I/O
0	IO_L33P_0	A7	I/O
0	IO_L35N_0	A4	I/O
0	IO_L35P_0	A5	I/O
0	IO_L36N_0	E7	I/O
0	IO_L36P_0	D7	I/O
0	IO_L38N_0/VREF_0	D6	VREF
0	IO_L38P_0	D5	I/O
0	IO_L39N_0	B4	I/O
0	IO_L39P_0	B3	I/O
0	IO_L40N_0/HSWAP	D4	DUAL
0	IO_L40P_0	C4	I/O
0	IP	B19	INPUT

Table 154: **FG484 Package Pinout *(Cont'd)***

Bank	XC3S1600E Pin Name	FG484 Ball	Type
2	IO_L19N_2/D6/GCLK13	U11	DUAL/ GCLK
2	IO_L19P_2/D7/GCLK12	V11	DUAL/ GCLK
2	IO_L20N_2/D3/GCLK15	T11	DUAL/ GCLK
2	IO_L20P_2/D4/GCLK14	R11	DUAL/ GCLK
2	IO_L22N_2/D1/GCLK3	W12	DUAL/ GCLK
2	IO_L22P_2/D2/GCLK2	Y12	DUAL/ GCLK
2	IO_L23N_2/DIN/D0	U12	DUAL
2	IO_L23P_2/M0	V12	DUAL
2	IO_L25N_2	Y13	I/O
2	IO_L25P_2	W13	I/O
2	IO_L26N_2/VREF_2	U14	VREF
2	IO_L26P_2	U13	I/O
2	IO_L27N_2	T14	I/O
2	IO_L27P_2	R14	I/O
2	IO_L28N_2	Y14	I/O
2	IO_L28P_2	AA14	I/O
2	IO_L29N_2	W14	I/O
2	IO_L29P_2	V14	I/O
2	IO_L30N_2	AB15	I/O
2	IO_L30P_2	AA15	I/O
2	IO_L32N_2	W15	I/O
2	IO_L32P_2	Y15	I/O
2	IO_L33N_2	U16	I/O
2	IO_L33P_2	V16	I/O
2	IO_L35N_2/A22	AB17	DUAL
2	IO_L35P_2/A23	AA17	DUAL
2	IO_L36N_2	W17	I/O
2	IO_L36P_2	Y17	I/O
2	IO_L38N_2/A20	Y18	DUAL
2	IO_L38P_2/A21	W18	DUAL
2	IO_L39N_2/VS1/A18	AA20	DUAL
2	IO_L39P_2/VS2/A19	AB20	DUAL
2	IO_L40N_2/CCLK	W19	DUAL
2	IO_L40P_2/VS0/A17	Y19	DUAL
2	IP	V17	INPUT
2	IP	AB2	INPUT
2	IP_L02N_2	AA4	INPUT
2	IP_L02P_2	Y4	INPUT
2	IP_L05N_2	Y6	INPUT
2	IP_L05P_2	AA6	INPUT

Table 154: **FG484 Package Pinout *(Cont'd)***

Bank	XC3S1600E Pin Name	FG484 Ball	Type
2	IP_L08N_2	AB7	INPUT
2	IP_L08P_2	AB6	INPUT
2	IP_L15N_2	Y10	INPUT
2	IP_L15P_2	W10	INPUT
2	IP_L18N_2/VREF_2	AA11	VREF
2	IP_L18P_2	Y11	INPUT
2	IP_L21N_2/M2/GCLK1	P12	DUAL/ GCLK
2	IP_L21P_2/RDWR_B/ GCLK0	R12	DUAL/ GCLK
2	IP_L24N_2	R13	INPUT
2	IP_L24P_2	T13	INPUT
2	IP_L31N_2/VREF_2	T15	VREF
2	IP_L31P_2	U15	INPUT
2	IP_L34N_2	Y16	INPUT
2	IP_L34P_2	W16	INPUT
2	IP_L37N_2	AA19	INPUT
2	IP_L37P_2	AB19	INPUT
2	VCCO_2	T12	VCCO
2	VCCO_2	U9	VCCO
2	VCCO_2	V15	VCCO
2	VCCO_2	AA5	VCCO
2	VCCO_2	AA9	VCCO
2	VCCO_2	AA13	VCCO
2	VCCO_2	AA18	VCCO
3	IO_L01N_3	C1	I/O
3	IO_L01P_3	C2	I/O
3	IO_L02N_3/VREF_3	D2	VREF
3	IO_L02P_3	D3	I/O
3	IO_L03N_3	E3	I/O
3	IO_L03P_3	E4	I/O
3	IO_L04N_3	E1	I/O
3	IO_L04P_3	D1	I/O
3	IO_L05N_3	F4	I/O
3	IO_L05P_3	F3	I/O
3	IO_L06N_3	G5	I/O
3	IO_L06P_3	G4	I/O
3	IO_L07N_3	F1	I/O
3	IO_L07P_3	G1	I/O
3	IO_L08N_3/VREF_3	G6	VREF
3	IO_L08P_3	G7	I/O
3	IO_L09N_3	H4	I/O
3	IO_L09P_3	H5	I/O
3	IO_L10N_3	H2	I/O
3	IO_L10P_3	H3	I/O