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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	3688
Number of Logic Elements/Cells	33192
Total RAM Bits	663552
Number of I/O	304
Number of Gates	1600000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	400-BGA
Supplier Device Package	400-FBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s1600e-4fgg400c

Package Marking

Figure 2 provides a top marking example for Spartan-3E FPGAs in the quad-flat packages. Figure 3 shows the top marking for Spartan-3E FPGAs in BGA packages except the 132-ball chip-scale package (CP132 and CPG132). The markings for the BGA packages are nearly identical to those for the quad-flat packages, except that the marking is rotated with respect to the ball A1 indicator. Figure 4 shows the top marking for Spartan-3E FPGAs in the CP132 and CPG132 packages.

On the QFP and BGA packages, the optional numerical Stepping Code follows the Lot Code.

The “5C” and “4I” part combinations can have a dual mark of “5C/4I”. Devices with a single mark are only guaranteed for the marked speed grade and temperature range. All “5C” and “4I” part combinations use the Stepping 1 production silicon.

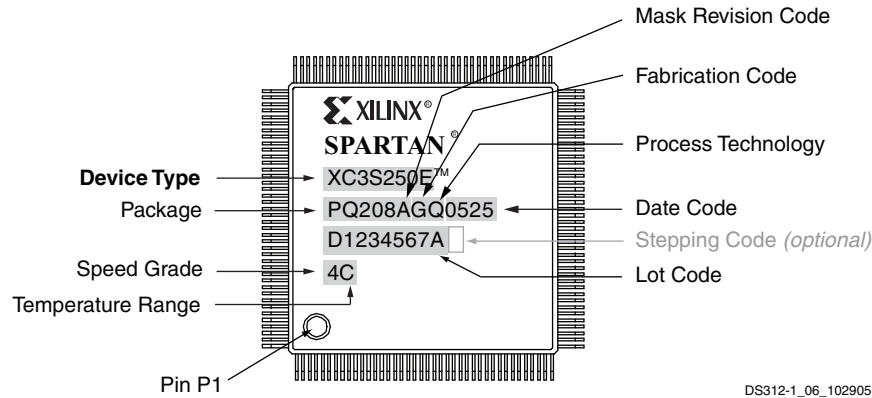


Figure 2: Spartan-3E QFP Package Marking Example

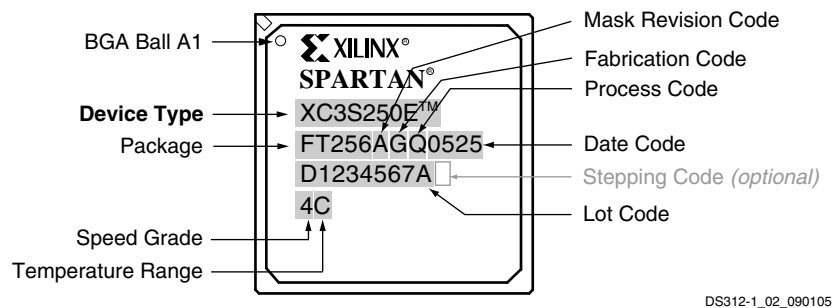


Figure 3: Spartan-3E BGA Package Marking Example

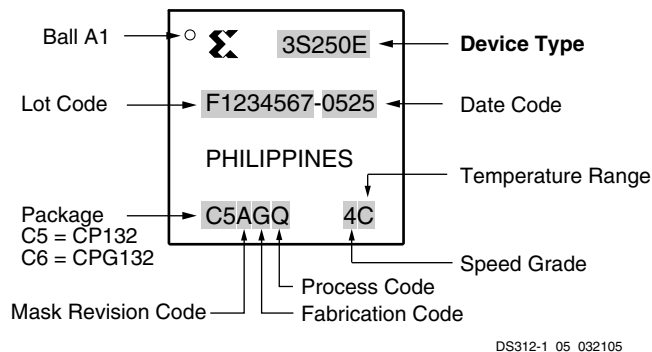


Figure 4: Spartan-3E CP132 and CPG132 Package Marking Example

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/01/05	1.0	Initial Xilinx release.
03/21/05	1.1	Added XC3S250E in CP132 package to Table 2 . Corrected number of differential I/O pairs for CP132 package. Added package markings for QFP packages (Figure 2) and CP132/CPG132 packages (Figure 4).
11/23/05	2.0	Added differential HSTL and SSTL I/O standards. Updated Table 2 to indicate number of input-only pins. Added Production Stepping information, including example top marking diagrams.
03/22/06	3.0	Upgraded data sheet status to Preliminary. Added XC3S100E in CP132 package and updated I/O counts for the XC3S1600E in FG320 package (Table 2). Added information about dual markings for –5C and –4I product combinations to Package Marking .
11/09/06	3.4	Added 66 MHz PCI support and links to the Xilinx PCI LogiCORE data sheet. Indicated that Stepping 1 parts are Production status. Promoted Module 1 to Production status. Synchronized all modules to v3.4.
04/18/08	3.7	Added XC3S500E VQG100 package. Added reference to XA Automotive version. Updated links.
08/26/09	3.8	Added paragraph to Configuration indicating the device supports MultiBoot configuration. Added package sizes to Table 2 . Described the speed grade and temperature range guarantee for devices having a single mark in paragraph 3 under Package Marking . Deleted Pb-Free Packaging example under Ordering Information . Revised information under Production Stepping . Revised description of Table 3 .
10/29/12	4.0	Added Notice of Disclaimer . This product is not recommended for new designs. Updated Table 2 footprint size of PQ208.

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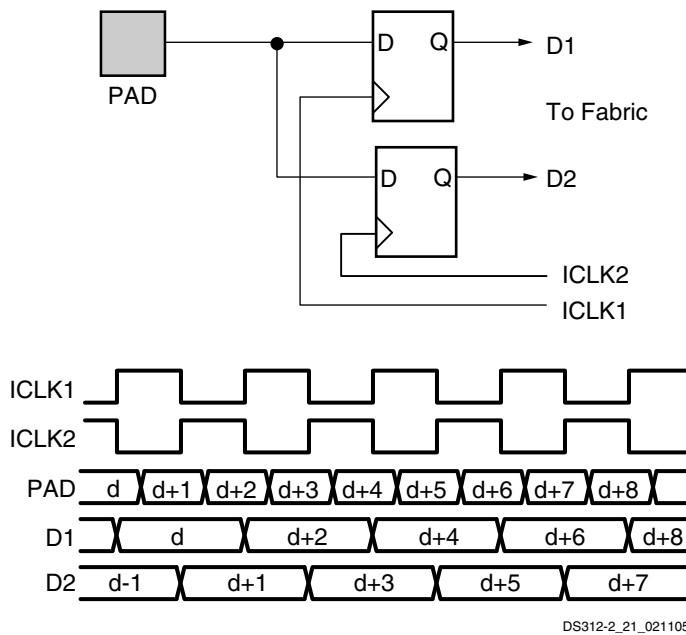


Figure 8: Input DDR (without Cascade Feature)

In the Spartan-3E device, the signal D2 can be cascaded into the storage element of the adjacent slave IOB. There it is re-registered to ICLK1, and only then fed to the FPGA fabric where it is now already in the same time domain as D1. Here, the FPGA fabric uses only the clock ICLK1 to process the received data. See Figure 9 for a graphical illustration of this function.

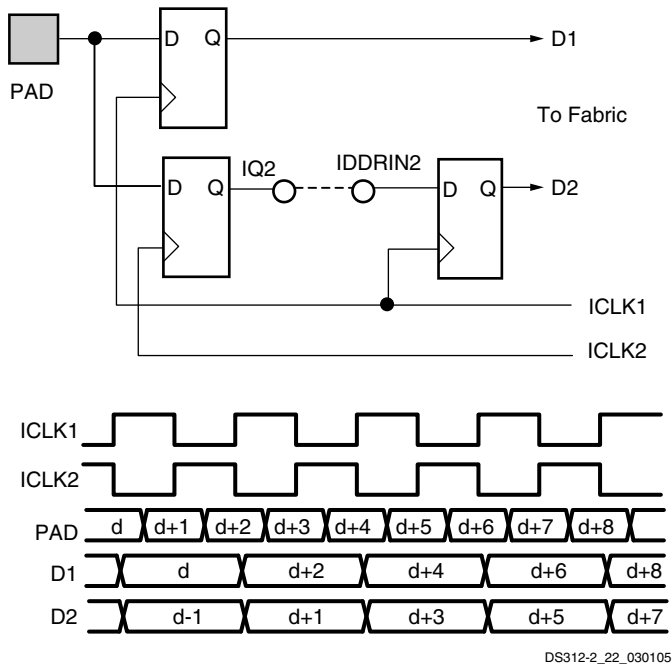


Figure 9: Input DDR Using Spartan-3E Cascade Feature

ODDR2

As a DDR output pair, the master IOB registers data coming from the FPGA fabric on the rising edge of OCLK1 (= D1)

and the rising edge of OCLK2 (= D2), which is typically the same as the falling edge of OCLK1. These two bits of data are multiplexed by the DDR mux and forwarded to the output pin. The D2 data signal must be re-synchronized from the OCLK1 clock domain to the OCLK2 domain using FPGA slice flip-flops. Placement is critical at high frequencies, because the time available is only one half a clock cycle. See Figure 10 for a graphical illustration of this function.

The C0 or C1 alignment feature of the ODDR2 flip-flop, originally introduced in the Spartan-3E FPGA family, is not recommended or supported in the ISE development software. The ODDR2 flip-flop without the alignment feature remains fully supported. Without the alignment feature, the ODDR2 feature behaves equivalent to the ODDR flip-flop on previous Xilinx FPGA families.

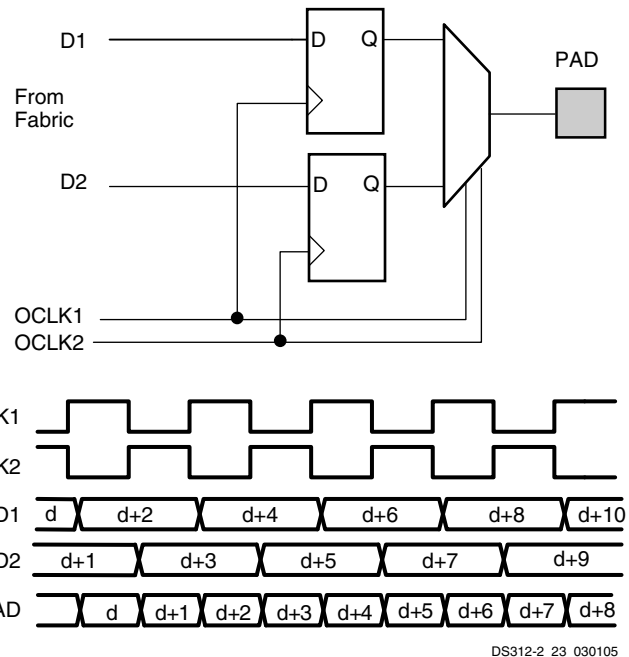


Figure 10: Output DDR

SelectIO Signal Standards

The Spartan-3E I/Os feature inputs and outputs that support a wide range of I/O signaling standards (Table 6 and Table 7). The majority of the I/Os also can be used to form differential pairs to support any of the differential signaling standards (Table 7).

To define the I/O signaling standard in a design, set the IOSTANDARD attribute to the appropriate setting. Xilinx provides a variety of different methods for applying the IOSTANDARD for maximum flexibility. For a full description of different methods of applying attributes to control IOSTANDARD, refer to the Xilinx Software Manuals and Help.

Configurable Logic Block (CLB) and Slice Resources

For additional information, refer to the “Using Configurable Logic Blocks (CLBs)” chapter in [UG331](#).

CLB Overview

The Configurable Logic Blocks (CLBs) constitute the main logic resource for implementing synchronous as well as combinatorial circuits. Each CLB contains four slices, and each slice contains two Look-Up Tables (LUTs) to implement logic and two dedicated storage elements that can be used as flip-flops or latches. The LUTs can be used as a 16x1 memory (RAM16) or as a 16-bit shift register

(SRL16), and additional multiplexers and carry logic simplify wide logic and arithmetic functions. Most general-purpose logic in a design is automatically mapped to the slice resources in the CLBs. Each CLB is identical, and the Spartan-3E family CLB structure is identical to that for the Spartan-3 family.

CLB Array

The CLBs are arranged in a regular array of rows and columns as shown in [Figure 14](#).

Each density varies by the number of rows and columns of CLBs (see [Table 9](#)).

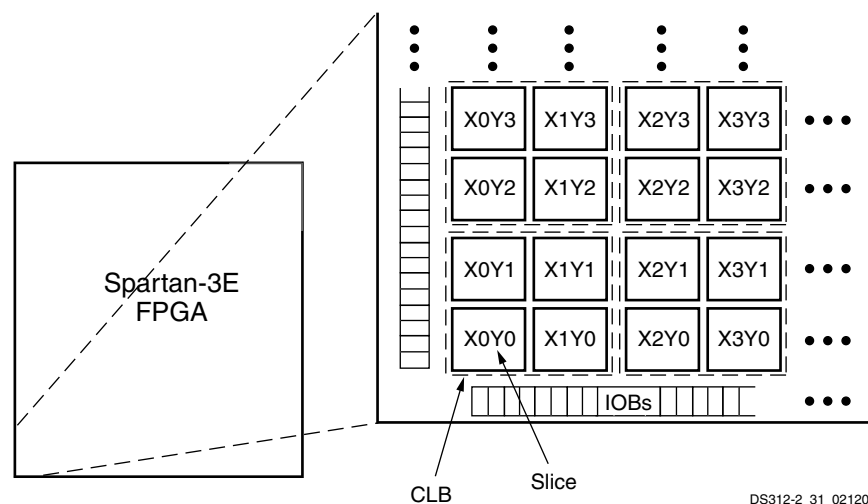


Figure 14: CLB Locations

Table 9: Spartan-3E CLB Resources

Device	CLB Rows	CLB Columns	CLB Total ⁽¹⁾	Slices	LUTs / Flip-Flops	Equivalent Logic Cells	RAM16 / SRL16	Distributed RAM Bits
XC3S100E	22	16	240	960	1,920	2,160	960	15,360
XC3S250E	34	26	612	2,448	4,896	5,508	2,448	39,168
XC3S500E	46	34	1,164	4,656	9,312	10,476	4,656	74,496
XC3S1200E	60	46	2,168	8,672	17,344	19,512	8,672	138,752
XC3S1600E	76	58	3,688	14,752	29,504	33,192	14,752	236,032

Notes:

- The number of CLBs is less than the multiple of the rows and columns because the block RAM/multiplier blocks and the DCMs are embedded in the array (see [Figure 1](#) in Module 1).

Slices

Each CLB comprises four interconnected slices, as shown in [Figure 16](#). These slices are grouped in pairs. Each pair is organized as a column with an independent carry chain. The left pair supports both logic and memory functions and its slices are called SLICEM. The right pair supports logic only and its slices are called SLICEL. Therefore half the

LUTs support both logic and memory (including both RAM16 and SRL16 shift registers) while half support logic only, and the two types alternate throughout the array columns. The SLICEL reduces the size of the CLB and lowers the cost of the device, and can also provide a performance advantage over the SLICEM.

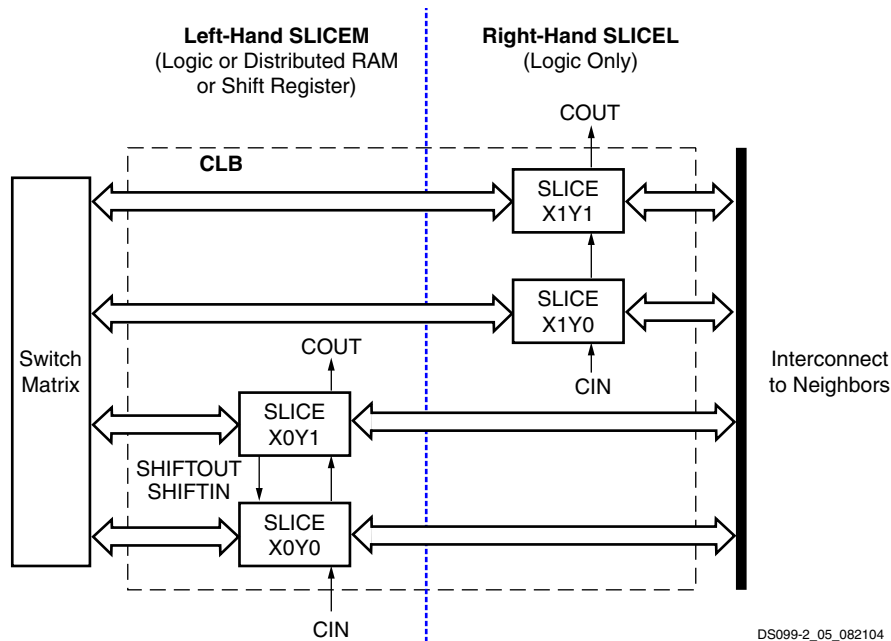


Figure 16: Arrangement of Slices within the CLB

Slice Location Designations

The Xilinx development software designates the location of a slice according to its X and Y coordinates, starting in the bottom left corner, as shown in Figure 14. The letter 'X' followed by a number identifies columns of slices, incrementing from the left side of the die to the right. The letter 'Y' followed by a number identifies the position of each slice in a pair as well as indicating the CLB row, incrementing from the bottom of the die. Figure 16 shows the CLB located in the lower left-hand corner of the die. The SLICEM always has an even 'X' number, and the SLICEL always has an odd 'X' number.

Slice Overview

A slice includes two LUT function generators and two storage elements, along with additional logic, as shown in Figure 17.

Both SLICEM and SLICEL have the following elements in common to provide logic, arithmetic, and ROM functions:

- Two 4-input LUT function generators, F and G
- Two storage elements
- Two wide-function multiplexers, F5MUX and FiMUX
- Carry and arithmetic logic

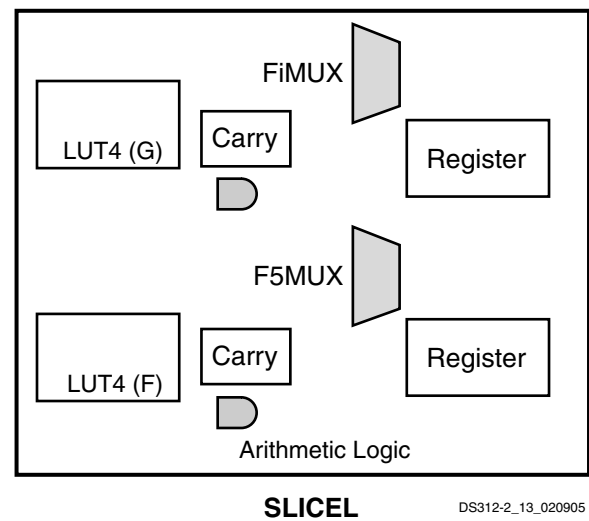
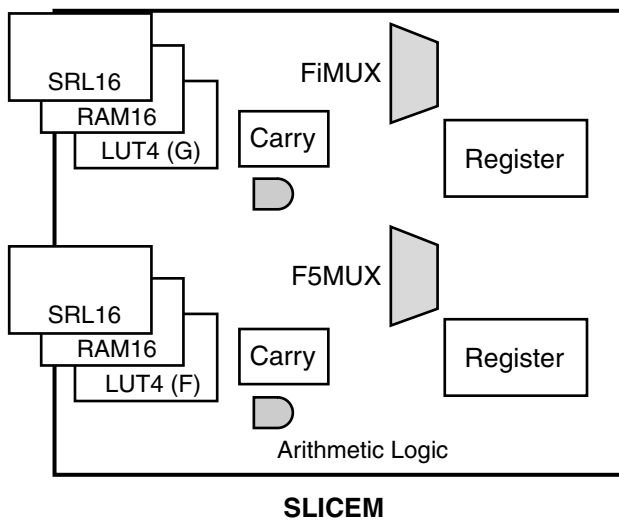
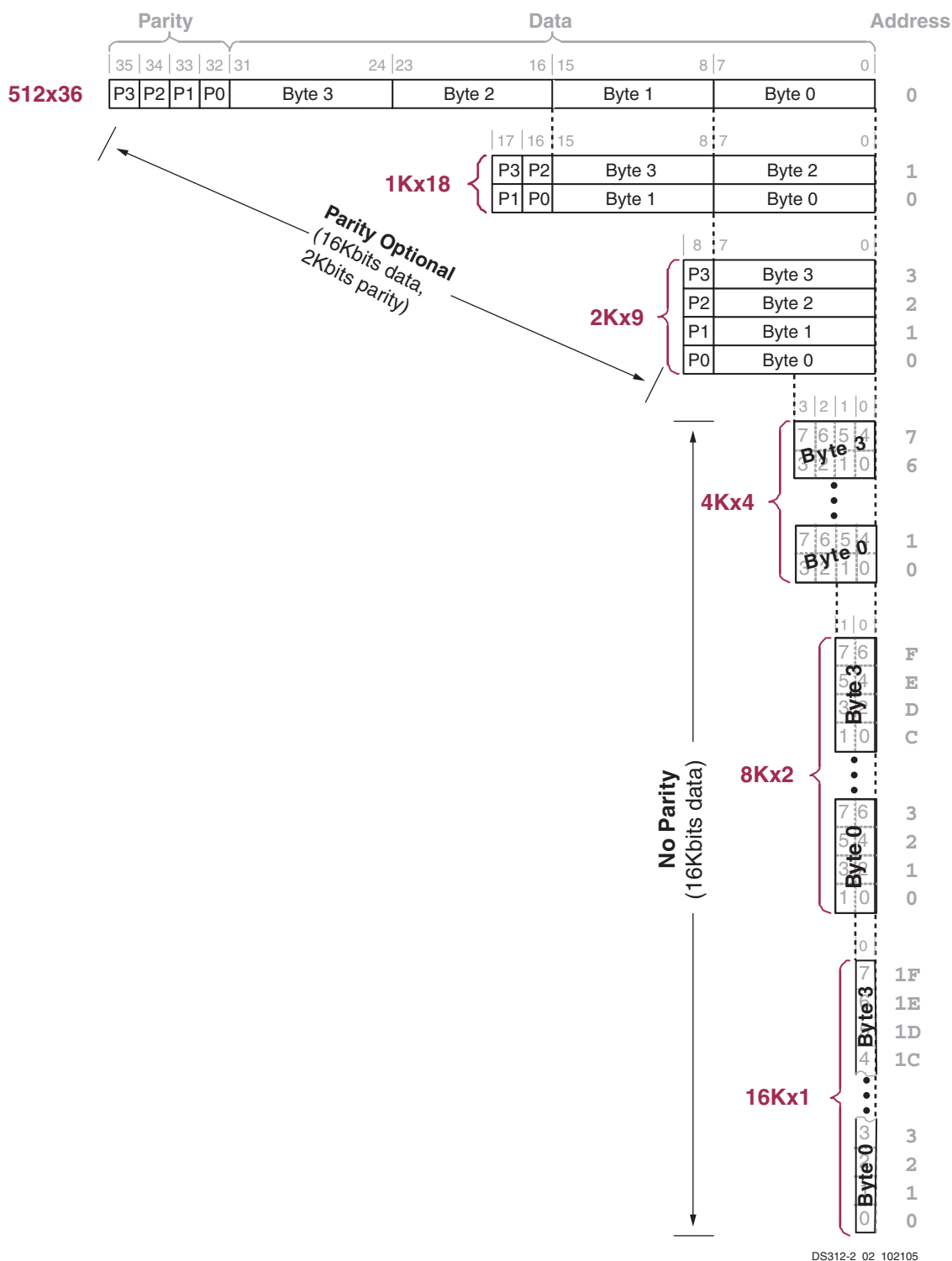


Figure 17: Resources in a Slice



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Figure 31: Data Organization and Bus-matching Operation with Different Port Widths on Port A and Port B

Table 23: Block RAM Port Signals

Signal Description	Port A Signal Name	Port B Signal Name	Direction	Function
Address Bus	ADDRA	ADDRB	Input	The Address Bus selects a memory location for read or write operations. The width (w) of the port's associated data path determines the number of available address lines (r), as per Table 22 . Whenever a port is enabled (ENA or ENB = High), address transitions must meet the data sheet setup and hold times with respect to the port clock (CLKA or CLKB), as shown in Table 103, page 138 . This requirement must be met even if the RAM read output is of no interest.
Data Input Bus	DIA	DIB	Input	Data at the DI input bus is written to the RAM location specified by the address input bus (ADDR) during the active edge of the CLK input, when the clock enable (EN) and write enable (WE) inputs are active. It is possible to configure a port's DI input bus width (w-p) based on Table 22 . This selection applies to both the DI and DO paths of a given port.
Parity Data Input(s)	DIPA	DIPB	Input	Parity inputs represent additional bits included in the data input path. Although referred to herein as "parity" bits, the parity inputs and outputs have no special functionality for generating or checking parity and can be used as additional data bits. The number of parity bits 'p' included in the DI (same as for the DO bus) depends on a port's total data path width (w). See Table 22 .
Data Output Bus	DOA	DOB	Output	Data is written to the DO output bus from the RAM location specified by the address input bus, ADDR. See the DI signal description for DO port width configurations. Basic data access occurs on the active edge of the CLK when WE is inactive and EN is active. The DO outputs mirror the data stored in the address ADDR memory location. Data access with WE active if the WRITE_MODE attribute is set to the value: WRITE_FIRST , which accesses data after the write takes place. READ_FIRST accesses data before the write occurs. A third attribute, NO_CHANGE , latches the DO outputs upon the assertion of WE. See Block RAM Data Operations for details on the WRITE_MODE attribute.
Parity Data Output(s)	DOPA	DOPB	Output	Parity outputs represent additional bits included in the data input path. The number of parity bits 'p' included in the DI bus (same as for the DO bus) depends on a port's total data path width (w). See the DIP signal description for configuration details.
Write Enable	WEA	WEB	Input	When asserted together with EN, this input enables the writing of data to the RAM. When WE is inactive with EN asserted, read operations are still possible. In this case, a latch passes data from the addressed memory location to the DO outputs.
Clock Enable	ENA	ENB	Input	When asserted, this input enables the CLK signal to perform read and write operations to the block RAM. When inactive, the block RAM does not perform any read or write operations.
Set/Reset	SSRA	SSRB	Input	When asserted, this pin forces the DO output latch to the value of the SRVAL attribute. It is synchronized to the CLK signal.
Clock	CLKA	CLKB	Input	This input accepts the clock signal to which read and write operations are synchronized. All associated port inputs are required to meet setup times with respect to the clock signal's active edge. The data output bus responds after a clock-to-out delay referenced to the clock signal's active edge.

cancel out the clock skew. When the DLL phase-aligns the CLK0 signal with the CLKIN signal, it asserts the LOCKED output, indicating a lock on to the CLKIN signal.

DLL Attributes and Related Functions

The DLL unit has a variety of associated attributes as described in [Table 29](#). Each attribute is described in detail in the sections that follow.

Table 29: DLL Attributes

Attribute	Description	Values
CLK_FEEDBACK	Chooses either the CLK0 or CLK2X output to drive the CLKFB input	NONE, <u>1X</u> , 2X
CLKIN_DIVIDE_BY_2	Halves the frequency of the CLKIN signal just as it enters the DCM	<u>FALSE</u> , TRUE
CLKDV_DIVIDE	Selects the constant used to divide the CLKIN input frequency to generate the CLKDV output frequency	1.5, <u>2</u> , 2.5, 3, 3.5, 4, 4.5, 5, 5.5, 6.0, 6.5, 7.0, 7.5, 8, 9, 10, 11, 12, 13, 14, 15, and 16
CLKIN_PERIOD	Additional information that allows the DLL to operate with the most efficient lock time and the best jitter tolerance	Floating-point value representing the CLKIN period in nanoseconds

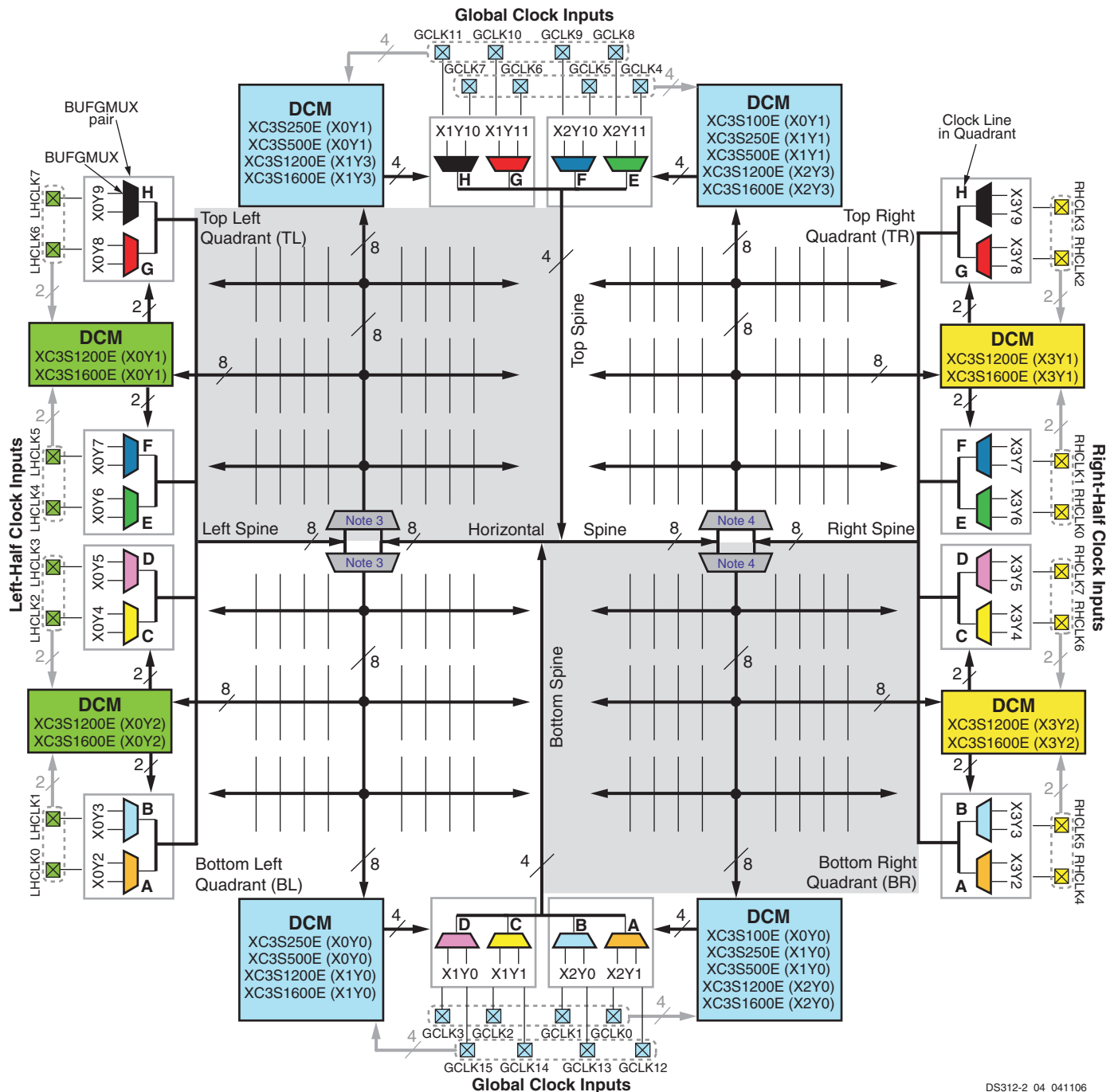
DLL Clock Input Connections

For best results, an external clock source enters the FPGA via a Global Clock Input (GCLK). Each specific DCM has four possible direct, optimal GCLK inputs that feed the DCM's CLKIN input, as shown in [Table 30](#). [Table 30](#) also provides the specific pin numbers by package for each GCLK input. The two additional DCM's on the XC3S1200E and XC3S1600E have similar optimal connections from the left-edge LHCLK and the right-edge RHCLK inputs, as described in [Table 31](#) and [Table 32](#).

- The DCM supports differential clock inputs (for example, LVDS, LVPECL_25) via a pair of GCLK inputs that feed an internal single-ended signal to the DCM's CLKIN input.

Design Note

Avoid using global clock input GCLK1 as it is always shared with the M2 mode select pin. Global clock inputs GCLK0, GCLK2, GCLK3, GCLK12, GCLK13, GCLK14, and GCLK15 have shared functionality in some configuration modes.



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Figure 45: Spartan-3E Internal Quadrant-Based Clock Network (Electrical Connectivity View)

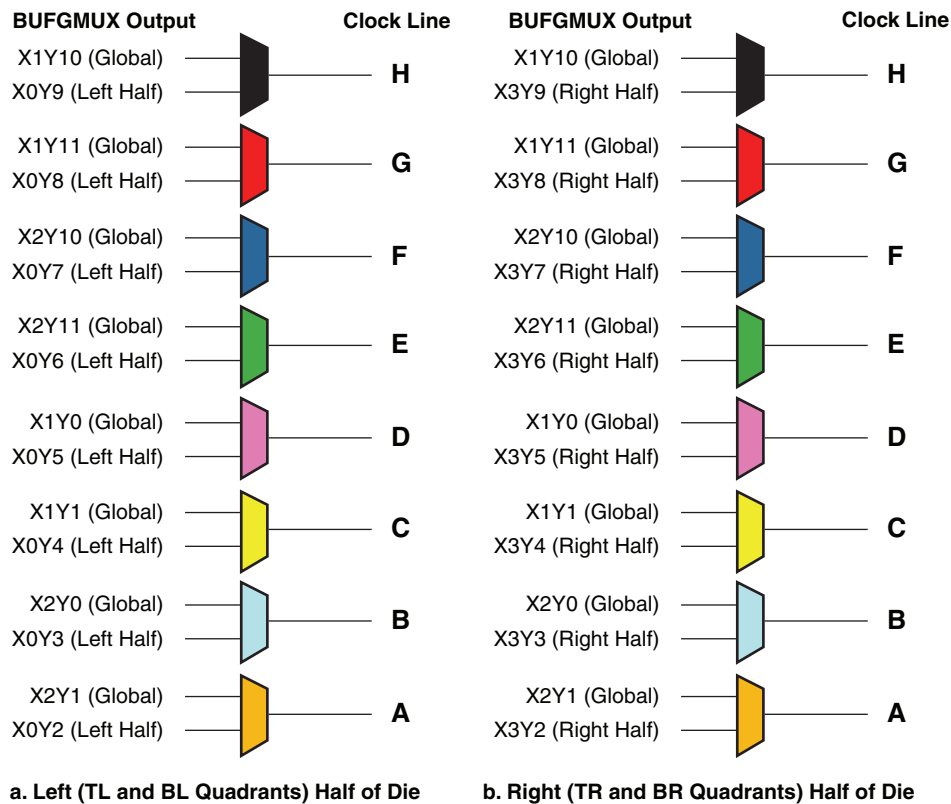


Figure 47: Clock Sources for the Eight Clock Lines within a Clock Quadrant

The outputs of the top or bottom BUFGMUX elements connect to two vertical spines, each comprising four vertical clock lines as shown in Figure 45. At the center of the die, these clock signals connect to the eight-line horizontal clock spine.

Outputs of the left and right BUFGMUX elements are routed onto the left or right horizontal spines, each comprising eight horizontal clock lines.

Each of the eight clock signals in a clock quadrant derives either from a global clock signal or a half clock signal. In other words, there are up to 24 total potential clock inputs to the FPGA, eight of which can connect to clocked elements in a single clock quadrant. Figure 47 shows how the clock lines in each quadrant are selected from associated BUFGMUX sources. For example, if quadrant clock 'A' in the bottom left (BL) quadrant originates from BUFGMUX_X2Y1, then the clock signal from BUFGMUX_X0Y2 is unavailable in the bottom left quadrant. However, the top left (TL) quadrant clock 'A' can still solely use the output from either BUFGMUX_X2Y1 or BUFGMUX_X0Y2 as the source.

To minimize the dynamic power dissipation of the clock network, the Xilinx development software automatically disables all clock segments not in use.

This addressing flexibility allows the FPGA to share the parallel Flash PROM with an external or embedded processor. Depending on the specific processor architecture, the processor boots either from the top or bottom of memory. The FPGA is flexible and boots from the opposite end of memory from the processor. Only the processor or the FPGA can boot at any given time. The FPGA can configure first, holding the processor in reset or the processor can boot first, asserting the FPGA's PROG_B pin.

The mode select pins, M[2:0], are sampled when the FPGA's INIT_B output goes High and must be at defined logic levels during this time. After configuration, when the FPGA's DONE output goes High, the mode pins are available as full-featured user-I/O pins.

Ⓟ Similarly, the FPGA's HSWAP pin must be Low to enable pull-up resistors on all user-I/O pins or High to disable the pull-up resistors. The HSWAP control must remain at a constant logic level throughout FPGA configuration. After configuration, when the FPGA's DONE output goes High, the HSWAP pin is available as

full-featured user-I/O pin and is powered by the VCCO_0 supply.

The RDWR_B and CSI_B must be Low throughout the configuration process. After configuration, these pins also become user I/O.

In a single-FPGA application, the FPGA's CSO_B and CCLK pins are not used but are actively driving during the configuration process. The BUSY pin is not used but also actively drives during configuration and is available as a user I/O after configuration.

After configuration, all of the interface pins except DONE and PROG_B are available as user I/Os. Furthermore, the bidirectional SelectMAP configuration peripheral interface (see [Slave Parallel Mode](#)) is available after configuration. To continue using SelectMAP mode, set the **Persist** bitstream generator option to **Yes**. An external host can then read and verify configuration data.

The Persist option will maintain A20-A23 as configuration pins although they are not used in SelectMAP mode.

Table 59: Byte-Wide Peripheral Interface (BPI) Connections

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
HSWAP Ⓟ	Input	User I/O Pull-Up Control. When Low during configuration, enables pull-up resistors in all I/O pins to respective I/O bank V _{CCO} input. 0: Pull-ups during configuration 1: No pull-ups	Drive at valid logic level throughout configuration.	User I/O
M[2:0] Ⓐ	Input	Mode Select. Selects the FPGA configuration mode. See Design Considerations for the HSWAP, M[2:0], and VS[2:0] Pins .	M2 = 0, M1 = 1. Set M0 = 0 to start at address 0, increment addresses. Set M0 = 1 to start at address 0xFFFFF and decrement addresses. Sampled when INIT_B goes High.	User I/O
CSI_B	Input	Chip Select Input. Active Low.	Must be Low throughout configuration.	User I/O. If bitstream option Persist=Yes , becomes part of SelectMap parallel peripheral interface.
RDWR_B	Input	Read/Write Control. Active Low write enable. Read functionality typically only used after configuration, if bitstream option Persist=Yes .	Must be Low throughout configuration.	User I/O. If bitstream option Persist=Yes , becomes part of SelectMap parallel peripheral interface.
LDC0	Output	PROM Chip Enable	Connect to PROM chip-select input (CE#). FPGA drives this signal Low throughout configuration.	User I/O. If the FPGA does not access the PROM after configuration, drive this pin High to deselect the PROM. A[23:0], D[7:0], LDC[2:1], and HDC then become available as user I/O.
LDC1	Output	PROM Output Enable	Connect to the PROM output-enable input (OE#). The FPGA drives this signal Low throughout configuration.	User I/O

Table 69: Spartan-3E FPGA Bitstream Generator (BitGen) Options (Cont'd)

Option Name	Pins/Function Affected	Values (default)	Description
DriveDone	DONE pin	No	When configuration completes, the DONE pin stops driving Low and relies on an external 330 Ω pull-up resistor to V_{CCAUX} for a valid logic High.
		Yes	When configuration completes, the DONE pin actively drives High. When using this option, an external pull-up resistor is no longer required. Only one device in an FPGA daisy-chain should use this setting.
DonePipe	DONE pin	No	The input path from DONE pin input back to the Startup sequencer is not pipelined.
		Yes	This option adds a pipeline register stage between the DONE pin input and the Startup sequencer. Used for high-speed daisy-chain configurations when DONE cannot rise in a single CCLK cycle. Releases GWE and GTS signals on the first rising edge of StartupClk after the DONE pin input goes High.
ProgPin	PROG_B pin	Pullup	Internally connects a pull-up resistor or between PROG_B pin and V_{CCAUX} . An external 4.7 k Ω pull-up resistor to V_{CCAUX} is still recommended since the internal pull-up value may be weaker (see Table 78).
		Pullnone	No internal pull-up resistor on PROG_B pin. An external 4.7 k Ω pull-up resistor to V_{CCAUX} is required.
TckPin	JTAG TCK pin	Pullup	Internally connects a pull-up resistor between JTAG TCK pin and V_{CCAUX} .
		Pulldown	Internally connects a pull-down resistor between JTAG TCK pin and GND.
		Pullnone	No internal pull-up resistor on JTAG TCK pin.
TdiPin	JTAG TDI pin	Pullup	Internally connects a pull-up resistor between JTAG TDI pin and V_{CCAUX} .
		Pulldown	Internally connects a pull-down resistor between JTAG TDI pin and GND.
		Pullnone	No internal pull-up resistor on JTAG TDI pin.
TdoPin	JTAG TDO pin	Pullup	Internally connects a pull-up resistor between JTAG TDO pin and V_{CCAUX} .
		Pulldown	Internally connects a pull-down resistor between JTAG TDO pin and GND.
		Pullnone	No internal pull-up resistor on JTAG TDO pin.
TmsPin	JTAG TMS pin	Pullup	Internally connects a pull-up resistor between JTAG TMS pin and V_{CCAUX} .
		Pulldown	Internally connects a pull-down resistor between JTAG TMS pin and GND.
		Pullnone	No internal pull-up resistor on JTAG TMS pin.
UserID	JTAG User ID register	User string	The 32-bit JTAG User ID register value is loaded during configuration. The default value is all ones, 0xFFFF_FFFF hexadecimal. To specify another value, enter an 8-character hexadecimal value.
Security	JTAG, SelectMAP, Readback, Partial reconfiguration	None	Readback and limited partial reconfiguration are available via the JTAG port or via the SelectMAP interface, if the Persist option is set to Yes .
		Level1	Readback function is disabled. Limited partial reconfiguration is still available via the JTAG port or via the SelectMAP interface, if the Persist option is set to Yes .
		Level2	Readback function is disabled. Limited partial reconfiguration is disabled.
CRC	Configuration	Enable	Default. Enable CRC checking on the FPGA bitstream. If error detected, FPGA asserts INIT_B Low and DONE pin stays Low.
		Disable	Turn off CRC checking.
Persist	SelectMAP interface pins, BPI mode, Slave mode, Configuration	No	All BPI and Slave mode configuration pins are available as user-I/O after configuration.
		Yes	This option is required for Readback and partial reconfiguration using the SelectMAP interface. The SelectMAP interface pins (see Slave Parallel Mode) are reserved after configuration and are not available as user-I/O.

Table 81: DC Characteristics of User I/Os Using Single-Ended Standards

IOSTANDARD Attribute	Test Conditions			Logic Level Characteristics	
	I_{OL} (mA)	I_{OH} (mA)		V_{OL} Max (V)	V_{OH} Min (V)
LVTTTL ⁽³⁾	2	2	-2	0.4	2.4
	4	4	-4		
	6	6	-6		
	8	8	-8		
	12	12	-12		
	16	16	-16		
LVCMOS33 ⁽³⁾	2	2	-2	0.4	$V_{CCO} - 0.4$
	4	4	-4		
	6	6	-6		
	8	8	-8		
	12	12	-12		
	16	16	-16		
LVCMOS25 ⁽³⁾	2	2	-2	0.4	$V_{CCO} - 0.4$
	4	4	-4		
	6	6	-6		
	8	8	-8		
	12	12	-12		
LVCMOS18 ⁽³⁾	2	2	-2	0.4	$V_{CCO} - 0.4$
	4	4	-4		
	6	6	-6		
	8	8	-8		
LVCMOS15 ⁽³⁾	2	2	-2	0.4	$V_{CCO} - 0.4$
	4	4	-4		
	6	6	-6		
LVCMOS12 ⁽³⁾	2	2	-2	0.4	$V_{CCO} - 0.4$
PCI33_3 ⁽⁴⁾	1.5	-0.5		10% V_{CCO}	90% V_{CCO}
PCI66_3 ⁽⁴⁾	1.5	-0.5		10% V_{CCO}	90% V_{CCO}
HSTL_I_18	8	-8		0.4	$V_{CCO} - 0.4$
HSTL_III_18	24	-8		0.4	$V_{CCO} - 0.4$
SSTL18_I	6.7	-6.7		$V_{TT} - 0.475$	$V_{TT} + 0.475$

Table 81: DC Characteristics of User I/Os Using Single-Ended Standards (Cont'd)

IOSTANDARD Attribute	Test Conditions		Logic Level Characteristics	
	I_{OL} (mA)	I_{OH} (mA)	V_{OL} Max (V)	V_{OH} Min (V)
SSTL2_I	8.1	-8.1	$V_{TT} - 0.61$	$V_{TT} + 0.61$

Notes:

- The numbers in this table are based on the conditions set forth in [Table 77](#) and [Table 80](#).
- Descriptions of the symbols used in this table are as follows:
 I_{OL} – the output current condition under which V_{OL} is tested
 I_{OH} – the output current condition under which V_{OH} is tested
 V_{OL} – the output voltage that indicates a Low logic level
 V_{OH} – the output voltage that indicates a High logic level
 V_{CCO} – the supply voltage for output drivers
 V_{TT} – the voltage applied to a resistor termination
- For the LVCMOS and LVTTTL standards: the same V_{OL} and V_{OH} limits apply for both the Fast and Slow slew attributes.
- Tested according to the relevant PCI specifications. For information on PCI IP solutions, see www.xilinx.com/pci. The PCIX IOSTANDARD is available and has equivalent characteristics but no PCI-X IP is supported.

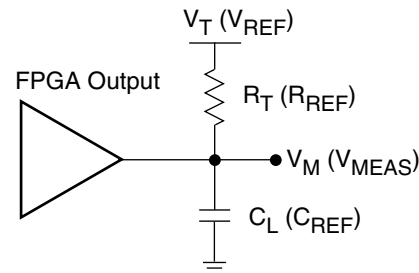
Timing Measurement Methodology

When measuring timing parameters at the programmable I/Os, different signal standards call for different test conditions. Table 95 lists the conditions to use for each standard.

The method for measuring Input timing is as follows: A signal that swings between a Low logic level of V_L and a High logic level of V_H is applied to the Input under test. Some standards also require the application of a bias voltage to the V_{REF} pins of a given bank to properly set the input-switching threshold. The measurement point of the Input signal (V_M) is commonly located halfway between V_L and V_H .

The Output test setup is shown in Figure 72. A termination voltage V_T is applied to the termination resistor R_T , the other end of which is connected to the Output. For each standard, R_T and V_T generally take on the standard values recommended for minimizing signal reflections. If the standard does not ordinarily use terminations (e.g.,

LVC MOS, LV TTL), then R_T is set to 1M Ω to indicate an open connection, and V_T is set to zero. The same measurement point (V_M) that was used at the Input is also used at the Output.



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Notes:

1. The names shown in parentheses are used in the IBIS file.

Figure 72: Output Test Setup

Table 95: Test Methods for Timing Measurement at I/Os

Signal Standard (IOSTANDARD)		Inputs			Outputs		Inputs and Outputs
		V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
Single-Ended							
LV TTL		-	0	3.3	1M	0	1.4
LVCMOS33		-	0	3.3	1M	0	1.65
LVCMOS25		-	0	2.5	1M	0	1.25
LVCMOS18		-	0	1.8	1M	0	0.9
LVCMOS15		-	0	1.5	1M	0	0.75
LVCMOS12		-	0	1.2	1M	0	0.6
PCI33_3	Rising	-	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
PCI66_3	Rising	-	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
HSTL_I_18		0.9	$V_{REF} - 0.5$	$V_{REF} + 0.5$	50	0.9	V_{REF}
HSTL_III_18		1.1	$V_{REF} - 0.5$	$V_{REF} + 0.5$	50	1.8	V_{REF}
SSTL18_I		0.9	$V_{REF} - 0.5$	$V_{REF} + 0.5$	50	0.9	V_{REF}
SSTL2_I		1.25	$V_{REF} - 0.75$	$V_{REF} + 0.75$	50	1.25	V_{REF}
Differential							
LVDS_25		-	$V_{ICM} - 0.125$	$V_{ICM} + 0.125$	50	1.2	V_{ICM}
BLVDS_25		-	$V_{ICM} - 0.125$	$V_{ICM} + 0.125$	1M	0	V_{ICM}
MINI_LVDS_25		-	$V_{ICM} - 0.125$	$V_{ICM} + 0.125$	50	1.2	V_{ICM}
LVPECL_25		-	$V_{ICM} - 0.3$	$V_{ICM} + 0.3$	1M	0	V_{ICM}
RSDS_25		-	$V_{ICM} - 0.1$	$V_{ICM} + 0.1$	50	1.2	V_{ICM}

Table 95: Test Methods for Timing Measurement at I/Os (Cont'd)

Signal Standard (IOSTANDARD)	Inputs			Outputs		Inputs and Outputs
	V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
DIFF_HSTL_I_18	-	$V_{REF} - 0.5$	$V_{REF} + 0.5$	50	0.9	V_{ICM}
DIFF_HSTL_III_18	-	$V_{REF} - 0.5$	$V_{REF} + 0.5$	50	1.8	V_{ICM}
DIFF_SSTL18_I	-	$V_{REF} - 0.5$	$V_{REF} + 0.5$	50	0.9	V_{ICM}
DIFF_SSTL2_I	-	$V_{REF} - 0.5$	$V_{REF} + 0.5$	50	1.25	V_{ICM}

Notes:

- Descriptions of the relevant symbols are as follows:
 V_{REF} – The reference voltage for setting the input switching threshold
 V_{ICM} – The common mode input voltage
 V_M – Voltage of measurement point on signal transition
 V_L – Low-level test voltage at Input pin
 V_H – High-level test voltage at Input pin
 R_T – Effective termination resistance, which takes on a value of 1M Ω when no parallel termination is required
 V_T – Termination voltage
- The load capacitance (C_L) at the Output pin is 0 pF for all signal standards.
- According to the PCI specification.

The capacitive load (C_L) is connected between the output and GND. *The Output timing for all standards, as published in the speed files and the data sheet, is always based on a C_L value of zero.* High-impedance probes (less than 1 pF) are used for all measurements. Any delay that the test fixture might contribute to test measurements is subtracted from those measurements to produce the final timing numbers as published in the speed files and data sheet.

Using IBIS Models to Simulate Load Conditions in Application

IBIS models permit the most accurate prediction of timing delays for a given application. The parameters found in the IBIS model (V_{REF} , R_{REF} , and V_{MEAS}) correspond directly with the parameters used in Table 95 (V_T , R_T , and V_M). Do not confuse V_{REF} (the termination voltage) from the IBIS model with V_{REF} (the input-switching threshold) from the table. A fourth parameter, C_{REF} is always zero. The four parameters describe all relevant output test conditions. IBIS models are found in the Xilinx development software as well as at the following link:

<http://www.xilinx.com/support/download/index.htm>

Delays for a given application are simulated according to its specific load conditions as follows:

- Simulate the desired signal standard with the output driver connected to the test setup shown in Figure 72. Use parameter values V_T , R_T , and V_M from Table 95. C_{REF} is zero.
- Record the time to V_M .
- Simulate the same signal standard with the output driver connected to the PCB trace with load. Use the appropriate IBIS model (including V_{REF} , R_{REF} , C_{REF} , and V_{MEAS} values) or capacitive value to represent the load.
- Record the time to V_{MEAS} .
- Compare the results of steps 2 and 4. Add (or subtract) the increase (or decrease) in delay to (or from) the appropriate Output standard adjustment (Table 94) to yield the worst-case delay of the PCB trace.

IEEE 1149.1/1532 JTAG Test Access Port Timing

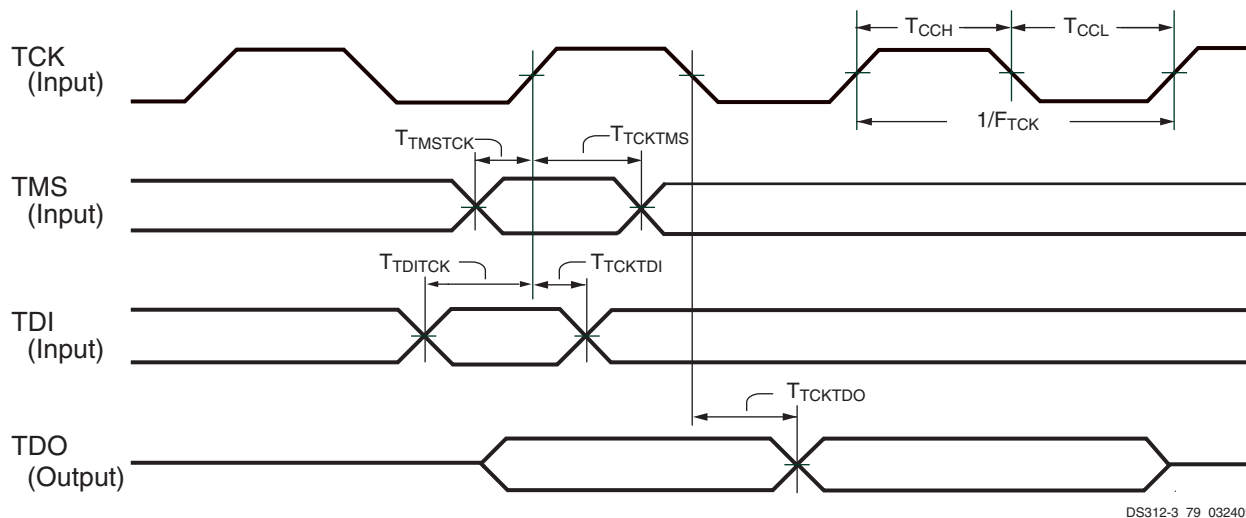


Figure 78: JTAG Waveforms

Table 123: Timing for the JTAG Test Access Port

Symbol	Description	All Speed Grades		Units
		Min	Max	
Clock-to-Output Times				
T _{TCKTDO}	The time from the falling transition on the TCK pin to data appearing at the TDO pin	1.0	11.0	ns
Setup Times				
T _{TDITCK}	The time from the setup of data at the TDI pin to the rising transition at the TCK pin	7.0	-	ns
T _{TMSTCK}	The time from the setup of a logic level at the TMS pin to the rising transition at the TCK pin	7.0	-	ns
Hold Times				
T _{TCKTDI}	The time from the rising transition at the TCK pin to the point when data is last held at the TDI pin	0	-	ns
T _{TCKTMS}	The time from the rising transition at the TCK pin to the point when a logic level is last held at the TMS pin	0	-	ns
Clock Timing				
T _{CCH}	The High pulse width at the TCK pin	5	-	ns
T _{CCL}	The Low pulse width at the TCK pin	5	-	ns
F _{TCK}	Frequency of the TCK signal	-	30	MHz

Notes:

- The numbers in this table are based on the operating conditions set forth in [Table 77](#).

Date	Version	Revision
08/26/09	3.8	Added reference to XAPP459 in Table 73 note 2. Updated BPI timing in Figure 77 , Table 119 , and Table 120 . Removed V_{REF} requirements for differential HSTL and differential SSTL in Table 95 . Added Spread Spectrum paragraph. Revised hold times for $T_{IOICKPD}$ in Table 88 and setup times for T_{DICK} in Table 98 . Added note 4 to Table 106 and note 3 to Table 107 , and updated note 6 for Table 107 to add input jitter.
10/29/12	4.0	Added Notice of Disclaimer . This product is not recommended for new designs. Revised note 2 in Table 73 . Revised note 2 and V_{IN} description in Table 77 , and added note 5. Added note 3 to Table 78 .

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User I/Os by Bank

Table 144, Table 145, and Table 146 indicate how the available user-I/O pins are distributed between the four I/O banks on the FT256 package.

The XC3S250E FPGA in the FT256 package has 18 unconnected balls, labeled with an “N.C.” type. These pins are also indicated with the black diamond (◆) symbol in Figure 85.

Table 144: User I/Os Per Bank on XC3S250E in the FT256 Package

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF ⁽¹⁾	CLK ⁽²⁾
Top	0	44	20	10	1	5	8
Right	1	42	10	7	21	4	0 ⁽²⁾
Bottom	2	44	8	9	24	3	0 ⁽²⁾
Left	3	42	24	7	0	3	8
TOTAL		172	62	33	46	15	16

Notes:

1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

Table 145: User I/Os Per Bank on XC3S500E in the FT256 Package

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF ⁽¹⁾	CLK ⁽²⁾
Top	0	46	22	10	1	5	8
Right	1	48	15	7	21	5	0 ⁽²⁾
Bottom	2	48	11	9	24	4	0 ⁽²⁾
Left	3	48	28	7	0	5	8
TOTAL		190	76	33	46	19	16

Notes:

1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

Table 146: User I/Os Per Bank on XC3S1200E in the FT256 Package

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF ⁽¹⁾	CLK ⁽²⁾
Top	0	46	24	8	1	5	8
Right	1	48	14	8	21	5	0 ⁽²⁾
Bottom	2	48	13	7	24	4	0 ⁽²⁾
Left	3	48	27	8	0	5	8
TOTAL		190	78	31	46	19	16

Notes:

1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

Table 148: FG320 Package Pinout (Cont'd)

Bank	XC3S500E Pin Name	XC3S1200E Pin Name	XC3S1600E Pin Name	FG320 Ball	Type
3	N.C. (◆)	IO_L22P_3	IO_L22P_3	P3	500E: N.C. 1200E: I/O 1600E: I/O
3	IO_L23N_3	IO_L23N_3	IO_L23N_3	R2	I/O
3	IO_L23P_3	IO_L23P_3	IO_L23P_3	R3	I/O
3	IO_L24N_3	IO_L24N_3	IO_L24N_3	T1	I/O
3	IO_L24P_3	IO_L24P_3	IO_L24P_3	T2	I/O
3	IP	IP	IP	D3	INPUT
3	IO	IP	IP	F4	500E: I/O 1200E: INPUT 1600E: INPUT
3	IP	IP	IP	F5	INPUT
3	IP	IP	IP	G1	INPUT
3	IP	IP	IP	J7	INPUT
3	IP	IP	IP	K2	INPUT
3	IP	IP	IP	K7	INPUT
3	IP	IP	IP	M1	INPUT
3	IP	IP	IP	N1	INPUT
3	IP	IP	IP	N2	INPUT
3	IP	IP	IP	R1	INPUT
3	IP	IP	IP	U1	INPUT
3	IP/VREF_3	IP/VREF_3	IP/VREF_3	J6	VREF
3	IO/VREF_3	IP/VREF_3	IP/VREF_3	R4	500E: VREF(I/O) 1200E: VREF(INPUT) 1600E: VREF(INPUT)
3	VCCO_3	VCCO_3	VCCO_3	F3	VCCO
3	VCCO_3	VCCO_3	VCCO_3	H7	VCCO
3	VCCO_3	VCCO_3	VCCO_3	K1	VCCO
3	VCCO_3	VCCO_3	VCCO_3	L7	VCCO
3	VCCO_3	VCCO_3	VCCO_3	N3	VCCO
GND	GND	GND	GND	A1	GND
GND	GND	GND	GND	A18	GND
GND	GND	GND	GND	B2	GND
GND	GND	GND	GND	B17	GND
GND	GND	GND	GND	C10	GND
GND	GND	GND	GND	G7	GND
GND	GND	GND	GND	G12	GND
GND	GND	GND	GND	H8	GND
GND	GND	GND	GND	H9	GND
GND	GND	GND	GND	H10	GND
GND	GND	GND	GND	H11	GND
GND	GND	GND	GND	J3	GND
GND	GND	GND	GND	J8	GND
GND	GND	GND	GND	J11	GND