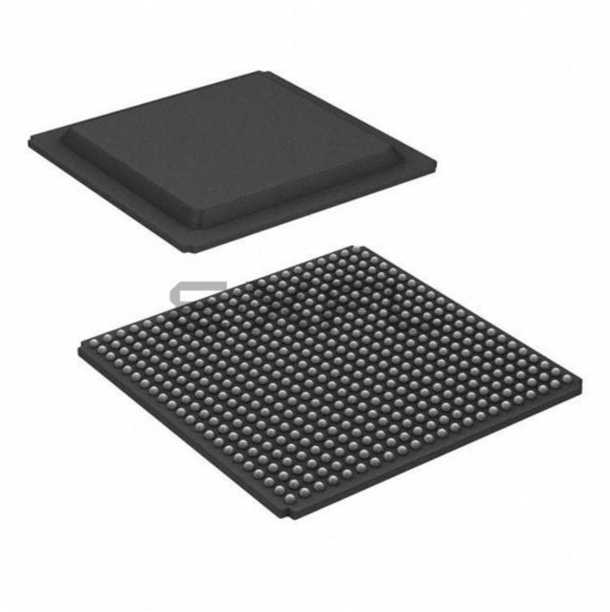
AMD Xilinx - XC3S1600E-4FGG484C Datasheet



Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	3688
Number of Logic Elements/Cells	33192
Total RAM Bits	663552
Number of I/O	376
Number of Gates	1600000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s1600e-4fgg484c

Architectural Overview

The Spartan-3E family architecture consists of five fundamental programmable functional elements:

- **Configurable Logic Blocks (CLBs)** contain flexible Look-Up Tables (LUTs) that implement logic plus storage elements used as flip-flops or latches. CLBs perform a wide variety of logical functions as well as store data.
- **Input/Output Blocks (IOBs)** control the flow of data between the I/O pins and the internal logic of the device. Each IOB supports bidirectional data flow plus 3-state operation. Supports a variety of signal standards, including four high-performance differential standards. Double Data-Rate (DDR) registers are included.
- **Block RAM** provides data storage in the form of 18-Kbit dual-port blocks.
- **Multiplier Blocks** accept two 18-bit binary numbers as inputs and calculate the product.
- **Digital Clock Manager (DCM) Blocks** provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase-shifting clock signals.

These elements are organized as shown in Figure 1. A ring of IOBs surrounds a regular array of CLBs. Each device has two columns of block RAM except for the XC3S100E, which has one column. Each RAM column consists of several 18-Kbit RAM blocks. Each block RAM is associated with a dedicated multiplier. The DCMs are positioned in the center with two at the top and two at the bottom of the device. The XC3S100E has only one DCM at the top and bottom, while the XC3S1200E and XC3S1600E add two DCMs in the middle of the left and right sides.

The Spartan-3E family features a rich network of traces that interconnect all five functional elements, transmitting signals among them. Each functional element has an associated switch matrix that permits multiple connections to the routing.

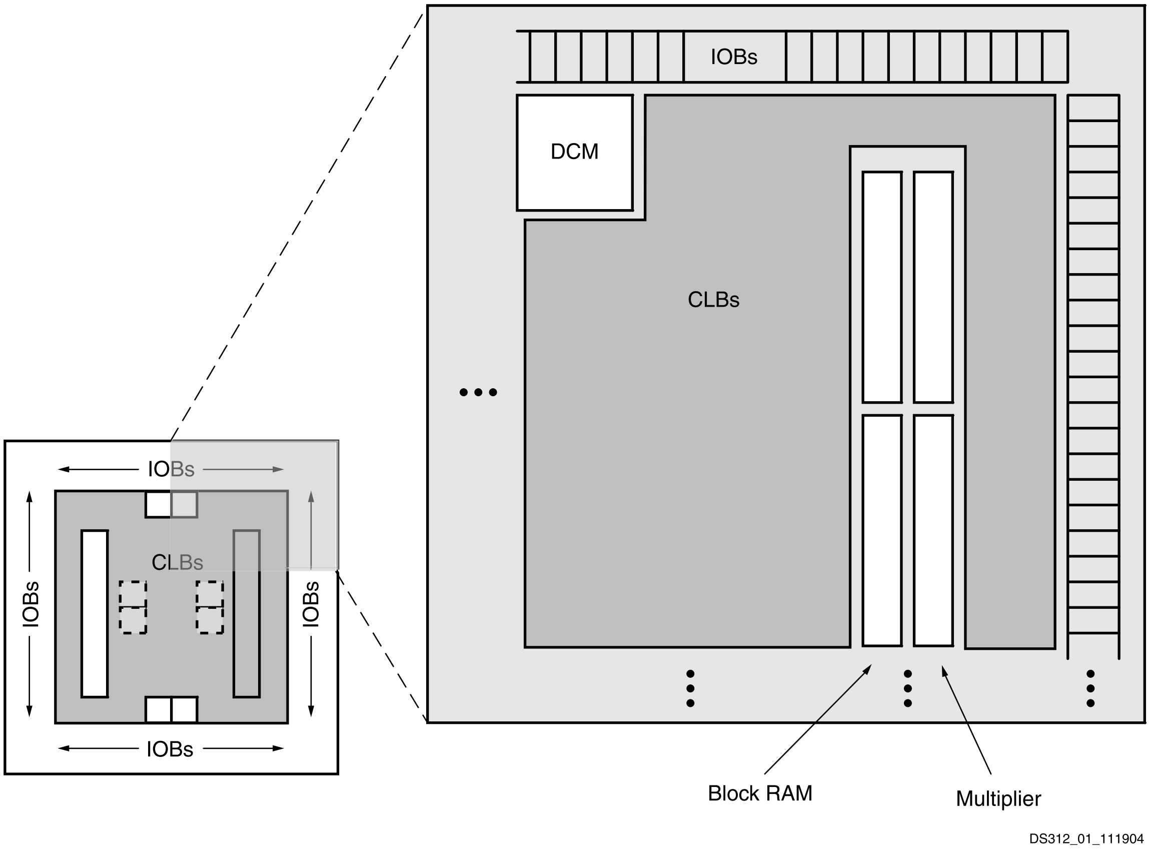


Figure 1: **Spartan-3E Family Architecture**

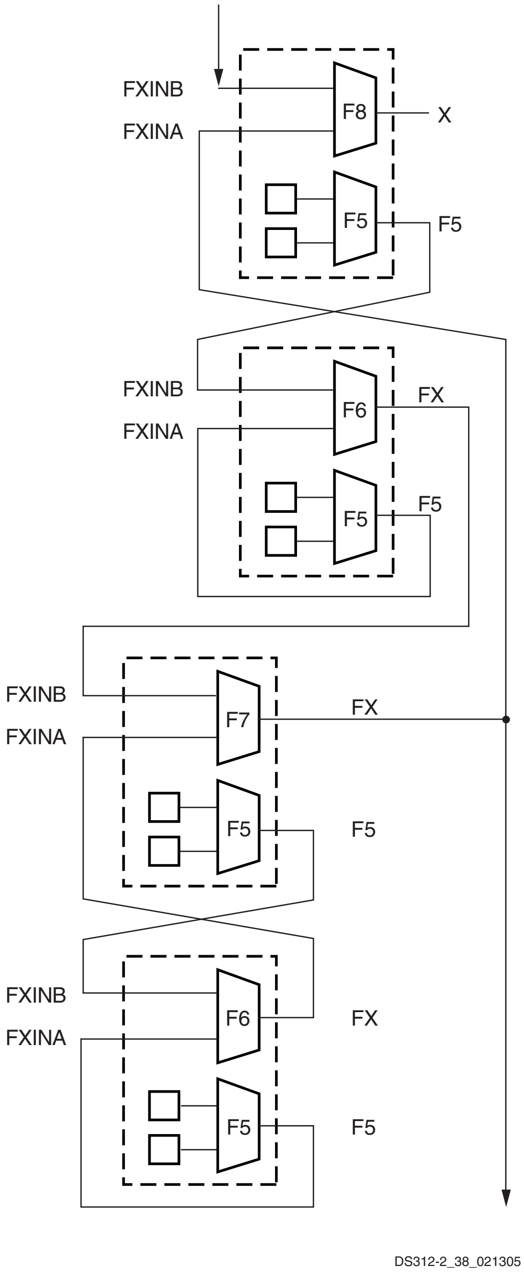


Figure 20: **MUXes and Dedicated Feedback in Spartan-3E CLB**

Table 11: **MUX Capabilities**

MUX	Usage	Input Source	Total Number of Inputs per Function		
			For Any Function	For MUX	For Limited Functions
F5MUX	F5MUX	LUTs	5	6 (4:1 MUX)	9
FiMUX	F6MUX	F5MUX	6	11 (8:1 MUX)	19
	F7MUX	F6MUX	7	20 (16:1 MUX)	39
	F8MUX	F7MUX	8	37 (32:1 MUX)	79

cancel out the clock skew. When the DLL phase-aligns the CLK0 signal with the CLKIN signal, it asserts the LOCKED output, indicating a lock on to the CLKIN signal.

DLL Attributes and Related Functions

The DLL unit has a variety of associated attributes as described in Table 29. Each attribute is described in detail in the sections that follow.

Table 29: **DLL Attributes**

Attribute	Description	Values
CLK_FEEDBACK	Chooses either the CLK0 or CLK2X output to drive the CLKFB input	NONE, ***1X***, 2X
CLKIN_DIVIDE_BY_2	Halves the frequency of the CLKIN signal just as it enters the DCM	***FALSE***, TRUE
CLKDV_DIVIDE	Selects the constant used to divide the CLKIN input frequency to generate the CLKDV output frequency	1.5, ***2***, 2.5, 3, 3.5, 4, 4.5, 5, 5.5, 6.0, 6.5, 7.0, 7.5, 8, 9, 10, 11, 12, 13, 14, 15, and 16
CLKIN_PERIOD	Additional information that allows the DLL to operate with the most efficient lock time and the best jitter tolerance	Floating-point value representing the CLKIN period in nanoseconds

DLL Clock Input Connections

For best results, an external clock source enters the FPGA via a Global Clock Input (GCLK). Each specific DCM has four possible direct, optimal GCLK inputs that feed the DCM's CLKIN input, as shown in Table 30. Table 30 also provides the specific pin numbers by package for each GCLK input. The two additional DCM's on the XC3S1200E and XC3S1600E have similar optimal connections from the left-edge LHCLK and the right-edge RHCLK inputs, as described in Table 31 and Table 32.

- The DCM supports differential clock inputs (for example, LVDS, LVPECL_25) via a pair of GCLK inputs that feed an internal single-ended signal to the DCM's CLKIN input.

Design Note

Avoid using global clock input GCLK1 as it is always shared with the M2 mode select pin. Global clock inputs GCLK0, GCLK2, GCLK3, GCLK12, GCLK13, GCLK14, and GCLK15 have shared functionality in some configuration modes.

VARIABLE Phase Shift Mode

In VARIABLE phase shift mode, the FPGA application dynamically adjusts the fine phase shift value using three inputs to the PS unit (PSEN, PSCLK, and PSINCDEC), as defined in Table 36 and shown in Figure 40.

Table 36: **Signals for Variable Phase Mode**

Signal	Direction	Description
PSEN[1]	Input	Enables the Phase Shift unit for variable phase adjustment.
PSCLK[1]	Input	Clock to synchronize phase shift adjustment.
PSINCDEC[1]	Input	When High, increments the current phase shift value. When Low, decrements the current phase shift value. This signal is synchronized to the PSCLK signal.
PSDONE	Output	Goes High to indicate that the present phase adjustment is complete and PS unit is ready for next phase adjustment request. This signal is synchronized to the PSCLK signal.

Notes:

1. This input supports either a true or inverted polarity.

The FPGA application uses the three PS inputs on the Phase Shift unit to dynamically and incrementally increase or decrease the phase shift amount on all nine DCM clock outputs.

To adjust the current phase shift value, the PSEN enable signal must be High to enable the PS unit. Coincidently, PSINCDEC must be High to increment the current phase shift amount or Low to decrement the current amount. All VARIABLE phase shift operations are controlled by the PSCLK input, which can be the CLKIN signal or any other clock signal.

Design Note

The VARIABLE phase shift feature operates differently from the Spartan-3 DCM; use the DCM_SP primitive, not the DCM primitive.

DCM_DELAY_STEP

DCM_DELAY_STEP is the finest delay resolution available in the PS unit. Its value is provided at the bottom of Table 105 in Module 3. For each enabled PSCLK cycle that PSINCDEC is High, the PS unit adds one DCM_DELAY_STEP of phase shift to all nine DCM outputs. Similarly, for each enabled PSCLK cycle that PSINCDEC is Low, the PS unit subtracts one DCM_ DELAY_STEP of phase shift from all nine DCM outputs.

Because each DCM_DELAY_STEP has a minimum and maximum value, the actual phase shift delay for the present phase increment/decrement value (VALUE) falls within the minimum and maximum values according to Equation 4 and Equation 5.

$$T_{PS}(Max) = VALUE \bullet \text{DCM\_DELAY\_STEP\_MAX} \qquad Eq\ 4$$

$$T_{PS}(Min) = VALUE \bullet \text{DCM\_DELAY\_STEP\_MIN} \qquad Eq\ 5$$

The maximum variable phase shift steps, MAX_STEPS, is described in Equation 6 or Equation 7, for a given CLKIN input period, T_{CLKIN}, in nanoseconds. To convert this to a phase shift range measured in time and not steps, use MAX_STEPS derived in Equation 6 and Equation 7 for VALUE in Equation 4 and Equation 5.

If CLKIN < 60 MHz:

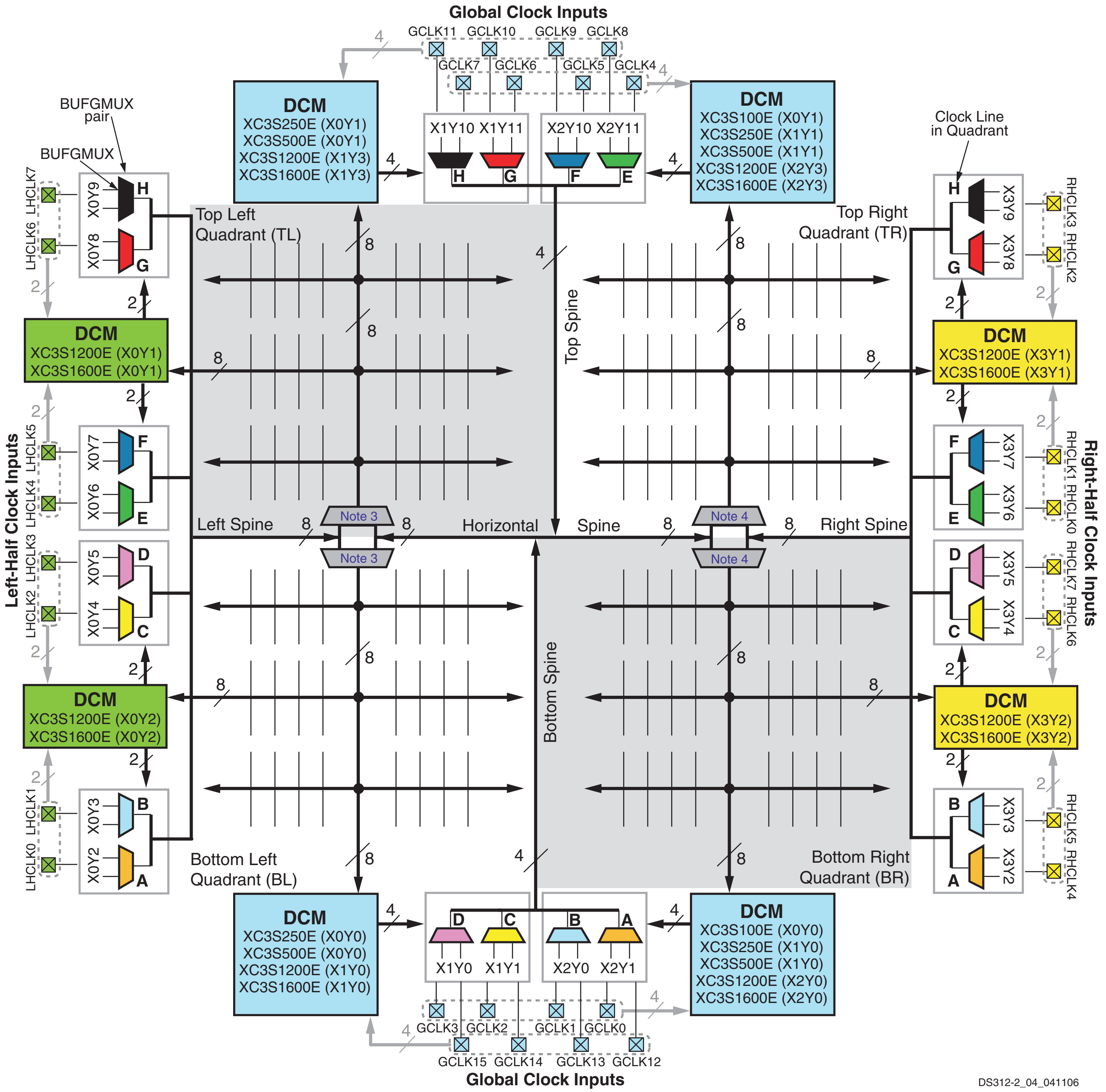
$$\text{MAX\_STEPS} = \pm[INTEGER(10 \bullet (T_{CLKIN} - 3))] \qquad Eq\ 6$$

If CLKIN ≥ 60 MHz:

$$\text{MAX\_STEPS} = \pm[INTEGER(15 \bullet (T_{CLKIN} - 3))] \qquad Eq\ 7$$

The phase adjustment might require as many as 100 CLKIN cycles plus 3 PSCLK cycles to take effect, at which point the DCM's PSDONE output goes High for one PSCLK cycle. This pulse indicates that the PS unit completed the previous adjustment and is now ready for the next request.

Asserting the Reset (RST) input returns the phase shift to zero.



Notes:

1. The diagram presents electrical connectivity. The diagram locations do not necessarily match the physical location on the device, although the coordinate locations shown are correct.
2. Number of DCMs and locations of these DCM varies for different device densities. The left and right DCMs are only in the XC3S1200E and XC3S1600E. The XC3S100E has only two DCMs, one on the top right and one on the bottom right of the die.
3. See Figure 47a, which shows how the eight clock lines are multiplexed on the left-hand side of the device.
4. See Figure 47b, which shows how the eight clock lines are multiplexed on the right-hand side of the device.
5. For best direct clock inputs to a particular clock buffer, not a DCM, see Table 41.
6. For best direct clock inputs to a particular DCM, not a BUFGMUX, see Table 30, Table 31, and Table 32. Direct pin inputs to a DCM are shown in gray.

Figure 45: **Spartan-3E Internal Quadrant-Based Clock Network (Electrical Connectivity View)**

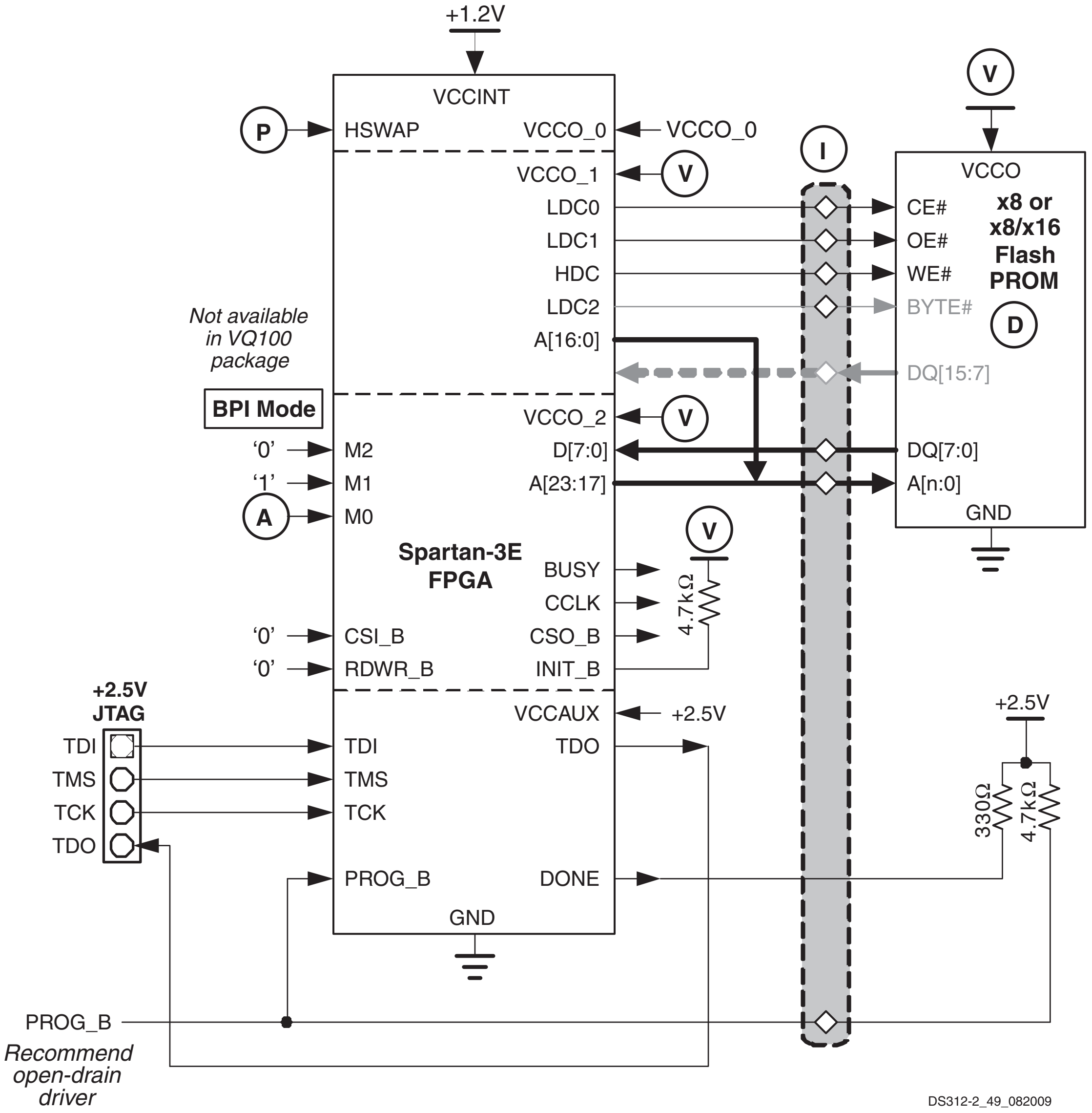


Figure 58: **Byte-wide Peripheral Interface (BPI) Mode Configured from Parallel NOR Flash PROMs**

Ⓐ During configuration, the value of the M0 mode pin determines how the FPGA generates addresses, as shown Table 58. When M0 = 0, the FPGA generates addresses starting at 0 and increments the address on every falling CCLK edge. Conversely, when M0 = 1, the FPGA generates addresses starting at `0xFF_FFFF` (all ones) and decrements the address on every falling CCLK edge.

Table 58: **BPI Addressing Control**

M2	M1	M0	Start Address	Addressing
0	1	0	0	Incrementing
		1	`0xFF_FFFF`	Decrementing

Switching Characteristics

All Spartan-3E FPGAs ship in two speed grades: -4 and the higher performance -5. Switching characteristics in this document may be designated as Advance, Preliminary, or Production, as shown in Table 84. Each category is defined as follows:

Advance: These specifications are based on simulations only and are typically available soon after establishing FPGA specifications. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These specifications are based on complete early silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting preliminary delays is greatly reduced compared to Advance data.

Production: These specifications are approved once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Software Version Requirements

Production-quality systems must use FPGA designs compiled using a speed file designated as PRODUCTION status. FPGAs designs using a less mature speed file designation should only be used during system prototyping or pre-production qualification. FPGA designs with speed files designated as Advance or Preliminary should not be used in a production-quality system.

Whenever a speed file designation changes, as a device matures toward Production status, rerun the latest Xilinx ISE software on the FPGA design to ensure that the FPGA design incorporates the latest timing information and software updates.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all Spartan-3E devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.**

Create a Xilinx user account and sign up to receive automatic e-mail notification whenever this data sheet or the associated user guides are updated.

Sign Up for Alerts on Xilinx.com
https://secure.xilinx.com/webreg/register.do?group=myprofile&languageID=1

Timing parameters and their representative values are selected for inclusion below either because they are important as general design requirements or they indicate fundamental device performance characteristics. The Spartan-3E speed files (v1.27), part of the Xilinx Development Software, are the original source for many but not all of the values. The speed grade designations for these files are shown in Table 84. For more complete, more precise, and worst-case data, use the values reported by the Xilinx static timing analyzer (TRACE in the Xilinx development software) and back-annotated to the simulation netlist.

Table 84: **Spartan-3E v1.27 Speed Grade Designations**

Device	Advance	Preliminary	Production
XC3S100E			-MIN, -4, -5
XC3S250E			-MIN, -4, -5
XC3S500E			-MIN, -4, -5
XC3S1200E			-MIN, -4, -5
XC3S1600E			-MIN, -4, -5

Table 85 provides the history of the Spartan-3E speed files since all devices reached Production status.

Table 85: **Spartan-3E Speed File Version History**

Version	ISE Release	Description
1.27	9.2.03i	Added XA Automotive.
1.26	8.2.02i	Added -0/-MIN speed grade, which includes minimum values.
1.25	8.2.01i	Added XA Automotive devices to speed file. Improved model for left and right DCMs.
1.23	8.2i	Updated input setup/hold values based on default IFD_DELAY_VALUE settings.
1.21	8.1.03i	All Spartan-3E FPGAs and all speed grades elevated to Production status.

Simultaneously Switching Output Guidelines

This section provides guidelines for the recommended maximum allowable number of Simultaneous Switching Outputs (SSOs). These guidelines describe the maximum number of user I/O pins of a given output signal standard that should simultaneously switch in the same direction, while maintaining a safe level of switching noise. Meeting these guidelines for the stated test conditions ensures that the FPGA operates free from the adverse effects of ground and power bounce.

Ground or power bounce occurs when a large number of outputs simultaneously switch in the same direction. The output drive transistors all conduct current to a common voltage rail. Low-to-High transitions conduct to the V_{CCO} rail; High-to-Low transitions conduct to the GND rail. The resulting cumulative current transient induces a voltage difference across the inductance that exists between the die pad and the power supply or ground return. The inductance is associated with bonding wires, the package lead frame, and any other signal routing inside the package. Other variables contribute to SSO noise levels, including stray inductance on the PCB as well as capacitive loading at receivers. Any SSO-induced voltage consequently affects internal switching noise margins and ultimately signal quality.

Table 96 and Table 97 provide the essential SSO guidelines. For each device/package combination, Table 96 provides the number of equivalent V_{CCO}/GND pairs. The equivalent number of pairs is based on characterization and might not match the physical number of pairs. For each output signal standard and drive strength, Table 97 recommends the maximum number of SSOs, switching in the same direction, allowed per V_{CCO}/GND pair within an I/O bank. The guidelines in Table 97 are categorized by package style. Multiply the appropriate numbers from Table 96 and Table 97 to calculate the maximum number of SSOs allowed within an I/O bank. Exceeding these SSO guidelines might result in increased power or ground bounce, degraded signal integrity, or increased system jitter.

SSO_{MAX}/IO Bank = Table 96 x Table 97

The recommended maximum SSO values assumes that the FPGA is soldered on the printed circuit board and that the board uses sound design practices. The SSO values do not apply for FPGAs mounted in sockets, due to the lead inductance introduced by the socket.

The number of SSOs allowed for quad-flat packages (VQ, TQ, PQ) is lower than for ball grid array packages (FG) due to the larger lead inductance of the quad-flat packages. The results for chip-scale packaging (CP132) are better than quad-flat packaging but not as high as for ball grid array packaging. Ball grid array packages are recommended for applications with a large number of simultaneously switching outputs.

Table 96: **Equivalent V_{CCO}/GND Pairs per Bank**

Device	Package Style *(including Pb-free)*							
	VQ100	CP132	TQ144	PQ208	FT256	FG320	FG400	FG484
XC3S100E	2	2	2	-	-	-	-	-
XC3S250E	2	2	2	3	4	-	-	-
XC3S500E	2	2	-	3	4	5	-	-
XC3S1200E	-	-	-	-	4	5	6	-
XC3S1600E	-	-	-	-	-	5	6	7

Block RAM Timing

Table 103: **Block RAM Timing**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{BCKO}	When reading from block RAM, the delay from the active transition at the CLK input to data appearing at the DOUT output	-	2.45	-	2.82	ns
Setup Times						
T_{BACK}	Setup time for the ADDR inputs before the active transition at the CLK input of the block RAM	0.33	-	0.38	-	ns
T_{BDCK}	Setup time for data at the DIN inputs before the active transition at the CLK input of the block RAM	0.23	-	0.23	-	ns
T_{BECK}	Setup time for the EN input before the active transition at the CLK input of the block RAM	0.67	-	0.77	-	ns
T_{BWCK}	Setup time for the WE input before the active transition at the CLK input of the block RAM	1.09	-	1.26	-	ns
Hold Times						
T_{BCKA}	Hold time on the ADDR inputs after the active transition at the CLK input	0.12	-	0.14	-	ns
T_{BCKD}	Hold time on the DIN inputs after the active transition at the CLK input	0.12	-	0.13	-	ns
T_{BCKE}	Hold time on the EN input after the active transition at the CLK input	0	-	0	-	ns
T_{BCKW}	Hold time on the WE input after the active transition at the CLK input	0	-	0	-	ns
Clock Timing						
T_{BPWH}	High pulse width of the CLK signal	1.39	-	1.59	-	ns
T_{BPWL}	Low pulse width of the CLK signal	1.39	-	1.59	-	ns
Clock Frequency						
F_{BRAM}	Block RAM clock frequency. RAM read output value written back into RAM, for shift-registers and circular buffers. Write-only or read-only performance is faster.	0	270	0	230	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 77.

Phase Shifter (PS)

Table 108: **Recommended Operating Conditions for the PS in Variable Phase Mode**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Operating Frequency Ranges						
PSCLK_FREQ (F_{PSCLK})	Frequency for the PSCLK input	1	167	1	167	MHz
Input Pulse Requirements						
PSCLK_PULSE	PSCLK pulse width as a percentage of the PSCLK period	40%	60%	40%	60%	-

Table 109: **Switching Characteristics for the PS in Variable Phase Mode**

Symbol	Description	Equation		Units
Phase Shifting Range				
MAX_STEPS[2]	Maximum allowed number of DCM_DELAY_STEP steps for a given CLKIN clock period, where T = CLKIN clock period in ns. If using CLKIN_DIVIDE_BY_2 = TRUE, double the effective clock period.[3]	CLKIN < 60 MHz	±[INTEGER(10 • (T_{CLKIN} – 3 ns))]	steps
		CLKIN ≥ 60 MHz	±[INTEGER(15 • (T_{CLKIN} – 3 ns))]	steps
FINE_SHIFT_RANGE_MIN	Minimum guaranteed delay for variable phase shifting	±[MAX_STEPS • DCM_DELAY_STEP_MIN]		ns
FINE_SHIFT_RANGE_MAX	Maximum guaranteed delay for variable phase shifting	±[MAX_STEPS • DCM_DELAY_STEP_MAX]		ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 77 and Table 108.
2. The maximum variable phase shift range, MAX_STEPS, is only valid when the DCM is has no initial fixed phase shifting, i.e., the PHASE_SHIFT attribute is set to 0.
3. The DCM_DELAY_STEP values are provided at the bottom of Table 105.

Miscellaneous DCM Timing

Table 110: **Miscellaneous DCM Timing**

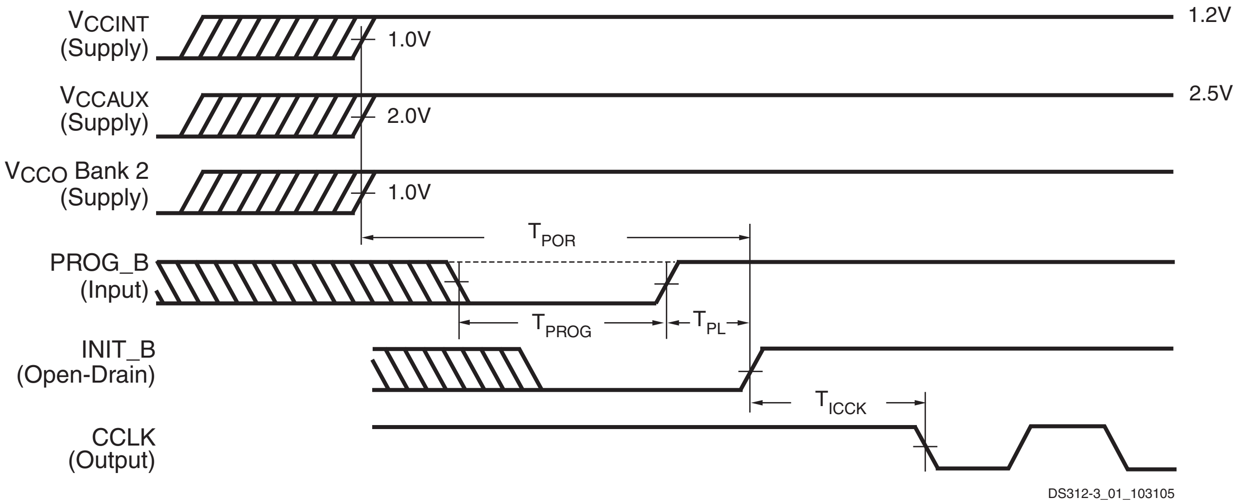
Symbol	Description	Min	Max	Units
DCM_RST_PW_MIN[1]	Minimum duration of a RST pulse width	3	-	CLKIN cycles
DCM_RST_PW_MAX[2]	Maximum duration of a RST pulse width	N/A	N/A	seconds
DCM_CONFIG_LAG_TIME[3]	Maximum duration from V_{CCINT} applied to FPGA configuration successfully completed (DONE pin goes High) and clocks applied to DCM DLL	N/A	N/A	minutes

Notes:

1. This limit only applies to applications that use the DCM DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV). The DCM DFS outputs (CLKFX, CLKFX180) are unaffected.
2. This specification is equivalent to the Virtex-4 DCM_RESET specfication.This specification does not apply for Spartan-3E FPGAs.
3. This specification is equivalent to the Virtex-4 TCONFIG specification. This specification does not apply for Spartan-3E FPGAs.

Configuration and JTAG Timing

General Configuration Power-On/Reconfigure Timing



Notes:

1. The V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies may be applied in any order.
2. The Low-going pulse on PROG_B is optional after power-on but necessary for reconfiguration without a power cycle.
3. The rising edge of INIT_B samples the voltage levels applied to the mode pins (M0 - M2).

Figure 73: **Waveforms for Power-On and the Beginning of Configuration**

Table 111: **Power-On Timing and the Beginning of Configuration**

Symbol	Description	Device	All Speed Grades		Units
			Min	Max	
T_{POR}[2]	The time from the application of V_{CCINT}, V_{CCAUX}, and V_{CCO} Bank 2 supply voltage ramps (whichever occurs last) to the rising transition of the INIT_B pin	XC3S100E	-	5	ms
		XC3S250E	-	5	ms
		XC3S500E	-	5	ms
		XC3S1200E	-	5	ms
		XC3S1600E	-	7	ms
T_{PROG}	The width of the low-going pulse on the PROG_B pin	All	0.5	-	µs
T_{PL}[2]	The time from the rising edge of the PROG_B pin to the rising transition on the INIT_B pin	XC3S100E	-	0.5	ms
		XC3S250E	-	0.5	ms
		XC3S500E	-	1	ms
		XC3S1200E	-	2	ms
		XC3S1600E	-	2	ms
T_{INIT}	Minimum Low pulse width on INIT_B output	All	250	-	ns
T_{ICCK}[3]	The time from the rising edge of the INIT_B pin to the generation of the configuration clock signal at the CCLK output pin	All	0.5	4.0	µs

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 77. This means power must be applied to all V_{CCINT}, V_{CCO}, and V_{CCAUX} lines.
2. Power-on reset and the clearing of configuration memory occurs during this period.
3. This specification applies only to the Master Serial, SPI, BPI-Up, and BPI-Down modes.

User I/Os by Bank

Table 138 and Table 139 indicate how the 108 available user-I/O pins are distributed between the four I/O banks on the TQ144 package.

Table 138: **User I/Os Per Bank for the XC3S100E in the TQ144 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF[1]	CLK[2]
Top	0	26	9	6	1	2	8
Right	1	28	0	5	21	2	0[2]
Bottom	2	26	0	4	20	2	0[2]
Left	3	28	13	4	0	3	8
TOTAL		**108**	**22**	**19**	**42**	**9**	**16**

Notes:

1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

Table 139: **User I/Os Per Bank for the XC3S250E in TQ144 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF[1]	CLK[2]
Top	0	26	9	6	1	2	8
Right	1	28	0	5	21	2	0[2]
Bottom	2	26	0	4	20	2	0[2]
Left	3	28	11	6	0	3	8
TOTAL		**108**	**20**	**21**	**42**	**9**	**16**

Notes:

1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

Footprint Migration Differences

Table 140 summarizes any footprint and functionality differences between the XC3S100E and the XC3S250E FPGAs that may affect easy migration between devices. There are four such pins. All other pins not listed in Table 140 unconditionally migrate between Spartan-3E devices available in the TQ144 package.

The arrows indicate the direction for easy migration. For example, a left-facing arrow indicates that the pin on the XC3S250E unconditionally migrates to the pin on the XC3S100E. It may be possible to migrate the opposite direction depending on the I/O configuration. For example, an I/O pin (Type = I/O) can migrate to an input-only pin (Type = INPUT) if the I/O pin is configured as an input.

Table 140: **TQ144 Footprint Migration Differences**

TQ144 Pin	Bank	XC3S100E Type	Migration	XC3S250E Type
P10	3	I/O	←	INPUT
P29	3	I/O	←	INPUT
P31	3	VREF(INPUT)	→	VREF(I/O)
P66	2	VREF(INPUT)	→	VREF(I/O)
DIFFERENCES			**4**	

Legend:

→	This pin can unconditionally migrate from the device on the left to the device on the right. Migration in the other direction may be possible depending on how the pin is configured for the device on the right.
←	This pin can unconditionally migrate from the device on the right to the device on the left. Migration in the other direction may be possible depending on how the pin is configured for the device on the left.

Table 143: **FT256 Package Pinout *(Cont'd)***

Bank	XC3S250E Pin Name	XC3S500E Pin Name	XC3S1200E Pin Name	FT256 Ball	Type
2	N.C. (◆)	IO_L14N_2/VREF_2	IO_L14N_2/VREF_2	R10	***250E:*** N.C. ***500E:*** VREF ***1200E:*** VREF
2	N.C. (◆)	IO_L14P_2	IO_L14P_2	P10	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O
2	IO_L15N_2	IO_L15N_2	IO_L15N_2	M10	I/O
2	IO_L15P_2	IO_L15P_2	IO_L15P_2	N10	I/O
2	IO_L16N_2/A22	IO_L16N_2/A22	IO_L16N_2/A22	P11	DUAL
2	IO_L16P_2/A23	IO_L16P_2/A23	IO_L16P_2/A23	R11	DUAL
2	IO_L18N_2/A20	IO_L18N_2/A20	IO_L18N_2/A20	N12	DUAL
2	IO_L18P_2/A21	IO_L18P_2/A21	IO_L18P_2/A21	P12	DUAL
2	IO_L19N_2/VS1/A18	IO_L19N_2/VS1/A18	IO_L19N_2/VS1/A18	R13	DUAL
2	IO_L19P_2/VS2/A19	IO_L19P_2/VS2/A19	IO_L19P_2/VS2/A19	T13	DUAL
2	IO_L20N_2/CCLK	IO_L20N_2/CCLK	IO_L20N_2/CCLK	R14	DUAL
2	IO_L20P_2/VS0/A17	IO_L20P_2/VS0/A17	IO_L20P_2/VS0/A17	P14	DUAL
2	IP	IP	IP	T2	INPUT
2	IP	IP	IP	T14	INPUT
2	IP_L02N_2	IP_L02N_2	IP_L02N_2	R3	INPUT
2	IP_L02P_2	IP_L02P_2	IP_L02P_2	T3	INPUT
2	IP_L08N_2/VREF_2	IP_L08N_2/VREF_2	IP_L08N_2/VREF_2	T7	VREF
2	IP_L08P_2	IP_L08P_2	IP_L08P_2	R7	INPUT
2	IP_L11N_2/M2/GCLK1	IP_L11N_2/M2/GCLK1	IP_L11N_2/M2/GCLK1	R9	DUAL/GCLK
2	IP_L11P_2/RDWR_B/ GCLK0	IP_L11P_2/RDWR_B/ GCLK0	IP_L11P_2/RDWR_B/ GCLK0	T9	DUAL/GCLK
2	IP_L17N_2	IP_L17N_2	IP_L17N_2	M11	INPUT
2	IP_L17P_2	IP_L17P_2	IP_L17P_2	N11	INPUT
2	VCCO_2	VCCO_2	VCCO_2	L7	VCCO
2	VCCO_2	VCCO_2	VCCO_2	L10	VCCO
2	VCCO_2	VCCO_2	VCCO_2	R5	VCCO
2	VCCO_2	VCCO_2	VCCO_2	R12	VCCO
3	IO_L01N_3	IO_L01N_3	IO_L01N_3	B2	I/O
3	IO_L01P_3	IO_L01P_3	IO_L01P_3	B1	I/O
3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	C2	VREF
3	IO_L02P_3	IO_L02P_3	IO_L02P_3	C1	I/O
3	IO_L03N_3	IO_L03N_3	IO_L03N_3	E4	I/O
3	IO_L03P_3	IO_L03P_3	IO_L03P_3	E3	I/O
3	N.C. (◆)	IO_L04N_3/VREF_3	IO_L04N_3/VREF_3	F4	***250E:*** N.C. ***500E:*** VREF ***1200E:*** VREF
3	N.C. (◆)	IO_L04P_3	IO_L04P_3	F3	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O
3	IO_L05N_3	IO_L05N_3	IO_L05N_3	E1	I/O
3	IO_L05P_3	IO_L05P_3	IO_L05P_3	D1	I/O
3	IO_L06N_3	IO_L06N_3	IO_L06N_3	G4	I/O

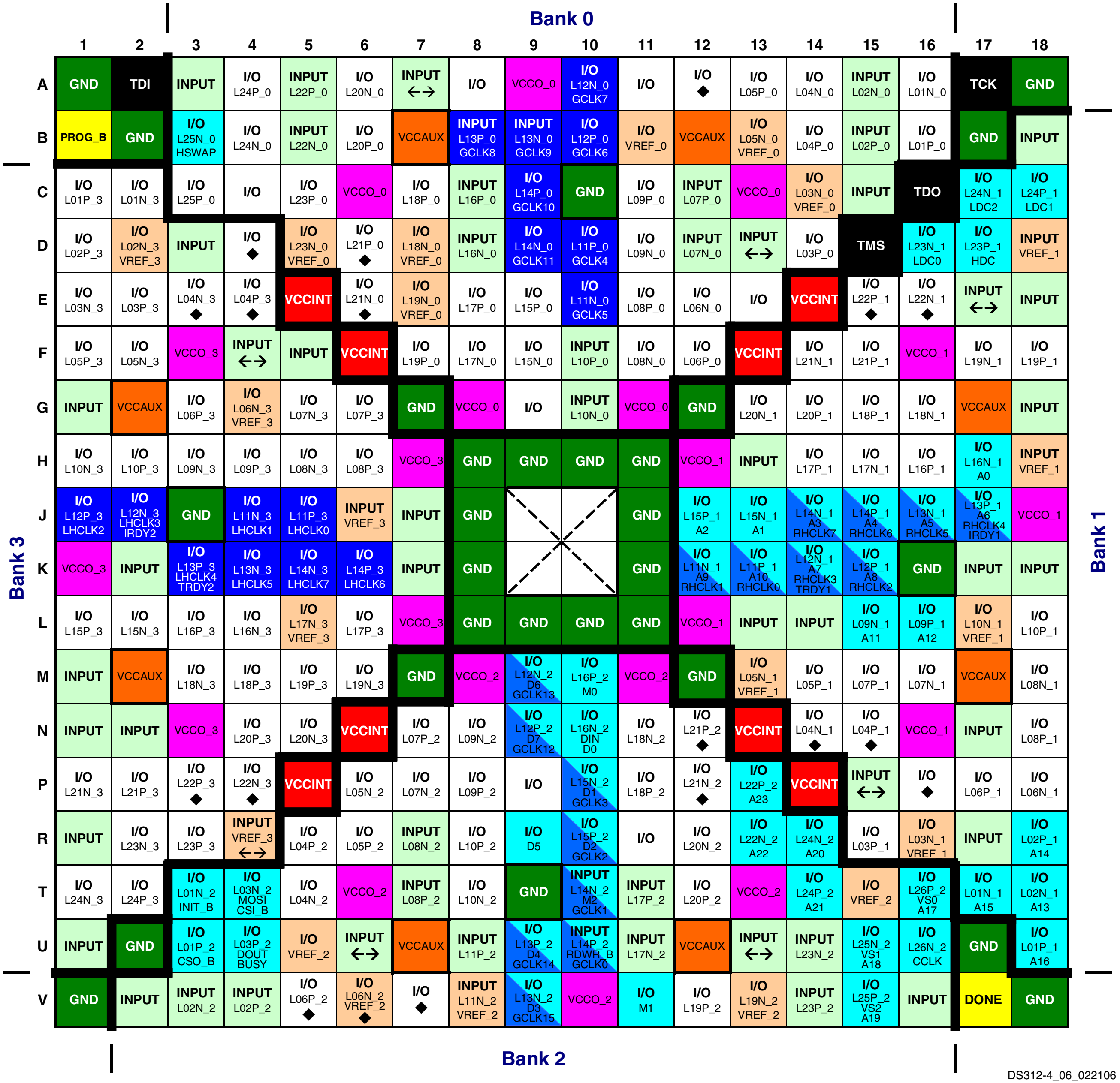
Table 143: **FT256 Package Pinout *(Cont'd)***

Bank	XC3S250E Pin Name	XC3S500E Pin Name	XC3S1200E Pin Name	FT256 Ball	Type
3	IP	IP	IP	N3	INPUT
3	IP/VREF_3	IP/VREF_3	IP/VREF_3	G1	VREF
3	IO/VREF_3	IO/VREF_3	IP/VREF_3	N2	***250E:*** VREF(I/O) ***500E:*** VREF(I/O) ***1200E:*** VREF(INPUT)
3	VCCO_3	VCCO_3	VCCO_3	E2	VCCO
3	VCCO_3	VCCO_3	VCCO_3	G6	VCCO
3	VCCO_3	VCCO_3	VCCO_3	K6	VCCO
3	VCCO_3	VCCO_3	VCCO_3	M2	VCCO
GND	GND	GND	GND	A1	GND
GND	GND	GND	GND	A16	GND
GND	GND	GND	GND	B9	GND
GND	GND	GND	GND	F6	GND
GND	GND	GND	GND	F11	GND
GND	GND	GND	GND	G7	GND
GND	GND	GND	GND	G8	GND
GND	GND	GND	GND	G9	GND
GND	GND	GND	GND	G10	GND
GND	GND	GND	GND	H2	GND
GND	GND	GND	GND	H7	GND
GND	GND	GND	GND	H8	GND
GND	GND	GND	GND	H9	GND
GND	GND	GND	GND	H10	GND
GND	GND	GND	GND	J7	GND
GND	GND	GND	GND	J8	GND
GND	GND	GND	GND	J9	GND
GND	GND	GND	GND	J10	GND
GND	GND	GND	GND	J15	GND
GND	GND	GND	GND	K7	GND
GND	GND	GND	GND	K8	GND
GND	GND	GND	GND	K9	GND
GND	GND	GND	GND	K10	GND
GND	GND	GND	GND	L6	GND
GND	GND	GND	GND	L11	GND
GND	GND	GND	GND	R8	GND
GND	GND	GND	GND	T1	GND
GND	GND	GND	GND	T16	GND
VCCAUX	DONE	DONE	DONE	T15	CONFIG
VCCAUX	PROG_B	PROG_B	PROG_B	D3	CONFIG
VCCAUX	TCK	TCK	TCK	A15	JTAG
VCCAUX	TDI	TDI	TDI	A2	JTAG
VCCAUX	TDO	TDO	TDO	C14	JTAG
VCCAUX	TMS	TMS	TMS	B15	JTAG
VCCAUX	VCCAUX	VCCAUX	VCCAUX	A6	VCCAUX

Table 148: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S500E Pin Name	XC3S1200E Pin Name	XC3S1600E Pin Name	FG320 Ball	Type
2	IP	IO	IO	U6	**500E:** INPUT **1200E:** I/O **1600E:** I/O
2	IP	IO	IO	U13	**500E:** INPUT **1200E:** I/O **1600E:** I/O
2	N.C. (◆)	IO	IO	V7	**500E:** N.C. **1200E:** I/O **1600E:** I/O
2	IO/D5	IO/D5	IO/D5	R9	DUAL
2	IO/M1	IO/M1	IO/M1	V11	DUAL
2	IO/VREF_2	IO/VREF_2	IO/VREF_2	T15	VREF
2	IO/VREF_2	IO/VREF_2	IO/VREF_2	U5	VREF
2	IO_L01N_2/INIT_B	IO_L01N_2/INIT_B	IO_L01N_2/INIT_B	T3	DUAL
2	IO_L01P_2/CSO_B	IO_L01P_2/CSO_B	IO_L01P_2/CSO_B	U3	DUAL
2	IO_L03N_2/MOSI/CSI_B	IO_L03N_2/MOSI/CSI_B	IO_L03N_2/MOSI/CSI_B	T4	DUAL
2	IO_L03P_2/DOUT/BUSY	IO_L03P_2/DOUT/BUSY	IO_L03P_2/DOUT/BUSY	U4	DUAL
2	IO_L04N_2	IO_L04N_2	IO_L04N_2	T5	I/O
2	IO_L04P_2	IO_L04P_2	IO_L04P_2	R5	I/O
2	IO_L05N_2	IO_L05N_2	IO_L05N_2	P6	I/O
2	IO_L05P_2	IO_L05P_2	IO_L05P_2	R6	I/O
2	N.C. (◆)	IO_L06N_2/VREF_2	IO_L06N_2/VREF_2	V6	**500E:** N.C. **1200E:** VREF **1600E:** VREF
2	N.C. (◆)	IO_L06P_2	IO_L06P_2	V5	**500E:** N.C. **1200E:** I/O **1600E:** I/O
2	IO_L07N_2	IO_L07N_2	IO_L07N_2	P7	I/O
2	IO_L07P_2	IO_L07P_2	IO_L07P_2	N7	I/O
2	IO_L09N_2	IO_L09N_2	IO_L09N_2	N8	I/O
2	IO_L09P_2	IO_L09P_2	IO_L09P_2	P8	I/O
2	IO_L10N_2	IO_L10N_2	IO_L10N_2	T8	I/O
2	IO_L10P_2	IO_L10P_2	IO_L10P_2	R8	I/O
2	IO_L12N_2/D6/GCLK13	IO_L12N_2/D6/GCLK13	IO_L12N_2/D6/GCLK13	M9	DUAL/GCLK
2	IO_L12P_2/D7/GCLK12	IO_L12P_2/D7/GCLK12	IO_L12P_2/D7/GCLK12	N9	DUAL/GCLK
2	IO_L13N_2/D3/GCLK15	IO_L13N_2/D3/GCLK15	IO_L13N_2/D3/GCLK15	V9	DUAL/GCLK
2	IO_L13P_2/D4/GCLK14	IO_L13P_2/D4/GCLK14	IO_L13P_2/D4/GCLK14	U9	DUAL/GCLK
2	IO_L15N_2/D1/GCLK3	IO_L15N_2/D1/GCLK3	IO_L15N_2/D1/GCLK3	P10	DUAL/GCLK
2	IO_L15P_2/D2/GCLK2	IO_L15P_2/D2/GCLK2	IO_L15P_2/D2/GCLK2	R10	DUAL/GCLK
2	IO_L16N_2/DIN/D0	IO_L16N_2/DIN/D0	IO_L16N_2/DIN/D0	N10	DUAL
2	IO_L16P_2/M0	IO_L16P_2/M0	IO_L16P_2/M0	M10	DUAL
2	IO_L18N_2	IO_L18N_2	IO_L18N_2	N11	I/O
2	IO_L18P_2	IO_L18P_2	IO_L18P_2	P11	I/O
2	IO_L19N_2/VREF_2	IO_L19N_2/VREF_2	IO_L19N_2/VREF_2	V13	VREF
2	IO_L19P_2	IO_L19P_2	IO_L19P_2	V12	I/O
2	IO_L20N_2	IO_L20N_2	IO_L20N_2	R12	I/O

FG320 Footprint



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	GND	TDI	INPUT	I/O L24P_0	INPUT L22P_0	I/O L20N_0	INPUT ←→	I/O	VCCO_0	I/O L12N_0 GCLK7	I/O	I/O ◆	I/O L05P_0	I/O L04N_0	INPUT L02N_0	I/O L01N_0	TCK	GND
B	PROG_B	GND	I/O L25N_0 HSWAP	I/O L24N_0	INPUT L22N_0	I/O L20P_0	VCCAUX	INPUT L13P_0 GCLK8	INPUT L13N_0 GCLK9	I/O L12P_0 GCLK6	I/O VREF_0	VCCAUX	I/O L05N_0 VREF_0	I/O L04P_0	INPUT L02P_0	I/O L01P_0	GND	INPUT
C	I/O L01P_3	I/O L01N_3	I/O L25P_0	I/O	I/O L23P_0	VCCO_0	I/O L18P_0	INPUT L16P_0	I/O L14P_0 GCLK10	GND	I/O L09P_0	INPUT L07P_0	VCCO_0	I/O L03N_0 VREF_0	INPUT	TDO	I/O L24N_1 LDC2	I/O L24P_1 LDC1
D	I/O L02P_3	I/O L02N_3 VREF_3	INPUT	I/O ◆	I/O L23N_0 VREF_0	I/O L21P_0 ◆	I/O L18N_0 VREF_0	INPUT L16N_0	I/O L14N_0 GCLK11	I/O L11P_0 GCLK4	I/O L09N_0	INPUT L07N_0	INPUT ←→	I/O L03P_0	TMS	I/O L23N_1 LDC0	I/O L23P_1 HDC	INPUT VREF_1
E	I/O L03N_3	I/O L03P_3	I/O L04N_3 ◆	I/O L04P_3 ◆	VCCINT	I/O L21N_0 ◆	I/O L19N_0 VREF_0	I/O L17P_0	I/O L15P_0	I/O L11N_0 GCLK5	I/O L08P_0	I/O L06N_0	I/O	VCCINT	I/O L22P_1 ◆	I/O L22N_1 ◆	INPUT ←→	INPUT
F	I/O L05P_3	I/O L05N_3	VCCO_3	INPUT ←→	INPUT	VCCINT	I/O L19P_0	I/O L17N_0	I/O L15N_0	INPUT L10P_0	I/O L08N_0	I/O L06P_0	VCCINT	I/O L21N_1	I/O L21P_1	VCCO_1	I/O L19N_1	I/O L19P_1
G	INPUT	VCCAUX	I/O L06P_3	I/O L06N_3 VREF_3	I/O L07N_3	I/O L07P_3	GND	VCCO_0	I/O	INPUT L10N_0	VCCO_0	GND	I/O L20N_1	I/O L20P_1	I/O L18P_1	I/O L18N_1	VCCAUX	INPUT
H	I/O L10N_3	I/O L10P_3	I/O L09N_3	I/O L09P_3	I/O L08N_3	I/O L08P_3	VCCO_3	GND	GND	GND	GND	VCCO_1	INPUT	I/O L17P_1	I/O L17N_1	I/O L16P_1	I/O L16N_1 A0	INPUT VREF_1
J	I/O L12P_3 LHCLK2	I/O L12N_3 LHCLK3 IRDY2	GND	I/O L11N_3 LHCLK1	I/O L11P_3 LHCLK0	INPUT VREF_3	INPUT	GND			GND	I/O L15P_1 A2	I/O L15N_1 A1	I/O L14N_1 A3 RHCLK7	I/O L14P_1 A4 RHCLK6	I/O L13N_1 A5 RHCLK5	I/O L13P_1 A6 RHCLK4 IRDY1	VCCO_1
K	VCCO_3	INPUT	I/O L13P_3 LHCLK4 TRDY2	I/O L13N_3 LHCLK5	I/O L14N_3 LHCLK7	I/O L14P_3 LHCLK6	INPUT	GND			GND	I/O L11N_1 A9 RHCLK1	I/O L11P_1 A10 RHCLK0	I/O L12N_1 A7 RHCLK3 TRDY1	I/O L12P_1 A8 RHCLK2	GND	INPUT	INPUT
L	I/O L15P_3	I/O L15N_3	I/O L16P_3	I/O L16N_3	I/O L17N_3 VREF_3	I/O L17P_3	VCCO_3	GND	GND	GND	GND	VCCO_1	INPUT	INPUT	I/O L09N_1 A11	I/O L09P_1 A12	I/O L10N_1 VREF_1	I/O L10P_1
M	INPUT	VCCAUX	I/O L18N_3	I/O L18P_3	I/O L19P_3	I/O L19N_3	GND	VCCO_2	I/O L12N_2 D6 GCLK13	I/O L16P_2 M0	VCCO_2	GND	I/O L05N_1 VREF_1	I/O L05P_1	I/O L07P_1	I/O L07N_1	VCCAUX	I/O L08N_1
N	INPUT	INPUT	VCCO_3	I/O L20P_3	I/O L20N_3	VCCINT	I/O L07P_2	I/O L09N_2	I/O L12P_2 D7 GCLK12	I/O L16N_2 DIN D0	I/O L18N_2	I/O L21P_2 ◆	VCCINT	I/O L04N_1 ◆	I/O L04P_1 ◆	VCCO_1	INPUT	I/O L08P_1
P	I/O L21N_3	I/O L21P_3	I/O L22P_3 ◆	I/O L22N_3 ◆	VCCINT	I/O L05N_2	I/O L07N_2	I/O L09P_2	I/O	I/O L15N_2 D1 GCLK3	I/O L18P_2	I/O L21N_2 ◆	I/O L22P_2 A23	VCCINT	INPUT ←→	I/O ◆	I/O L06P_1	I/O L06N_1
R	INPUT	I/O L23N_3	I/O L23P_3	INPUT VREF_3 ←→	I/O L04P_2	I/O L05P_2	INPUT L08N_2	I/O L10P_2	I/O D5	I/O L15P_2 D2 GCLK2	I/O	I/O L20N_2	I/O L22N_2 A22	I/O L24N_2 A20	I/O L03P_1	I/O L03N_1 VREF_1	INPUT	I/O L02P_1 A14
T	I/O L24N_3	I/O L24P_3	I/O L01N_2 INIT_B	I/O L03N_2 MOSI CSI_B	I/O L04N_2	VCCO_2	INPUT L08P_2	I/O L10N_2	GND	INPUT L14N_2 M2 GCLK1	INPUT L17P_2	I/O L20P_2	VCCO_2	I/O L24P_2 A21	I/O VREF_2	I/O L26P_2 VS0 A17	I/O L01N_1 A15	I/O L02N_1 A13
U	INPUT	GND	I/O L01P_2 CSO_B	I/O L03P_2 DOUT BUSY	I/O VREF_2	INPUT ←→	VCCAUX	INPUT L11P_2	I/O L13P_2 D4 GCLK14	INPUT L14P_2 RDWR_B GCLK0	INPUT L17N_2	VCCAUX	INPUT ←→	INPUT L23N_2	I/O L25N_2 VS1 A18	I/O L26N_2 CCLK	GND	I/O L01P_1 A16
V	GND	INPUT	INPUT L02N_2	INPUT L02P_2	I/O L06P_2 ◆	I/O L06N_2 VREF_2 ◆	I/O ◆	INPUT L11N_2 VREF_2	I/O L13N_2 D3 GCLK15	VCCO_2	I/O M1	I/O L19P_2	I/O L19N_2 VREF_2	INPUT L23P_2	I/O L25P_2 VS2 A19	INPUT	DONE	GND

Figure 86: **FG320 Package Footprint (top view)**

102-120	**I/O:** Unrestricted, general-purpose user I/O
47-48	**INPUT:** Unrestricted, general-purpose input pin
2	**CONFIG:** Dedicated configuration pins
18	**N.C.:** Not connected. Only the XC3S500E has these pins (◆).
46	**DUAL:** Configuration pin, then possible user-I/O
16	**CLK:** User I/O, input, or global buffer input
4	**JTAG:** Dedicated JTAG port pins
28	**GND:** Ground
20-21	**VREF:** User I/O or input voltage reference for bank
20	**VCCO:** Output voltage supply for bank
8	**VCCINT:** Internal core supply voltage (+1.2V)
8	**VCCAUX:** Auxiliary supply voltage (+2.5V)

Table 152: **FG400 Package Pinout *(Cont'd)***

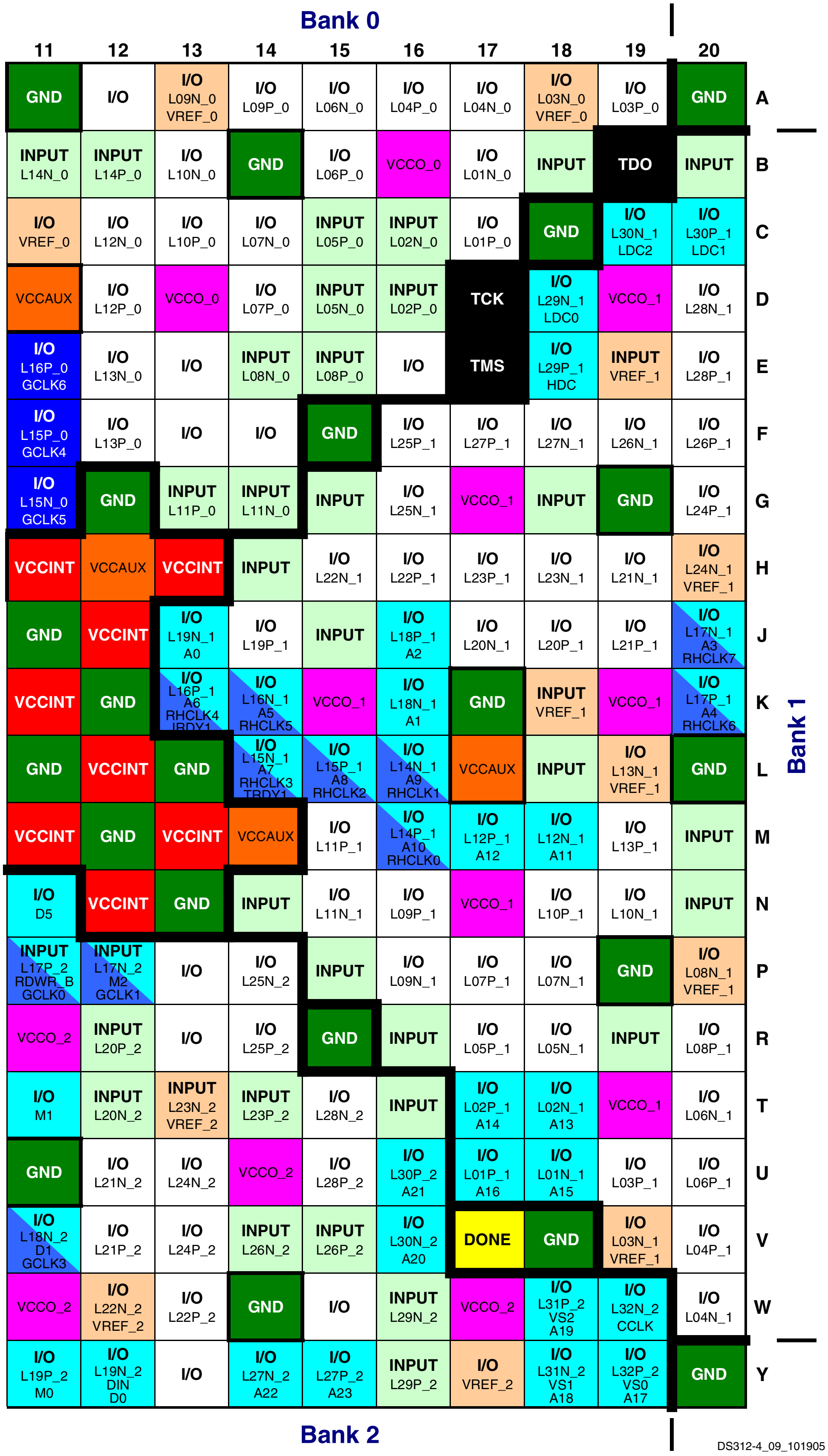
Bank	XC3S1200E XC3S1600E Pin Name	FG400 Ball	Type
0	IP_L17P_0/GCLK8	H10	GCLK
0	IP_L20N_0	G9	INPUT
0	IP_L20P_0	G8	INPUT
0	IP_L23N_0	C8	INPUT
0	IP_L23P_0	D8	INPUT
0	IP_L26N_0	E6	INPUT
0	IP_L26P_0	E7	INPUT
0	IP_L29N_0	A4	INPUT
0	IP_L29P_0	A5	INPUT
0	VCCO_0	B4	VCCO
0	VCCO_0	B10	VCCO
0	VCCO_0	B16	VCCO
0	VCCO_0	D7	VCCO
0	VCCO_0	D13	VCCO
0	VCCO_0	F10	VCCO
1	IO_L01N_1/A15	U18	DUAL
1	IO_L01P_1/A16	U17	DUAL
1	IO_L02N_1/A13	T18	DUAL
1	IO_L02P_1/A14	T17	DUAL
1	IO_L03N_1/VREF_1	V19	VREF
1	IO_L03P_1	U19	I/O
1	IO_L04N_1	W20	I/O
1	IO_L04P_1	V20	I/O
1	IO_L05N_1	R18	I/O
1	IO_L05P_1	R17	I/O
1	IO_L06N_1	T20	I/O
1	IO_L06P_1	U20	I/O
1	IO_L07N_1	P18	I/O
1	IO_L07P_1	P17	I/O
1	IO_L08N_1/VREF_1	P20	VREF
1	IO_L08P_1	R20	I/O
1	IO_L09N_1	P16	I/O
1	IO_L09P_1	N16	I/O
1	IO_L10N_1	N19	I/O
1	IO_L10P_1	N18	I/O
1	IO_L11N_1	N15	I/O
1	IO_L11P_1	M15	I/O
1	IO_L12N_1/A11	M18	DUAL
1	IO_L12P_1/A12	M17	DUAL
1	IO_L13N_1/VREF_1	L19	VREF
1	IO_L13P_1	M19	I/O
1	IO_L14N_1/A9/RHCLK1	L16	RHCLK/ DUAL

Table 152: **FG400 Package Pinout *(Cont'd)***

Bank	XC3S1200E XC3S1600E Pin Name	FG400 Ball	Type
1	IO_L14P_1/A10/RHCLK0	M16	RHCLK/ DUAL
1	IO_L15N_1/A7/RHCLK3/ TRDY1	L14	RHCLK/ DUAL
1	IO_L15P_1/A8/RHCLK2	L15	RHCLK/ DUAL
1	IO_L16N_1/A5/RHCLK5	K14	RHCLK/ DUAL
1	IO_L16P_1/A6/RHCLK4/ IRDY1	K13	RHCLK/ DUAL
1	IO_L17N_1/A3/RHCLK7	J20	RHCLK/ DUAL
1	IO_L17P_1/A4/RHCLK6	K20	RHCLK/ DUAL
1	IO_L18N_1/A1	K16	DUAL
1	IO_L18P_1/A2	J16	DUAL
1	IO_L19N_1/A0	J13	DUAL
1	IO_L19P_1	J14	I/O
1	IO_L20N_1	J17	I/O
1	IO_L20P_1	J18	I/O
1	IO_L21N_1	H19	I/O
1	IO_L21P_1	J19	I/O
1	IO_L22N_1	H15	I/O
1	IO_L22P_1	H16	I/O
1	IO_L23N_1	H18	I/O
1	IO_L23P_1	H17	I/O
1	IO_L24N_1/VREF_1	H20	VREF
1	IO_L24P_1	G20	I/O
1	IO_L25N_1	G16	I/O
1	IO_L25P_1	F16	I/O
1	IO_L26N_1	F19	I/O
1	IO_L26P_1	F20	I/O
1	IO_L27N_1	F18	I/O
1	IO_L27P_1	F17	I/O
1	IO_L28N_1	D20	I/O
1	IO_L28P_1	E20	I/O
1	IO_L29N_1/LDC0	D18	DUAL
1	IO_L29P_1/HDC	E18	DUAL
1	IO_L30N_1/LDC2	C19	DUAL
1	IO_L30P_1/LDC1	C20	DUAL
1	IP	B20	INPUT
1	IP	G15	INPUT
1	IP	G18	INPUT
1	IP	H14	INPUT
1	IP	J15	INPUT

FG400 Footprint

Right Half of Package (top view)

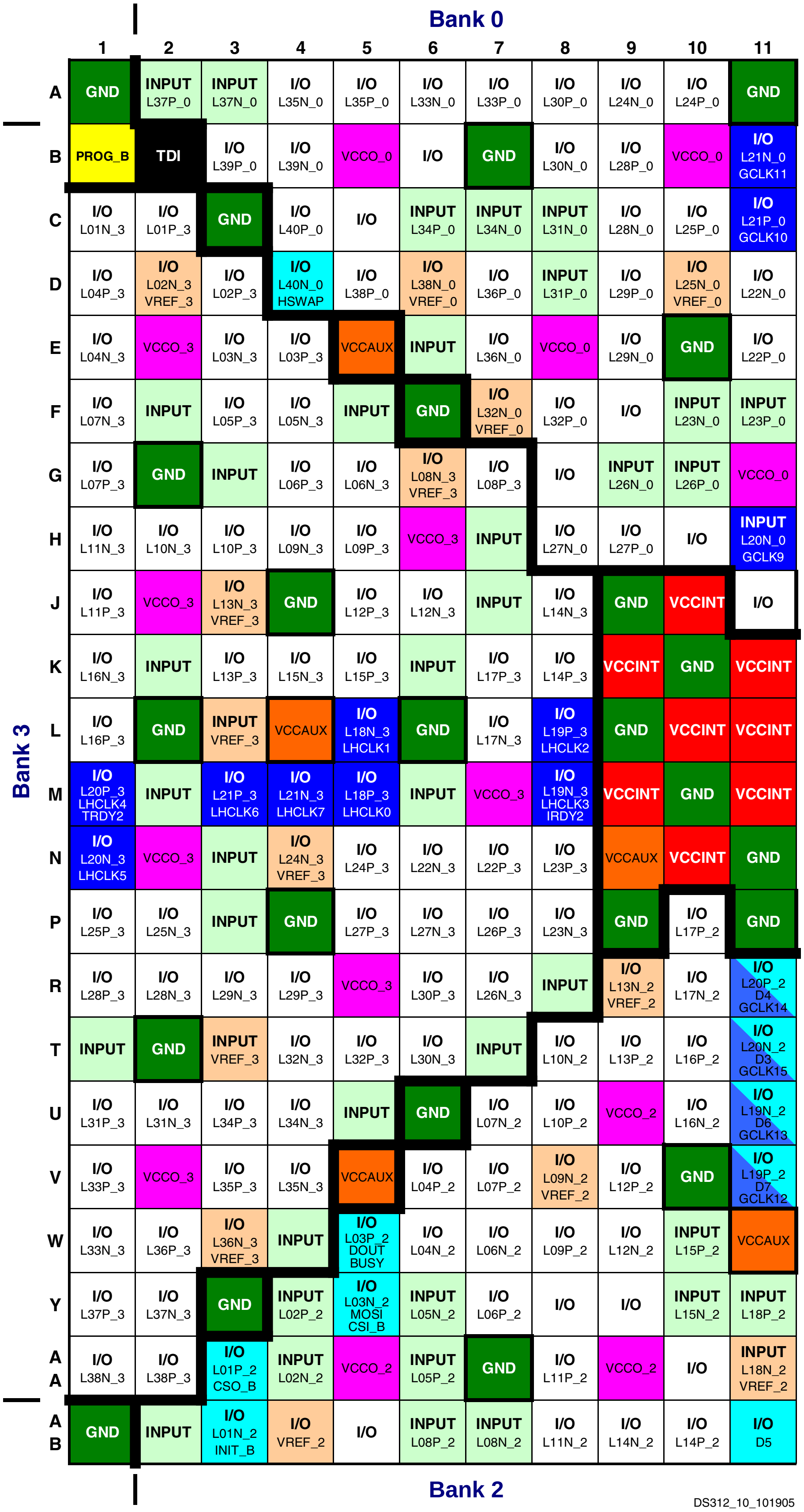


	11	12	13	14	15	16	17	18	19	20
A	GND	I/O	I/O L09N_0 VREF_0	I/O L09P_0	I/O L06N_0	I/O L04P_0	I/O L04N_0	I/O L03N_0 VREF_0	I/O L03P_0	GND
B	INPUT L14N_0	INPUT L14P_0	I/O L10N_0	GND	I/O L06P_0	VCCO_0	I/O L01N_0	INPUT	TDO	INPUT
C	I/O VREF_0	I/O L12N_0	I/O L10P_0	I/O L07N_0	INPUT L05P_0	INPUT L02N_0	I/O L01P_0	GND	I/O L30N_1 LDC2	I/O L30P_1 LDC1
D	VCCAUX	I/O L12P_0	VCCO_0	I/O L07P_0	INPUT L05N_0	INPUT L02P_0	TCK	I/O L29N_1 LDC0	VCCO_1	I/O L28N_1
E	I/O L16P_0 GCLK6	I/O L13N_0	I/O	INPUT L08N_0	INPUT L08P_0	I/O	TMS	I/O L29P_1 HDC	INPUT VREF_1	I/O L28P_1
F	I/O L15P_0 GCLK4	I/O L13P_0	I/O	I/O	GND	I/O L25P_1	I/O L27P_1	I/O L27N_1	I/O L26N_1	I/O L26P_1
G	I/O L15N_0 GCLK5	GND	INPUT L11P_0	INPUT L11N_0	INPUT	I/O L25N_1	VCCO_1	INPUT	GND	I/O L24P_1
H	VCCINT	VCCAUX	VCCINT	INPUT	I/O L22N_1	I/O L22P_1	I/O L23P_1	I/O L23N_1	I/O L21N_1	I/O L24N_1 VREF_1
J	GND	VCCINT	I/O L19N_1 A0	I/O L19P_1	INPUT	I/O L18P_1 A2	I/O L20N_1	I/O L20P_1	I/O L21P_1	I/O L17N_1 A3 RHCLK7
K	VCCINT	GND	I/O L16P_1 A6 RHCLK4 IRDY1	I/O L16N_1 A5 RHCLK5	VCCO_1	I/O L18N_1 A1	GND	INPUT VREF_1	VCCO_1	I/O L17P_1 A4 RHCLK6
L	GND	VCCINT	GND	I/O L15N_1 A7 RHCLK3 TRDY1	I/O L15P_1 A8 RHCLK2	I/O L14N_1 A9 RHCLK1	VCCAUX	INPUT	I/O L13N_1 VREF_1	GND
M	VCCINT	GND	VCCINT	VCCAUX	I/O L11P_1	I/O L14P_1 A10 RHCLK0	I/O L12P_1 A12	I/O L12N_1 A11	I/O L13P_1	INPUT
N	I/O D5	VCCINT	GND	INPUT	I/O L11N_1	I/O L09P_1	VCCO_1	I/O L10P_1	I/O L10N_1	INPUT
P	INPUT L17P_2 RDWR_B GCLK0	INPUT L17N_2 M2 GCLK1	I/O	I/O L25N_2	INPUT	I/O L09N_1	I/O L07P_1	I/O L07N_1	GND	I/O L08N_1 VREF_1
R	VCCO_2	INPUT L20P_2	I/O	I/O L25P_2	GND	INPUT	I/O L05P_1	I/O L05N_1	INPUT	I/O L08P_1
T	I/O M1	INPUT L20N_2	INPUT L23N_2 VREF_2	INPUT L23P_2	I/O L28N_2	INPUT	I/O L02P_1 A14	I/O L02N_1 A13	VCCO_1	I/O L06N_1
U	GND	I/O L21N_2	I/O L24N_2	VCCO_2	I/O L28P_2	I/O L30P_2 A21	I/O L01P_1 A16	I/O L01N_1 A15	I/O L03P_1	I/O L06P_1
V	I/O L18N_2 D1 GCLK3	I/O L21P_2	I/O L24P_2	INPUT L26N_2	INPUT L26P_2	I/O L30N_2 A20	DONE	GND	I/O L03N_1 VREF_1	I/O L04P_1
W	VCCO_2	I/O L22N_2 VREF_2	I/O L22P_2	GND	I/O	INPUT L29N_2	VCCO_2	I/O L31P_2 VS2 A19	I/O L32N_2 CCLK	I/O L04N_1
Y	I/O L19P_2 M0	I/O L19N_2 DIN D0	I/O	I/O L27N_2 A22	I/O L27P_2 A23	INPUT L29P_2	I/O VREF_2	I/O L31N_2 VS1 A18	I/O L32P_2 VS0 A17	GND

FG484 Footprint

Left Half of Package (top view)

214	**I/O:** Unrestricted, general-purpose user I/O
72	**INPUT:** User I/O or reference resistor input for bank
46	**DUAL:** Configuration pin, then possible user I/O
28	**VREF:** User I/O or input voltage reference for bank
16	**CLK:** User I/O, input, or clock buffer input
2	**CONFIG:** Dedicated configuration pins
4	**JTAG:** Dedicated JTAG port pins
48	**GND:** Ground
28	**VCCO:** Output voltage supply for bank
16	**VCCINT:** Internal core supply voltage (+1.2V)
10	**VCCAUX:** Auxiliary supply voltage (+2.5V)
0	**N.C.:** Not connected

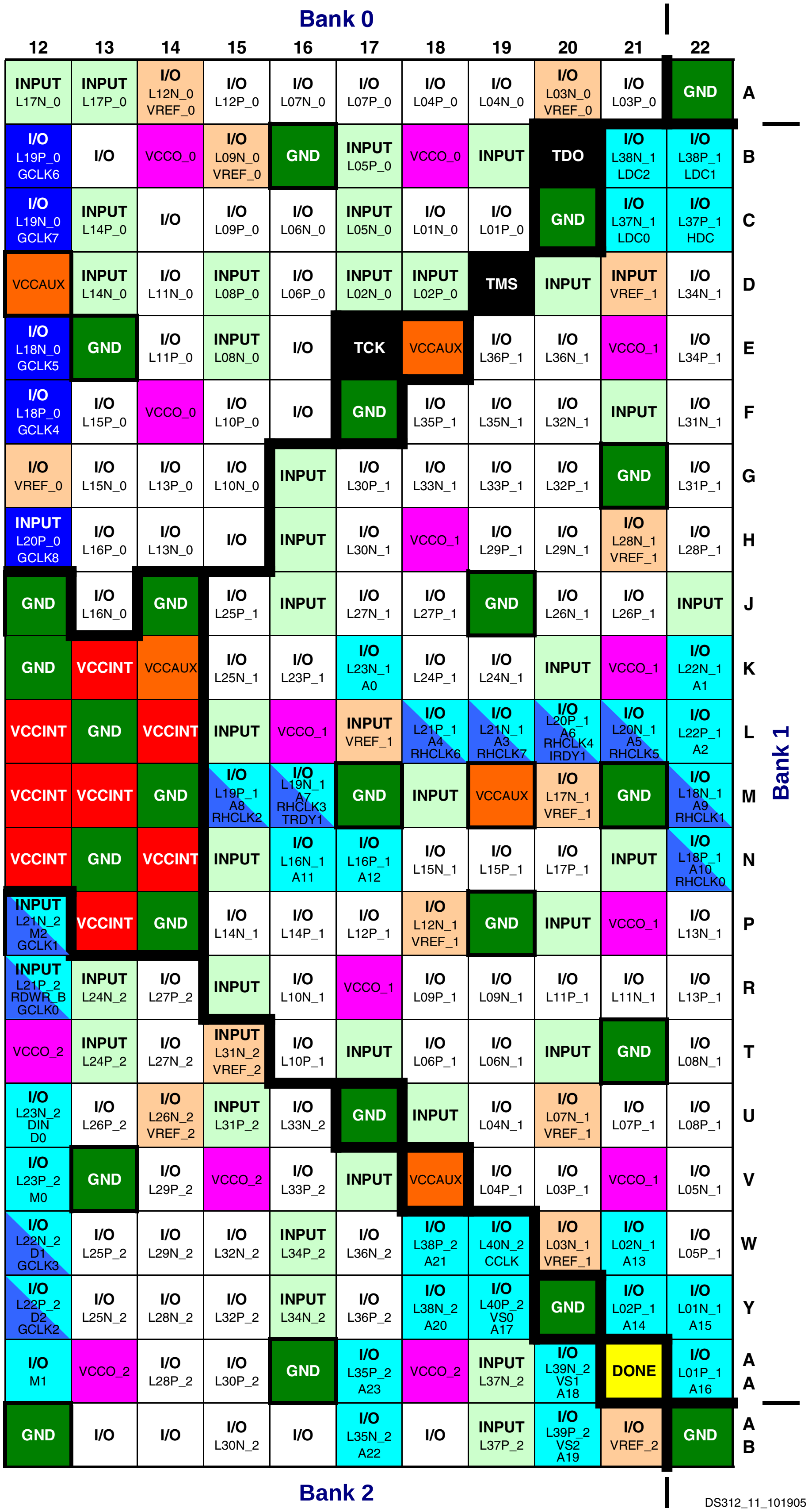


	1	2	3	4	5	6	7	8	9	10	11
A	GND	INPUT L37P_0	INPUT L37N_0	I/O L35N_0	I/O L35P_0	I/O L33N_0	I/O L33P_0	I/O L30P_0	I/O L24N_0	I/O L24P_0	GND
B	PROG_B	TDI	I/O L39P_0	I/O L39N_0	VCCO_0	I/O	GND	I/O L30N_0	I/O L28P_0	VCCO_0	I/O L21N_0 GCLK11
C	I/O L01N_3	I/O L01P_3	GND	I/O L40P_0	I/O	INPUT L34P_0	INPUT L34N_0	INPUT L31N_0	I/O L28N_0	I/O L25P_0	I/O L21P_0 GCLK10
D	I/O L04P_3	I/O L02N_3 VREF_3	I/O L02P_3	I/O L40N_0 HSWAP	I/O L38P_0	I/O L38N_0 VREF_0	I/O L36P_0	INPUT L31P_0	I/O L29P_0	I/O L25N_0 VREF_0	I/O L22N_0
E	I/O L04N_3	VCCO_3	I/O L03N_3	I/O L03P_3	VCCAUX	INPUT	I/O L36N_0	VCCO_0	I/O L29N_0	GND	I/O L22P_0
F	I/O L07N_3	INPUT	I/O L05P_3	I/O L05N_3	INPUT	GND	I/O L32N_0 VREF_0	I/O L32P_0	I/O	INPUT L23N_0	INPUT L23P_0
G	I/O L07P_3	GND	INPUT	I/O L06P_3	I/O L06N_3	I/O L08N_3 VREF_3	I/O L08P_3	I/O	INPUT L26N_0	INPUT L26P_0	VCCO_0
H	I/O L11N_3	I/O L10N_3	I/O L10P_3	I/O L09N_3	I/O L09P_3	VCCO_3	INPUT	I/O L27N_0	I/O L27P_0	I/O	INPUT L20N_0 GCLK9
J	I/O L11P_3	VCCO_3	I/O L13N_3 VREF_3	GND	I/O L12P_3	I/O L12N_3	INPUT	I/O L14N_3	GND	VCCINT	I/O
K	I/O L16N_3	INPUT	I/O L13P_3	I/O L15N_3	I/O L15P_3	INPUT	I/O L17P_3	I/O L14P_3	VCCINT	GND	VCCINT
L	I/O L16P_3	GND	INPUT VREF_3	VCCAUX	I/O L18N_3 LHCLK1	GND	I/O L17N_3	I/O L19P_3 LHCLK2	GND	VCCINT	VCCINT
M	I/O L20P_3 LHCLK4 TRDY2	INPUT	I/O L21P_3 LHCLK6	I/O L21N_3 LHCLK7	I/O L18P_3 LHCLK0	INPUT	VCCO_3	I/O L19N_3 LHCLK3 IRDY2	VCCINT	GND	VCCINT
N	I/O L20N_3 LHCLK5	VCCO_3	INPUT	I/O L24N_3 VREF_3	I/O L24P_3	I/O L22N_3	I/O L22P_3	I/O L23P_3	VCCAUX	VCCINT	GND
P	I/O L25P_3	I/O L25N_3	INPUT	GND	I/O L27P_3	I/O L27N_3	I/O L26P_3	I/O L23N_3	GND	I/O L17P_2	GND
R	I/O L28P_3	I/O L28N_3	I/O L29N_3	I/O L29P_3	VCCO_3	I/O L30P_3	I/O L26N_3	INPUT	I/O L13N_2 VREF_2	I/O L17N_2	I/O L20P_2 D4 GCLK14
T	INPUT	GND	INPUT VREF_3	I/O L32N_3	I/O L32P_3	I/O L30N_3	INPUT	I/O L10N_2	I/O L13P_2	I/O L16P_2	I/O L20N_2 D3 GCLK15
U	I/O L31P_3	I/O L31N_3	I/O L34P_3	I/O L34N_3	INPUT	GND	I/O L07N_2	I/O L10P_2	VCCO_2	I/O L16N_2	I/O L19N_2 D6 GCLK13
V	I/O L33P_3	VCCO_3	I/O L35P_3	I/O L35N_3	VCCAUX	I/O L04P_2	I/O L07P_2	I/O L09N_2 VREF_2	I/O L12P_2	GND	I/O L19P_2 D7 GCLK12
W	I/O L33N_3	I/O L36P_3	I/O L36N_3 VREF_3	INPUT	I/O L03P_2 DOUT BUSY	I/O L04N_2	I/O L06N_2	I/O L09P_2	I/O L12N_2	INPUT L15P_2	VCCAUX
Y	I/O L37P_3	I/O L37N_3	GND	INPUT L02P_2	I/O L03N_2 MOSI CSI_B	INPUT L05N_2	I/O L06P_2	I/O	I/O	INPUT L15N_2	INPUT L18P_2
AA	I/O L38N_3	I/O L38P_3	I/O L01P_2 CSO_B	INPUT L02N_2	VCCO_2	INPUT L05P_2	GND	I/O L11P_2	VCCO_2	I/O	INPUT L18N_2 VREF_2
AB	GND	INPUT	I/O L01N_2 INIT_B	I/O VREF_2	I/O	INPUT L08P_2	INPUT L08N_2	I/O L11N_2	I/O L14N_2	I/O L14P_2	I/O D5

Figure 88: **FG484 Package Footprint (top view)**

FG484 Footprint

Right Half of Package (top view)



12	13	14	15	16	17	18	19	20	21	22	
INPUT L17N_0	INPUT L17P_0	I/O L12N_0 VREF_0	I/O L12P_0	I/O L07N_0	I/O L07P_0	I/O L04P_0	I/O L04N_0	I/O L03N_0 VREF_0	I/O L03P_0	GND	A
I/O L19P_0 GCLK6	I/O	VCCO_0	I/O L09N_0 VREF_0	GND	INPUT L05P_0	VCCO_0	INPUT	TDO	I/O L38N_1 LDC2	I/O L38P_1 LDC1	B
I/O L19N_0 GCLK7	INPUT L14P_0	I/O	I/O L09P_0	I/O L06N_0	INPUT L05N_0	I/O L01N_0	I/O L01P_0	GND	I/O L37N_1 LDC0	I/O L37P_1 HDC	C
VCCAUX	INPUT L14N_0	I/O L11N_0	INPUT L08P_0	I/O L06P_0	INPUT L02N_0	INPUT L02P_0	TMS	INPUT	INPUT VREF_1	I/O L34N_1	D
I/O L18N_0 GCLK5	GND	I/O L11P_0	INPUT L08N_0	I/O	TCK	VCCAUX	I/O L36P_1	I/O L36N_1	VCCO_1	I/O L34P_1	E
I/O L18P_0 GCLK4	I/O L15P_0	VCCO_0	I/O L10P_0	I/O	GND	I/O L35P_1	I/O L35N_1	I/O L32N_1	INPUT	I/O L31N_1	F
I/O VREF_0	I/O L15N_0	I/O L13P_0	I/O L10N_0	INPUT	I/O L30P_1	I/O L33N_1	I/O L33P_1	I/O L32P_1	GND	I/O L31P_1	G
INPUT L20P_0 GCLK8	I/O L16P_0	I/O L13N_0	I/O	INPUT	I/O L30N_1	VCCO_1	I/O L29P_1	I/O L29N_1	I/O L28N_1 VREF_1	I/O L28P_1	H
GND	I/O L16N_0	GND	I/O L25P_1	INPUT	I/O L27N_1	I/O L27P_1	GND	I/O L26N_1	I/O L26P_1	INPUT	J
GND	VCCINT	VCCAUX	I/O L25N_1	I/O L23P_1	I/O L23N_1 A0	I/O L24P_1	I/O L24N_1	INPUT	VCCO_1	I/O L22N_1 A1	K
VCCINT	GND	VCCINT	INPUT	VCCO_1	INPUT VREF_1	I/O L21P_1 A4 RHCLK6	I/O L21N_1 A3 RHCLK7	I/O L20P_1 A6 RHCLK4 IRDY1	I/O L20N_1 A5 RHCLK5	I/O L22P_1 A2	L
VCCINT	VCCINT	GND	I/O L19P_1 A8 RHCLK2	I/O L19N_1 A7 RHCLK3 TRDY1	GND	INPUT	VCCAUX	I/O L17N_1 VREF_1	GND	I/O L18N_1 A9 RHCLK1	M
VCCINT	GND	VCCINT	INPUT	I/O L16N_1 A11	I/O L16P_1 A12	I/O L15N_1	I/O L15P_1	I/O L17P_1	INPUT	I/O L18P_1 A10 RHCLK0	N
INPUT L21N_2 M2 GCLK1	VCCINT	GND	I/O L14N_1	I/O L14P_1	I/O L12P_1	I/O L12N_1 VREF_1	GND	INPUT	VCCO_1	I/O L13N_1	P
INPUT L21P_2 RDWR_B GCLK0	INPUT L24N_2	I/O L27P_2	INPUT	I/O L10N_1	VCCO_1	I/O L09P_1	I/O L09N_1	I/O L11P_1	I/O L11N_1	I/O L13P_1	R
VCCO_2	INPUT L24P_2	I/O L27N_2	INPUT L31N_2 VREF_2	I/O L10P_1	INPUT	I/O L06P_1	I/O L06N_1	INPUT	GND	I/O L08N_1	T
I/O L23N_2 DIN D0	I/O L26P_2	I/O L26N_2 VREF_2	INPUT L31P_2	I/O L33N_2	GND	INPUT	I/O L04N_1	I/O L07N_1 VREF_1	I/O L07P_1	I/O L08P_1	U
I/O L23P_2 M0	GND	I/O L29P_2	VCCO_2	I/O L33P_2	INPUT	VCCAUX	I/O L04P_1	I/O L03P_1	VCCO_1	I/O L05N_1	V
I/O L22N_2 D1 GCLK3	I/O L25P_2	I/O L29N_2	I/O L32N_2	INPUT L34P_2	I/O L36N_2	I/O L38P_2 A21	I/O L40N_2 CCLK	I/O L03N_1 VREF_1	I/O L02N_1 A13	I/O L05P_1	W
I/O L22P_2 D2 GCLK2	I/O L25N_2	I/O L28N_2	I/O L32P_2	INPUT L34N_2	I/O L36P_2	I/O L38N_2 A20	I/O L40P_2 VS0 A17	GND	I/O L02P_1 A14	I/O L01N_1 A15	Y
I/O M1	VCCO_2	I/O L28P_2	I/O L30P_2	GND	I/O L35P_2 A23	VCCO_2	INPUT L37N_2	I/O L39N_2 VS1 A18	DONE	I/O L01P_1 A16	AA
GND	I/O	I/O	I/O L30N_2	I/O	I/O L35N_2 A22	I/O	INPUT L37P_2	I/O L39P_2 VS2 A19	I/O VREF_2	GND	AB

DS312_11_101905