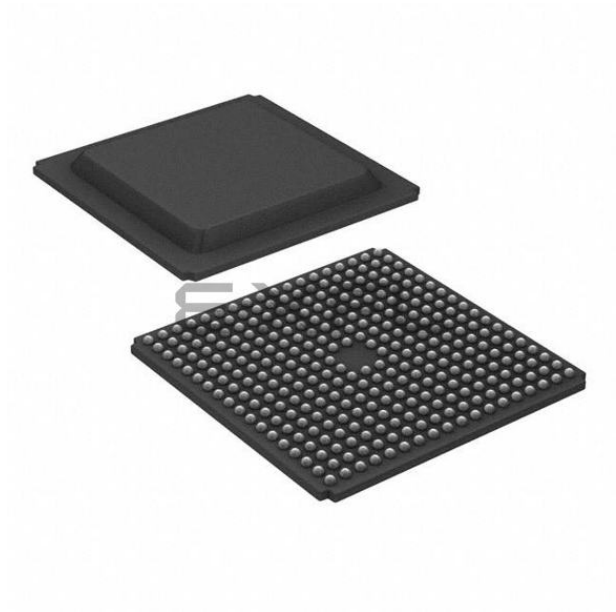

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 3688 |
| Number of Logic Elements/Cells | 33192 |
| Total RAM Bits | 663552 |
| Number of I/O | 250 |
| Number of Gates | 1600000 |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 320-BGA |
| Supplier Device Package | 320-FBGA (19x19) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc3s1600e-5fg320c |

*Table 14:* **Carry Logic Functions *(Cont'd)***

| Function | Description |
|---|---|
| CY0G | Carry generation for top half of slice. Fixed selection of:<br>· G1 or G2 inputs to the LUT (both equal 1 when a carry is to be generated)<br>· GAND gate for multiplication<br>· BY input for carry initialization<br>· Fixed 1 or 0 input for use as a simple Boolean function |
| CYMUXF | Carry generation or propagation mux for bottom half of slice. Dynamic selection via CYSELF of:<br>· CYINIT carry propagation (CYSELF = 1)<br>· CY0F carry generation (CYSELF = 0) |
| CYMUXG | Carry generation or propagation mux for top half of slice. Dynamic selection via CYSELF of:<br>· CYMUXF carry propagation (CYSELG = 1)<br>· CY0G carry generation (CYSELG = 0) |
| CYSELF | Carry generation or propagation select for bottom half of slice. Fixed selection of:<br>· F-LUT output (typically XOR result)<br>· Fixed 1 to always propagate |
| CYSELG | Carry generation or propagation select for top half of slice. Fixed selection of:<br>· G-LUT output (typically XOR result)<br>· Fixed 1 to always propagate |
| XORF | Sum generation for bottom half of slice. Inputs from:<br>· F-LUT<br>· CYINIT carry signal from previous stage<br>Result is sent to either the combinatorial or registered output for the top of the slice. |
| XORG | Sum generation for top half of slice. Inputs from:<br>· G-LUT<br>· CYMUXF carry signal from previous stage<br>Result is sent to either the combinatorial or registered output for the top of the slice. |
| FAND | Multiplier partial product for bottom half of slice. Inputs:<br>· F-LUT F1 input<br>· F-LUT F2 input<br>Result is sent through CY0F to become the carry generate signal into CYMUXF |
| GAND | Multiplier partial product for top half of slice. Inputs:<br>· G-LUT G1 input<br>· G-LUT G2 input<br>Result is sent through CY0G to become the carry generate signal into CYMUXG |

The basic usage of the carry logic is to generate a half-sum in the LUT via an XOR function, which generates or propagates a carry out COUT via the carry mux CYMUXF (or CYMUXG), and then complete the sum with the dedicated XORF (or XORG) gate and the carry input CIN. This structure allows two bits of an arithmetic function in each slice. The CYMUXF (or CYMUXG) can be instantiated using the MUXCY element, and the XORF (or XORG) can be instantiated using the XORCY element.

The FAND (or GAND) gate is used for partial product multiplication and can be instantiated using the MULT_AND component. Partial products are generated by two-input AND gates and then added. The carry logic is efficient for the adder, but one of the inputs must be outside the LUT as shown in Figure 23.

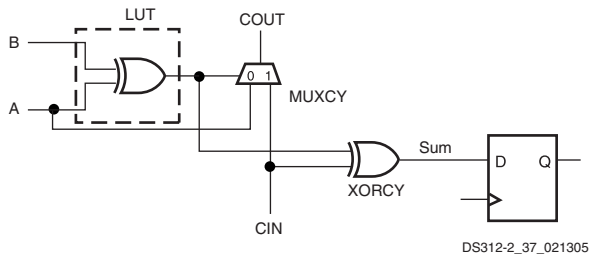



*Figure 23:* **Using the MUXCY and XORCY in the Carry Logic**

The FAND (or GAND) gate is used to duplicate one of the partial products, while the LUT generates both partial products and the XOR function, as shown in Figure 24.

*Table 46:* **Pin Behavior during Configuration *(Cont'd)***

| Pin Name | Master Serial | SPI (Serial Flash) | BPI (Parallel NOR Flash) | JTAG | Slave Parallel | Slave Serial | I/O Bank[3] |
|---|---|---|---|---|---|---|---|
| **D0/DIN** | DIN | DIN | D0 | | D0 | DIN | 2 |
| **RDWR_B** | | | RDWR_B | | RDWR_B | | 2 |
| **A23** | | | A23 | | | | 2 |
| **A22** | | | A22 | | | | 2 |
| **A21** | | | A21 | | | | 2 |
| **A20** | | | A20 | | | | 2 |
| **A19/VS2** | | VS2 | A19 | | | | 2 |
| **A18/VS1** | | VS1 | A18 | | | | 2 |
| **A17/VS0** | | VS0 | A17 | | | | 2 |
| **A16** | | | A16 | | | | 1 |
| **A15** | | | A15 | | | | 1 |
| **A14** | | | A14 | | | | 1 |
| **A13** | | | A13 | | | | 1 |
| **A12** | | | A12 | | | | 1 |
| **A11** | | | A11 | | | | 1 |
| **A10** | | | A10 | | | | 1 |
| **A9** | | | A9 | | | | 1 |
| **A8** | | | A8 | | | | 1 |
| **A7** | | | A7 | | | | 1 |
| **A6** | | | A6 | | | | 1 |
| **A5** | | | A5 | | | | 1 |
| **A4** | | | A4 | | | | 1 |
| **A3** | | | A3 | | | | 1 |
| **A2** | | | A2 | | | | 1 |
| **A1** | | | A1 | | | | 1 |
| **A0** | | | A0 | | | | 1 |
| **LDC0** | | | LDC0 | | | | 1 |
| **LDC1** | | | LDC1 | | | | 1 |
| **LDC2** | | | LDC2 | | | | 1 |
| **HDC** | | | HDC | | | | 1 |

**Notes:**
1. Gray shaded cells represent pins that are in a high-impedance state (Hi-Z, floating) during configuration. These pins have an optional internal pull-up resistor to their respective $V_{CCO}$ supply pin that is active throughout configuration if the HSWAP input is Low.
2. Yellow shaded cells represent pins with an internal pull-up resistor to its respective voltage supply rail that is active during configuration, regardless of the HSWAP pin.
3. Note that dual-purpose outputs are supplied by $V_{CCO}$, and configuration inputs are supplied by $V_{CCAUX}$.

The HSWAP pin itself has a pull-up resistor enabled during configuration. However, the VCCO_0 supply voltage must be applied before the pull-up resistor becomes active. If the VCCO_0 supply ramps after the VCCO_2 power supply, do not let HSWAP float; tie HSWAP to the desired logic level externally.

Spartan-3E FPGAs have only six dedicated configuration pins, including the DONE and PROG_B pins, and the four JTAG boundary-scan pins: TDI, TDO, TMS, and TCK. All other configuration pins are dual-purpose I/O pins and are available to the FPGA application after the DONE pin goes High. See Start-Up for additional information.

Table 47 shows the default I/O standard setting for the various configuration pins during the configuration process. The configuration interface is designed primarily for 2.5V operation when the VCCO_2 (and VCCO_1 in BPI mode) connects to 2.5V.

*Table 47:* **Default I/O Standard Setting During Configuration (VCCO_2 = 2.5V)**

| Pin(s) | I/O Standard | Output Drive | Slew Rate |
|---|---|---|---|
| All, including CCLK | LVCMOS25 | 8 mA | Slow |

*Table 49:* **Pull-up or Pull-down Values for HSWAP, M[2:0], and VS[2:0]**

| HSWAP Value | I/O Pull-up Resistors during Configuration | Required Resistor Value to Define Logic Level on HSWAP, M[2:0], or VS[2:0] | |
|---|---|---|---|
| | | High | Low |
| 0 | Enabled | Pulled High via an internal pull-up resistor to the associated $V_{CCO}$ supply. No external pull-up resistor is necessary. | Pulled Low using an appropriately sized pull-down resistor to GND.<br>For a 2.5V or 3.3V interface: R ≤ 560Ω. For a 1.8V interface: R ≤ 1.1kΩ. |
| 1 | Disabled | Pulled High using a 3.3 to 4.7kΩ resistor to the associated $V_{CCO}$ supply. | Pulled Low using a 3.3 to 4.7kΩ resistor to GND. |

The logic level on HSWAP dictates how to define the logic levels on M[2:0] and VS[2:0], as shown in Table 49. If the application requires HSWAP to be High, the HSWAP pin is pulled High using an external 3.3kΩ to 4.7kΩ resistor to VCCO_0. If the application requires HSWAP to be Low during configuration, then HSWAP is either connected to GND or pulled Low using an appropriately sized external pull-down resistor to GND. When HSWAP is Low, its pin has an internal pull-up resistor to VCCO_0. The external pull-down resistor must be strong enough to define a logic Low on HSWAP for the I/O standard used during configuration. For 2.5V or 3.3V I/O, the pull-down resistor is 560Ω or lower. For 1.8V I/O, the pull-down resistor is 1.1kΩ or lower.

Once HSWAP is defined, use Table 49 to define the logic values for M[2:0] and VS[2:0].

Use the weakest external pull-up or pull-down resistor value allowed by the application. The resistor must be strong enough to define a logic Low or High during configuration. However, when driving the HSWAP, M[2:0], or VS[2:0] pins after configuration, the output driver must be strong enough to overcome the pull-up or pull-down resistor value and generate the appropriate logic levels. For example, to overcome a 560Ω pull-down resistor, a 3.3V FPGA I/O pin must use a 6 mA or stronger driver.

## Master Serial Mode

For additional information, refer to the “Master Serial Mode” chapter in UG332.

In Master Serial mode (M[2:0] = <0:0:0>), the Spartan-3E FPGA configures itself from an attached Xilinx Platform Flash PROM, as illustrated in Figure 51. The FPGA supplies the CCLK output clock from its internal oscillator to the attached Platform Flash PROM. In response, the Platform Flash PROM supplies bit-serial data to the FPGA’s DIN input, and the FPGA accepts this data on each rising CCLK edge.

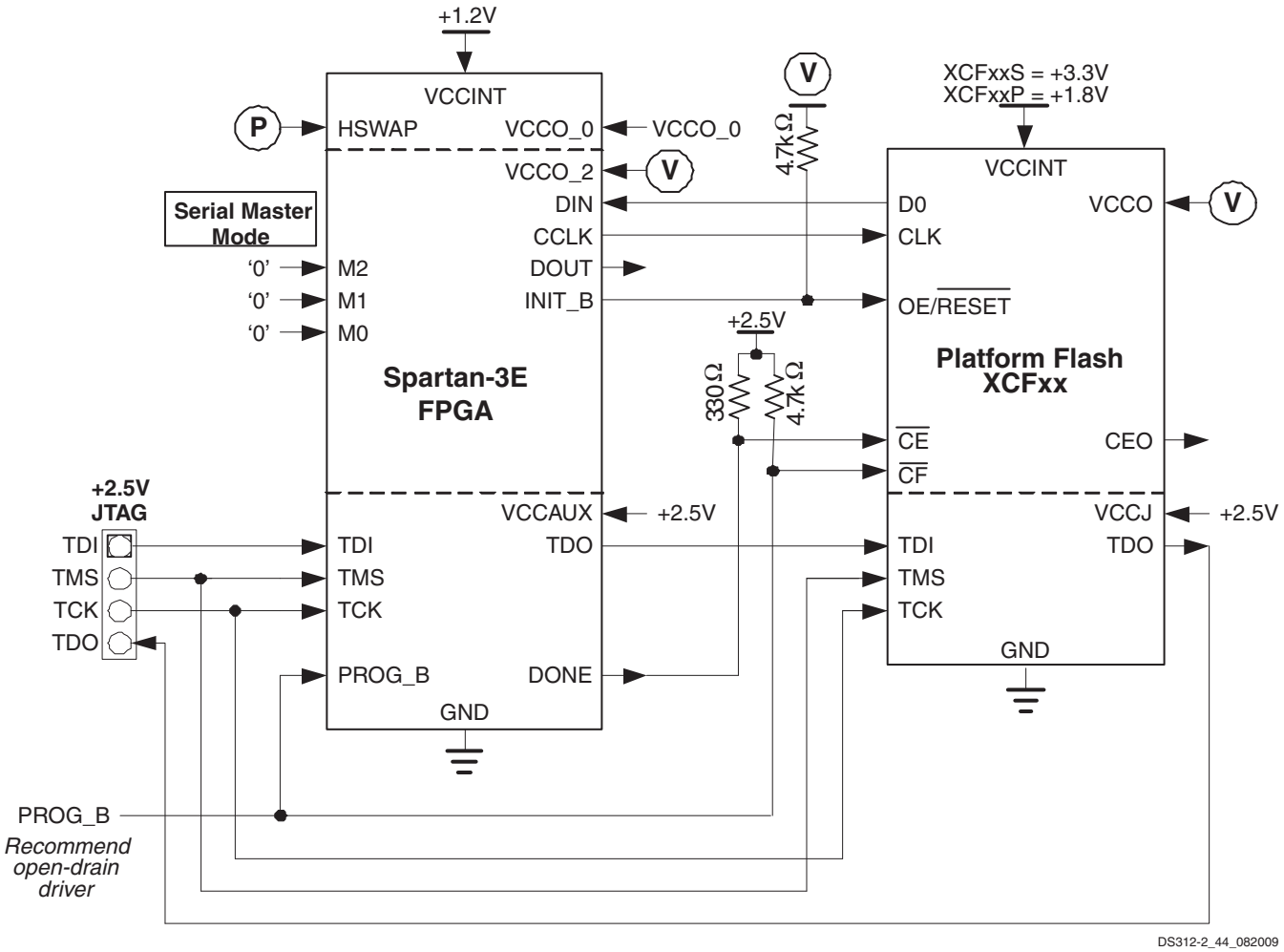



*Figure 51:* **Master Serial Mode using Platform Flash PROM**

All mode select pins, M[2:0], must be Low when sampled, when the FPGA’s INIT_B output goes High. After configuration, when the FPGA’s DONE output goes High, the mode select pins are available as full-featured user-I/O pins.

## SPI Serial Flash Mode

For additional information, refer to the “Master SPI Mode” chapter in UG332.

In SPI Serial Flash mode (M[2:0] = <0:0:1>), the Spartan-3E FPGA configures itself from an attached industry-standard SPI serial Flash PROM, as illustrated in Figure 53 and Figure 54. The FPGA supplies the CCLK output clock from its internal oscillator to the clock input of the attached SPI Flash PROM.

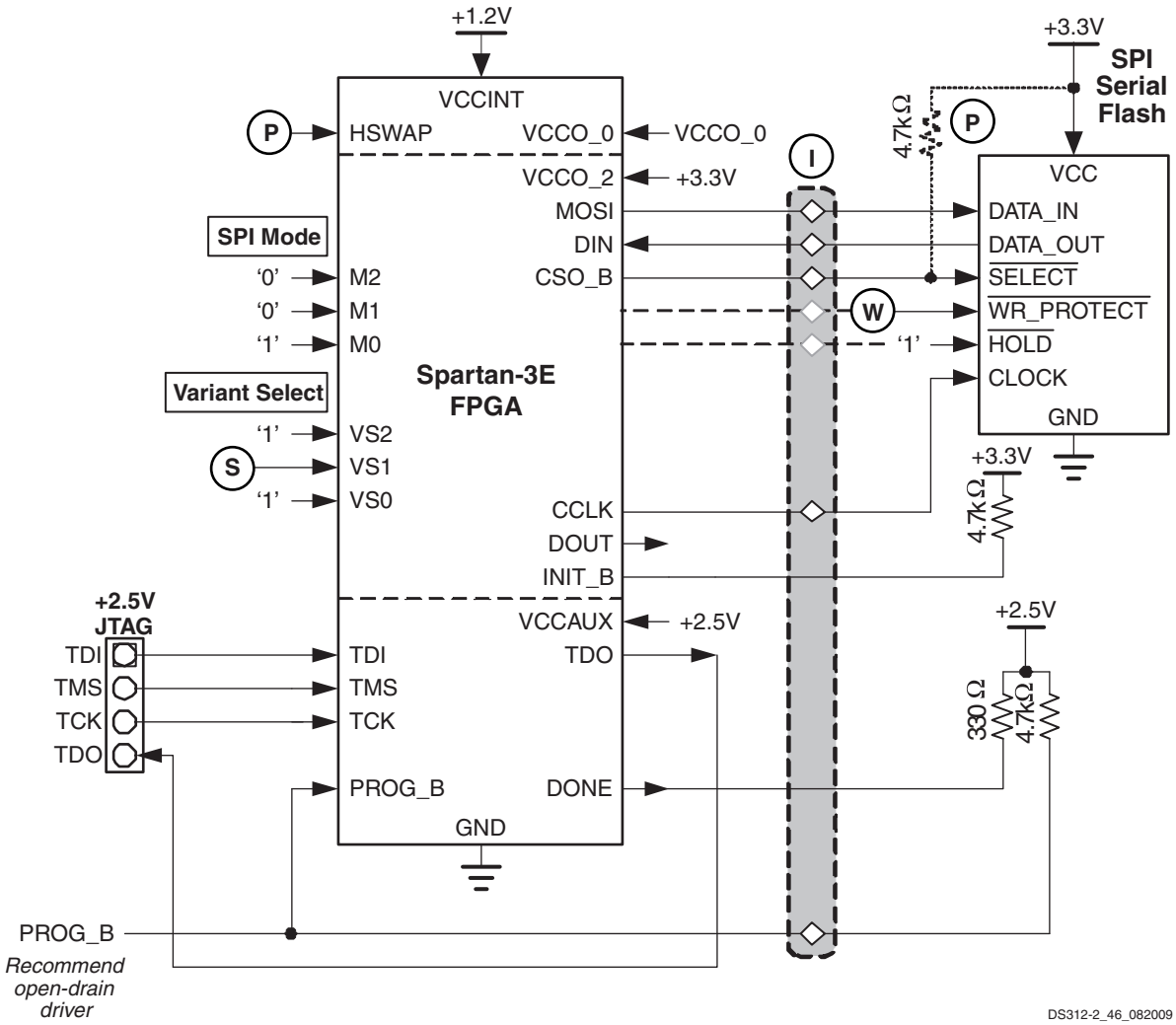



*Figure 53:* **SPI Flash PROM Interface for PROMs Supporting READ (0x03) and FAST_READ (0x0B) Commands**

Ⓢ Although SPI is a standard four-wire interface, various available SPI Flash PROMs use different command protocols. The FPGA’s variant select pins, VS[2:0], define how the FPGA communicates with the SPI Flash, including which SPI Flash command the FPGA issues to start the read operation and the number of dummy bytes inserted before the FPGA expects to receive valid data from the SPI Flash. Table 53 shows the available SPI Flash PROMs expected to operate with Spartan-3E FPGAs. Other compatible devices might work but have not been tested for suitability with Spartan-3E FPGAs. All other VS[2:0] values are reserved for future use. Consult the data sheet for the desired SPI Flash device to determine its suitability. The basic timing requirements and waveforms are provided in Serial Peripheral Interface (SPI) Configuration Timing in Module 3.

Figure 53 shows the general connection diagram for those SPI Flash PROMs that support the 0x03 READ command or the 0x0B FAST READ commands.

Figure 54 shows the connection diagram for Atmel DataFlash serial PROMs, which also use an SPI-based protocol. ‘B’-series DataFlash devices are limited to FPGA applications operating over the commercial temperature range. Industrial temperature range applications must use ‘C’- or ‘D’-series DataFlash devices, which have a shorter DataFlash select setup time, because of the faster FPGA CCLK frequency at cold temperatures.

*Table 53:* **Variant Select Codes for Various SPI Serial Flash PROMs**

| VS2 | VS1 | VS0 | SPI Read Command | Dummy Bytes | SPI Serial Flash Vendor | SPI Flash Family | iMPACT Programming Support |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | FAST READ (0x0B) (see Figure 53) | 1 | STMicroelectronics (ST) | M25Pxx<br>M25PExx/M45PExx | Yes |
| | | | | | Atmel | AT45DB 'D'-Series Data Flash | Yes |
| | | | | | | AT26 / AT25(1) | |
| | | | | | Intel | S33 | |
| | | | | | Spansion *(AMD, Fujitsu)* | S25FLxxxA | |
| | | | | | Winbond *(NexFlash)* | NX25 / W25 | |
| | | | | | Macronix | MX25Lxxxx | |
| | | | | | Silicon Storage Technology (SST) | SST25LFxxxA<br>SST25VFxxxA | |
| | | | | | Programmable Microelectronics Corp. (PMC) | Pm25LVxxx | |
| | | | | | AMIC Technology | A25L | |
| | | | | | Eon Silicon Solution, Inc. | EN25 | |
| 1 | 0 | 1 | READ (0x03) (see Figure 53) | 0 | STMicroelectronics (ST) | M25Pxx<br>M25PExx/M45PExx | Yes |
| | | | | | Spansion *(AMD, Fujitsu)* | S25FLxxxA | |
| | | | | | Winbond *(NexFlash)* | NX25 / W25 | |
| | | | | | Macronix | MX25Lxxxx | |
| | | | | | Silicon Storage Technology (SST) | SST25LFxxxA<br>SST25VFxxxA<br>SST25VFxxx | |
| | | | | | Programmable Microelectronics Corp. (PMC) | Pm25LVxxx | |
| 1 | 1 | 0 | READ ARRAY (0xE8) (see Figure 54) | 4 | Atmel Corporation | AT45DB DataFlash *(use only 'C' or 'D' Series for Industrial temperature range)* | Yes |
| Others | | | Reserved | | | | |

**Notes:**
1. See iMPACT documentation for specific device support.

***WRITER NOTE:*** Many of the URLs in this table are obsolete or otherwise broken.

This addressing flexibility allows the FPGA to share the parallel Flash PROM with an external or embedded processor. Depending on the specific processor architecture, the processor boots either from the top or bottom of memory. The FPGA is flexible and boots from the opposite end of memory from the processor. Only the processor or the FPGA can boot at any given time. The FPGA can configure first, holding the processor in reset or the processor can boot first, asserting the FPGA's PROG_B pin.

The mode select pins, M[2:0], are sampled when the FPGA's INIT_B output goes High and must be at defined logic levels during this time. After configuration, when the FPGA's DONE output goes High, the mode pins are available as full-featured user-I/O pins.

(P) Similarly, the FPGA's HSWAP pin must be Low to enable pull-up resistors on all user-I/O pins or High to disable the pull-up resistors. The HSWAP control must remain at a constant logic level throughout FPGA configuration. After configuration, when the FPGA's DONE output goes High, the HSWAP pin is available as full-featured user-I/O pin and is powered by the VCCO_0 supply.

The RDWR_B and CSI_B must be Low throughout the configuration process. After configuration, these pins also become user I/O.

In a single-FPGA application, the FPGA's CSO_B and CCLK pins are not used but are actively driving during the configuration process. The BUSY pin is not used but also actively drives during configuration and is available as a user I/O after configuration.

After configuration, all of the interface pins except DONE and PROG_B are available as user I/Os. Furthermore, the bidirectional SelectMAP configuration peripheral interface (see Slave Parallel Mode) is available after configuration. To continue using SelectMAP mode, set the ***Persist*** bitstream generator option to ***Yes***. An external host can then read and verify configuration data.

The Persist option will maintain A20-A23 as configuration pins although they are not used in SelectMAP mode.

*Table 59:* **Byte-Wide Peripheral Interface (BPI) Connections**

| Pin Name | FPGA Direction | Description | During Configuration | After Configuration |
|---|---|---|---|---|
| HSWAP (P) | Input | **User I/O Pull-Up Control**. When Low during configuration, enables pull-up resistors in all I/O pins to respective I/O bank $V_{CCO}$ input.<br>0: Pull-ups during configuration<br>1: No pull-ups | Drive at valid logic level throughout configuration. | User I/O |
| M[2:0] (A) | Input | **Mode Select**. Selects the FPGA configuration mode. See Design Considerations for the HSWAP, M[2:0], and VS[2:0] Pins. | M2 = 0, M1 = 1. Set M0 = 0 to start at address 0, increment addresses. Set M0 = 1 to start at address 0xFFFFFF and decrement addresses. Sampled when INIT_B goes High. | User I/O |
| CSI_B | Input | **Chip Select Input**. Active Low. | Must be Low throughout configuration. | User I/O. If bitstream option ***Persist=Yes***, becomes part of SelectMap parallel peripheral interface. |
| RDWR_B | Input | **Read/Write Control**. Active Low write enable. Read functionality typically only used after configuration, if bitstream option ***Persist=Yes***. | Must be Low throughout configuration. | User I/O. If bitstream option ***Persist=Yes***, becomes part of SelectMap parallel peripheral interface. |
| LDC0 | Output | PROM Chip Enable | Connect to PROM chip-select input (CE#). FPGA drives this signal Low throughout configuration. | User I/O. If the FPGA does not access the PROM after configuration, drive this pin High to deselect the PROM. A[23:0], D[7:0], LDC[2:1], and HDC then become available as user I/O. |
| LDC1 | Output | PROM Output Enable | Connect to the PROM output-enable input (OE#). The FPGA drives this signal Low throughout configuration. | User I/O |

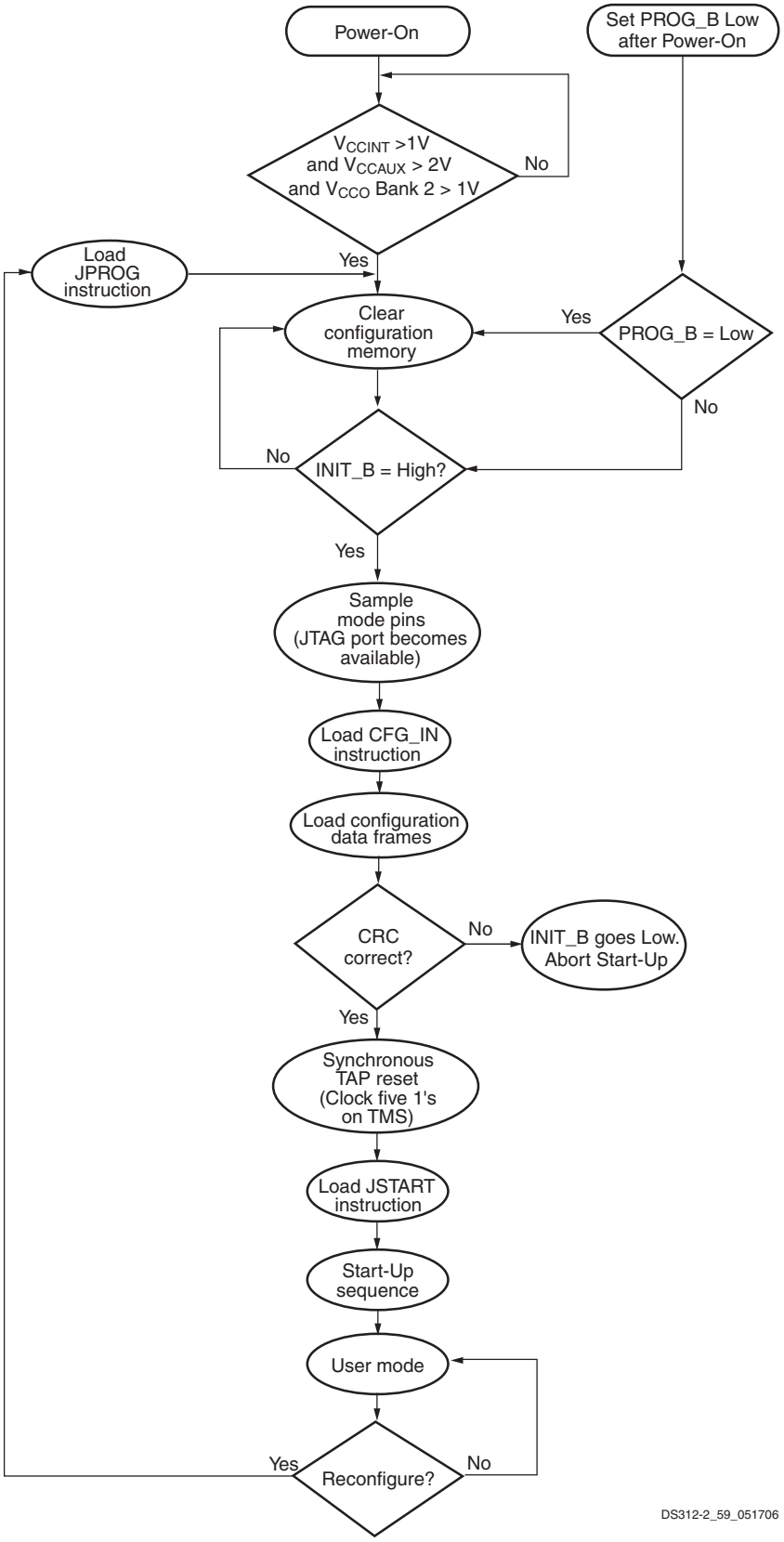



*Figure 67:* **Boundary-Scan Configuration Flow Diagram**

## Voltage Regulators

Various power supply manufacturers offer complete power solutions for Xilinx FPGAs including some with integrated three-rail regulators specifically designed for Spartan-3 and Spartan-3E FPGAs. The Xilinx Power Corner website provides links to vendor solution guides and Xilinx power estimation and analysis tools.

## Power Distribution System (PDS) Design and Decoupling/Bypass Capacitors

Good power distribution system (PDS) design is important for all FPGA designs, but especially so for high performance applications, greater than 100 MHz. Proper design results in better overall performance, lower clock and DCM jitter, and a generally more robust system. Before designing the printed circuit board (PCB) for the FPGA design, please review XAPP623: *Power Distribution System (PDS) Design: Using Bypass/Decoupling Capacitors*.

## Power-On Behavior

For additional power-on behavior information, including I/O behavior before and during configuration, refer to the "Sequence of Events" chapter in UG332.

Spartan-3E FPGAs have a built-in Power-On Reset (POR) circuit that monitors the three power rails required to successfully configure the FPGA. At power-up, the POR circuit holds the FPGA in a reset state until the $V_{CCINT}$, $V_{CCAUX}$, and $V_{CCO}$ Bank 2 supplies reach their respective input threshold levels (see Table 74 in Module 3). After all three supplies reach their respective thresholds, the POR reset is released and the FPGA begins its configuration process.

### Supply Sequencing

Because the three FPGA supply inputs must be valid to release the POR reset and can be supplied in any order, there are no FPGA-specific voltage sequencing requirements. Applying the FPGA's $V_{CCAUX}$ supply before the $V_{CCINT}$ supply uses the least $I_{CCINT}$ current.

Although the FPGA has no specific voltage sequence requirements, be sure to consider any potential sequencing requirement of the configuration device attached to the FPGA, such as an SPI serial Flash PROM, a parallel NOR Flash PROM, or a microcontroller. For example, Flash PROMs have a minimum time requirement before the PROM can be selected and this must be considered if the 3.3V supply is the last in the sequence. See Power-On Precautions if 3.3V Supply is Last in Sequence for more details.

When all three supplies are valid, the minimum current required to power-on the FPGA equals the worst-case quiescent current, specified in Table 79. Spartan-3E FPGAs do not require Power-On Surge (POS) current to successfully configure.

### Surplus $I_{CCINT}$ if $V_{CCINT}$ Applied before $V_{CCAUX}$

If the $V_{CCINT}$ supply is applied before the $V_{CCAUX}$ supply, the FPGA might draw a surplus $I_{CCINT}$ current in addition to the $I_{CCINT}$ quiescent current levels specified in Table 79, page 118. The momentary additional $I_{CCINT}$ surplus current might be a few hundred milliamperes under nominal conditions, significantly less than the instantaneous current consumed by the bypass capacitors at power-on. However, the surplus current immediately disappears when the $V_{CCAUX}$ supply is applied, and, in response, the FPGA's $I_{CCINT}$ quiescent current demand drops to the levels specified in Table 79. The FPGA does not use or require the surplus current to successfully power-on and configure. If applying $V_{CCINT}$ before $V_{CCAUX}$, ensure that the regulator does not have a foldback feature that could inadvertently shut down in the presence of the surplus current.

## Configuration Data Retention, Brown-Out

The FPGA's configuration data is stored in robust CMOS configuration latches. The data in these latches is retained even when the voltages drop to the minimum levels necessary to preserve RAM contents, as specified in Table 76.

If, after configuration, the $V_{CCAUX}$ or $V_{CCINT}$ supply drops below its data retention voltage, the current device configuration must be cleared using one of the following methods:

- Force the $V_{CCAUX}$ or $V_{CCINT}$ supply voltage below the minimum Power On Reset (POR) voltage threshold (Table 74).
- Assert PROG_B Low.

The POR circuit does not monitor the VCCO_2 supply after configuration. Consequently, dropping the VCCO_2 voltage does not reset the device by triggering a Power-On Reset (POR) event.

## No Internal Charge Pumps or Free-Running Oscillators

Some system applications are sensitive to sources of analog noise. Spartan-3E FPGA circuitry is fully static and does not employ internal charge pumps.

The CCLK configuration clock is active during the FPGA configuration process. After configuration completes, the CCLK oscillator is automatically disabled unless the Bitstream Generator (BitGen) option ***Persist=Yes***.

## General Recommended Operating Conditions

*Table 77:* **General Recommended Operating Conditions**

| Symbol | Description | | | Min | Nominal | Max | Units |
|---|---|---|---|---|---|---|---|
| $T_J$ | Junction temperature | Commercial | | 0 | – | 85 | °C |
| | | Industrial | | –40 | – | 100 | °C |
| $V_{CCINT}$ | Internal supply voltage | | | 1.140 | 1.200 | 1.260 | V |
| $V_{CCO}$ (1) | Output driver supply voltage | | | 1.100 | - | 3.465 | V |
| $V_{CCAUX}$ | Auxiliary supply voltage | | | 2.375 | 2.500 | 2.625 | V |
| $V_{IN}$ (2,3) | Input voltage extremes to avoid turning on I/O protection diodes | I/O, Input-only, and Dual-Purpose pins (4) | IP or IO_# | –0.5 | – | $V_{CCO}$ + 0.5 | V |
| | | | IO_Lxxy_# (5) | –0.5 | – | $V_{CCO}$ + 0.5 | V |
| | | Dedicated pins (6) | | –0.5 | – | $V_{CCAUX}$ + 0.5 | V |
| $T_{IN}$ | Input signal transition time (7) | | | – | – | 500 | ns |

**Notes:**

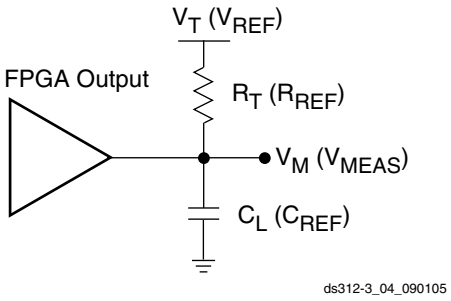
1. This $V_{CCO}$ range spans the lowest and highest operating voltages for all supported I/O standards. Table 80 lists the recommended $V_{CCO}$ range specific to each of the single-ended I/O standards, and Table 82 lists that specific to the differential standards.
2. Input voltages outside the recommended range require the $I_{IK}$ input clamp diode rating is met and no more than 100 pins exceed the range simultaneously. Refer to Table 73.
3. See XAPP459: *Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins on Spartan-3 Families*.
4. Each of the User I/O and Dual-Purpose pins is associated with one of the four banks' $V_{CCO}$ rails. Meeting the $V_{IN}$ limit ensures that the internal diode junctions that exist between these pins and their associated $V_{CCO}$ and GND rails do not turn on. The absolute maximum rating is provided in Table 73.
5. For single-ended signals that are placed on a differential-capable I/O, $V_{IN}$ of –0.2V to –0.5V is supported but can cause increased leakage between the two pins. See *Parasitic Leakage* in UG331, *Spartan-3 Generation FPGA User Guide*.
6. All Dedicated pins (PROG_B, DONE, TCK, TDI, TDO, and TMS) draw power from the $V_{CCAUX}$ rail (2.5V). Meeting the $V_{IN}$ max limit ensures that the internal diode junctions that exist between each of these pins and the $V_{CCAUX}$ and GND rails do not turn on.
7. Measured between 10% and 90% $V_{CCO}$. Follow Signal Integrity recommendations.

## Timing Measurement Methodology

When measuring timing parameters at the programmable I/Os, different signal standards call for different test conditions. Table 95 lists the conditions to use for each standard.

The method for measuring Input timing is as follows: A signal that swings between a Low logic level of $V_L$ and a High logic level of $V_H$ is applied to the Input under test. Some standards also require the application of a bias voltage to the $V_{REF}$ pins of a given bank to properly set the input-switching threshold. The measurement point of the Input signal ($V_M$) is commonly located halfway between $V_L$ and $V_H$.

The Output test setup is shown in Figure 72. A termination voltage $V_T$ is applied to the termination resistor $R_T$, the other end of which is connected to the Output. For each standard, $R_T$ and $V_T$ generally take on the standard values recommended for minimizing signal reflections. If the standard does not ordinarily use terminations (e.g., LVCMOS, LVTTL), then $R_T$ is set to 1MΩ to indicate an open connection, and $V_T$ is set to zero. The same measurement point ($V_M$) that was used at the Input is also used at the Output.




**Notes:**

1. The names shown in parentheses are used in the IBIS file.

*Figure 72:* **Output Test Setup**

*Table 95:* **Test Methods for Timing Measurement at I/Os**

| Signal Standard (IOSTANDARD) | | Inputs | | | Outputs | | Inputs and Outputs |
|---|---|---|---|---|---|---|---|
| | | $V_{REF}$ (V) | $V_L$ (V) | $V_H$ (V) | $R_T$ (Ω) | $V_T$ (V) | $V_M$ (V) |
| **Single-Ended** | | | | | | | |
| LVTTL | | - | 0 | 3.3 | 1M | 0 | 1.4 |
| LVCMOS33 | | - | 0 | 3.3 | 1M | 0 | 1.65 |
| LVCMOS25 | | - | 0 | 2.5 | 1M | 0 | 1.25 |
| LVCMOS18 | | - | 0 | 1.8 | 1M | 0 | 0.9 |
| LVCMOS15 | | - | 0 | 1.5 | 1M | 0 | 0.75 |
| LVCMOS12 | | - | 0 | 1.2 | 1M | 0 | 0.6 |
| PCI33_3 | Rising | - | Note 3 | Note 3 | 25 | 0 | 0.94 |
| | Falling | | | | 25 | 3.3 | 2.03 |
| PCI66_3 | Rising | - | Note 3 | Note 3 | 25 | 0 | 0.94 |
| | Falling | | | | 25 | 3.3 | 2.03 |
| HSTL_I_18 | | 0.9 | $V_{REF}$ – 0.5 | $V_{REF}$ + 0.5 | 50 | 0.9 | $V_{REF}$ |
| HSTL_III_18 | | 1.1 | $V_{REF}$ – 0.5 | $V_{REF}$ + 0.5 | 50 | 1.8 | $V_{REF}$ |
| SSTL18_I | | 0.9 | $V_{REF}$ – 0.5 | $V_{REF}$ + 0.5 | 50 | 0.9 | $V_{REF}$ |
| SSTL2_I | | 1.25 | $V_{REF}$ – 0.75 | $V_{REF}$ + 0.75 | 50 | 1.25 | $V_{REF}$ |
| **Differential** | | | | | | | |
| LVDS_25 | | - | $V_{ICM}$ – 0.125 | $V_{ICM}$ + 0.125 | 50 | 1.2 | $V_{ICM}$ |
| BLVDS_25 | | - | $V_{ICM}$ – 0.125 | $V_{ICM}$ + 0.125 | 1M | 0 | $V_{ICM}$ |
| MINI_LVDS_25 | | - | $V_{ICM}$ – 0.125 | $V_{ICM}$ + 0.125 | 50 | 1.2 | $V_{ICM}$ |
| LVPECL_25 | | - | $V_{ICM}$ – 0.3 | $V_{ICM}$ + 0.3 | 1M | 0 | $V_{ICM}$ |
| RSDS_25 | | - | $V_{ICM}$ – 0.1 | $V_{ICM}$ + 0.1 | 50 | 1.2 | $V_{ICM}$ |

## Package Thermal Characteristics

The power dissipated by an FPGA application has implications on package selection and system design. The power consumed by a Spartan-3E FPGA is reported using either the XPower Estimator or the XPower Analyzer calculator integrated in the Xilinx ISE® development software. Table 130 provides the thermal characteristics for the various Spartan-3E package offerings.

The junction-to-case thermal resistance ($\theta_{JC}$) indicates the difference between the temperature measured on the package body (case) and the die junction temperature per watt of power consumption. The junction-to-board ($\theta_{JB}$) value similarly reports the difference between the board and junction temperature. The junction-to-ambient ($\theta_{JA}$) value reports the temperature difference per watt between the ambient environment and the junction temperature. The $\theta_{JA}$ value is reported at different air velocities, measured in linear feet per minute (LFM). The Still Air (0 LFM) column shows the $\theta_{JA}$ value in a system without a fan. The thermal resistance drops with increasing air flow.

*Table 130:* **Spartan-3E Package Thermal Characteristics**

| Device | Package | Junction-to-Case ($\theta_{JC}$) | Junction-to-Board ($\theta_{JB}$) | Junction-to-Ambient ($\theta_{JA}$) at Different Air Flows | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | Still Air (0 LFM) | 250 LFM | 500 LFM | 750 LFM | |
| XC3S100E | VQ100 | 13.0 | 30.9 | 49.0 | 40.7 | 37.9 | 37.0 | °C/Watt |
| XC3S250E | | 11.0 | 25.9 | 43.3 | 36.0 | 33.6 | 32.7 | °C/Watt |
| XC3S500E | | 9.8 | | 40.0 | 33.3 | 31.0 | 30.2 | °C/Watt |
| XC3S100E | CP132 | 19.3 | 42.0 | 62.1 | 55.3 | 52.8 | 51.2 | °C/Watt |
| XC3S250E | | 11.8 | 28.1 | 48.3 | 41.8 | 39.5 | 38.0 | °C/Watt |
| XC3S500E | | 8.5 | 21.3 | 41.5 | 35.2 | 32.9 | 31.5 | °C/Watt |
| XC3S100E | TQ144 | 8.2 | 31.9 | 52.1 | 40.5 | 34.6 | 32.5 | °C/Watt |
| XC3S250E | | 7.2 | 25.7 | 37.6 | 29.2 | 25.0 | 23.4 | °C/Watt |
| XC3S250E | PQ208 | 9.8 | 29.0 | 37.0 | 27.3 | 24.1 | 22.4 | °C/Watt |
| XC3S500E | | 8.5 | 26.8 | 36.1 | 26.6 | 23.6 | 21.8 | °C/Watt |
| XC3S250E | FT256 | 12.4 | 27.7 | 35.8 | 29.3 | 28.4 | 28.1 | °C/Watt |
| XC3S500E | | 9.6 | 22.2 | 31.1 | 25.0 | 24.0 | 23.6 | °C/Watt |
| XC3S1200E | | 6.5 | 16.4 | 26.2 | 20.5 | 19.3 | 18.9 | °C/Watt |
| XC3S500E | FG320 | 9.8 | 15.6 | 26.1 | 20.6 | 19.4 | 18.6 | °C/Watt |
| XC3S1200E | | 8.2 | 12.5 | 23.0 | 17.7 | 16.4 | 15.7 | °C/Watt |
| XC3S1600E | | 7.1 | 10.6 | 21.1 | 15.9 | 14.6 | 13.8 | °C/Watt |
| XC3S1200E | FG400 | 7.5 | 12.4 | 22.3 | 17.2 | 16.0 | 15.3 | °C/Watt |
| XC3S1600E | | 6.0 | 10.4 | 20.3 | 15.2 | 14.0 | 13.3 | °C/Watt |
| XC3S1600E | FG484 | 5.7 | 9.4 | 18.8 | 12.5 | 11.3 | 10.8 | °C/Watt |

*Table 131:* **VQ100 Package Pinout *(Cont'd)***

| Bank | XC3S100E XC3S250E XC3S500E Pin Name | VQ100 Pin Number | Type |
|---|---|---|---|
| 3 | IO_L02P_3 | P4 | I/O |
| 3 | IO_L03N_3/LHCLK1 | P10 | LHCLK |
| 3 | IO_L03P_3/LHCLK0 | P9 | LHCLK |
| 3 | IO_L04N_3/LHCLK3 | P12 | LHCLK |
| 3 | IO_L04P_3/LHCLK2 | P11 | LHCLK |
| 3 | IO_L05N_3/LHCLK5 | P16 | LHCLK |
| 3 | IO_L05P_3/LHCLK4 | P15 | LHCLK |
| 3 | IO_L06N_3/LHCLK7 | P18 | LHCLK |
| 3 | IO_L06P_3/LHCLK6 | P17 | LHCLK |
| 3 | IO_L07N_3 | P23 | I/O |
| 3 | IO_L07P_3 | P22 | I/O |
| 3 | IP | P13 | INPUT |
| 3 | VCCO_3 | P8 | VCCO |
| 3 | VCCO_3 | P20 | VCCO |
| GND | GND | P7 | GND |
| GND | GND | P14 | GND |
| GND | GND | P19 | GND |
| GND | GND | P29 | GND |
| GND | GND | P37 | GND |
| GND | GND | P52 | GND |
| GND | GND | P59 | GND |
| GND | GND | P64 | GND |
| GND | GND | P72 | GND |
| GND | GND | P81 | GND |
| GND | GND | P87 | GND |
| GND | GND | P93 | GND |
| VCCAUX | DONE | P51 | CONFIG |
| VCCAUX | PROG_B | P1 | CONFIG |
| VCCAUX | TCK | P77 | JTAG |
| VCCAUX | TDI | P100 | JTAG |
| VCCAUX | TDO | P76 | JTAG |
| VCCAUX | TMS | P75 | JTAG |
| VCCAUX | VCCAUX | P21 | VCCAUX |
| VCCAUX | VCCAUX | P46 | VCCAUX |
| VCCAUX | VCCAUX | P74 | VCCAUX |
| VCCAUX | VCCAUX | P96 | VCCAUX |
| VCCINT | VCCINT | P6 | VCCINT |
| VCCINT | VCCINT | P28 | VCCINT |
| VCCINT | VCCINT | P56 | VCCINT |
| VCCINT | VCCINT | P80 | VCCINT |

## User I/Os by Bank

Table 138 and Table 139 indicate how the 108 available user-I/O pins are distributed between the four I/O banks on the TQ144 package.

*Table 138:* **User I/Os Per Bank for the XC3S100E in the TQ144 Package**

| Package Edge | I/O Bank | Maximum I/O | All Possible I/O Pins by Type | | | | |
|---|---|---|---|---|---|---|---|
| | | | I/O | INPUT | DUAL | VREF[1] | CLK[2] |
| Top | 0 | 26 | 9 | 6 | 1 | 2 | 8 |
| Right | 1 | 28 | 0 | 5 | 21 | 2 | 0[2] |
| Bottom | 2 | 26 | 0 | 4 | 20 | 2 | 0[2] |
| Left | 3 | 28 | 13 | 4 | 0 | 3 | 8 |
| **TOTAL** | | **108** | **22** | **19** | **42** | **9** | **16** |

**Notes:**

1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

*Table 139:* **User I/Os Per Bank for the XC3S250E in TQ144 Package**

| Package Edge | I/O Bank | Maximum I/O | All Possible I/O Pins by Type | | | | |
|---|---|---|---|---|---|---|---|
| | | | I/O | INPUT | DUAL | VREF[1] | CLK[2] |
| Top | 0 | 26 | 9 | 6 | 1 | 2 | 8 |
| Right | 1 | 28 | 0 | 5 | 21 | 2 | 0[2] |
| Bottom | 2 | 26 | 0 | 4 | 20 | 2 | 0[2] |
| Left | 3 | 28 | 11 | 6 | 0 | 3 | 8 |
| **TOTAL** | | **108** | **20** | **21** | **42** | **9** | **16** |

**Notes:**

1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

## Footprint Migration Differences

Table 140 summarizes any footprint and functionality differences between the XC3S100E and the XC3S250E FPGAs that may affect easy migration between devices. There are four such pins. All other pins not listed in Table 140 unconditionally migrate between Spartan-3E devices available in the TQ144 package.

The arrows indicate the direction for easy migration. For example, a left-facing arrow indicates that the pin on the XC3S250E unconditionally migrates to the pin on the XC3S100E. It may be possible to migrate the opposite direction depending on the I/O configuration. For example, an I/O pin (Type = I/O) can migrate to an input-only pin (Type = INPUT) if the I/O pin is configured as an input.

*Table 140:* **TQ144 Footprint Migration Differences**

| TQ144 Pin | Bank | XC3S100E Type | Migration | XC3S250E Type |
|---|---|---|---|---|
| P10 | 3 | I/O | ← | INPUT |
| P29 | 3 | I/O | ← | INPUT |
| P31 | 3 | VREF(INPUT) | → | VREF(I/O) |
| P66 | 2 | VREF(INPUT) | → | VREF(I/O) |
| **DIFFERENCES** | | | **4** | |

Legend:

→ This pin can unconditionally migrate from the device on the left to the device on the right. Migration in the other direction may be possible depending on how the pin is configured for the device on the right.

← This pin can unconditionally migrate from the device on the right to the device on the left. Migration in the other direction may be possible depending on how the pin is configured for the device on the left.

# PQ208: 208-pin Plastic Quad Flat Package

The 208-pin plastic quad flat package, PQ208, supports two different Spartan-3E FPGAs, including the XC3S250E and the XC3S500E.

Table 141 lists all the PQ208 package pins. They are sorted by bank number and then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at:

http://www.xilinx.com/support/documentation/data_sheets/s3e_pin.zip

## Pinout Table

*Table 141:* **PQ208 Package Pinout**

| Bank | XC3S250E XC3S500E Pin Name | PQ208 Pin | Type |
|---|---|---|---|
| 0 | IO | P187 | I/O |
| 0 | IO/VREF_0 | P179 | VREF |
| 0 | IO_L01N_0 | P161 | I/O |
| 0 | IO_L01P_0 | P160 | I/O |
| 0 | IO_L02N_0/VREF_0 | P163 | VREF |
| 0 | IO_L02P_0 | P162 | I/O |
| 0 | IO_L03N_0 | P165 | I/O |
| 0 | IO_L03P_0 | P164 | I/O |
| 0 | IO_L04N_0/VREF_0 | P168 | VREF |
| 0 | IO_L04P_0 | P167 | I/O |
| 0 | IO_L05N_0 | P172 | I/O |
| 0 | IO_L05P_0 | P171 | I/O |
| 0 | IO_L07N_0/GCLK5 | P178 | GCLK |
| 0 | IO_L07P_0/GCLK4 | P177 | GCLK |
| 0 | IO_L08N_0/GCLK7 | P181 | GCLK |
| 0 | IO_L08P_0/GCLK6 | P180 | GCLK |
| 0 | IO_L10N_0/GCLK11 | P186 | GCLK |
| 0 | IO_L10P_0/GCLK10 | P185 | GCLK |
| 0 | IO_L11N_0 | P190 | I/O |
| 0 | IO_L11P_0 | P189 | I/O |
| 0 | IO_L12N_0/VREF_0 | P193 | VREF |
| 0 | IO_L12P_0 | P192 | I/O |
| 0 | IO_L13N_0 | P197 | I/O |
| 0 | IO_L13P_0 | P196 | I/O |
| 0 | IO_L14N_0/VREF_0 | P200 | VREF |
| 0 | IO_L14P_0 | P199 | I/O |
| 0 | IO_L15N_0 | P203 | I/O |

*Table 141:* **PQ208 Package Pinout *(Cont'd)***

| Bank | XC3S250E XC3S500E Pin Name | PQ208 Pin | Type |
|---|---|---|---|
| 0 | IO_L15P_0 | P202 | I/O |
| 0 | IO_L16N_0/HSWAP | P206 | DUAL |
| 0 | IO_L16P_0 | P205 | I/O |
| 0 | IP | P159 | INPUT |
| 0 | IP | P169 | INPUT |
| 0 | IP | P194 | INPUT |
| 0 | IP | P204 | INPUT |
| 0 | IP_L06N_0 | P175 | INPUT |
| 0 | IP_L06P_0 | P174 | INPUT |
| 0 | IP_L09N_0/GCLK9 | P184 | GCLK |
| 0 | IP_L09P_0/GCLK8 | P183 | GCLK |
| 0 | VCCO_0 | P176 | VCCO |
| 0 | VCCO_0 | P191 | VCCO |
| 0 | VCCO_0 | P201 | VCCO |
| 1 | IO_L01N_1/A15 | P107 | DUAL |
| 1 | IO_L01P_1/A16 | P106 | DUAL |
| 1 | IO_L02N_1/A13 | P109 | DUAL |
| 1 | IO_L02P_1/A14 | P108 | DUAL |
| 1 | IO_L03N_1/VREF_1 | P113 | VREF |
| 1 | IO_L03P_1 | P112 | I/O |
| 1 | IO_L04N_1 | P116 | I/O |
| 1 | IO_L04P_1 | P115 | I/O |
| 1 | IO_L05N_1/A11 | P120 | DUAL |
| 1 | IO_L05P_1/A12 | P119 | DUAL |
| 1 | IO_L06N_1/VREF_1 | P123 | VREF |
| 1 | IO_L06P_1 | P122 | I/O |
| 1 | IO_L07N_1/A9/RHCLK1 | P127 | RHCLK/DUAL |
| 1 | IO_L07P_1/A10/RHCLK0 | P126 | RHCLK/DUAL |
| 1 | IO_L08N_1/A7/RHCLK3 | P129 | RHCLK/DUAL |
| 1 | IO_L08P_1/A8/RHCLK2 | P128 | RHCLK/DUAL |
| 1 | IO_L09N_1/A5/RHCLK5 | P133 | RHCLK/DUAL |
| 1 | IO_L09P_1/A6/RHCLK4 | P132 | RHCLK/DUAL |
| 1 | IO_L10N_1/A3/RHCLK7 | P135 | RHCLK/DUAL |
| 1 | IO_L10P_1/A4/RHCLK6 | P134 | RHCLK/DUAL |
| 1 | IO_L11N_1/A1 | P138 | DUAL |
| 1 | IO_L11P_1/A2 | P137 | DUAL |
| 1 | IO_L12N_1/A0 | P140 | DUAL |
| 1 | IO_L12P_1 | P139 | I/O |
| 1 | IO_L13N_1 | P145 | I/O |
| 1 | IO_L13P_1 | P144 | I/O |
| 1 | IO_L14N_1 | P147 | I/O |
| 1 | IO_L14P_1 | P146 | I/O |

*Table 143:* **FT256 Package Pinout *(Cont'd)***

| Bank | XC3S250E Pin Name | XC3S500E Pin Name | XC3S1200E Pin Name | FT256 Ball | Type |
|---|---|---|---|---|---|
| 1 | IO | IO | IP | M14 | ***250E:*** I/O ***500E:*** I/O ***1200E:*** INPUT |
| 1 | IO/VREF_1 | IP/VREF_1 | IP/VREF_1 | D16 | ***250E:*** VREF(I/O) ***500E:*** VREF(INPUT) ***1200E:*** VREF(INPUT) |
| 1 | IP/VREF_1 | IP/VREF_1 | IP/VREF_1 | H13 | VREF |
| 1 | VCCO_1 | VCCO_1 | VCCO_1 | E15 | VCCO |
| 1 | VCCO_1 | VCCO_1 | VCCO_1 | G11 | VCCO |
| 1 | VCCO_1 | VCCO_1 | VCCO_1 | K11 | VCCO |
| 1 | VCCO_1 | VCCO_1 | VCCO_1 | M15 | VCCO |
| 2 | IP | IP | IO | M7 | ***250E:*** INPUT ***500E:*** INPUT ***1200E:*** I/O |
| 2 | IP | IP | IO | T12 | ***250E:*** INPUT ***500E:*** INPUT ***1200E:*** I/O |
| 2 | IO/D5 | IO/D5 | IO/D5 | T8 | DUAL |
| 2 | IO/M1 | IO/M1 | IO/M1 | T10 | DUAL |
| 2 | IO/VREF_2 | IO/VREF_2 | IO/VREF_2 | P13 | VREF |
| 2 | IO/VREF_2 | IO/VREF_2 | IO/VREF_2 | R4 | VREF |
| 2 | IO_L01N_2/INIT_B | IO_L01N_2/INIT_B | IO_L01N_2/INIT_B | P4 | DUAL |
| 2 | IO_L01P_2/CSO_B | IO_L01P_2/CSO_B | IO_L01P_2/CSO_B | P3 | DUAL |
| 2 | IO_L03N_2/MOSI/CSI_B | IO_L03N_2/MOSI/CSI_B | IO_L03N_2/MOSI/CSI_B | N5 | DUAL |
| 2 | IO_L03P_2/DOUT/BUSY | IO_L03P_2/DOUT/BUSY | IO_L03P_2/DOUT/BUSY | P5 | DUAL |
| 2 | IO_L04N_2 | IO_L04N_2 | IO_L04N_2 | T5 | I/O |
| 2 | IO_L04P_2 | IO_L04P_2 | IO_L04P_2 | T4 | I/O |
| 2 | IO_L05N_2 | IO_L05N_2 | IO_L05N_2 | N6 | I/O |
| 2 | IO_L05P_2 | IO_L05P_2 | IO_L05P_2 | M6 | I/O |
| 2 | IO_L06N_2 | IO_L06N_2 | IO_L06N_2 | P6 | I/O |
| 2 | IO_L06P_2 | IO_L06P_2 | IO_L06P_2 | R6 | I/O |
| 2 | N.C. (◆) | IO_L07N_2 | IO_L07N_2 | P7 | ***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O |
| 2 | N.C. (◆) | IO_L07P_2 | IO_L07P_2 | N7 | ***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O |
| 2 | IO_L09N_2/D6/GCLK13 | IO_L09N_2/D6/GCLK13 | IO_L09N_2/D6/GCLK13 | L8 | DUAL/GCLK |
| 2 | IO_L09P_2/D7/GCLK12 | IO_L09P_2/D7/GCLK12 | IO_L09P_2/D7/GCLK12 | M8 | DUAL/GCLK |
| 2 | IO_L10N_2/D3/GCLK15 | IO_L10N_2/D3/GCLK15 | IO_L10N_2/D3/GCLK15 | P8 | DUAL/GCLK |
| 2 | IO_L10P_2/D4/GCLK14 | IO_L10P_2/D4/GCLK14 | IO_L10P_2/D4/GCLK14 | N8 | DUAL/GCLK |
| 2 | IO_L12N_2/D1/GCLK3 | IO_L12N_2/D1/GCLK3 | IO_L12N_2/D1/GCLK3 | N9 | DUAL/GCLK |
| 2 | IO_L12P_2/D2/GCLK2 | IO_L12P_2/D2/GCLK2 | IO_L12P_2/D2/GCLK2 | P9 | DUAL/GCLK |
| 2 | IO_L13N_2/DIN/D0 | IO_L13N_2/DIN/D0 | IO_L13N_2/DIN/D0 | M9 | DUAL |
| 2 | IO_L13P_2/M0 | IO_L13P_2/M0 | IO_L13P_2/M0 | L9 | DUAL |

*Table 143:* **FT256 Package Pinout *(Cont'd)***

| Bank | XC3S250E Pin Name | XC3S500E Pin Name | XC3S1200E Pin Name | FT256 Ball | Type |
|---|---|---|---|---|---|
| 3 | IP | IP | IP | N3 | INPUT |
| 3 | IP/VREF_3 | IP/VREF_3 | IP/VREF_3 | G1 | VREF |
| 3 | IO/VREF_3 | IO/VREF_3 | IP/VREF_3 | N2 | ***250E:*** VREF(I/O)<br>***500E:*** VREF(I/O)<br>***1200E:*** VREF(INPUT) |
| 3 | VCCO_3 | VCCO_3 | VCCO_3 | E2 | VCCO |
| 3 | VCCO_3 | VCCO_3 | VCCO_3 | G6 | VCCO |
| 3 | VCCO_3 | VCCO_3 | VCCO_3 | K6 | VCCO |
| 3 | VCCO_3 | VCCO_3 | VCCO_3 | M2 | VCCO |
| GND | GND | GND | GND | A1 | GND |
| GND | GND | GND | GND | A16 | GND |
| GND | GND | GND | GND | B9 | GND |
| GND | GND | GND | GND | F6 | GND |
| GND | GND | GND | GND | F11 | GND |
| GND | GND | GND | GND | G7 | GND |
| GND | GND | GND | GND | G8 | GND |
| GND | GND | GND | GND | G9 | GND |
| GND | GND | GND | GND | G10 | GND |
| GND | GND | GND | GND | H2 | GND |
| GND | GND | GND | GND | H7 | GND |
| GND | GND | GND | GND | H8 | GND |
| GND | GND | GND | GND | H9 | GND |
| GND | GND | GND | GND | H10 | GND |
| GND | GND | GND | GND | J7 | GND |
| GND | GND | GND | GND | J8 | GND |
| GND | GND | GND | GND | J9 | GND |
| GND | GND | GND | GND | J10 | GND |
| GND | GND | GND | GND | J15 | GND |
| GND | GND | GND | GND | K7 | GND |
| GND | GND | GND | GND | K8 | GND |
| GND | GND | GND | GND | K9 | GND |
| GND | GND | GND | GND | K10 | GND |
| GND | GND | GND | GND | L6 | GND |
| GND | GND | GND | GND | L11 | GND |
| GND | GND | GND | GND | R8 | GND |
| GND | GND | GND | GND | T1 | GND |
| GND | GND | GND | GND | T16 | GND |
| VCCAUX | DONE | DONE | DONE | T15 | CONFIG |
| VCCAUX | PROG_B | PROG_B | PROG_B | D3 | CONFIG |
| VCCAUX | TCK | TCK | TCK | A15 | JTAG |
| VCCAUX | TDI | TDI | TDI | A2 | JTAG |
| VCCAUX | TDO | TDO | TDO | C14 | JTAG |
| VCCAUX | TMS | TMS | TMS | B15 | JTAG |
| VCCAUX | VCCAUX | VCCAUX | VCCAUX | A6 | VCCAUX |

## User I/Os by Bank

Table 144, Table 145, and Table 146 indicate how the available user-I/O pins are distributed between the four I/O banks on the FT256 package.

The XC3S250E FPGA in the FT256 package has 18 unconnected balls, labeled with an "N.C." type. These pins are also indicated with the black diamond (◆) symbol in Figure 85.

*Table 144:* **User I/Os Per Bank on XC3S250E in the FT256 Package**

| Package Edge | I/O Bank | Maximum I/O | All Possible I/O Pins by Type | | | | |
|---|---|---|---|---|---|---|---|
| | | | I/O | INPUT | DUAL | VREF(1) | CLK(2) |
| Top | 0 | 44 | 20 | 10 | 1 | 5 | 8 |
| Right | 1 | 42 | 10 | 7 | 21 | 4 | 0(2) |
| Bottom | 2 | 44 | 8 | 9 | 24 | 3 | 0(2) |
| Left | 3 | 42 | 24 | 7 | 0 | 3 | 8 |
| **TOTAL** | | **172** | **62** | **33** | **46** | **15** | **16** |

**Notes:**

1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

*Table 145:* **User I/Os Per Bank on XC3S500E in the FT256 Package**

| Package Edge | I/O Bank | Maximum I/O | All Possible I/O Pins by Type | | | | |
|---|---|---|---|---|---|---|---|
| | | | I/O | INPUT | DUAL | VREF(1) | CLK(2) |
| Top | 0 | 46 | 22 | 10 | 1 | 5 | 8 |
| Right | 1 | 48 | 15 | 7 | 21 | 5 | 0(2) |
| Bottom | 2 | 48 | 11 | 9 | 24 | 4 | 0(2) |
| Left | 3 | 48 | 28 | 7 | 0 | 5 | 8 |
| **TOTAL** | | **190** | **76** | **33** | **46** | **19** | **16** |

**Notes:**

1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

*Table 146:* **User I/Os Per Bank on XC3S1200E in the FT256 Package**

| Package Edge | I/O Bank | Maximum I/O | All Possible I/O Pins by Type | | | | |
|---|---|---|---|---|---|---|---|
| | | | I/O | INPUT | DUAL | VREF(1) | CLK(2) |
| Top | 0 | 46 | 24 | 8 | 1 | 5 | 8 |
| Right | 1 | 48 | 14 | 8 | 21 | 5 | 0(2) |
| Bottom | 2 | 48 | 13 | 7 | 24 | 4 | 0(2) |
| Left | 3 | 48 | 27 | 8 | 0 | 5 | 8 |
| **TOTAL** | | **190** | **78** | **31** | **46** | **19** | **16** |

**Notes:**

1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

# FG400: 400-ball Fine-pitch Ball Grid Array

The 400-ball fine-pitch ball grid array, FG400, supports two different Spartan-3E FPGAs, including the XC3S1200E and the XC3S1600E. Both devices share a common footprint for this package as shown in Table 152 and Figure 87.

Table 152 lists all the FG400 package pins. They are sorted by bank number and then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at:

http://www.xilinx.com/support/documentation/data_sheets/s3e_pin.zip

## Pinout Table

*Table 152:* **FG400 Package Pinout**

| Bank | XC3S1200E XC3S1600E Pin Name | FG400 Ball | Type |
|---|---|---|---|
| 0 | IO | A3 | I/O |
| 0 | IO | A8 | I/O |
| 0 | IO | A12 | I/O |
| 0 | IO | C7 | I/O |
| 0 | IO | C10 | I/O |
| 0 | IO | E8 | I/O |
| 0 | IO | E13 | I/O |
| 0 | IO | E16 | I/O |
| 0 | IO | F13 | I/O |
| 0 | IO | F14 | I/O |
| 0 | IO | G7 | I/O |
| 0 | IO/VREF_0 | C11 | VREF |
| 0 | IO_L01N_0 | B17 | I/O |
| 0 | IO_L01P_0 | C17 | I/O |
| 0 | IO_L03N_0/VREF_0 | A18 | VREF |
| 0 | IO_L03P_0 | A19 | I/O |
| 0 | IO_L04N_0 | A17 | I/O |
| 0 | IO_L04P_0 | A16 | I/O |
| 0 | IO_L06N_0 | A15 | I/O |
| 0 | IO_L06P_0 | B15 | I/O |
| 0 | IO_L07N_0 | C14 | I/O |
| 0 | IO_L07P_0 | D14 | I/O |
| 0 | IO_L09N_0/VREF_0 | A13 | VREF |
| 0 | IO_L09P_0 | A14 | I/O |
| 0 | IO_L10N_0 | B13 | I/O |
| 0 | IO_L10P_0 | C13 | I/O |
| 0 | IO_L12N_0 | C12 | I/O |
| 0 | IO_L12P_0 | D12 | I/O |
| 0 | IO_L13N_0 | E12 | I/O |
| 0 | IO_L13P_0 | F12 | I/O |
| 0 | IO_L15N_0/GCLK5 | G11 | GCLK |
| 0 | IO_L15P_0/GCLK4 | F11 | GCLK |
| 0 | IO_L16N_0/GCLK7 | E10 | GCLK |
| 0 | IO_L16P_0/GCLK6 | E11 | GCLK |
| 0 | IO_L18N_0/GCLK11 | A9 | GCLK |
| 0 | IO_L18P_0/GCLK10 | A10 | GCLK |
| 0 | IO_L19N_0 | F9 | I/O |
| 0 | IO_L19P_0 | E9 | I/O |
| 0 | IO_L21N_0 | C9 | I/O |
| 0 | IO_L21P_0 | D9 | I/O |
| 0 | IO_L22N_0/VREF_0 | B8 | VREF |
| 0 | IO_L22P_0 | B9 | I/O |
| 0 | IO_L24N_0/VREF_0 | F7 | VREF |
| 0 | IO_L24P_0 | F8 | I/O |
| 0 | IO_L25N_0 | A6 | I/O |
| 0 | IO_L25P_0 | A7 | I/O |
| 0 | IO_L27N_0 | B5 | I/O |
| 0 | IO_L27P_0 | B6 | I/O |
| 0 | IO_L28N_0 | D6 | I/O |
| 0 | IO_L28P_0 | C6 | I/O |
| 0 | IO_L30N_0/VREF_0 | C5 | VREF |
| 0 | IO_L30P_0 | D5 | I/O |
| 0 | IO_L31N_0 | A2 | I/O |
| 0 | IO_L31P_0 | B2 | I/O |
| 0 | IO_L32N_0/HSWAP | D4 | DUAL |
| 0 | IO_L32P_0 | C4 | I/O |
| 0 | IP | B18 | INPUT |
| 0 | IP | E5 | INPUT |
| 0 | IP_L02N_0 | C16 | INPUT |
| 0 | IP_L02P_0 | D16 | INPUT |
| 0 | IP_L05N_0 | D15 | INPUT |
| 0 | IP_L05P_0 | C15 | INPUT |
| 0 | IP_L08N_0 | E14 | INPUT |
| 0 | IP_L08P_0 | E15 | INPUT |
| 0 | IP_L11N_0 | G14 | INPUT |
| 0 | IP_L11P_0 | G13 | INPUT |
| 0 | IP_L14N_0 | B11 | INPUT |
| 0 | IP_L14P_0 | B12 | INPUT |
| 0 | IP_L17N_0/GCLK9 | G10 | GCLK |

*Table 152:* **FG400 Package Pinout *(Cont'd)***

| Bank | XC3S1200E XC3S1600E Pin Name | FG400 Ball | Type |
|---|---|---|---|
| 0 | IP_L17P_0/GCLK8 | H10 | GCLK |
| 0 | IP_L20N_0 | G9 | INPUT |
| 0 | IP_L20P_0 | G8 | INPUT |
| 0 | IP_L23N_0 | C8 | INPUT |
| 0 | IP_L23P_0 | D8 | INPUT |
| 0 | IP_L26N_0 | E6 | INPUT |
| 0 | IP_L26P_0 | E7 | INPUT |
| 0 | IP_L29N_0 | A4 | INPUT |
| 0 | IP_L29P_0 | A5 | INPUT |
| 0 | VCCO_0 | B4 | VCCO |
| 0 | VCCO_0 | B10 | VCCO |
| 0 | VCCO_0 | B16 | VCCO |
| 0 | VCCO_0 | D7 | VCCO |
| 0 | VCCO_0 | D13 | VCCO |
| 0 | VCCO_0 | F10 | VCCO |
| 1 | IO_L01N_1/A15 | U18 | DUAL |
| 1 | IO_L01P_1/A16 | U17 | DUAL |
| 1 | IO_L02N_1/A13 | T18 | DUAL |
| 1 | IO_L02P_1/A14 | T17 | DUAL |
| 1 | IO_L03N_1/VREF_1 | V19 | VREF |
| 1 | IO_L03P_1 | U19 | I/O |
| 1 | IO_L04N_1 | W20 | I/O |
| 1 | IO_L04P_1 | V20 | I/O |
| 1 | IO_L05N_1 | R18 | I/O |
| 1 | IO_L05P_1 | R17 | I/O |
| 1 | IO_L06N_1 | T20 | I/O |
| 1 | IO_L06P_1 | U20 | I/O |
| 1 | IO_L07N_1 | P18 | I/O |
| 1 | IO_L07P_1 | P17 | I/O |
| 1 | IO_L08N_1/VREF_1 | P20 | VREF |
| 1 | IO_L08P_1 | R20 | I/O |
| 1 | IO_L09N_1 | P16 | I/O |
| 1 | IO_L09P_1 | N16 | I/O |
| 1 | IO_L10N_1 | N19 | I/O |
| 1 | IO_L10P_1 | N18 | I/O |
| 1 | IO_L11N_1 | N15 | I/O |
| 1 | IO_L11P_1 | M15 | I/O |
| 1 | IO_L12N_1/A11 | M18 | DUAL |
| 1 | IO_L12P_1/A12 | M17 | DUAL |
| 1 | IO_L13N_1/VREF_1 | L19 | VREF |
| 1 | IO_L13P_1 | M19 | I/O |
| 1 | IO_L14N_1/A9/RHCLK1 | L16 | RHCLK/ DUAL |

*Table 152:* **FG400 Package Pinout *(Cont'd)***

| Bank | XC3S1200E XC3S1600E Pin Name | FG400 Ball | Type |
|---|---|---|---|
| 1 | IO_L14P_1/A10/RHCLK0 | M16 | RHCLK/ DUAL |
| 1 | IO_L15N_1/A7/RHCLK3/ TRDY1 | L14 | RHCLK/ DUAL |
| 1 | IO_L15P_1/A8/RHCLK2 | L15 | RHCLK/ DUAL |
| 1 | IO_L16N_1/A5/RHCLK5 | K14 | RHCLK/ DUAL |
| 1 | IO_L16P_1/A6/RHCLK4/ IRDY1 | K13 | RHCLK/ DUAL |
| 1 | IO_L17N_1/A3/RHCLK7 | J20 | RHCLK/ DUAL |
| 1 | IO_L17P_1/A4/RHCLK6 | K20 | RHCLK/ DUAL |
| 1 | IO_L18N_1/A1 | K16 | DUAL |
| 1 | IO_L18P_1/A2 | J16 | DUAL |
| 1 | IO_L19N_1/A0 | J13 | DUAL |
| 1 | IO_L19P_1 | J14 | I/O |
| 1 | IO_L20N_1 | J17 | I/O |
| 1 | IO_L20P_1 | J18 | I/O |
| 1 | IO_L21N_1 | H19 | I/O |
| 1 | IO_L21P_1 | J19 | I/O |
| 1 | IO_L22N_1 | H15 | I/O |
| 1 | IO_L22P_1 | H16 | I/O |
| 1 | IO_L23N_1 | H18 | I/O |
| 1 | IO_L23P_1 | H17 | I/O |
| 1 | IO_L24N_1/VREF_1 | H20 | VREF |
| 1 | IO_L24P_1 | G20 | I/O |
| 1 | IO_L25N_1 | G16 | I/O |
| 1 | IO_L25P_1 | F16 | I/O |
| 1 | IO_L26N_1 | F19 | I/O |
| 1 | IO_L26P_1 | F20 | I/O |
| 1 | IO_L27N_1 | F18 | I/O |
| 1 | IO_L27P_1 | F17 | I/O |
| 1 | IO_L28N_1 | D20 | I/O |
| 1 | IO_L28P_1 | E20 | I/O |
| 1 | IO_L29N_1/LDC0 | D18 | DUAL |
| 1 | IO_L29P_1/HDC | E18 | DUAL |
| 1 | IO_L30N_1/LDC2 | C19 | DUAL |
| 1 | IO_L30P_1/LDC1 | C20 | DUAL |
| 1 | IP | B20 | INPUT |
| 1 | IP | G15 | INPUT |
| 1 | IP | G18 | INPUT |
| 1 | IP | H14 | INPUT |
| 1 | IP | J15 | INPUT |