Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	3688
Number of Logic Elements/Cells	33192
Total RAM Bits	663552
Number of I/O	304
Number of Gates	1600000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	400-BGA
Supplier Device Package	400-FBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s1600e-5fg400c

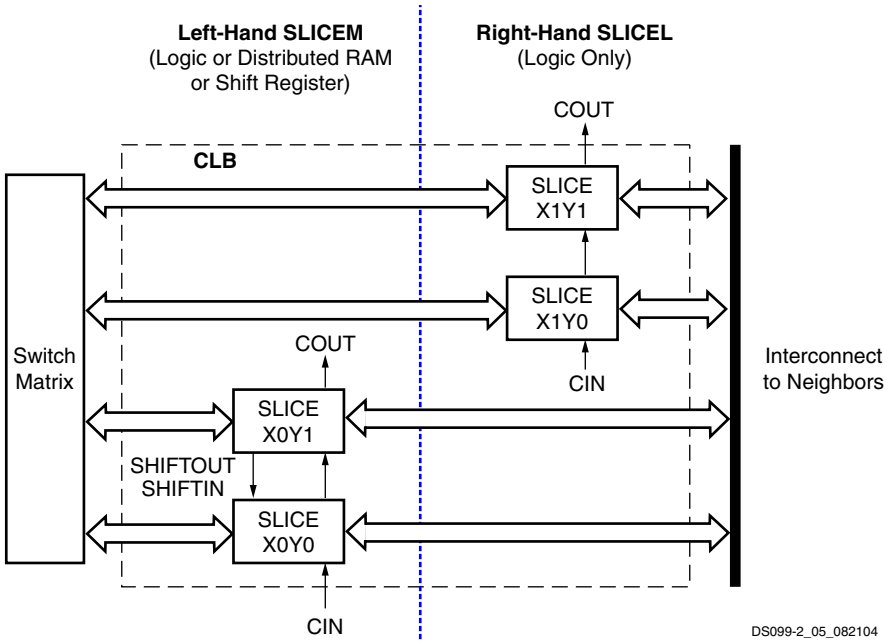

Figure 16: **Arrangement of Slices within the CLB**

Slice Location Designations

The Xilinx development software designates the location of a slice according to its X and Y coordinates, starting in the bottom left corner, as shown in Figure 14. The letter 'X' followed by a number identifies columns of slices, incrementing from the left side of the die to the right. The letter 'Y' followed by a number identifies the position of each slice in a pair as well as indicating the CLB row, incrementing from the bottom of the die. Figure 16 shows the CLB located in the lower left-hand corner of the die. The SLICEM always has an even 'X' number, and the SLICEL always has an odd 'X' number.

Slice Overview

A slice includes two LUT function generators and two storage elements, along with additional logic, as shown in Figure 17.

Both SLICEM and SLICEL have the following elements in common to provide logic, arithmetic, and ROM functions:

- Two 4-input LUT function generators, F and G
- Two storage elements
- Two wide-function multiplexers, F5MUX and FiMUX
- Carry and arithmetic logic

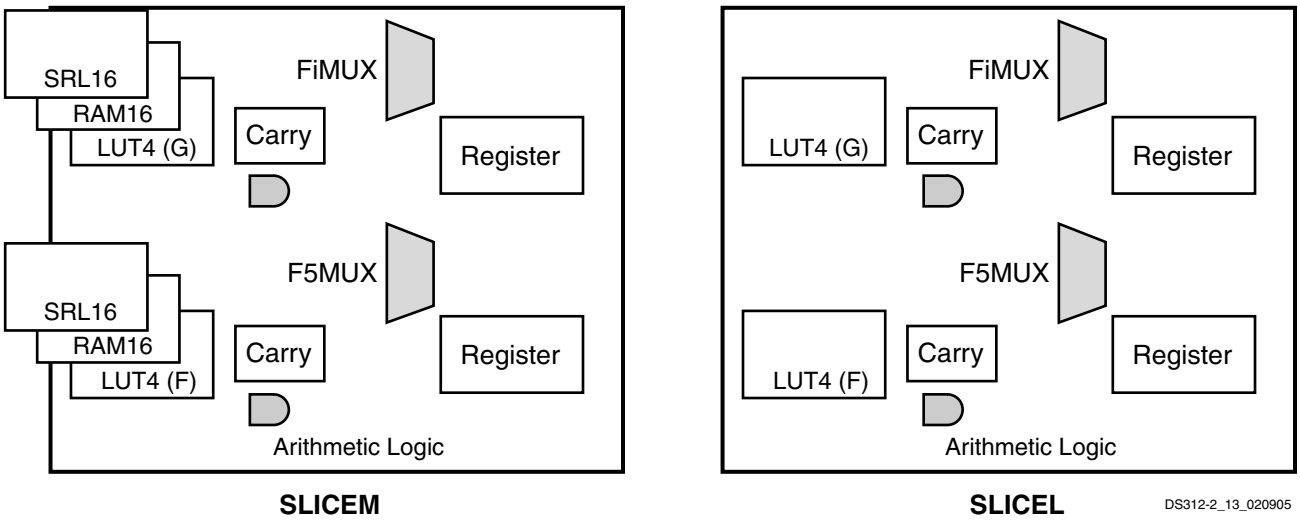

Figure 17: **Resources in a Slice**

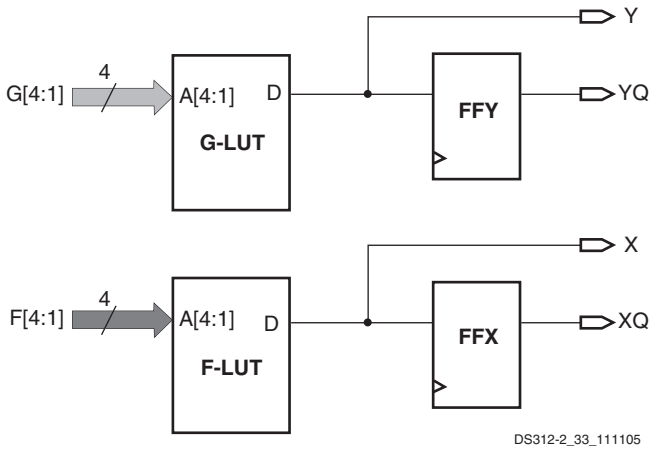

Figure 18: **LUT Resources in a Slice**

Wide Multiplexers

For additional information, refer to the “Using Dedicated Multiplexers” chapter in UG331.

Wide-function multiplexers effectively combine LUTs in order to permit more complex logic operations. Each slice has two of these multiplexers with F5MUX in the bottom portion of the slice and FiMUX in the top portion. The F5MUX multiplexes the two LUTs in a slice. The FiMUX multiplexes two CLB inputs which connect directly to the F5MUX and FiMUX results from the same slice or from other slices. See Figure 19.

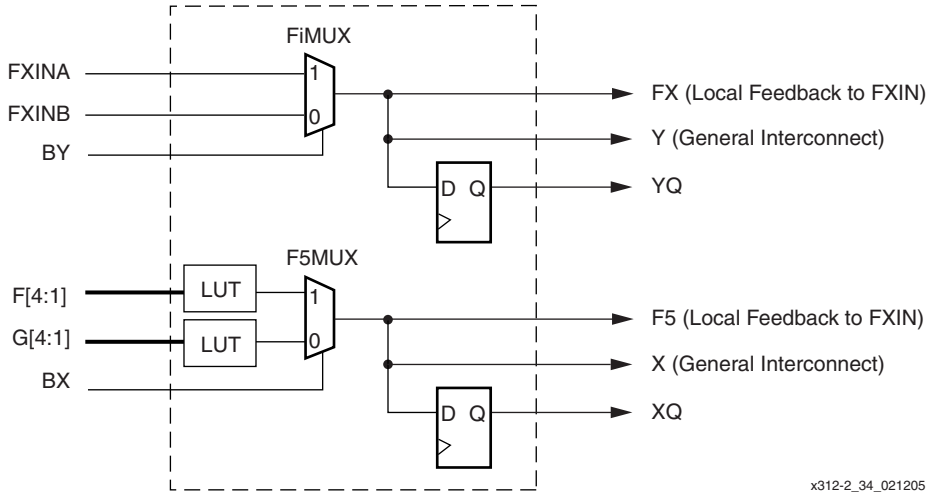

Figure 19: **Dedicated Multiplexers in Spartan-3E CLB**

Depending on the slice, FiMUX takes on the name F6MUX, F7MUX, or F8MUX. The designation indicates the number of inputs possible without restriction on the function. For example, an F7MUX can generate any function of seven inputs. Figure 20 shows the names of the multiplexers in each position in the Spartan-3E CLB. The figure also includes the direct connections within the CLB, along with the F7MUX connection to the CLB below.

Each mux can create logic functions of more inputs than indicated by its name. The F5MUX, for example, can generate any function of five inputs, with four inputs duplicated to two LUTs and the fifth input controlling the mux. Because each LUT can implement independent 2:1 muxes, the F5MUX can combine them to create a 4:1 mux, which is a six-input function. If the two LUTs have completely independent sets of inputs, some functions of all nine inputs can be implemented. Table 11 shows the connections for each multiplexer and the number of inputs possible for different types of functions.

The connections for the bottom-edge BUFGMUX elements are similar to the top-edge connections (see Figure 46).

On the left and right edges, only two clock inputs feed each pair of BUFGMUX elements.

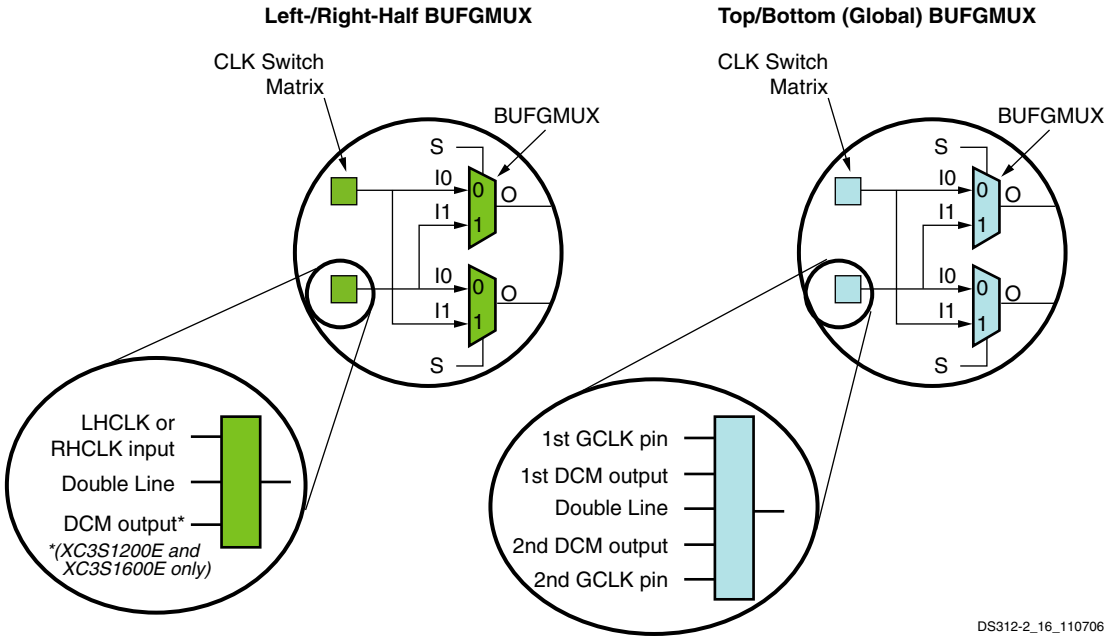

Figure 46: **Clock Switch Matrix to BUFGMUX Pair Connectivity**

Quadrant Clock Routing

The clock routing within the FPGA is quadrant-based, as shown in Figure 45. Each clock quadrant supports eight total clock signals, labeled 'A' through 'H' in Table 41 and Figure 47. The clock source for an individual clock line originates either from a global BUFGMUX element along the top and bottom edges or from a BUFGMUX element along the associated edge, as shown in Figure 47. The clock lines feed the synchronous resource elements (CLBs, IOBs, block RAM, multipliers, and DCMs) within the quadrant.

The four quadrants of the device are:

- Top Right (TR)
- Bottom Right (BR)
- Bottom Left (BL)
- Top Left (TL)

Note that the quadrant clock notation (TR, BR, BL, TL) is separate from that used for similar IOB placement constraints.

To estimate the quadrant location for a particular I/O, see the footprint diagrams in Module 4, Pinout Descriptions. For exact quadrant locations, use the floorplanning tool. In the QFP packages (VQ100, TQ144 and PQ208) the quadrant borders fall in the middle of each side of the package, at a GND pin. The clock inputs fall on the quadrant boundaries, as indicated in Table 42.

Table 42: **QFP Package Clock Quadrant Locations**

Clock Pins	Quadrant
GCLK[3:0]	BR
GCLK[7:4]	TR
GCLK[11:8]	TL
GCLK[15:12]	BL
RHCLK[3:0]	BR
RHCLK[7:4]	TR
LHCLK[3:0]	TL
LHCLK[7:4]	BL

In a few cases, a dedicated input is physically in one quadrant of the device but connects to a different clock quadrant:

- FT256, H16 is in clock quadrant BR
- FG320, K2 is in clock quadrant BL
- FG400, L8 is in clock quadrant TL and the I/O at N11 is in clock quadrant BL
- FG484, M2 is in clock quadrant TL and L15 is in clock quadrant BR

Table 46: **Pin Behavior during Configuration *(Cont'd)***

Pin Name	Master Serial	SPI (Serial Flash)	BPI (Parallel NOR Flash)	JTAG	Slave Parallel	Slave Serial	I/O Bank[3]
D0/DIN	DIN	DIN	D0		D0	DIN	2
RDWR_B			RDWR_B		RDWR_B		2
A23			A23				2
A22			A22				2
A21			A21				2
A20			A20				2
A19/VS2		VS2	A19				2
A18/VS1		VS1	A18				2
A17/VS0		VS0	A17				2
A16			A16				1
A15			A15				1
A14			A14				1
A13			A13				1
A12			A12				1
A11			A11				1
A10			A10				1
A9			A9				1
A8			A8				1
A7			A7				1
A6			A6				1
A5			A5				1
A4			A4				1
A3			A3				1
A2			A2				1
A1			A1				1
A0			A0				1
LDC0			LDC0				1
LDC1			LDC1				1
LDC2			LDC2				1
HDC			HDC				1

Notes:
1. Gray shaded cells represent pins that are in a high-impedance state (Hi-Z, floating) during configuration. These pins have an optional internal pull-up resistor to their respective V_{CCO} supply pin that is active throughout configuration if the HSWAP input is Low.
2. Yellow shaded cells represent pins with an internal pull-up resistor to its respective voltage supply rail that is active during configuration, regardless of the HSWAP pin.
3. Note that dual-purpose outputs are supplied by V_{CCO}, and configuration inputs are supplied by V_{CCAUX}.

The HSWAP pin itself has a pull-up resistor enabled during configuration. However, the VCCO_0 supply voltage must be applied before the pull-up resistor becomes active. If the VCCO_0 supply ramps after the VCCO_2 power supply, do not let HSWAP float; tie HSWAP to the desired logic level externally.

Spartan-3E FPGAs have only six dedicated configuration pins, including the DONE and PROG_B pins, and the four JTAG boundary-scan pins: TDI, TDO, TMS, and TCK. All other configuration pins are dual-purpose I/O pins and are available to the FPGA application after the DONE pin goes High. See Start-Up for additional information.

Table 47 shows the default I/O standard setting for the various configuration pins during the configuration process. The configuration interface is designed primarily for 2.5V operation when the VCCO_2 (and VCCO_1 in BPI mode) connects to 2.5V.

Table 47: **Default I/O Standard Setting During Configuration (VCCO_2 = 2.5V)**

Pin(s)	I/O Standard	Output Drive	Slew Rate
All, including CCLK	LVCMOS25	8 mA	Slow

Voltage Compatibility

The PROM's V_{CCINT} supply must be either 3.3V for the serial XCFxxS Platform Flash PROMs or 1.8V for the serial/parallel XCFxxP PROMs.

Ⓥ The FPGA's VCCO_2 supply input and the Platform Flash PROM's V_{CCO} supply input must be the same voltage, ideally +2.5V. Both devices also support 1.8V and 3.3V interfaces but the FPGA's PROG_B and DONE pins require special attention as they are powered by the FPGA's V_{CCAUX} supply, nominally 2.5V. See application note XAPP453: *The 3.3V Configuration of Spartan-3 FPGAs* for additional information.

Supported Platform Flash PROMs

Table 51 shows the smallest available Platform Flash PROM to program one Spartan-3E FPGA. A multiple-FPGA daisy-chain application requires a Platform Flash PROM large enough to contain the sum of the various FPGA file sizes.

Table 51: **Number of Bits to Program a Spartan-3E FPGA and Smallest Platform Flash PROM**

Spartan-3E FPGA	Number of Configuration Bits	Smallest Available Platform Flash
XC3S100E	581,344	XCF01S
XC3S250E	1,353,728	XCF02S
XC3S500E	2,270,208	XCF04S
XC3S1200E	3,841,184	XCF04S
XC3S1600E	5,969,696	XCF08P or 2 x XCF04S

The XC3S1600E requires an 8 Mbit PROM. Two solutions are possible: either a single 8 Mbit XCF08P parallel/serial PROM or two 4 Mbit XCF04S serial PROMs cascaded. The two XCF04S PROMs use a 3.3V V_{CCINT} supply while the XCF08P requires a 1.8V V_{CCINT} supply. If the board does not already have a 1.8V supply available, the two cascaded XCF04S PROM solution is recommended.

CCLK Frequency

In Master Serial mode, the FPGA's internal oscillator generates the configuration clock frequency. The FPGA provides this clock on its CCLK output pin, driving the PROM's CLK input pin. The FPGA starts configuration at its lowest frequency and increases its frequency for the remainder of the configuration process if so specified in the configuration bitstream. The maximum frequency is specified using the ***ConfigRate*** bitstream generator option. Table 52 shows the maximum ***ConfigRate*** settings, approximately equal to MHz, for various Platform Flash devices and I/O voltages. For the serial XCFxxS PROMs, the maximum frequency also depends on the interface voltage.

Table 52: **Maximum ConfigRate Settings for Platform Flash**

Platform Flash Part Number	I/O Voltage (VCCO_2, V_{CCO})	Maximum *ConfigRate* Setting
XCF01S XCF02S XCF04S	3.3V or 2.5V	25
	1.8V	12
XCF08P XCF16P XCF32P	3.3V, 2.5V, or 1.8V	25

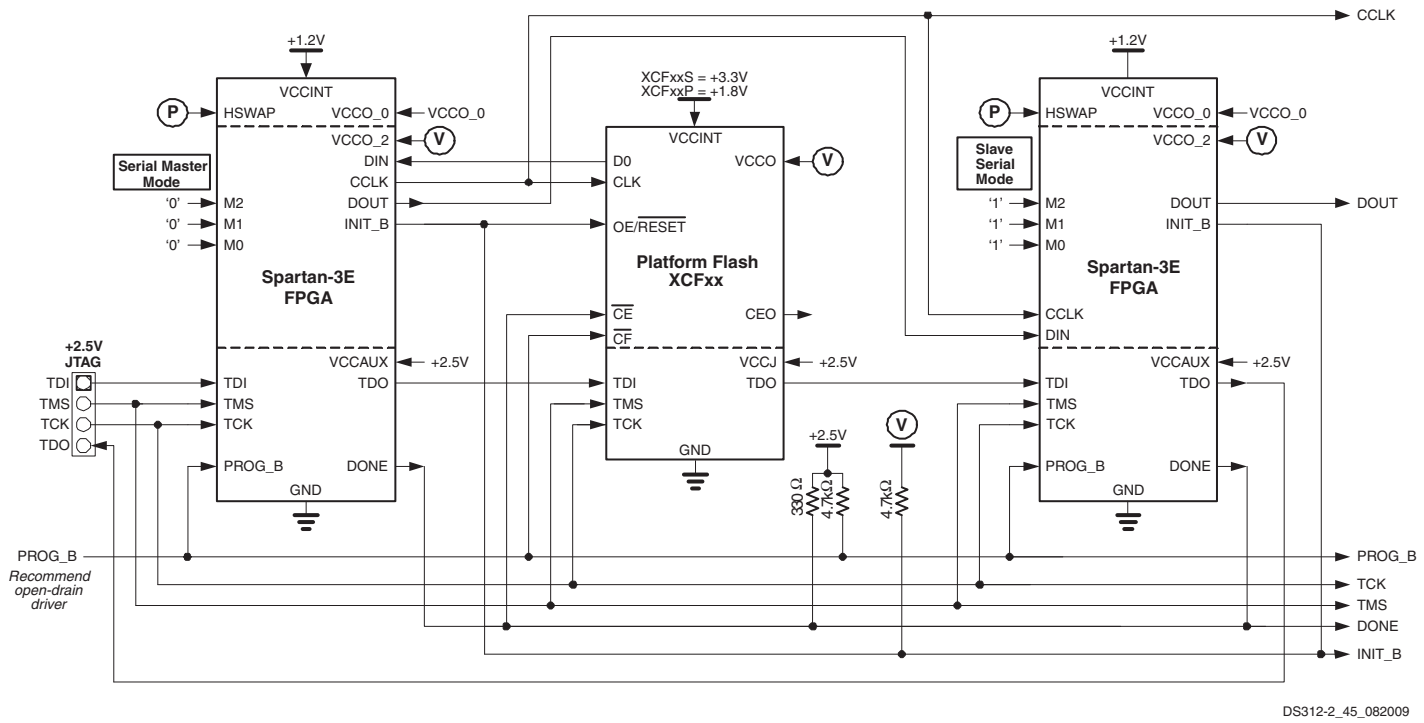

Figure 52: **Daisy-Chaining from Master Serial Mode**

Daisy-Chaining

If the application requires multiple FPGAs with different configurations, then configure the FPGAs using a daisy chain, as shown in Figure 52. Use Master Serial mode (M[2:0] = <0:0:0>) for the FPGA connected to the Platform Flash PROM and Slave Serial mode (M[2:0] = <1:1:1>) for all other FPGAs in the daisy-chain. After the master FPGA—the FPGA on the left in the diagram—finishes loading its configuration data from the Platform Flash, the master device supplies data using its DOUT output pin to the next device in the daisy-chain, on the falling CCLK edge.

JTAG Interface

Both the Spartan-3E FPGA and the Platform Flash PROM have a four-wire IEEE 1149.1/1532 JTAG port. Both devices share the TCK clock input and the TMS mode select input. The devices may connect in either order on the JTAG chain with the TDO output of one device feeding the TDI input of the following device in the chain. The TDO output of the last device in the JTAG chain drives the JTAG connector.

The JTAG interface on Spartan-3E FPGAs is powered by the 2.5V V_{CCAUX} supply. Consequently, the PROM's V_{CCJ} supply input must also be 2.5V. To create a 3.3V JTAG interface, please refer to application note XAPP453: *The 3.3V Configuration of Spartan-3 FPGAs* for additional information.

In-System Programming Support

Both the FPGA and the Platform Flash PROM are in-system programmable via the JTAG chain. Download support is provided by the Xilinx iMPACT programming software and the associated Xilinx Parallel Cable IV or Platform Cable USB programming cables.

Storing Additional User Data in Platform Flash

After configuration, the FPGA application can continue to use the Master Serial interface pins to communicate with the Platform Flash PROM. If desired, use a larger Platform Flash PROM to hold additional non-volatile application data, such as MicroBlaze processor code, or other user data such as serial numbers and Ethernet MAC IDs. The FPGA first configures from Platform Flash PROM. Then using FPGA logic after configuration, the FPGA copies MicroBlaze code from Platform Flash into external DDR SDRAM for code execution.

See XAPP694: *Reading User Data from Configuration PROMs* and XAPP482: *MicroBlaze Platform Flash/PROM Boot Loader and User Data Storage* for specific details on how to implement such an interface.

Figure 57, page 82 demonstrates how to configure multiple FPGAs with different configurations, all stored in a single SPI Flash. The diagram uses standard SPI Flash memories but the same general technique applies for Atmel DataFlash.

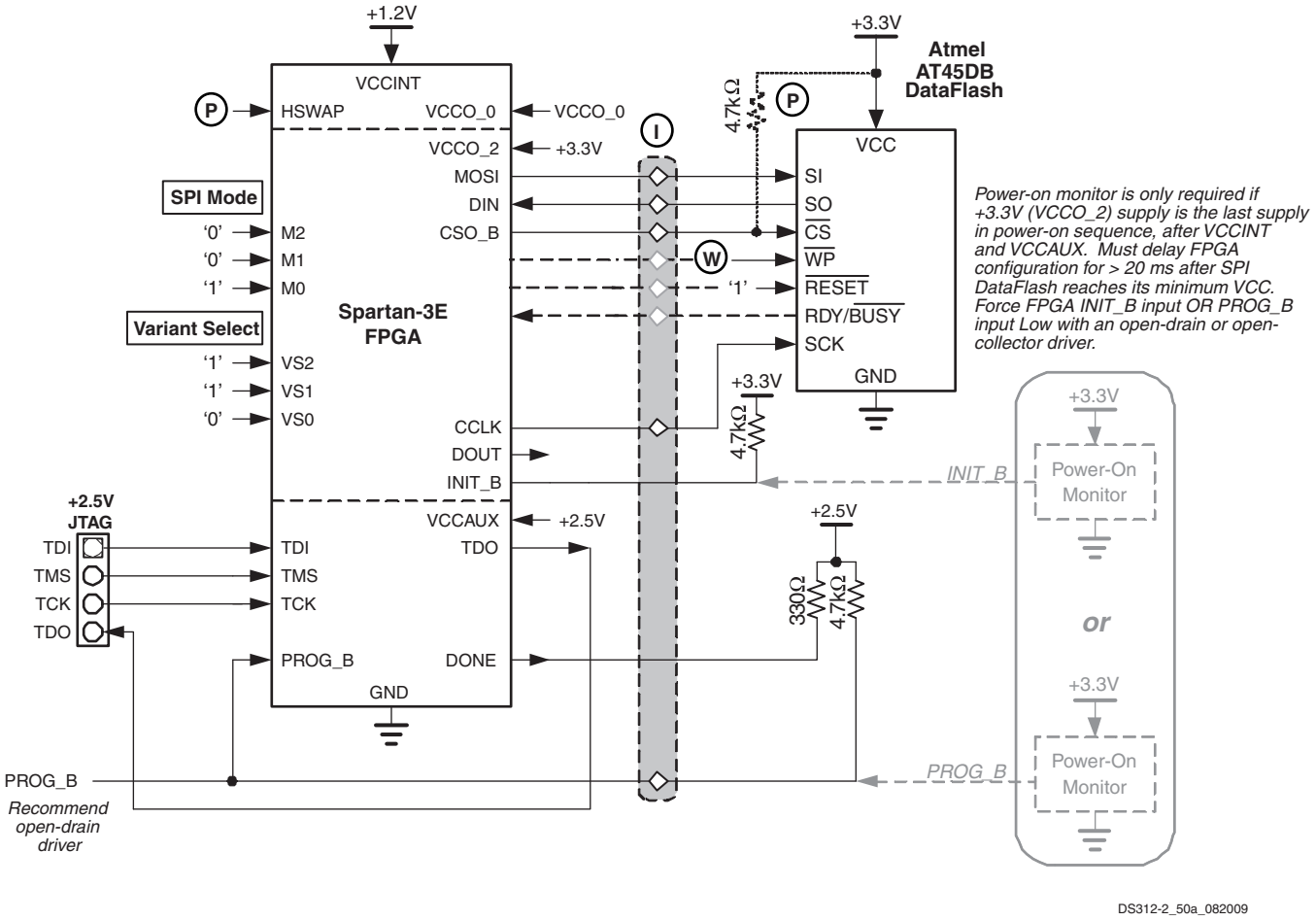

Figure 54: **Atmel SPI-based DataFlash Configuration Interface**

(W) Table 54 shows the connections between the SPI Flash PROM and the FPGA's SPI configuration interface. Each SPI Flash PROM vendor uses slightly different signal naming. The SPI Flash PROM's write protect and hold controls are not used by the FPGA during configuration. However, the $\overline{\text{HOLD}}$ pin must be High during the configuration process. The PROM's write protect input must be High in order to write or program the Flash memory.

Table 54: **Example SPI Flash PROM Connections and Pin Naming**

SPI Flash Pin	FPGA Connection	STMicro	NexFlash	Silicon Storage Technology	Atmel DataFlash
DATA_IN	MOSI	D	DI	SI	SI
DATA_OUT	DIN	Q	DO	SO	SO
$\overline{\text{SELECT}}$	CSO_B	$\overline{\text{S}}$	$\overline{\text{CS}}$	CE#	$\overline{\text{CS}}$
CLOCK	CCLK	C	CLK	SCK	SCK
$\overline{\text{WR\_PROTECT}}$ (W)	Not required for FPGA configuration. Must be High to program SPI Flash. Optional connection to FPGA user I/O after configuration.	$\overline{\text{W}}$	$\overline{\text{WP}}$	WP#	$\overline{\text{WP}}$
$\overline{\text{HOLD}}$ (see Figure 53)	Not required for FPGA configuration but must be High during configuration. Optional connection to FPGA user I/O after configuration. Not applicable to Atmel DataFlash.	$\overline{\text{HOLD}}$	$\overline{\text{HOLD}}$	HOLD#	N/A
$\overline{\text{RESET}}$ (see Figure 54)	Only applicable to Atmel DataFlash. Not required for FPGA configuration but must be High during configuration. Optional connection to FPGA user I/O after configuration. Do not connect to FPGA's PROG_B as this will prevent direct programming of the DataFlash.	N/A	N/A	N/A	$\overline{\text{RESET}}$
RDY/$\overline{\text{BUSY}}$ (see Figure 54)	Only applicable to Atmel DataFlash and only available on certain packages. Not required for FPGA configuration. Output from DataFlash PROM. Optional connection to FPGA user I/O after configuration.	N/A	N/A	N/A	RDY/$\overline{\text{BUSY}}$

The mode select pins, M[2:0], and the variant select pins, VS[2:0] are sampled when the FPGA's INIT_B output goes High and must be at defined logic levels during this time. After configuration, when the FPGA's DONE output goes High, these pins are all available as full-featured user-I/O pins.

(P) Similarly, the FPGA's HSWAP pin must be Low to enable pull-up resistors on all user-I/O pins or High to disable the pull-up resistors. The HSWAP control must remain at a constant logic level throughout FPGA configuration. After configuration, when the FPGA's DONE output goes High, the HSWAP pin is available as full-featured user-I/O pin and is powered by the VCCO_0 supply.

In a single-FPGA application, the FPGA's DOUT pin is not used but is actively driving during the configuration process.

Table 55: **Serial Peripheral Interface (SPI) Connections**

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
HSWAP (P)	Input	**User I/O Pull-Up Control**. When Low during configuration, enables pull-up resistors in all I/O pins to respective I/O bank V_{CCO} input. 0: Pull-ups during configuration 1: No pull-ups	Drive at valid logic level throughout configuration.	User I/O
M[2:0]	Input	**Mode Select**. Selects the FPGA configuration mode. See Design Considerations for the HSWAP, M[2:0], and VS[2:0] Pins.	M2 = 0, M1 = 0, M0 = 1. Sampled when INIT_B goes High.	User I/O

Table 55: **Serial Peripheral Interface (SPI) Connections *(Cont'd)***

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
VS[2:0] Ⓢ	Input	**Variant Select**. Instructs the FPGA how to communicate with the attached SPI Flash PROM. See Design Considerations for the HSWAP, M[2:0], and VS[2:0] Pins.	Must be at the logic levels shown in Table 53. Sampled when INIT_B goes High.	User I/O
MOSI	Output	**Serial Data Output**.	FPGA sends SPI Flash memory read commands and starting address to the PROM's serial data input.	User I/O
DIN	Input	**Serial Data Input**.	FPGA receives serial data from PROM's serial data output.	User I/O
CSO_B	Output	**Chip Select Output**. Active Low.	Connects to the SPI Flash PROM's chip-select input. If HSWAP = 1, connect this signal to a 4.7 kΩ pull-up resistor to 3.3V.	Drive CSO_B High after configuration to disable the SPI Flash and reclaim the MOSI, DIN, and CCLK pins. Optionally, re-use this pin and MOSI, DIN, and CCLK to continue communicating with SPI Flash.
CCLK	Output	**Configuration Clock**. Generated by FPGA internal oscillator. Frequency controlled by ***ConfigRate*** bitstream generator option. If CCLK PCB trace is long or has multiple connections, terminate this output to maintain signal integrity. See CCLK Design Considerations.	Drives PROM's clock input.	User I/O
DOUT	Output	**Serial Data Output**.	Actively drives. Not used in single-FPGA designs. In a daisy-chain configuration, this pin connects to DIN input of the next FPGA in the chain.	User I/O
INIT_B	Open-drain bidirectional I/O	**Initialization Indicator**. Active Low. Goes Low at start of configuration during Initialization memory clearing process. Released at end of memory clearing, when mode select pins are sampled. In daisy-chain applications, this signal requires an external 4.7 kΩ pull-up resistor to VCCO_2.	Active during configuration. If SPI Flash PROM requires > 2 ms to awake after powering on, hold INIT_B Low until PROM is ready. If CRC error detected during configuration, FPGA drives INIT_B Low.	User I/O. If unused in the application, drive INIT_B High.
DONE	Open-drain bidirectional I/O	**FPGA Configuration Done**. Low during configuration. Goes High when FPGA successfully completes configuration. Requires external 330 Ω pull-up resistor to 2.5V.	Low indicates that the FPGA is not yet configured.	Pulled High via external pull-up. When High, indicates that the FPGA successfully configured.
PROG_B	Input	**Program FPGA**. Active Low. When asserted Low for 500 ns or longer, forces the FPGA to restart its configuration process by clearing configuration memory and resetting the DONE and INIT_B pins once PROG_B returns High. Recommend external 4.7 kΩ pull-up resistor to 2.5V. Internal pull-up value may be weaker (see Table 78). If driving externally with a 3.3V output, use an open-drain or open-collector driver or use a current limiting series resistor.	Must be High to allow configuration to start.	Drive PROG_B Low and release to reprogram FPGA. Hold PROG_B to force FPGA I/O pins into Hi-Z, allowing direct programming access to SPI Flash PROM pins.

Voltage Compatibility

Available SPI Flash PROMs use a single 3.3V supply voltage. All of the FPGA's SPI Flash interface signals are within I/O Bank 2. Consequently, the FPGA's VCCO_2 supply voltage must also be 3.3V to match the SPI Flash PROM.

Power-On Precautions if 3.3V Supply is Last in Sequence

Spartan-3E FPGAs have a built-in power-on reset (POR) circuit, as shown in Figure 66, page 102. The FPGA waits for its three power supplies — V_{CCINT}, V_{CCAUX}, and V_{CCO} to I/O Bank 2 (VCCO_2) — to reach their respective power-on thresholds before beginning the configuration process.

The SPI Flash PROM is powered by the same voltage supply feeding the FPGA's VCCO_2 voltage input, typically 3.3V. SPI Flash PROMs specify that they cannot be accessed until their V_{CC} supply reaches its minimum data sheet voltage, followed by an additional delay. For some devices, this additional delay is as little as 10 µs as shown in Table 56. For other vendors, this delay is as much as 20 ms.

Table 56: **Example Minimum Power-On to Select Times for Various SPI Flash PROMs**

Vendor	SPI Flash PROM Part Number	Data Sheet Minimum Time from V_{CC} min to Select = Low		
		Symbol	Value	Units
STMicroelectronics	M25Pxx	T_{VSL}	10	µs
Spansion	S25FLxxxA	t_{PU}	10	ms
NexFlash	NX25xx	T_{VSL}	10	µs
Macronix	MX25Lxxxx	t_{VSL}	10	µs
Silicon Storage Technology	SST25LFxx	$T_{PU-READ}$	10	µs
Programmable Microelectronics Corporation	Pm25LVxxx	T_{VCS}	50	µs
Atmel Corporation	AT45DBxxxD	t_{VCSL}	30	µs
	AT45DBxxxB		20	ms

In many systems, the 3.3V supply feeding the FPGA's VCCO_2 input is valid before the FPGA's other V_{CCINT} and V_{CCAUX} supplies, and consequently, there is no issue. However, if the 3.3V supply feeding the FPGA's VCCO_2 supply is last in the sequence, a potential race occurs between the FPGA and the SPI Flash PROM, as shown in Figure 55.

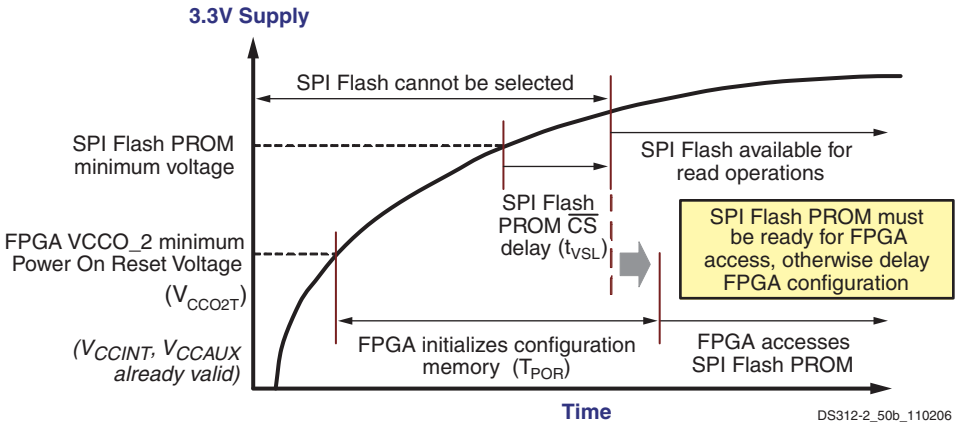

Figure 55: **SPI Flash PROM/FPGA Power-On Timing if 3.3V Supply is Last in Power-On Sequence**

If the FPGA's V_{CCINT} and V_{CCAUX} supplies are already valid, then the FPGA waits for VCCO_2 to reach its minimum threshold voltage before starting configuration. This threshold voltage is labeled as V_{CCO2T} in Table 74 of Module 3 and ranges from approximately 0.4V to 1.0V, substantially lower than the SPI Flash PROM's minimum voltage. Once all three FPGA supplies reach their respective Power On Reset (POR) thresholds, the FPGA starts the configuration process and begins initializing its internal configuration memory. Initialization requires approximately 1 ms (T_{POR}, minimum in Table 111 of Module 3, after which the FPGA de-asserts INIT_B, selects the SPI Flash PROM, and starts sending the appropriate read command. The SPI Flash PROM must be ready for

Table 65: **Slave Parallel Mode Connections *(Cont'd)***

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
INIT_B	Open-drain bidirectional I/O	**Initialization Indicator**. Active Low. Goes Low at the start of configuration during the Initialization memory clearing process. Released at the end of memory clearing, when mode select pins are sampled. In daisy-chain applications, this signal requires an external 4.7 kΩ pull-up resistor to VCCO_2.	Active during configuration. If CRC error detected during configuration, FPGA drives INIT_B Low.	User I/O. If unused in the application, drive INIT_B High.
DONE	Open-drain bidirectional I/O	**FPGA Configuration Done**. Low during configuration. Goes High when FPGA successfully completes configuration. Requires external 330 Ω pull-up resistor to 2.5V.	Low indicates that the FPGA is not yet configured.	Pulled High via external pull-up. When High, indicates that the FPGA successfully configured.
PROG_B	Input	**Program FPGA**. Active Low. When asserted Low for 500 ns or longer, forces the FPGA to restart its configuration process by clearing configuration memory and resetting the DONE and INIT_B pins once PROG_B returns High. Recommend external 4.7 kΩ pull-up resistor to 2.5V. Internal pull-up value may be weaker (see Table 78). If driving externally with a 3.3V output, use an open-drain or open-collector driver or use a current limiting series resistor.	Must be High to allow configuration to start.	Drive PROG_B Low and release to reprogram FPGA.

Voltage Compatibility

Ⓥ Most Slave Parallel interface signals are within the FPGA's I/O Bank 2, supplied by the VCCO_2 supply input. The VCCO_2 voltage can be 1.8V, 2.5V, or 3.3V to match the requirements of the external host, ideally 2.5V. Using 1.8V or 3.3V requires additional design considerations as the DONE and PROG_B pins are powered by the FPGA's 2.5V V_{CCAUX} supply. See XAPP453: *The 3.3V Configuration of Spartan-3 FPGAs* for additional information.

Daisy-Chaining

If the application requires multiple FPGAs with different configurations, then configure the FPGAs using a daisy chain. Use Slave Parallel mode (M[2:0] = <1:1:0>) for all FPGAs in the daisy-chain. The schematic in Figure 62 is optimized for FPGA downloading and does not support the SelectMAP read interface. The FPGA's RDWR_B pin must be Low during configuration.

After the lead FPGA is filled with its configuration data, the lead FPGA enables the next FPGA in the daisy-chain by asserting is chip-select output, CSO_B.

Maximum Bitstream Size for Daisy-Chains

The maximum bitstream length supported by Spartan-3E FPGAs in serial daisy-chains is 4,294,967,264 bits (4 Gbits), roughly equivalent to a daisy-chain with 720 XC3S1600E FPGAs. This is a limit only for serial daisy-chains where configuration data is passed via the FPGA's DOUT pin. There is no such limit for JTAG chains.

Configuration Sequence

For additional information including I/O behavior before and during configuration, refer to the "Sequence of Events" chapter in UG332.

The Spartan-3E configuration process is three-stage process that begins after the FPGA powers on (a POR event) or after the PROG_B input is asserted. Power-On Reset (POR) occurs after the V_{CCINT}, V_{CCAUX}, and the V_{CCO} Bank 2 supplies reach their respective input threshold levels. After either a POR or PROG_B event, the three-stage configuration process begins.

1. The FPGA clears (initializes) the internal configuration memory.
2. Configuration data is loaded into the internal memory.
3. The user-application is activated by a start-up process.

Figure 66 is a generalized block diagram of the Spartan-3E configuration logic, showing the interaction of different device inputs and Bitstream Generator (BitGen) options. A flow diagram for the configuration sequence of the Serial and Parallel modes appears in Figure 66. Figure 67 shows the Boundary-Scan or JTAG configuration sequence.

Initialization

Configuration automatically begins after power-on or after asserting the FPGA PROG_B pin, unless delayed using the FPGA's INIT_B pin. The FPGA holds the open-drain INIT_B signal Low while it clears its internal configuration memory. Externally holding the INIT_B pin Low forces the configuration sequencer to wait until INIT_B again goes High.

The FPGA signals when the memory-clearing phase is complete by releasing the open-drain INIT_B pin, allowing the pin to go High via the external pull-up resistor to VCCO_2.

Loading Configuration Data

After initialization, configuration data is written to the FPGA's internal memory. The FPGA holds the Global Set/Reset (GSR) signal active throughout configuration, holding all FPGA flip-flops in a reset state. The FPGA signals when the entire configuration process completes by releasing the DONE pin, allowing it to go High.

The FPGA configuration sequence can also be initiated by asserting PROG_B. Once released, the FPGA begins clearing its internal configuration memory, and progresses through the remainder of the configuration process.

Bitstream Generator (BitGen) Options

For additional information, refer to the "Configuration Bitstream Generator (BitGen) Settings" chapter in UG332.

Various Spartan-3E FPGA functions are controlled by specific bits in the configuration bitstream image. These values are specified when creating the bitstream image with the Bitstream Generator (BitGen) software.

Table 69 provides a list of all BitGen options for Spartan-3E FPGAs.

Table 69: **Spartan-3E FPGA Bitstream Generator (BitGen) Options**

Option Name	Pins/Function Affected	Values (***default***)	Description
ConfigRate	CCLK, Configuration	***1***, 3, 6, 12, 25, 50	Sets the approximate frequency, in MHz, of the internal oscillator using for Master Serial, SPI, and BPI configuration modes. The internal oscillator powers up at its lowest frequency, and the new setting is loaded as part of the configuration bitstream. The software default value is 1 (~1.5 MHz) starting with ISE 8.1, Service Pack 1.
StartupClk	Configuration, Startup	***Cclk***	***Default.*** The CCLK signal (internally or externally generated) controls the startup sequence when the FPGA transitions from configuration mode to the user mode. See Start-Up.
		UserClk	A clock signal from within the FPGA application controls the startup sequence when the FPGA transitions from configuration mode to the user mode. See Start-Up. The FPGA application supplies the user clock on the CLK pin on the STARTUP_SPARTAN3E primitive.
		Jtag	The JTAG TCK input controls the startup sequence when the FPGA transitions from the configuration mode to the user mode. See Start-Up.
UnusedPin	Unused I/O Pins	***Pulldown***	***Default.*** All unused I/O pins and input-only pins have a pull-down resistor to GND.
		Pullup	All unused I/O pins and input-only pins have a pull-up resistor to the VCCO_# supply for its associated I/O bank.
		Pullnone	All unused I/O pins and input-only pins are left floating (Hi-Z, high-impedance, three-state). Use external pull-up or pull-down resistors or logic to apply a valid signal level.
DONE_cycle	DONE pin, Configuration Startup	1, 2, 3, ***4***, 5, 6	Selects the Configuration Startup phase that activates the FPGA's DONE pin. See Start-Up.
GWE_cycle	All flip-flops, LUT RAMs, and SRL16 shift registers, Block RAM, Configuration Startup	1, 2, 3, 4, 5, ***6***	Selects the Configuration Startup phase that asserts the internal write-enable signal to all flip-flops, LUT RAMs and shift registers (SRL16). It also enables block RAM read and write operations. See Start-Up.
		Done	Waits for the DONE pin input to go High before asserting the internal write-enable signal to all flip-flops, LUT RAMs and shift registers (SRL16). Block RAM read and write operations are enabled at this time.
		Keep	Retains the current GWE_cycle setting for partial reconfiguration applications.
GTS_cycle	All I/O pins, Configuration	1, 2, 3, 4, ***5***, 6	Selects the Configuration Startup phase that releases the internal three-state control, holding all I/O buffers in high-impedance (Hi-Z). Output buffers actively drive, if so configured, after this point. See Start-Up.
		Done	Waits for the DONE pin input to go High before releasing the internal three-state control, holding all I/O buffers in high-impedance (Hi-Z). Output buffers actively drive, if so configured, after this point.
		Keep	Retains the current GTS_cycle setting for partial reconfiguration applications.
LCK_cycle	DCMs, Configuration Startup	***NoWait***	The FPGA does not wait for selected DCMs to lock before completing configuration.
		0, 1, 2, 3, 4, 5, 6	If one or more DCMs in the design have the STARTUP_WAIT attribute set to TRUE, the FPGA waits for such DCMs to acquire their respective input clock and assert their LOCKED output. This setting selects the Configuration Startup phase where the FPGA waits for the DCMs to lock.
DonePin	DONE pin	***Pullup***	Internally connects a pull-up resistor between DONE pin and V_{CCAUX}. An external 330 Ω pull-up resistor to V_{CCAUX} is still recommended.
		Pullnone	No internal pull-up resistor on DONE pin. An external 330 Ω pull-up resistor to V_{CCAUX} is required.

Quiescent Current Requirements

Table 79: **Quiescent Supply Current Characteristics**

Symbol	Description	Device	Typical	Commercial Maximum(1)	Industrial Maximum(1)	Units
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC3S100E	8	27	36	mA
		XC3S250E	15	78	104	mA
		XC3S500E	25	106	145	mA
		XC3S1200E	50	259	324	mA
		XC3S1600E	65	366	457	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC3S100E	0.8	1.0	1.5	mA
		XC3S250E	0.8	1.0	1.5	mA
		XC3S500E	0.8	1.0	1.5	mA
		XC3S1200E	1.5	2.0	2.5	mA
		XC3S1600E	1.5	2.0	2.5	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC3S100E	8	12	13	mA
		XC3S250E	12	22	26	mA
		XC3S500E	18	31	34	mA
		XC3S1200E	35	52	59	mA
		XC3S1600E	45	76	86	mA

Notes:

1. The maximum numbers in this table indicate the minimum current each power rail requires in order for the FPGA to power-on successfully.
2. The numbers in this table are based on the conditions set forth in Table 77.
3. Quiescent supply current is measured with all I/O drivers in a high-impedance state and with all pull-up/pull-down resistors at the I/O pads disabled. Typical values are characterized using typical devices at room temperature (T_J of 25°C at V_{CCINT} = 1.2 V, V_{CCO} = 3.3V, and V_{CCAUX} = 2.5V). The maximum limits are tested for each device at the respective maximum specified junction temperature and at maximum voltage limits with V_{CCINT} = 1.26V, V_{CCO} = 3.465V, and V_{CCAUX} = 2.625V. The FPGA is programmed with a "blank" configuration data file (i.e., a design with no functional elements instantiated). For conditions other than those described above, (e.g., a design including functional elements), measured quiescent current levels may be different than the values in the table. For more accurate estimates for a specific design, use the Xilinx® XPower tools.
4. There are two recommended ways to estimate the total power consumption (quiescent plus dynamic) for a specific design: a) The Spartan-3E XPower Estimator provides quick, approximate, typical estimates, and does not require a netlist of the design. b) XPower Analyzer uses a netlist as input to provide maximum estimates as well as more accurate typical estimates.

Configuration Clock (CCLK) Characteristics

Table 112: **Master Mode CCLK Output Period by *ConfigRate* Option Setting**

Symbol	Description	*ConfigRate* Setting	Temperature Range	Minimum	Maximum	Units
T_{CCLK1}	CCLK clock period by ***ConfigRate*** setting	1 *(power-on value and default value)*	Commercial	570	1,250	ns
			Industrial	485		ns
T_{CCLK3}		3	Commercial	285	625	ns
			Industrial	242		ns
T_{CCLK6}		6	Commercial	142	313	ns
			Industrial	121		ns
T_{CCLK12}		12	Commercial	71.2	157	ns
			Industrial	60.6		ns
T_{CCLK25}		25	Commercial	35.5	78.2	ns
			Industrial	30.3		ns
T_{CCLK50}		50	Commercial	17.8	39.1	ns
			Industrial	15.1		ns

Notes:

1. Set the ***ConfigRate*** option value when generating a configuration bitstream. See Bitstream Generator (BitGen) Options in Module 2.

Table 113: **Master Mode CCLK Output Frequency by *ConfigRate* Option Setting**

Symbol	Description	*ConfigRate* Setting	Temperature Range	Minimum	Maximum	Units
F_{CCLK1}	Equivalent CCLK clock frequency by ***ConfigRate*** setting	1 *(power-on value and default value)*	Commercial	0.8	1.8	MHz
			Industrial		2.1	MHz
F_{CCLK3}		3	Commercial	1.6	3.6	MHz
			Industrial		4.2	MHz
F_{CCLK6}		6	Commercial	3.2	7.1	MHz
			Industrial		8.3	MHz
F_{CCLK12}		12	Commercial	6.4	14.1	MHz
			Industrial		16.5	MHz
F_{CCLK25}		25	Commercial	12.8	28.1	MHz
			Industrial		33.0	MHz
F_{CCLK50}		50	Commercial	25.6	56.2	MHz
			Industrial		66.0	MHz

Table 114: **Master Mode CCLK Output Minimum Low and High Time**

Symbol	Description		*ConfigRate* Setting						Units
			1	3	6	12	25	50	
T_{MCCL}, T_{MCCH}	Master mode CCLK minimum Low and High time	Commercial	276	138	69	34.5	17.1	8.5	ns
		Industrial	235	117	58	29.3	14.5	7.3	ns

Table 115: **Slave Mode CCLK Input Low and High Time**

Symbol	Description	Min	Max	Units
T_{SCCL}, T_{SCCH}	CCLK Low and High time	5	∞	ns

Table 124: **Types of Pins on Spartan-3E FPGAs *(Cont'd)***

Type / Color Code	Description	Pin Name(s) in Type[1]
VCCAUX	Dedicated auxiliary power supply pin. The number of VCCAUX pins depends on the package used. All must be connected to +2.5V. See the Powering Spartan-3E FPGAs section in Module 2 for details.	VCCAUX
VCCINT	Dedicated internal core logic power supply pin. The number of VCCINT pins depends on the package used. All must be connected to +1.2V. See the Powering Spartan-3E FPGAs section in Module 2 for details.	VCCINT
VCCO	Along with all the other VCCO pins in the same bank, this pin supplies power to the output buffers within the I/O bank and sets the input threshold voltage for some I/O standards. See the Powering Spartan-3E FPGAs section in Module 2 for details.	VCCO_#
N.C.	This package pin is not connected in this specific device/package combination but may be connected in larger devices in the same package.	N.C.

Notes:

1. # = I/O bank number, an integer between 0 and 3.
2. IRDY/TRDY designations are for PCI designs; refer to PCI documentation for details.

Differential Pair Labeling

I/Os with Lxxy_# are part of a differential pair. 'L' indicates differential capability. The 'xx' field is a two-digit integer, unique to each bank that identifies a differential pin-pair. The 'y' field is either 'P' for the true signal or 'N' for the inverted signal in the differential pair. The '#' field is the I/O bank number.

The pin name suffix has the following significance. Figure 79 provides a specific example showing a differential input to and a differential output from Bank 1.

'L' indicates that the pin is part of a differential pair.

'xx' is a two-digit integer, unique for each bank, that identifies a differential pin-pair.

'y' is replaced by 'P' for the true signal or 'N' for the inverted. These two pins form one differential pin-pair.

'#' is an integer, 0 through 3, indicating the associated I/O bank.

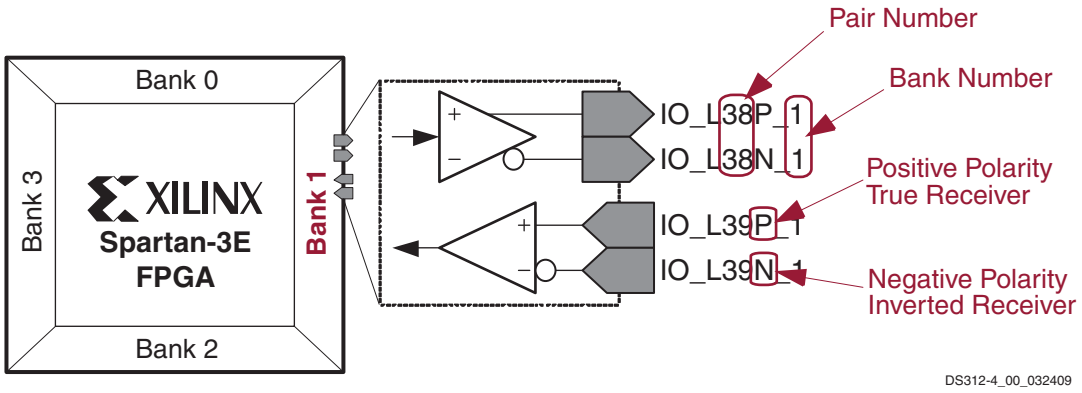

Figure 79: **Differential Pair Labeling**

Table 148: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S500E Pin Name	XC3S1200E Pin Name	XC3S1600E Pin Name	FG320 Ball	Type
0	VCCO_0	VCCO_0	VCCO_0	A9	VCCO
0	VCCO_0	VCCO_0	VCCO_0	C6	VCCO
0	VCCO_0	VCCO_0	VCCO_0	C13	VCCO
0	VCCO_0	VCCO_0	VCCO_0	G8	VCCO
0	VCCO_0	VCCO_0	VCCO_0	G11	VCCO
1	N.C. (◆)	IO	IO	P16	**500E:** N.C. **1200E:** I/O **1600E:** I/O
1	IO_L01N_1/A15	IO_L01N_1/A15	IO_L01N_1/A15	T17	DUAL
1	IO_L01P_1/A16	IO_L01P_1/A16	IO_L01P_1/A16	U18	DUAL
1	IO_L02N_1/A13	IO_L02N_1/A13	IO_L02N_1/A13	T18	DUAL
1	IO_L02P_1/A14	IO_L02P_1/A14	IO_L02P_1/A14	R18	DUAL
1	IO_L03N_1/VREF_1	IO_L03N_1/VREF_1	IO_L03N_1/VREF_1	R16	VREF
1	IO_L03P_1	IO_L03P_1	IO_L03P_1	R15	I/O
1	N.C. (◆)	IO_L04N_1	IO_L04N_1	N14	**500E:** N.C. **1200E:** I/O **1600E:** I/O
1	N.C. (◆)	IO_L04P_1	IO_L04P_1	N15	**500E:** N.C. **1200E:** I/O **1600E:** I/O
1	IO_L05N_1/VREF_1	IO_L05N_1/VREF_1	IO_L05N_1/VREF_1	M13	VREF
1	IO_L05P_1	IO_L05P_1	IO_L05P_1	M14	I/O
1	IO_L06N_1	IO_L06N_1	IO_L06N_1	P18	I/O
1	IO_L06P_1	IO_L06P_1	IO_L06P_1	P17	I/O
1	IO_L07N_1	IO_L07N_1	IO_L07N_1	M16	I/O
1	IO_L07P_1	IO_L07P_1	IO_L07P_1	M15	I/O
1	IO_L08N_1	IO_L08N_1	IO_L08N_1	M18	I/O
1	IO_L08P_1	IO_L08P_1	IO_L08P_1	N18	I/O
1	IO_L09N_1/A11	IO_L09N_1/A11	IO_L09N_1/A11	L15	DUAL
1	IO_L09P_1/A12	IO_L09P_1/A12	IO_L09P_1/A12	L16	DUAL
1	IO_L10N_1/VREF_1	IO_L10N_1/VREF_1	IO_L10N_1/VREF_1	L17	VREF
1	IO_L10P_1	IO_L10P_1	IO_L10P_1	L18	I/O
1	IO_L11N_1/A9/RHCLK1	IO_L11N_1/A9/RHCLK1	IO_L11N_1/A9/RHCLK1	K12	RHCLK/DUAL
1	IO_L11P_1/A10/RHCLK0	IO_L11P_1/A10/RHCLK0	IO_L11P_1/A10/RHCLK0	K13	RHCLK/DUAL
1	IO_L12N_1/A7/RHCLK3/ TRDY1	IO_L12N_1/A7/RHCLK3/ TRDY1	IO_L12N_1/A7/RHCLK3/ TRDY1	K14	RHCLK/DUAL
1	IO_L12P_1/A8/RHCLK2	IO_L12P_1/A8/RHCLK2	IO_L12P_1/A8/RHCLK2	K15	RHCLK/DUAL
1	IO_L13N_1/A5/RHCLK5	IO_L13N_1/A5/RHCLK5	IO_L13N_1/A5/RHCLK5	J16	RHCLK/DUAL
1	IO_L13P_1/A6/RHCLK4/ IRDY1	IO_L13P_1/A6/RHCLK4/ IRDY1	IO_L13P_1/A6/RHCLK4/ IRDY1	J17	RHCLK/DUAL
1	IO_L14N_1/A3/RHCLK7	IO_L14N_1/A3/RHCLK7	IO_L14N_1/A3/RHCLK7	J14	RHCLK/DUAL
1	IO_L14P_1/A4/RHCLK6	IO_L14P_1/A4/RHCLK6	IO_L14P_1/A4/RHCLK6	J15	RHCLK/DUAL
1	IO_L15N_1/A1	IO_L15N_1/A1	IO_L15N_1/A1	J13	DUAL
1	IO_L15P_1/A2	IO_L15P_1/A2	IO_L15P_1/A2	J12	DUAL
1	IO_L16N_1/A0	IO_L16N_1/A0	IO_L16N_1/A0	H17	DUAL
1	IO_L16P_1	IO_L16P_1	IO_L16P_1	H16	I/O

Table 148: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S500E Pin Name	XC3S1200E Pin Name	XC3S1600E Pin Name	FG320 Ball	Type
1	IO_L17N_1	IO_L17N_1	IO_L17N_1	H15	I/O
1	IO_L17P_1	IO_L17P_1	IO_L17P_1	H14	I/O
1	IO_L18N_1	IO_L18N_1	IO_L18N_1	G16	I/O
1	IO_L18P_1	IO_L18P_1	IO_L18P_1	G15	I/O
1	IO_L19N_1	IO_L19N_1	IO_L19N_1	F17	I/O
1	IO_L19P_1	IO_L19P_1	IO_L19P_1	F18	I/O
1	IO_L20N_1	IO_L20N_1	IO_L20N_1	G13	I/O
1	IO_L20P_1	IO_L20P_1	IO_L20P_1	G14	I/O
1	IO_L21N_1	IO_L21N_1	IO_L21N_1	F14	I/O
1	IO_L21P_1	IO_L21P_1	IO_L21P_1	F15	I/O
1	N.C. (◆)	IO_L22N_1	IO_L22N_1	E16	**500E:** N.C. **1200E:** I/O **1600E:** I/O
1	N.C. (◆)	IO_L22P_1	IO_L22P_1	E15	**500E:** N.C. **1200E:** I/O **1600E:** I/O
1	IO_L23N_1/LDC0	IO_L23N_1/LDC0	IO_L23N_1/LDC0	D16	DUAL
1	IO_L23P_1/HDC	IO_L23P_1/HDC	IO_L23P_1/HDC	D17	DUAL
1	IO_L24N_1/LDC2	IO_L24N_1/LDC2	IO_L24N_1/LDC2	C17	DUAL
1	IO_L24P_1/LDC1	IO_L24P_1/LDC1	IO_L24P_1/LDC1	C18	DUAL
1	IP	IP	IP	B18	INPUT
1	IO	IP	IP	E17	**500E:** I/O **1200E:** INPUT **1600E:** INPUT
1	IP	IP	IP	E18	INPUT
1	IP	IP	IP	G18	INPUT
1	IP	IP	IP	H13	INPUT
1	IP	IP	IP	K17	INPUT
1	IP	IP	IP	K18	INPUT
1	IP	IP	IP	L13	INPUT
1	IP	IP	IP	L14	INPUT
1	IP	IP	IP	N17	INPUT
1	IO	IP	IP	P15	**500E:** I/O **1200E:** INPUT **1600E:** INPUT
1	IP	IP	IP	R17	INPUT
1	IP/VREF_1	IP/VREF_1	IP/VREF_1	D18	VREF
1	IP/VREF_1	IP/VREF_1	IP/VREF_1	H18	VREF
1	VCCO_1	VCCO_1	VCCO_1	F16	VCCO
1	VCCO_1	VCCO_1	VCCO_1	H12	VCCO
1	VCCO_1	VCCO_1	VCCO_1	J18	VCCO
1	VCCO_1	VCCO_1	VCCO_1	L12	VCCO
1	VCCO_1	VCCO_1	VCCO_1	N16	VCCO
2	IO	IO	IO	P9	I/O
2	IO	IO	IO	R11	I/O

Table 152: **FG400 Package Pinout *(Cont'd)***

Bank	XC3S1200E XC3S1600E Pin Name	FG400 Ball	Type
1	IP	L18	INPUT
1	IP	M20	INPUT
1	IP	N14	INPUT
1	IP	N20	INPUT
1	IP	P15	INPUT
1	IP	R16	INPUT
1	IP	R19	INPUT
1	IP/VREF_1	E19	VREF
1	IP/VREF_1	K18	VREF
1	VCCO_1	D19	VCCO
1	VCCO_1	G17	VCCO
1	VCCO_1	K15	VCCO
1	VCCO_1	K19	VCCO
1	VCCO_1	N17	VCCO
1	VCCO_1	T19	VCCO
2	IO	P8	I/O
2	IO	P13	I/O
2	IO	R9	I/O
2	IO	R13	I/O
2	IO	W15	I/O
2	IO	Y5	I/O
2	IO	Y7	I/O
2	IO	Y13	I/O
2	IO/D5	N11	DUAL
2	IO/M1	T11	DUAL
2	IO/VREF_2	Y3	VREF
2	IO/VREF_2	Y17	VREF
2	IO_L01N_2/INIT_B	V4	DUAL
2	IO_L01P_2/CSO_B	U4	DUAL
2	IO_L03N_2/MOSI/CSI_B	V5	DUAL
2	IO_L03P_2/DOUT/BUSY	U5	DUAL
2	IO_L04N_2	Y4	I/O
2	IO_L04P_2	W4	I/O
2	IO_L06N_2	T6	I/O
2	IO_L06P_2	T5	I/O
2	IO_L07N_2	U7	I/O
2	IO_L07P_2	V7	I/O
2	IO_L09N_2/VREF_2	R7	VREF
2	IO_L09P_2	T7	I/O
2	IO_L10N_2	V8	I/O
2	IO_L10P_2	W8	I/O
2	IO_L12N_2	U9	I/O
2	IO_L12P_2	V9	I/O

Table 152: **FG400 Package Pinout *(Cont'd)***

Bank	XC3S1200E XC3S1600E Pin Name	FG400 Ball	Type
2	IO_L13N_2	Y8	I/O
2	IO_L13P_2	Y9	I/O
2	IO_L15N_2/D6/GCLK13	W10	DUAL/ GCLK
2	IO_L15P_2/D7/GCLK12	W9	DUAL/ GCLK
2	IO_L16N_2/D3/GCLK15	P10	DUAL/ GCLK
2	IO_L16P_2/D4/GCLK14	R10	DUAL/ GCLK
2	IO_L18N_2/D1/GCLK3	V11	DUAL/ GCLK
2	IO_L18P_2/D2/GCLK2	V10	DUAL/ GCLK
2	IO_L19N_2/DIN/D0	Y12	DUAL
2	IO_L19P_2/M0	Y11	DUAL
2	IO_L21N_2	U12	I/O
2	IO_L21P_2	V12	I/O
2	IO_L22N_2/VREF_2	W12	VREF
2	IO_L22P_2	W13	I/O
2	IO_L24N_2	U13	I/O
2	IO_L24P_2	V13	I/O
2	IO_L25N_2	P14	I/O
2	IO_L25P_2	R14	I/O
2	IO_L27N_2/A22	Y14	DUAL
2	IO_L27P_2/A23	Y15	DUAL
2	IO_L28N_2	T15	I/O
2	IO_L28P_2	U15	I/O
2	IO_L30N_2/A20	V16	DUAL
2	IO_L30P_2/A21	U16	DUAL
2	IO_L31N_2/VS1/A18	Y18	DUAL
2	IO_L31P_2/VS2/A19	W18	DUAL
2	IO_L32N_2/CCLK	W19	DUAL
2	IO_L32P_2/VS0/A17	Y19	DUAL
2	IP	T16	INPUT
2	IP	W3	INPUT
2	IP_L02N_2	Y2	INPUT
2	IP_L02P_2	W2	INPUT
2	IP_L05N_2	V6	INPUT
2	IP_L05P_2	U6	INPUT
2	IP_L08N_2	Y6	INPUT
2	IP_L08P_2	W6	INPUT
2	IP_L11N_2	R8	INPUT
2	IP_L11P_2	T8	INPUT
2	IP_L14N_2/VREF_2	T10	VREF

Table 152: **FG400 Package Pinout *(Cont'd)***

Bank	XC3S1200E XC3S1600E Pin Name	FG400 Ball	Type
2	IP_L14P_2	T9	INPUT
2	IP_L17N_2/M2/GCLK1	P12	DUAL/ GCLK
2	IP_L17P_2/RDWR_B/ GCLK0	P11	DUAL/ GCLK
2	IP_L20N_2	T12	INPUT
2	IP_L20P_2	R12	INPUT
2	IP_L23N_2/VREF_2	T13	VREF
2	IP_L23P_2	T14	INPUT
2	IP_L26N_2	V14	INPUT
2	IP_L26P_2	V15	INPUT
2	IP_L29N_2	W16	INPUT
2	IP_L29P_2	Y16	INPUT
2	VCCO_2	R11	VCCO
2	VCCO_2	U8	VCCO
2	VCCO_2	U14	VCCO
2	VCCO_2	W5	VCCO
2	VCCO_2	W11	VCCO
2	VCCO_2	W17	VCCO
3	IO_L01N_3	D2	I/O
3	IO_L01P_3	D3	I/O
3	IO_L02N_3/VREF_3	E3	VREF
3	IO_L02P_3	E4	I/O
3	IO_L03N_3	C1	I/O
3	IO_L03P_3	B1	I/O
3	IO_L04N_3	E1	I/O
3	IO_L04P_3	D1	I/O
3	IO_L05N_3	F3	I/O
3	IO_L05P_3	F4	I/O
3	IO_L06N_3	F1	I/O
3	IO_L06P_3	F2	I/O
3	IO_L07N_3	G4	I/O
3	IO_L07P_3	G3	I/O
3	IO_L08N_3	G5	I/O
3	IO_L08P_3	H5	I/O
3	IO_L09N_3/VREF_3	H3	VREF
3	IO_L09P_3	H2	I/O
3	IO_L10N_3	H7	I/O
3	IO_L10P_3	H6	I/O
3	IO_L11N_3	J4	I/O
3	IO_L11P_3	J3	I/O
3	IO_L12N_3	J1	I/O
3	IO_L12P_3	J2	I/O
3	IO_L13N_3	J6	I/O

Table 152: **FG400 Package Pinout *(Cont'd)***

Bank	XC3S1200E XC3S1600E Pin Name	FG400 Ball	Type
3	IO_L13P_3	K6	I/O
3	IO_L14N_3/LHCLK1	K2	LHCLK
3	IO_L14P_3/LHCLK0	K3	LHCLK
3	IO_L15N_3/LHCLK3/IRDY2	L7	LHCLK
3	IO_L15P_3/LHCLK2	K7	LHCLK
3	IO_L16N_3/LHCLK5	L1	LHCLK
3	IO_L16P_3/LHCLK4/TRDY2	M1	LHCLK
3	IO_L17N_3/LHCLK7	L3	LHCLK
3	IO_L17P_3/LHCLK6	M3	LHCLK
3	IO_L18N_3	M7	I/O
3	IO_L18P_3	M8	I/O
3	IO_L19N_3	M4	I/O
3	IO_L19P_3	M5	I/O
3	IO_L20N_3/VREF_3	N6	VREF
3	IO_L20P_3	M6	I/O
3	IO_L21N_3	N2	I/O
3	IO_L21P_3	N1	I/O
3	IO_L22N_3	P7	I/O
3	IO_L22P_3	N7	I/O
3	IO_L23N_3	N4	I/O
3	IO_L23P_3	N3	I/O
3	IO_L24N_3	R1	I/O
3	IO_L24P_3	P1	I/O
3	IO_L25N_3	R5	I/O
3	IO_L25P_3	P5	I/O
3	IO_L26N_3	T2	I/O
3	IO_L26P_3	R2	I/O
3	IO_L27N_3	R4	I/O
3	IO_L27P_3	R3	I/O
3	IO_L28N_3/VREF_3	T1	VREF
3	IO_L28P_3	U1	I/O
3	IO_L29N_3	T3	I/O
3	IO_L29P_3	U3	I/O
3	IO_L30N_3	V1	I/O
3	IO_L30P_3	V2	I/O
3	IP	F5	INPUT
3	IP	G1	INPUT
3	IP	G6	INPUT
3	IP	H1	INPUT
3	IP	J5	INPUT
3	IP	L5	INPUT
3	IP	L8	INPUT
3	IP	M2	INPUT