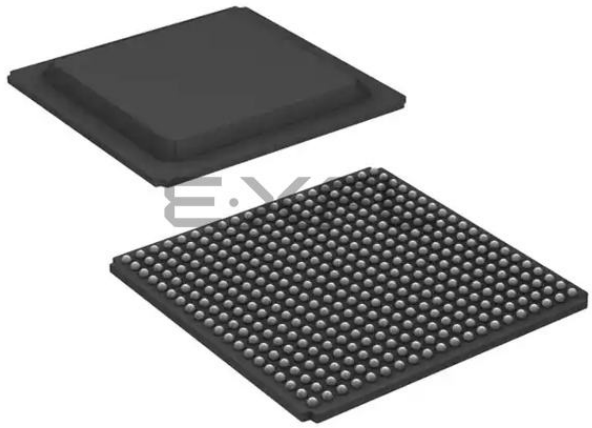

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	3688
Number of Logic Elements/Cells	33192
Total RAM Bits	663552
Number of I/O	304
Number of Gates	1600000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	400-BGA
Supplier Device Package	400-FBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s1600e-5fgg400c

Spartan-3 FPGA Family: Introduction and Ordering Information

DS312 (4.0) October 29, 2012 **Product Specification**

Introduction

The Spartan®-3E family of Field-Programmable Gate Arrays (FPGAs) is specifically designed to meet the needs of high volume, cost-sensitive consumer electronic applications. The five-member family offers densities ranging from 100,000 to 1.6 million system gates, as shown in Table 1.

The Spartan-3E family builds on the success of the earlier Spartan-3 family by increasing the amount of logic per I/O, significantly reducing the cost per logic cell. New features improve system performance and reduce the cost of configuration. These Spartan-3E FPGA enhancements, combined with advanced 90 nm process technology, deliver more functionality and bandwidth per dollar than was previously possible, setting new standards in the programmable logic industry.

Because of their exceptionally low cost, Spartan-3E FPGAs are ideally suited to a wide range of consumer electronics applications, including broadband access, home networking, display/projection, and digital television equipment.

The Spartan-3E family is a superior alternative to mask programmed ASICs. FPGAs avoid the high initial cost, the lengthy development cycles, and the inherent inflexibility of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary, an impossibility with ASICs.

Features

- Very low cost, high-performance logic solution for high-volume, consumer-oriented applications
- Proven advanced 90-nanometer process technology
- Multi-voltage, multi-standard SelectIO™ interface pins
  - Up to 376 I/O pins or 156 differential signal pairs
  - LVCMOS, LVTTL, HSTL, and SSTL single-ended signal standards
  - 3.3V, 2.5V, 1.8V, 1.5V, and 1.2V signaling
  - 622+ Mb/s data transfer rate per I/O
  - True LVDS, RSDS, mini-LVDS, differential HSTL/SSTL differential I/O
  - Enhanced Double Data Rate (DDR) support
  - DDR SDRAM support up to 333 Mb/s
- Abundant, flexible logic resources
  - Densities up to 33,192 logic cells, including optional shift register or distributed RAM support
  - Efficient wide multiplexers, wide logic
  - Fast look-ahead carry logic
  - Enhanced 18 x 18 multipliers with optional pipeline
  - IEEE 1149.1/1532 JTAG programming/debug port
- Hierarchical SelectRAM™ memory architecture
  - Up to 648 Kbits of fast block RAM
  - Up to 231 Kbits of efficient distributed RAM
- Up to eight Digital Clock Managers (DCMs)
  - Clock skew elimination (delay locked loop)
  - Frequency synthesis, multiplication, division
  - High-resolution phase shifting
  - Wide frequency range (5 MHz to over 300 MHz)
- Eight global clocks plus eight additional clocks per each half of device, plus abundant low-skew routing
- Configuration interface to industry-standard PROMs
  - Low-cost, space-saving SPI serial Flash PROM
  - x8 or x8/x16 parallel NOR Flash PROM
  - Low-cost Xilinx® Platform Flash with JTAG
- Complete Xilinx ISE® and WebPACK™ software
- MicroBlaze™ and PicoBlaze™ embedded processor cores
- Fully compliant 32-/64-bit 33 MHz PCI support (66 MHz in some devices)
- Low-cost QFP and BGA packaging options
- Common footprints support easy density migration
- Pb-free packaging options
- XA Automotive version available

Table 1: **Summary of Spartan-3E FPGA Attributes**

Device	System Gates	Equivalent Logic Cells	CLB Array (One CLB = Four Slices)				Distributed RAM bits(1)	Block RAM bits(1)	Dedicated Multipliers	DCMs	Maximum User I/O	Maximum Differential I/O Pairs
			Rows	Columns	Total CLBs	Total Slices						
XC3S100E	100K	2,160	22	16	240	960	15K	72K	4	2	108	40
XC3S250E	250K	5,508	34	26	612	2,448	38K	216K	12	4	172	68
XC3S500E	500K	10,476	46	34	1,164	4,656	73K	360K	20	4	232	92
XC3S1200E	1200K	19,512	60	46	2,168	8,672	136K	504K	28	8	304	124
XC3S1600E	1600K	33,192	76	58	3,688	14,752	231K	648K	36	8	376	156

Notes:
1. By convention, one Kb is equivalent to 1,024 bits.

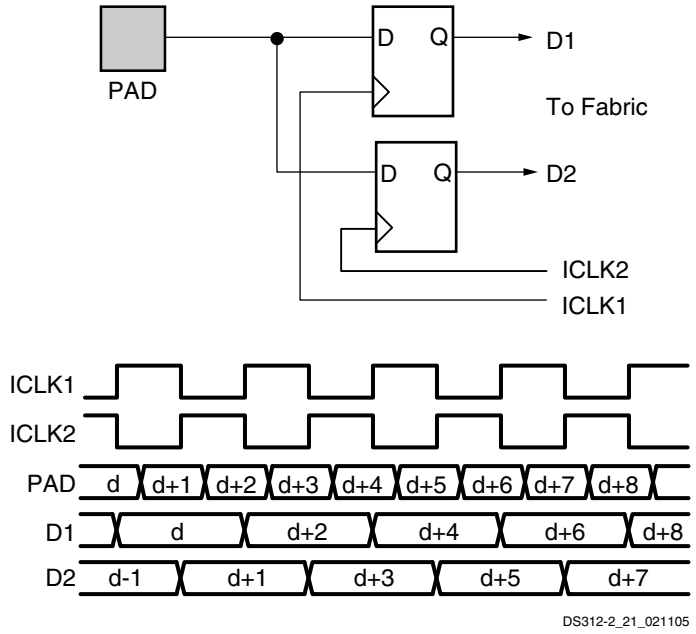

Figure 8: **Input DDR (without Cascade Feature)**

In the Spartan-3E device, the signal D2 can be cascaded into the storage element of the adjacent slave IOB. There it is re-registered to ICLK1, and only then fed to the FPGA fabric where it is now already in the same time domain as D1. Here, the FPGA fabric uses only the clock ICLK1 to process the received data. See Figure 9 for a graphical illustration of this function.

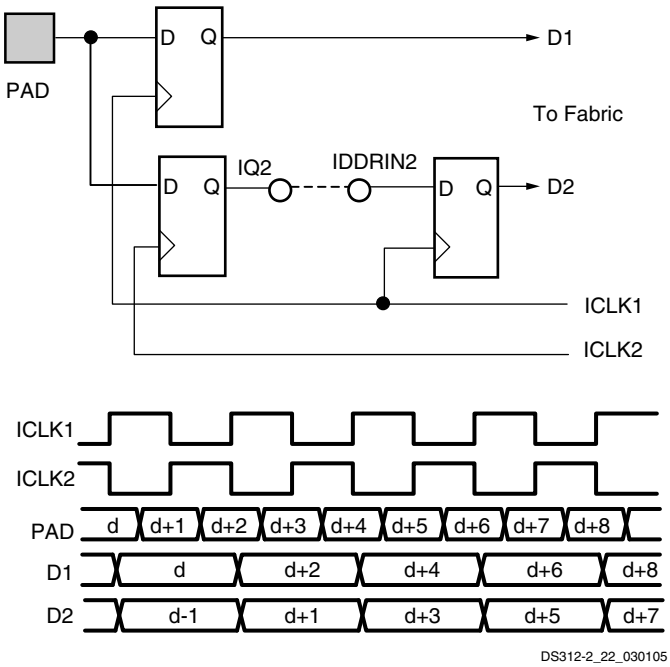

Figure 9: **Input DDR Using Spartan-3E Cascade Feature**

ODDR2

As a DDR output pair, the master IOB registers data coming from the FPGA fabric on the rising edge of OCLK1 (= D1) and the rising edge of OCLK2 (= D2), which is typically the same as the falling edge of OCLK1. These two bits of data are multiplexed by the DDR mux and forwarded to the output pin. The D2 data signal must be re-synchronized from the OCLK1 clock domain to the OCLK2 domain using FPGA slice flip-flops. Placement is critical at high frequencies, because the time available is only one half a clock cycle. See Figure 10 for a graphical illustration of this function.

The C0 or C1 alignment feature of the ODDR2 flip-flop, originally introduced in the Spartan-3E FPGA family, is not recommended or supported in the ISE development software. The ODDR2 flip-flop without the alignment feature remains fully supported. Without the alignment feature, the ODDR2 feature behaves equivalent to the ODDR flip-flop on previous Xilinx FPGA families.

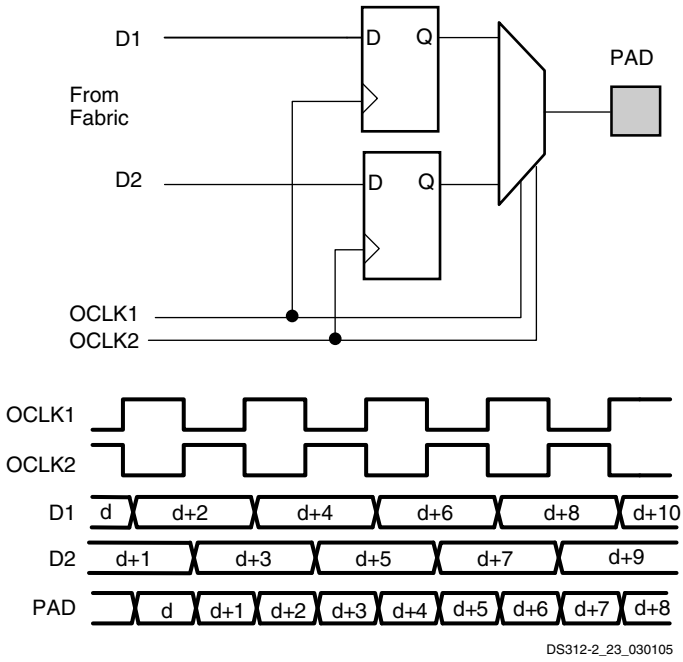

Figure 10: **Output DDR**

SelectIO Signal Standards

The Spartan-3E I/Os feature inputs and outputs that support a wide range of I/O signaling standards (Table 6 and Table 7). The majority of the I/Os also can be used to form differential pairs to support any of the differential signaling standards (Table 7).

To define the I/O signaling standard in a design, set the IOSTANDARD attribute to the appropriate setting. Xilinx provides a variety of different methods for applying the IOSTANDARD for maximum flexibility. For a full description of different methods of applying attributes to control IOSTANDARD, refer to the Xilinx Software Manuals and Help.

Table 14: **Carry Logic Functions *(Cont'd)***

Function	Description
CY0G	Carry generation for top half of slice. Fixed selection of: · G1 or G2 inputs to the LUT (both equal 1 when a carry is to be generated) · GAND gate for multiplication · BY input for carry initialization · Fixed 1 or 0 input for use as a simple Boolean function
CYMUXF	Carry generation or propagation mux for bottom half of slice. Dynamic selection via CYSELF of: · CYINIT carry propagation (CYSELF = 1) · CY0F carry generation (CYSELF = 0)
CYMUXG	Carry generation or propagation mux for top half of slice. Dynamic selection via CYSELF of: · CYMUXF carry propagation (CYSELG = 1) · CY0G carry generation (CYSELG = 0)
CYSELF	Carry generation or propagation select for bottom half of slice. Fixed selection of: · F-LUT output (typically XOR result) · Fixed 1 to always propagate
CYSELG	Carry generation or propagation select for top half of slice. Fixed selection of: · G-LUT output (typically XOR result) · Fixed 1 to always propagate
XORF	Sum generation for bottom half of slice. Inputs from: · F-LUT · CYINIT carry signal from previous stage Result is sent to either the combinatorial or registered output for the top of the slice.
XORG	Sum generation for top half of slice. Inputs from: · G-LUT · CYMUXF carry signal from previous stage Result is sent to either the combinatorial or registered output for the top of the slice.
FAND	Multiplier partial product for bottom half of slice. Inputs: · F-LUT F1 input · F-LUT F2 input Result is sent through CY0F to become the carry generate signal into CYMUXF
GAND	Multiplier partial product for top half of slice. Inputs: · G-LUT G1 input · G-LUT G2 input Result is sent through CY0G to become the carry generate signal into CYMUXG

The basic usage of the carry logic is to generate a half-sum in the LUT via an XOR function, which generates or propagates a carry out COUT via the carry mux CYMUXF (or CYMUXG), and then complete the sum with the dedicated XORF (or XORG) gate and the carry input CIN. This structure allows two bits of an arithmetic function in each slice. The CYMUXF (or CYMUXG) can be instantiated using the MUXCY element, and the XORF (or XORG) can be instantiated using the XORCY element.

The FAND (or GAND) gate is used for partial product multiplication and can be instantiated using the MULT_AND component. Partial products are generated by two-input AND gates and then added. The carry logic is efficient for the adder, but one of the inputs must be outside the LUT as shown in Figure 23.

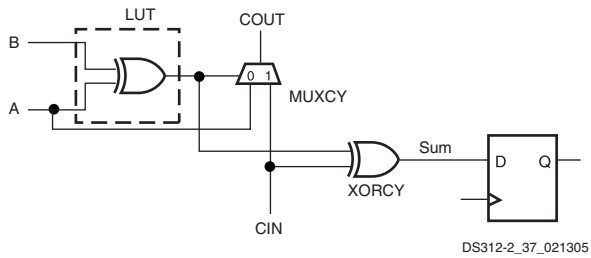

Figure 23: **Using the MUXCY and XORCY in the Carry Logic**

The FAND (or GAND) gate is used to duplicate one of the partial products, while the LUT generates both partial products and the XOR function, as shown in Figure 24.

Clocking Infrastructure

For additional information, refer to the “Using Global Clock Resources” chapter in UG331.

The Spartan-3E clocking infrastructure, shown in Figure 45, provides a series of low-capacitance, low-skew interconnect lines well-suited to carrying high-frequency signals throughout the FPGA. The infrastructure also includes the clock inputs and BUFGMUX clock buffers/multiplexers. The Xilinx Place-and-Route (PAR) software automatically routes high-fanout clock signals using these resources.

Clock Inputs

Clock pins accept external clock signals and connect directly to DCMs and BUFGMUX elements. Each Spartan-3E FPGA has:

- 16 Global Clock inputs (GCLK0 through GCLK15) located along the top and bottom edges of the FPGA
- 8 Right-Half Clock inputs (RHCLK0 through RHCLK7) located along the right edge
- 8 Left-Half Clock inputs (LHCLK0 through LHCLK7) located along the left edge

Clock inputs optionally connect directly to DCMs using dedicated connections. Table 30, Table 31, and Table 32 show the clock inputs that best feed a specific DCM within a given Spartan-3E part number. Different Spartan-3E FPGA densities have different numbers of DCMs. The XC3S1200E and XC3S1600E are the only two densities with the left- and right-edge DCMs.

Each clock input is also optionally a user-I/O pin and connects to internal interconnect. Some clock pad pins are input-only pins as indicated in Module 4, Pinout Descriptions.

Design Note

Avoid using global clock input GCLK1 as it is always shared with the M2 mode select pin. Global clock inputs GCLK0, GCLK2, GCLK3, GCLK12, GCLK13, GCLK14, and GCLK15 have shared functionality in some configuration modes.

Clock Buffers/Multiplexers

Clock Buffers/Multiplexers either drive clock input signals directly onto a clock line (BUFG) or optionally provide a multiplexer to switch between two unrelated, possibly asynchronous clock signals (BUFGMUX).

Each BUFGMUX element, shown in Figure 46, is a 2-to-1 multiplexer. The select line, S, chooses which of the two inputs, I0 or I1, drives the BUFGMUX’s output signal, O, as described in Table 40. The switching from one clock to the other is glitch-less, and done in such a way that the output High and Low times are never shorter than the shortest High or Low time of either input clock. The two clock inputs can be asynchronous with regard to each other, and the S input can change at any time, except for a short setup time prior to the rising edge of the presently selected clock (I0 or I1). This setup time is specified as TGSI in Table 101, page 136. Violating this setup time requirement possibly results in an undefined runt pulse output.

Table 40: **BUFGMUX Select Mechanism**

S Input	O Output
0	I0 Input
1	I1 Input

The BUFG clock buffer primitive drives a single clock signal onto the clock network and is essentially the same element as a BUFGMUX, just without the clock select mechanism. Similarly, the BUFGCE primitive creates an enabled clock buffer using the BUFGMUX select mechanism.

The I0 and I1 inputs to an BUFGMUX element originate from clock input pins, DCMs, or Double-Line interconnect, as shown in Figure 46. As shown in Figure 45, there are 24 BUFGMUX elements distributed around the four edges of the device. Clock signals from the four BUFGMUX elements at the top edge and the four at the bottom edge are truly global and connect to all clocking quadrants. The eight left-edge BUFGMUX elements only connect to the two clock quadrants in the left half of the device. Similarly, the eight right-edge BUFGMUX elements only connect to the right half of the device.

BUFGMUX elements are organized in pairs and share I0 and I1 connections with adjacent BUFGMUX elements from a common clock switch matrix as shown in Figure 46. For example, the input on I0 of one BUFGMUX is also a shared input to I1 of the adjacent BUFGMUX.

The clock switch matrix for the left- and right-edge BUFGMUX elements receive signals from any of the three following sources: an LHCLK or RHCLK pin as appropriate, a Double-Line interconnect, or a DCM in the XC3S1200E and XC3S1600E devices.

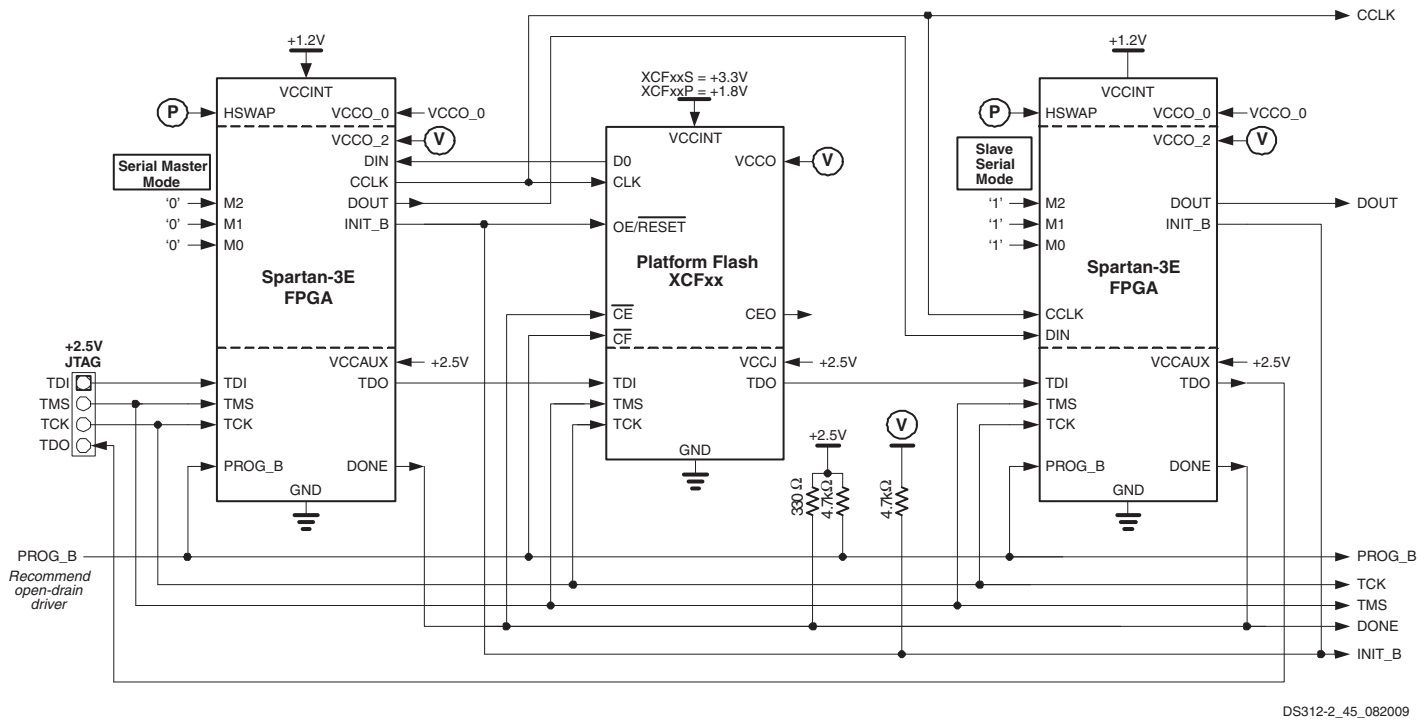

Figure 52: **Daisy-Chaining from Master Serial Mode**

Daisy-Chaining

If the application requires multiple FPGAs with different configurations, then configure the FPGAs using a daisy chain, as shown in Figure 52. Use Master Serial mode (M[2:0] = <0:0:0>) for the FPGA connected to the Platform Flash PROM and Slave Serial mode (M[2:0] = <1:1:1>) for all other FPGAs in the daisy-chain. After the master FPGA—the FPGA on the left in the diagram—finishes loading its configuration data from the Platform Flash, the master device supplies data using its DOUT output pin to the next device in the daisy-chain, on the falling CCLK edge.

JTAG Interface

Both the Spartan-3E FPGA and the Platform Flash PROM have a four-wire IEEE 1149.1/1532 JTAG port. Both devices share the TCK clock input and the TMS mode select input. The devices may connect in either order on the JTAG chain with the TDO output of one device feeding the TDI input of the following device in the chain. The TDO output of the last device in the JTAG chain drives the JTAG connector.

The JTAG interface on Spartan-3E FPGAs is powered by the 2.5V V_{CCAUX} supply. Consequently, the PROM's V_{CCJ} supply input must also be 2.5V. To create a 3.3V JTAG interface, please refer to application note XAPP453: *The 3.3V Configuration of Spartan-3 FPGAs* for additional information.

In-System Programming Support

Both the FPGA and the Platform Flash PROM are in-system programmable via the JTAG chain. Download support is provided by the Xilinx iMPACT programming software and the associated Xilinx Parallel Cable IV or Platform Cable USB programming cables.

Storing Additional User Data in Platform Flash

After configuration, the FPGA application can continue to use the Master Serial interface pins to communicate with the Platform Flash PROM. If desired, use a larger Platform Flash PROM to hold additional non-volatile application data, such as MicroBlaze processor code, or other user data such as serial numbers and Ethernet MAC IDs. The FPGA first configures from Platform Flash PROM. Then using FPGA logic after configuration, the FPGA copies MicroBlaze code from Platform Flash into external DDR SDRAM for code execution.

See XAPP694: *Reading User Data from Configuration PROMs* and XAPP482: *MicroBlaze Platform Flash/PROM Boot Loader and User Data Storage* for specific details on how to implement such an interface.

Also, in a multi-FPGA daisy-chain configuration of more than two devices, all intermediate FPGAs between the first and last devices must be Spartan-3E or Virtex-5 FPGAs. The last FPGA in the chain can be from any Xilinx FPGA family.

BPI Mode Interaction with Right and Bottom Edge Global Clock Inputs

Some of the BPI mode configuration pins are shared with global clock inputs along the right and bottom edges of the device (Bank 1 and Bank 2, respectively). These pins are not easily reclaimable for clock inputs after configuration, especially if the FPGA application access the parallel NOR Flash after configuration. Table 64 summarizes the shared pins.

Table 64: **Shared BPI Configuration Mode and Global Buffer Input Pins**

Device Edge	Global Buffer Input Pin	BPI Mode Configuration Pin
Bottom	GCLK0	RDWR_B
	GCLK2	D2
	GCLK3	D1
	GCLK12	D7
	GCLK13	D6
	GCLK14	D4
	GCLK15	D3
Right	RHCLK0	A10
	RHCLK1	A9
	RHCLK2	A8
	RHCLK3	A7
	RHCLK4	A6
	RHCLK5	A5
	RHCLK6	A4
	RHCLK7	A3

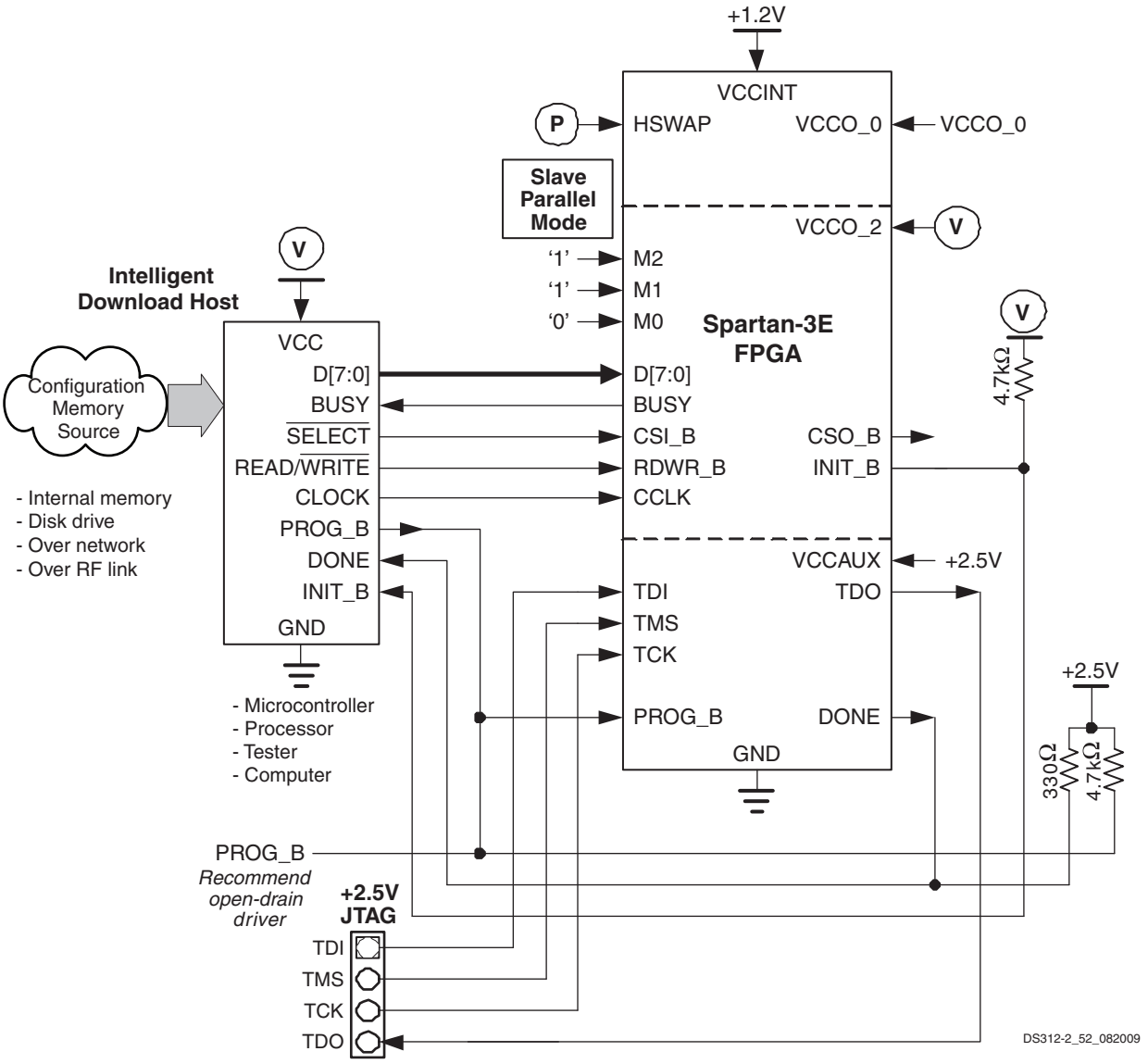

Figure 61: **Slave Parallel Configuration Mode**

Slave Parallel Mode

For additional information, refer to the "Slave Parallel (SelectMAP) Mode" chapter in UG332.

In Slave Parallel mode (M[2:0] = <1:1:0>), an external host, such as a microprocessor or microcontroller, writes byte-wide configuration data into the FPGA, using a typical peripheral interface as shown in Figure 61.

The external download host starts the configuration process by pulsing PROG_B and monitoring that the INIT_B pin goes High, indicating that the FPGA is ready to receive its first data. The host asserts the active-Low chip-select signal (CSI_B) and the active-Low Write signal (RDWR_B). The host then continues supplying data and clock signals until either the FPGA's DONE pin goes High, indicating a successful configuration, or until the FPGA's INIT_B pin goes Low, indicating a configuration error.

The FPGA captures data on the rising CCLK edge. If the CCLK frequency exceeds 50 MHz, then the host must also monitor the FPGA's BUSY output. If the FPGA asserts BUSY High, the host must hold the data for an additional clock cycle, until BUSY returns Low. If the CCLK frequency is 50 MHz or below, the BUSY pin may be ignored but actively drives during configuration.

The configuration process requires more clock cycles than indicated from the configuration file size. Additional clocks are required during the FPGA's start-up sequence, especially if the FPGA is programmed to wait for selected Digital Clock Managers (DCMs) to lock to their respective clock inputs (see Start-Up, page 105).

If the Slave Parallel interface is only used to configure the FPGA, never to read data back, then the RDWR_B signal

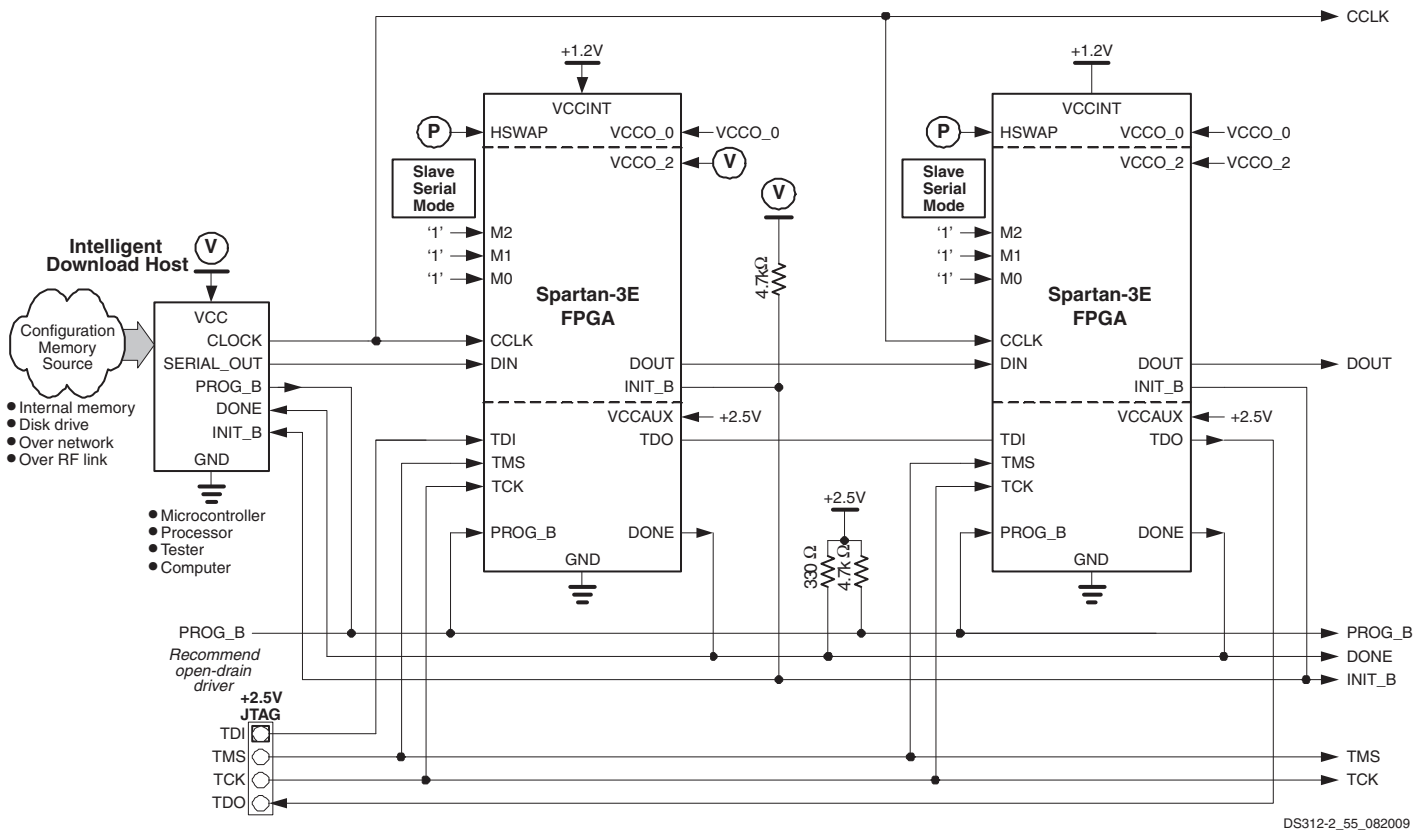

Figure 64: **Daisy-Chaining using Slave Serial Mode**

JTAG Mode

For additional information, refer to the "JTAG Configuration Mode and Boundary-Scan" chapter in UG332.

The Spartan-3E FPGA has a dedicated four-wire IEEE 1149.1/1532 JTAG port that is always available any time the FPGA is powered and regardless of the mode pin settings. However, when the FPGA mode pins are set for JTAG mode (M[2:0] = <1:0:1>), the FPGA waits to be configured via the JTAG port after a power-on event or when PROG_B is asserted. Selecting the JTAG mode simply disables the other configuration modes. No other pins are required as part of the configuration interface.

Figure 65 illustrates a JTAG-only configuration interface. The JTAG interface is easily cascaded to any number of FPGAs by connecting the TDO output of one device to the TDI input of the next device in the chain. The TDO output of the last device in the chain loops back to the port connector.

Design Note

If using software versions prior to ISE 9.1.01i, avoid configuring the FPGA using JTAG if...

- the mode pins are set for a Master mode
- the attached Master mode PROM contains a valid FPGA configuration bitstream.

The FPGA bitstream may be corrupted and the DONE pin may go High. The following Answer Record contains additional information.

http://www.xilinx.com/support/answers/22255.htm

Production Stepping

The Spartan-3E FPGA family uses production stepping to indicate improved capabilities or enhanced features.

Stepping 1 is, by definition, a functional superset of Stepping 0. Furthermore, configuration bitstreams generated for Stepping 0 are compatible with Stepping 1.

Designs operating on the Stepping 0 devices perform similarly on a Stepping 1 device.

Differences Between Steppings

Table 71 summarizes the feature and performance differences between Stepping 0 devices and Stepping 1 devices.

Table 71: **Differences between Spartan-3E Production Stepping Levels**

	Stepping 0	Stepping 1
Production status	Production from 2005 to 2007	Production starting March 2006
Speed grade and operating conditions	-4C only	-4C, -4I, -5C
JTAG ID code	Different revision fields. See Table 67.	
DCM DLL maximum input frequency	90 MHz (200 MHz for XC3S1200E)	240 MHz (-4 speed grade) 275 MHz (-5 speed grade)
DCM DFS output frequency range(s)	Split ranges at 5 – 90 MHz and 220 – 307 MHz (single range 5 – 307 MHz for XC3S1200E)	Continuous range: 5 – 311 MHz (-4) 5 – 333 MHz (-5)
Supports multi-FPGA daisy-chain configurations from SPI Flash	No, single FPGA only	Yes
JTAG configuration supported when FPGA in BPI mode with a valid image in the attached parallel NOR Flash PROM	No(1)	Yes
JTAG EXTEST, INTEST, SAMPLE support	Yes: XC3S100E, XC3S250E, XC3S500E No(2): XC3S1200E, XC3S1600E	Yes All Devices
Power sequencing when using HSWAP Pull-Up	Requires V_{CCINT} before V_{CCAUX}	Any sequence
PCI compliance	No	Yes

Notes:

1. Workarounds exist. See Stepping 0 Limitations when Reprogramming via JTAG if FPGA Set for BPI Configuration.
2. JTAG BYPASS and JTAG configuration are supported

Ordering a Later Stepping

-5C and -4I devices, and -4C devices (with date codes 0901 (2009) and later) always support the Stepping 1 feature set independent of the stepping code. Optionally, to order only Stepping 1 for the -4C devices, append an “S1” suffix to the standard ordering code, where ‘1’ is the stepping number, as indicated in Table 72.

Table 72: **Spartan-3E Optional Stepping Ordering**

Stepping Number	Suffix Code	Status
0	None	Production
1	S1	Production

Software Version Requirements

Production Spartan-3E applications must be processed using the Xilinx ISE 8.1i, Service Pack 3 or later development software, using the v1.21 or later speed files. The ISE 8.1i software implements critical bitstream generator updates.

For additional information on Spartan-3E development software and known issues, see the following Answer Record:

- Xilinx Answer #22253
  http://www.xilinx.com/support/answers/22253.htm

General Recommended Operating Conditions

Table 77: **General Recommended Operating Conditions**

Symbol	Description			Min	Nominal	Max	Units
T_J	Junction temperature	Commercial		0	–	85	°C
		Industrial		–40	–	100	°C
V_{CCINT}	Internal supply voltage			1.140	1.200	1.260	V
V_{CCO} (1)	Output driver supply voltage			1.100	-	3.465	V
V_{CCAUX}	Auxiliary supply voltage			2.375	2.500	2.625	V
V_{IN} (2,3)	Input voltage extremes to avoid turning on I/O protection diodes	I/O, Input-only, and Dual-Purpose pins (4)	IP or IO_#	–0.5	–	V_{CCO} + 0.5	V
			IO_Lxxy_# (5)	–0.5	–	V_{CCO} + 0.5	V
		Dedicated pins (6)		–0.5	–	V_{CCAUX} + 0.5	V
T_{IN}	Input signal transition time (7)			–	–	500	ns

Notes:

1. This V_{CCO} range spans the lowest and highest operating voltages for all supported I/O standards. Table 80 lists the recommended V_{CCO} range specific to each of the single-ended I/O standards, and Table 82 lists that specific to the differential standards.
2. Input voltages outside the recommended range require the I_{IK} input clamp diode rating is met and no more than 100 pins exceed the range simultaneously. Refer to Table 73.
3. See XAPP459: *Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins on Spartan-3 Families*.
4. Each of the User I/O and Dual-Purpose pins is associated with one of the four banks' V_{CCO} rails. Meeting the V_{IN} limit ensures that the internal diode junctions that exist between these pins and their associated V_{CCO} and GND rails do not turn on. The absolute maximum rating is provided in Table 73.
5. For single-ended signals that are placed on a differential-capable I/O, V_{IN} of –0.2V to –0.5V is supported but can cause increased leakage between the two pins. See *Parasitic Leakage* in UG331, *Spartan-3 Generation FPGA User Guide*.
6. All Dedicated pins (PROG_B, DONE, TCK, TDI, TDO, and TMS) draw power from the V_{CCAUX} rail (2.5V). Meeting the V_{IN} max limit ensures that the internal diode junctions that exist between each of these pins and the V_{CCAUX} and GND rails do not turn on.
7. Measured between 10% and 90% V_{CCO}. Follow Signal Integrity recommendations.

General DC Characteristics for I/O Pins

Table 78: **General DC Characteristics of User I/O, Dual-Purpose, and Dedicated Pins**

Symbol	Description	Test Conditions	Min	Typ	Max	Units
I_L (3)	Leakage current at User I/O, Input-only, Dual-Purpose, and Dedicated pins	Driver is in a high-impedance state, V_{IN} = 0V or V_{CCO} max, sample-tested	–10	–	+10	µA
I_{RPU} (2)	Current through pull-up resistor at User I/O, Dual-Purpose, Input-only, and Dedicated pins	V_{IN} = 0V, V_{CCO} = 3.3V	–0.36	–	–1.24	mA
		V_{IN} = 0V, V_{CCO} = 2.5V	–0.22	–	–0.80	mA
		V_{IN} = 0V, V_{CCO} = 1.8V	–0.10	–	–0.42	mA
		V_{IN} = 0V, V_{CCO} = 1.5V	–0.06	–	–0.27	mA
		V_{IN} = 0V, V_{CCO} = 1.2V	–0.04	–	–0.22	mA
R_{PU} (2)	Equivalent pull-up resistor value at User I/O, Dual-Purpose, Input-only, and Dedicated pins (based on I_{RPU} per Note 2)	V_{IN} = 0V, V_{CCO} = 3.0V to 3.465V	2.4	–	10.8	kΩ
		V_{IN} = 0V, V_{CCO} = 2.3V to 2.7V	2.7	–	11.8	kΩ
		V_{IN} = 0V, V_{CCO} = 1.7V to 1.9V	4.3	–	20.2	kΩ
		V_{IN} = 0V, V_{CCO} =1.4V to 1.6V	5.0	–	25.9	kΩ
		V_{IN} = 0V, V_{CCO} = 1.14V to 1.26V	5.5	–	32.0	kΩ
I_{RPD} (2)	Current through pull-down resistor at User I/O, Dual-Purpose, Input-only, and Dedicated pins	V_{IN} = V_{CCO}	0.10	–	0.75	mA
R_{PD} (2)	Equivalent pull-down resistor value at User I/O, Dual-Purpose, Input-only, and Dedicated pins (based on I_{RPD} per Note 2)	V_{IN} = V_{CCO} = 3.0V to 3.465V	4.0	–	34.5	kΩ
		V_{IN} = V_{CCO} = 2.3V to 2.7V	3.0	–	27.0	kΩ
		V_{IN} = V_{CCO} = 1.7V to 1.9V	2.3	–	19.0	kΩ
		V_{IN} = V_{CCO} = 1.4V to 1.6V	1.8	–	16.0	kΩ
		V_{IN} = V_{CCO} = 1.14V to 1.26V	1.5	–	12.6	kΩ
I_{REF}	V_{REF} current per pin	All V_{CCO} levels	–10	–	+10	µA
C_{IN}	Input capacitance	–	–	–	10	pF
R_{DT}	Resistance of optional differential termination circuit within a differential I/O pair. Not available on Input-only pairs.	V_{OCM} Min ≤ V_{ICM} ≤ V_{OCM} Max V_{OD} Min ≤ V_{ID} ≤ V_{OD} Max V_{CCO} = 2.5V	–	120	–	Ω

Notes:

1. The numbers in this table are based on the conditions set forth in Table 77.
2. This parameter is based on characterization. The pull-up resistance R_{PU} = V_{CCO} / I_{RPU}. The pull-down resistance R_{PD} = V_{IN} / I_{RPD}.
3. For single-ended signals that are placed on a differential-capable I/O, V_{IN} of –0.2V to –0.5V is supported but can cause increased leakage between the two pins. See *Parasitic Leakage* in UG331, *Spartan-3 Generation FPGA User Guide*.

Differential I/O Standards

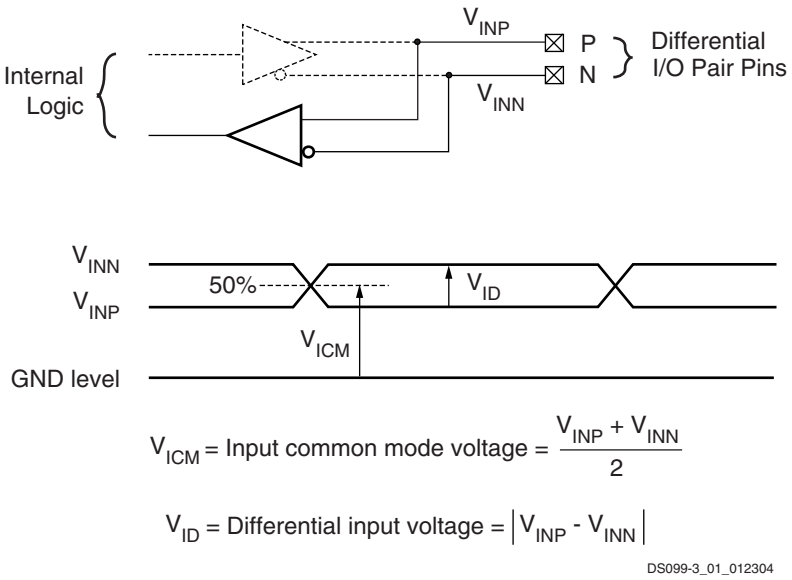

Figure 69: **Differential Input Voltages**

Table 82: **Recommended Operating Conditions for User I/Os Using Differential Signal Standards**

IOSTANDARD Attribute	V_{CCO} for Drivers[1]			V_{ID}			V_{ICM}		
	Min (V)	Nom (V)	Max (V)	Min (mV)	Nom (mV)	Max (mV)	Min (V)	Nom (V)	Max (V)
LVDS_25	2.375	2.50	2.625	100	350	600	0.30	1.25	2.20
BLVDS_25	2.375	2.50	2.625	100	350	600	0.30	1.25	2.20
MINI_LVDS_25	2.375	2.50	2.625	200	-	600	0.30	-	2.2
LVPECL_25[2]	Inputs Only			100	800	1000	0.5	1.2	2.0
RSDS_25	2.375	2.50	2.625	100	200	-	0.3	1.20	1.4
DIFF_HSTL_I_18	1.7	1.8	1.9	100	-	-	0.8	-	1.1
DIFF_HSTL_III_18	1.7	1.8	1.9	100	-	-	0.8	-	1.1
DIFF_SSTL18_I	1.7	1.8	1.9	100	-	-	0.7	-	1.1
DIFF_SSTL2_I	2.3	2.5	2.7	100	-	-	1.0	-	1.5

Notes:

1. The V_{CCO} rails supply only differential output drivers, not input circuits.
2. V_{REF} inputs are not used for any of the differential I/O standards.

Switching Characteristics

All Spartan-3E FPGAs ship in two speed grades: -4 and the higher performance -5. Switching characteristics in this document may be designated as Advance, Preliminary, or Production, as shown in Table 84. Each category is defined as follows:

Advance: These specifications are based on simulations only and are typically available soon after establishing FPGA specifications. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These specifications are based on complete early silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting preliminary delays is greatly reduced compared to Advance data.

Production: These specifications are approved once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Software Version Requirements

Production-quality systems must use FPGA designs compiled using a speed file designated as PRODUCTION status. FPGAs designs using a less mature speed file designation should only be used during system prototyping or pre-production qualification. FPGA designs with speed files designated as Advance or Preliminary should not be used in a production-quality system.

Whenever a speed file designation changes, as a device matures toward Production status, rerun the latest Xilinx ISE software on the FPGA design to ensure that the FPGA design incorporates the latest timing information and software updates.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all Spartan-3E devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.**

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Timing parameters and their representative values are selected for inclusion below either because they are important as general design requirements or they indicate fundamental device performance characteristics. The Spartan-3E speed files (v1.27), part of the Xilinx Development Software, are the original source for many but not all of the values. The speed grade designations for these files are shown in Table 84. For more complete, more precise, and worst-case data, use the values reported by the Xilinx static timing analyzer (TRACE in the Xilinx development software) and back-annotated to the simulation netlist.

Table 84: **Spartan-3E v1.27 Speed Grade Designations**

Device	Advance	Preliminary	Production
XC3S100E			-MIN, -4, -5
XC3S250E			-MIN, -4, -5
XC3S500E			-MIN, -4, -5
XC3S1200E			-MIN, -4, -5
XC3S1600E			-MIN, -4, -5

Table 85 provides the history of the Spartan-3E speed files since all devices reached Production status.

Table 85: **Spartan-3E Speed File Version History**

Version	ISE Release	Description
1.27	9.2.03i	Added XA Automotive.
1.26	8.2.02i	Added -0/-MIN speed grade, which includes minimum values.
1.25	8.2.01i	Added XA Automotive devices to speed file. Improved model for left and right DCMs.
1.23	8.2i	Updated input setup/hold values based on default IFD_DELAY_VALUE settings.
1.21	8.1.03i	All Spartan-3E FPGAs and all speed grades elevated to Production status.

Table 99: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	-5		-4		Units
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{SHCKO}	Time from the active edge at the CLK input to data appearing on the distributed RAM output	-	2.05	-	2.35	ns
Setup Times						
T_{DS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the distributed RAM	0.40	-	0.46	-	ns
T_{AS}	Setup time of the F/G address inputs before the active transition at the CLK input of the distributed RAM	0.46	-	0.52	-	ns
T_{WS}	Setup time of the write enable input before the active transition at the CLK input of the distributed RAM	0.34	-	0.40	-	ns
Hold Times						
T_{DH}	Hold time of the BX, BY data inputs after the active transition at the CLK input of the distributed RAM	0.13	-	0.15	-	ns
T_{AH}, T_{WH}	Hold time of the F/G address inputs or the write enable input after the active transition at the CLK input of the distributed RAM	0	-	0	-	ns
Clock Pulse Width						
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	0.88	-	1.01	-	ns

Table 100: **CLB Shift Register Switching Characteristics**

Symbol	Description	-5		-4		Units
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{REG}	Time from the active edge at the CLK input to data appearing on the shift register output	-	3.62	-	4.16	ns
Setup Times						
T_{SRLDS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the shift register	0.41	-	0.46	-	ns
Hold Times						
T_{SRLDH}	Hold time of the BX or BY data input after the active transition at the CLK input of the shift register	0.14	-	0.16	-	ns
Clock Pulse Width						
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	0.88	-	1.01	-	ns

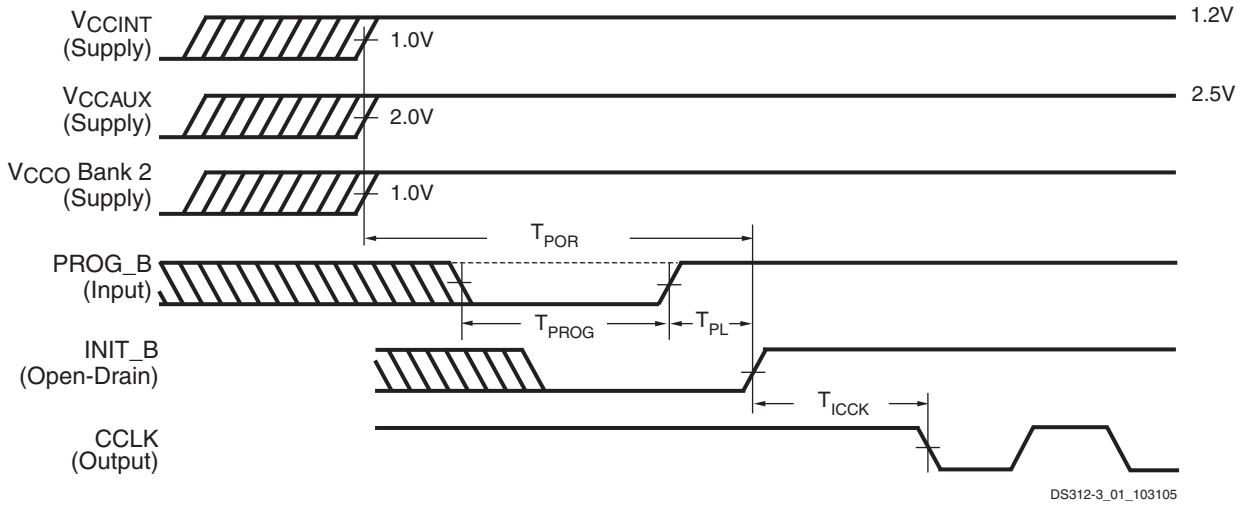
Clock Buffer/Multiplexer Switching Characteristics

Table 101: **Clock Distribution Switching Characteristics**

Description	Symbol	Maximum		Units
		Speed Grade		
		-5	-4	
Global clock buffer (BUFG, BUFGMUX, BUFGCE) I input to O-output delay	T_{GIO}	1.46	1.46	ns
Global clock multiplexer (BUFGMUX) select S-input setup to I0 and I1 inputs. Same as BUFGCE enable CE-input	T_{GSI}	0.55	0.63	ns
Frequency of signals distributed on global buffers (all sides)	F_{BUFG}	333	311	MHz

Configuration and JTAG Timing

General Configuration Power-On/Reconfigure Timing



Notes:

1. The V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies may be applied in any order.
2. The Low-going pulse on PROG_B is optional after power-on but necessary for reconfiguration without a power cycle.
3. The rising edge of INIT_B samples the voltage levels applied to the mode pins (M0 - M2).

Figure 73: **Waveforms for Power-On and the Beginning of Configuration**

Table 111: **Power-On Timing and the Beginning of Configuration**

Symbol	Description	Device	All Speed Grades		Units
			Min	Max	
T_{POR}(2)	The time from the application of V_{CCINT}, V_{CCAUX}, and V_{CCO} Bank 2 supply voltage ramps (whichever occurs last) to the rising transition of the INIT_B pin	XC3S100E	-	5	ms
		XC3S250E	-	5	ms
		XC3S500E	-	5	ms
		XC3S1200E	-	5	ms
		XC3S1600E	-	7	ms
T_{PROG}	The width of the low-going pulse on the PROG_B pin	All	0.5	-	µs
T_{PL}(2)	The time from the rising edge of the PROG_B pin to the rising transition on the INIT_B pin	XC3S100E	-	0.5	ms
		XC3S250E	-	0.5	ms
		XC3S500E	-	1	ms
		XC3S1200E	-	2	ms
		XC3S1600E	-	2	ms
T_{INIT}	Minimum Low pulse width on INIT_B output	All	250	-	ns
T_{ICCK}(3)	The time from the rising edge of the INIT_B pin to the generation of the configuration clock signal at the CCLK output pin	All	0.5	4.0	µs

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 77. This means power must be applied to all V_{CCINT}, V_{CCO}, and V_{CCAUX} lines.
2. Power-on reset and the clearing of configuration memory occurs during this period.
3. This specification applies only to the Master Serial, SPI, BPI-Up, and BPI-Down modes.

Table 121: **Configuration Timing Requirements for Attached Parallel NOR Flash**

Symbol	Description	Requirement	Units
T_{CE} (t_{ELQV})	Parallel NOR Flash PROM chip-select time	$T_{CE} \leq T_{INITADDR}$	ns
T_{OE} (t_{GLQV})	Parallel NOR Flash PROM output-enable time	$T_{OE} \leq T_{INITADDR}$	ns
T_{ACC} (t_{AVQV})	Parallel NOR Flash PROM read access time	$T_{ACC} \leq 0.5\,T_{CCLKn(min)} - T_{CCO} - T_{DCC} - PCB$	ns
T_{BYTE} (t_{FLQV}, t_{FHQV})	For x8/x16 PROMs only: BYTE# to output valid time(3)	$T_{BYTE} \leq T_{INITADDR}$	ns

Notes:

1. These requirements are for successful FPGA configuration in BPI mode, where the FPGA provides the CCLK frequency. The post configuration timing can be different to support the specific needs of the application loaded int o the FPGA and the resulting clock source.
2. Subtract additional printed circuit board routing delay as required by the application.
3. The initial BYTE# timing can be extended using an external, appropriately sized pull-down resistor on the FPGA's LDC2 pin. The resistor value also depends on whether the FPGA's HSWAP pin is High or Low.

Table 122: **MultiBoot Trigger (MBT) Timing**

Symbol	Description	Minimum	Maximum	Units
T_{MBT}	MultiBoot Trigger (MBT) Low pulse width required to initiate MultiBoot reconfiguration	300	∞	ns

Notes:

1. MultiBoot re-configuration starts on the rising edge after MBT is Low for at least the prescribed minimum period.

Table 133: **CP132 Package Pinout *(Cont'd)***

Bank	XC3S100E Pin Name	XC3S250E XC3S500E Pin Name	CP132 Ball	Type
0	VCCO_0	VCCO_0	B10	VCCO
1	IO/A0	IO/A0	F12	DUAL
1	IO/VREF_1	IO/VREF_1	K13	VREF
1	IO_L01N_1/A15	IO_L01N_1/A15	N14	DUAL
1	IO_L01P_1/A16	IO_L01P_1/A16	N13	DUAL
1	IO_L02N_1/A13	IO_L02N_1/A13	M13	DUAL
1	IO_L02P_1/A14	IO_L02P_1/A14	M12	DUAL
1	IO_L03N_1/A11	IO_L03N_1/A11	L14	DUAL
1	IO_L03P_1/A12	IO_L03P_1/A12	L13	DUAL
1	IO_L04N_1/A9/RHCLK1	IO_L04N_1/A9/RHCLK1	J12	RHCLK/DUAL
1	IO_L04P_1/A10/RHCLK0	IO_L04P_1/A10/RHCLK0	K14	RHCLK/DUAL
1	IO_L05N_1/A7/RHCLK3/TRDY1	IO_L05N_1/A7/RHCLK3/TRDY1	J14	RHCLK/DUAL
1	IO_L05P_1/A8/RHCLK2	IO_L05P_1/A8/RHCLK2	J13	RHCLK/DUAL
1	IO_L06N_1/A5/RHCLK5	IO_L06N_1/A5/RHCLK5	H12	RHCLK/DUAL
1	IO_L06P_1/A6/RHCLK4/IRDY1	IO_L06P_1/A6/RHCLK4/IRDY1	H13	RHCLK/DUAL
1	IO_L07N_1/A3/RHCLK7	IO_L07N_1/A3/RHCLK7	G13	RHCLK/DUAL
1	IO_L07P_1/A4/RHCLK6	IO_L07P_1/A4/RHCLK6	G14	RHCLK/DUAL
1	IO_L08N_1/A1	IO_L08N_1/A1	F13	DUAL
1	IO_L08P_1/A2	IO_L08P_1/A2	F14	DUAL
1	IO_L09N_1/LDC0	IO_L09N_1/LDC0	D12	DUAL
1	IO_L09P_1/HDC	IO_L09P_1/HDC	D13	DUAL
1	IO_L10N_1/LDC2	IO_L10N_1/LDC2	C13	DUAL
1	IO_L10P_1/LDC1	IO_L10P_1/LDC1	C14	DUAL
1	IP/VREF_1	IP/VREF_1	G12	VREF
1	VCCO_1	VCCO_1	E13	VCCO
1	VCCO_1	VCCO_1	M14	VCCO
2	IO/D5	IO/D5	P4	DUAL
2	IO/M1	IO/M1	N7	DUAL
2	IP/VREF_2	IO/VREF_2	P11	***100E:*** VREF(INPUT) ***Others:*** VREF(I/O)
2	IO_L01N_2/INIT_B	IO_L01N_2/INIT_B	N1	DUAL
2	IO_L01P_2/CSO_B	IO_L01P_2/CSO_B	M2	DUAL
2	IO_L02N_2/MOSI/CSI_B	IO_L02N_2/MOSI/CSI_B	N2	DUAL
2	IO_L02P_2/DOUT/BUSY	IO_L02P_2/DOUT/BUSY	P1	DUAL
2	IO_L03N_2/D6/GCLK13	IO_L03N_2/D6/GCLK13	N4	DUAL/GCLK
2	IO_L03P_2/D7/GCLK12	IO_L03P_2/D7/GCLK12	M4	DUAL/GCLK
2	IO_L04N_2/D3/GCLK15	IO_L04N_2/D3/GCLK15	N5	DUAL/GCLK
2	IO_L04P_2/D4/GCLK14	IO_L04P_2/D4/GCLK14	M5	DUAL/GCLK
2	IO_L06N_2/D1/GCLK3	IO_L06N_2/D1/GCLK3	P7	DUAL/GCLK
2	IO_L06P_2/D2/GCLK2	IO_L06P_2/D2/GCLK2	P6	DUAL/GCLK
2	IO_L07N_2/DIN/D0	IO_L07N_2/DIN/D0	N8	DUAL
2	IO_L07P_2/M0	IO_L07P_2/M0	P8	DUAL
2	N.C. (◆)	IO_L08N_2/A22	M9	***100E:*** N.C. ***Others:*** DUAL

Table 143: **FT256 Package Pinout *(Cont'd)***

Bank	XC3S250E Pin Name	XC3S500E Pin Name	XC3S1200E Pin Name	FT256 Ball	Type
0	IO_L12P_0	IO_L12P_0	IO_L12P_0	E8	I/O
0	N.C. (◆)	IO_L13N_0	IO_L13N_0	C7	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O
0	N.C. (◆)	IO_L13P_0	IO_L13P_0	B7	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O
0	IO_L14N_0/VREF_0	IO_L14N_0/VREF_0	IO_L14N_0/VREF_0	D7	VREF
0	IO_L14P_0	IO_L14P_0	IO_L14P_0	E7	I/O
0	IO_L15N_0	IO_L15N_0	IO_L15N_0	D6	I/O
0	IO_L15P_0	IO_L15P_0	IO_L15P_0	C6	I/O
0	IO_L17N_0/VREF_0	IO_L17N_0/VREF_0	IO_L17N_0/VREF_0	A4	VREF
0	IO_L17P_0	IO_L17P_0	IO_L17P_0	A5	I/O
0	IO_L18N_0	IO_L18N_0	IO_L18N_0	C4	I/O
0	IO_L18P_0	IO_L18P_0	IO_L18P_0	C5	I/O
0	IO_L19N_0/HSWAP	IO_L19N_0/HSWAP	IO_L19N_0/HSWAP	B3	DUAL
0	IO_L19P_0	IO_L19P_0	IO_L19P_0	C3	I/O
0	IP	IP	IP	A3	INPUT
0	IP	IP	IP	C13	INPUT
0	IP_L02N_0	IP_L02N_0	IP_L02N_0	C12	INPUT
0	IP_L02P_0	IP_L02P_0	IP_L02P_0	D12	INPUT
0	IP_L07N_0	IP_L07N_0	IP_L07N_0	C9	INPUT
0	IP_L07P_0	IP_L07P_0	IP_L07P_0	C10	INPUT
0	IP_L10N_0/GCLK9	IP_L10N_0/GCLK9	IP_L10N_0/GCLK9	B8	GCLK
0	IP_L10P_0/GCLK8	IP_L10P_0/GCLK8	IP_L10P_0/GCLK8	A8	GCLK
0	IP_L16N_0	IP_L16N_0	IP_L16N_0	E6	INPUT
0	IP_L16P_0	IP_L16P_0	IP_L16P_0	D5	INPUT
0	VCCO_0	VCCO_0	VCCO_0	B5	VCCO
0	VCCO_0	VCCO_0	VCCO_0	B12	VCCO
0	VCCO_0	VCCO_0	VCCO_0	F7	VCCO
0	VCCO_0	VCCO_0	VCCO_0	F10	VCCO
1	IO_L01N_1/A15	IO_L01N_1/A15	IO_L01N_1/A15	R15	DUAL
1	IO_L01P_1/A16	IO_L01P_1/A16	IO_L01P_1/A16	R16	DUAL
1	IO_L02N_1/A13	IO_L02N_1/A13	IO_L02N_1/A13	P15	DUAL
1	IO_L02P_1/A14	IO_L02P_1/A14	IO_L02P_1/A14	P16	DUAL
1	N.C. (◆)	IO_L03N_1/VREF_1	IO_L03N_1/VREF_1	N15	***250E:*** N.C. ***500E:*** VREF ***1200E:*** VREF
1	N.C. (◆)	IO_L03P_1	IO_L03P_1	N14	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O
1	IO_L04N_1/VREF_1	IO_L04N_1/VREF_1	IO_L04N_1/VREF_1	M16	VREF
1	IO_L04P_1	IO_L04P_1	IO_L04P_1	N16	I/O
1	N.C. (◆)	IO_L05N_1	IO_L05N_1	L13	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O

FG320: 320-ball Fine-pitch Ball Grid Array

The 320-ball fine-pitch ball grid array package, FG320, supports three different Spartan-3E FPGAs, including the XC3S500E, the XC3S1200E, and the XC3S1600E, as shown in Table 148 and Figure 86.

The FG320 package is an 18 x 18 array of solder balls minus the four center balls.

Table 148 lists all the package pins. They are sorted by bank number and then by pin name of the largest device. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The highlighted rows indicate pinout differences between the XC3S500E, the XC3S1200E, and the XC3S1600E FPGAs. The XC3S500E has 18 unconnected balls, indicated as N.C. (No Connection) in Table 148 and with the black diamond character (◆) in Table 148 and Figure 86.

If the table row is highlighted in tan, then this is an instance where an unconnected pin on the XC3S500E FPGA maps to a VREF pin on the XC3S1200E and XC3S1600E FPGA. If the FPGA application uses an I/O standard that requires a VREF voltage reference, connect the highlighted pin to the VREF voltage supply, even though this does not actually connect to the XC3S500E FPGA. This VREF connection on the board allows future migration to the larger devices without modifying the printed-circuit board.

All other balls have nearly identical functionality on all three devices. Table 147 summarizes the Spartan-3E footprint migration differences for the FG320 package.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx web site at:

http://www.xilinx.com/support/documentation/data_sheets/s3e_pin.zip

Pinout Table

Table 148: **FG320 Package Pinout**

Bank	XC3S500E Pin Name	XC3S1200E Pin Name	XC3S1600E Pin Name	FG320 Ball	Type
0	IP	IO	IO	A7	**500E:** INPUT **1200E:** I/O **1600E:** I/O
0	IO	IO	IO	A8	I/O
0	IO	IO	IO	A11	I/O
0	N.C. (◆)	IO	IO	A12	**500E:** N.C. **1200E:** I/O **1600E:** I/O
0	IO	IO	IO	C4	I/O
0	IP	IO	IO	D13	**500E:** INPUT **1200E:** I/O **1600E:** I/O
0	IO	IO	IO	E13	I/O
0	IO	IO	IO	G9	I/O
0	IO/VREF_0	IO/VREF_0	IO/VREF_0	B11	VREF
0	IO_L01N_0	IO_L01N_0	IO_L01N_0	A16	I/O
0	IO_L01P_0	IO_L01P_0	IO_L01P_0	B16	I/O
0	IO_L03N_0/VREF_0	IO_L03N_0/VREF_0	IO_L03N_0/VREF_0	C14	VREF
0	IO_L03P_0	IO_L03P_0	IO_L03P_0	D14	I/O
0	IO_L04N_0	IO_L04N_0	IO_L04N_0	A14	I/O
0	IO_L04P_0	IO_L04P_0	IO_L04P_0	B14	I/O
0	IO_L05N_0/VREF_0	IO_L05N_0/VREF_0	IO_L05N_0/VREF_0	B13	VREF
0	IO_L05P_0	IO_L05P_0	IO_L05P_0	A13	I/O
0	IO_L06N_0	IO_L06N_0	IO_L06N_0	E12	I/O
0	IO_L06P_0	IO_L06P_0	IO_L06P_0	F12	I/O
0	IO_L08N_0	IO_L08N_0	IO_L08N_0	F11	I/O

Table 154: **FG484 Package Pinout *(Cont'd)***

Bank	XC3S1600E Pin Name	FG484 Ball	Type
3	IO_L11N_3	H1	I/O
3	IO_L11P_3	J1	I/O
3	IO_L12N_3	J6	I/O
3	IO_L12P_3	J5	I/O
3	IO_L13N_3/VREF_3	J3	VREF
3	IO_L13P_3	K3	I/O
3	IO_L14N_3	J8	I/O
3	IO_L14P_3	K8	I/O
3	IO_L15N_3	K4	I/O
3	IO_L15P_3	K5	I/O
3	IO_L16N_3	K1	I/O
3	IO_L16P_3	L1	I/O
3	IO_L17N_3	L7	I/O
3	IO_L17P_3	K7	I/O
3	IO_L18N_3/LHCLK1	L5	LHCLK
3	IO_L18P_3/LHCLK0	M5	LHCLK
3	IO_L19N_3/LHCLK3/IRDY2	M8	LHCLK
3	IO_L19P_3/LHCLK2	L8	LHCLK
3	IO_L20N_3/LHCLK5	N1	LHCLK
3	IO_L20P_3/LHCLK4/TRDY2	M1	LHCLK
3	IO_L21N_3/LHCLK7	M4	LHCLK
3	IO_L21P_3/LHCLK6	M3	LHCLK
3	IO_L22N_3	N6	I/O
3	IO_L22P_3	N7	I/O
3	IO_L23N_3	P8	I/O
3	IO_L23P_3	N8	I/O
3	IO_L24N_3/VREF_3	N4	VREF
3	IO_L24P_3	N5	I/O
3	IO_L25N_3	P2	I/O
3	IO_L25P_3	P1	I/O
3	IO_L26N_3	R7	I/O
3	IO_L26P_3	P7	I/O
3	IO_L27N_3	P6	I/O
3	IO_L27P_3	P5	I/O
3	IO_L28N_3	R2	I/O
3	IO_L28P_3	R1	I/O
3	IO_L29N_3	R3	I/O
3	IO_L29P_3	R4	I/O
3	IO_L30N_3	T6	I/O
3	IO_L30P_3	R6	I/O
3	IO_L31N_3	U2	I/O
3	IO_L31P_3	U1	I/O
3	IO_L32N_3	T4	I/O
3	IO_L32P_3	T5	I/O

Table 154: **FG484 Package Pinout *(Cont'd)***

Bank	XC3S1600E Pin Name	FG484 Ball	Type
3	IO_L33N_3	W1	I/O
3	IO_L33P_3	V1	I/O
3	IO_L34N_3	U4	I/O
3	IO_L34P_3	U3	I/O
3	IO_L35N_3	V4	I/O
3	IO_L35P_3	V3	I/O
3	IO_L36N_3/VREF_3	W3	VREF
3	IO_L36P_3	W2	I/O
3	IO_L37N_3	Y2	I/O
3	IO_L37P_3	Y1	I/O
3	IO_L38N_3	AA1	I/O
3	IO_L38P_3	AA2	I/O
3	IP	F2	INPUT
3	IP	F5	INPUT
3	IP	G3	INPUT
3	IP	H7	INPUT
3	IP	J7	INPUT
3	IP	K2	INPUT
3	IP	K6	INPUT
3	IP	M2	INPUT
3	IP	M6	INPUT
3	IP	N3	INPUT
3	IP	P3	INPUT
3	IP	R8	INPUT
3	IP	T1	INPUT
3	IP	T7	INPUT
3	IP	U5	INPUT
3	IP	W4	INPUT
3	IP/VREF_3	L3	VREF
3	IP/VREF_3	T3	VREF
3	VCCO_3	E2	VCCO
3	VCCO_3	H6	VCCO
3	VCCO_3	J2	VCCO
3	VCCO_3	M7	VCCO
3	VCCO_3	N2	VCCO
3	VCCO_3	R5	VCCO
3	VCCO_3	V2	VCCO
GND	GND	A1	GND
GND	GND	A11	GND
GND	GND	A22	GND
GND	GND	B7	GND
GND	GND	B16	GND
GND	GND	C3	GND
GND	GND	C20	GND