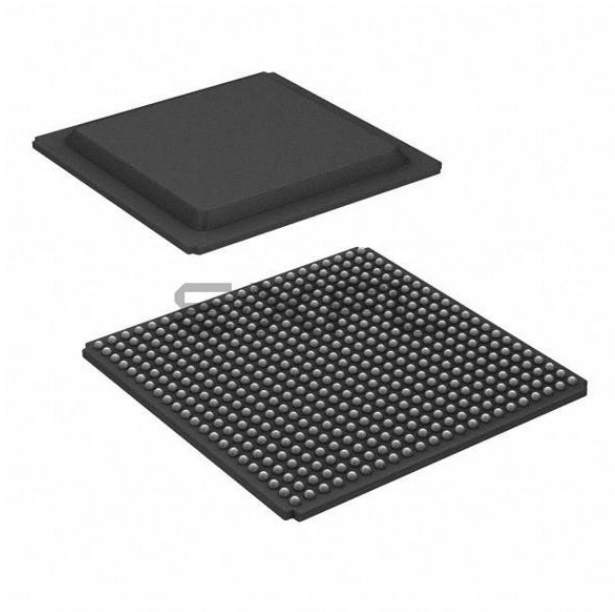
AMD Xilinx - XC3S1600E-5FGG484C Datasheet



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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	3688
Number of Logic Elements/Cells	33192
Total RAM Bits	663552
Number of I/O	376
Number of Gates	1600000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s1600e-5fgg484c

Architectural Overview

The Spartan-3E family architecture consists of five fundamental programmable functional elements:

- **Configurable Logic Blocks (CLBs)** contain flexible Look-Up Tables (LUTs) that implement logic plus storage elements used as flip-flops or latches. CLBs perform a wide variety of logical functions as well as store data.
- **Input/Output Blocks (IOBs)** control the flow of data between the I/O pins and the internal logic of the device. Each IOB supports bidirectional data flow plus 3-state operation. Supports a variety of signal standards, including four high-performance differential standards. Double Data-Rate (DDR) registers are included.
- **Block RAM** provides data storage in the form of 18-Kbit dual-port blocks.
- **Multiplier Blocks** accept two 18-bit binary numbers as inputs and calculate the product.
- **Digital Clock Manager (DCM) Blocks** provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase-shifting clock signals.

These elements are organized as shown in Figure 1. A ring of IOBs surrounds a regular array of CLBs. Each device has two columns of block RAM except for the XC3S100E, which has one column. Each RAM column consists of several 18-Kbit RAM blocks. Each block RAM is associated with a dedicated multiplier. The DCMs are positioned in the center with two at the top and two at the bottom of the device. The XC3S100E has only one DCM at the top and bottom, while the XC3S1200E and XC3S1600E add two DCMs in the middle of the left and right sides.

The Spartan-3E family features a rich network of traces that interconnect all five functional elements, transmitting signals among them. Each functional element has an associated switch matrix that permits multiple connections to the routing.

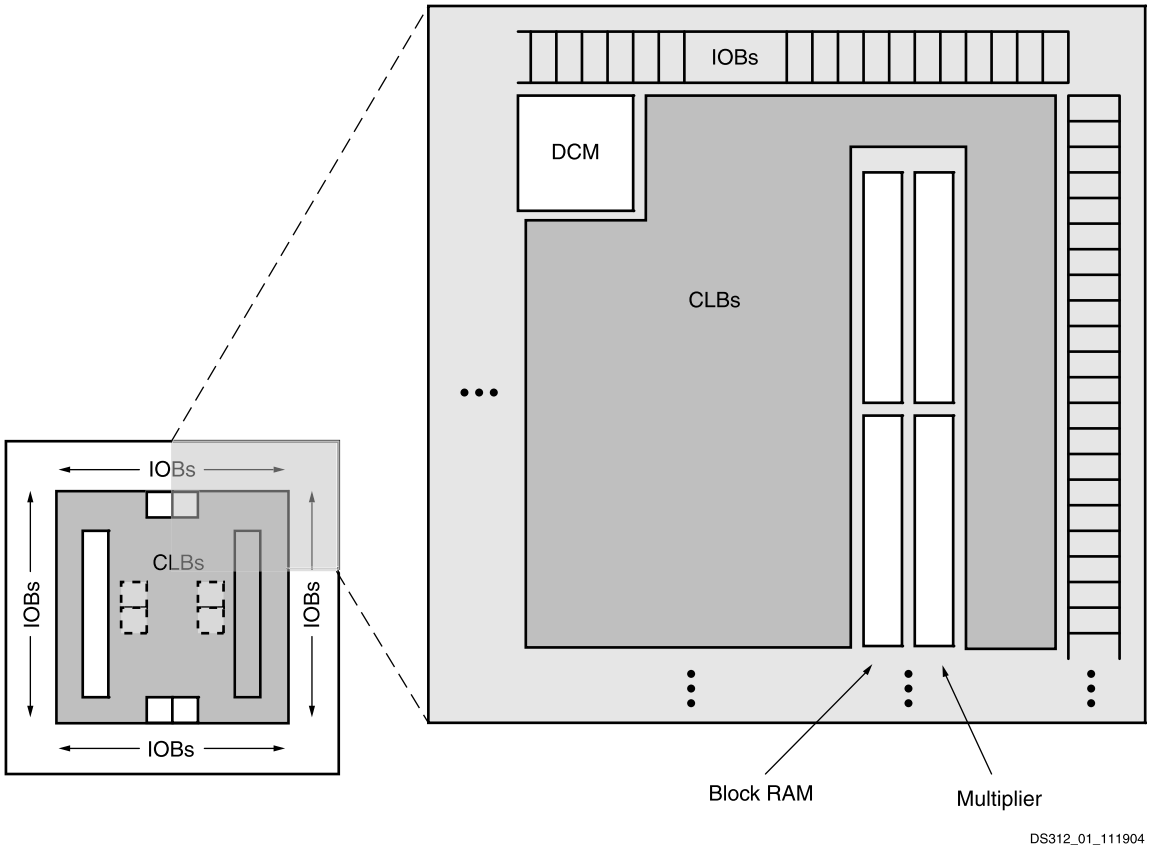


Figure 1: **Spartan-3E Family Architecture**

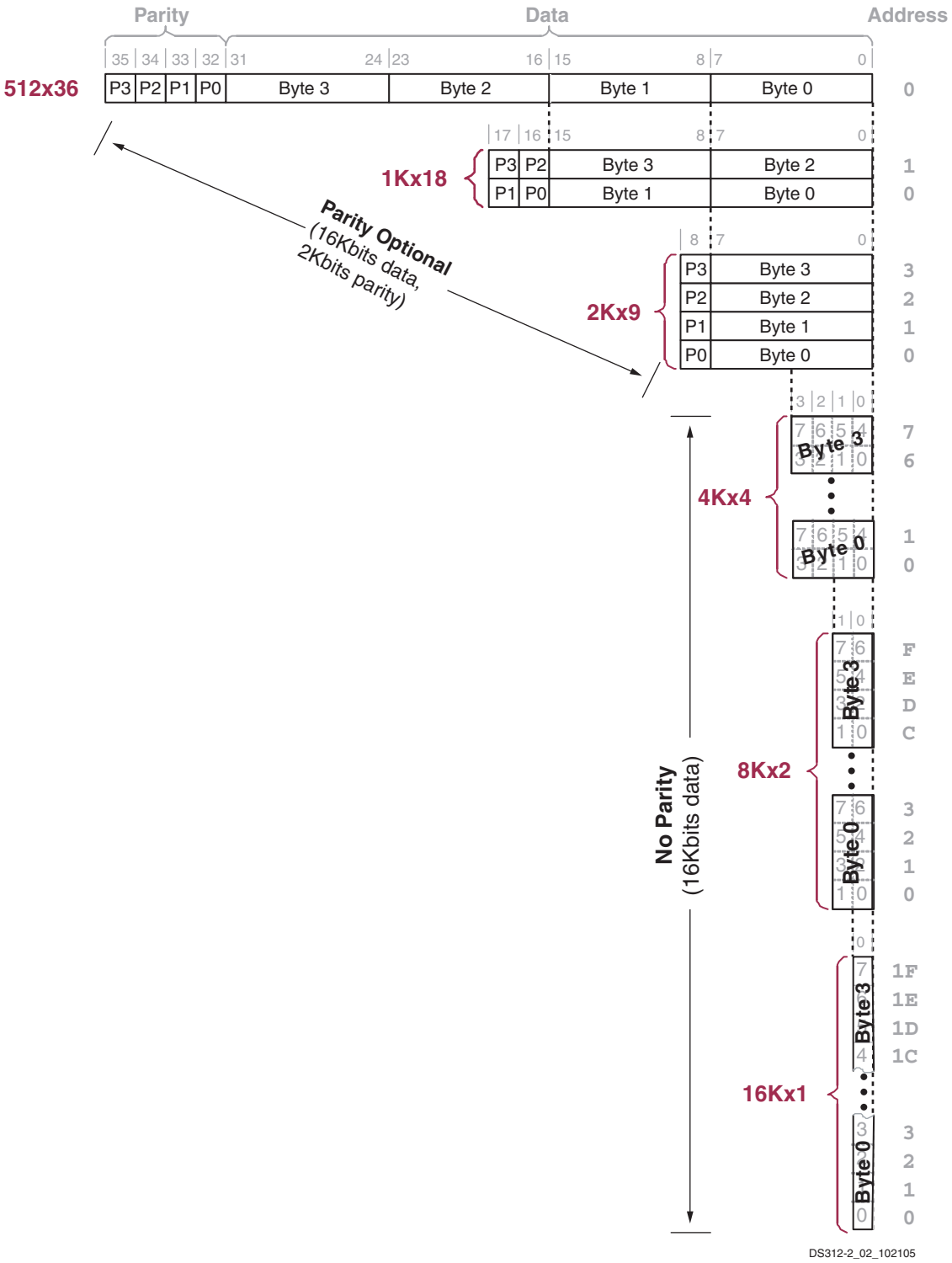


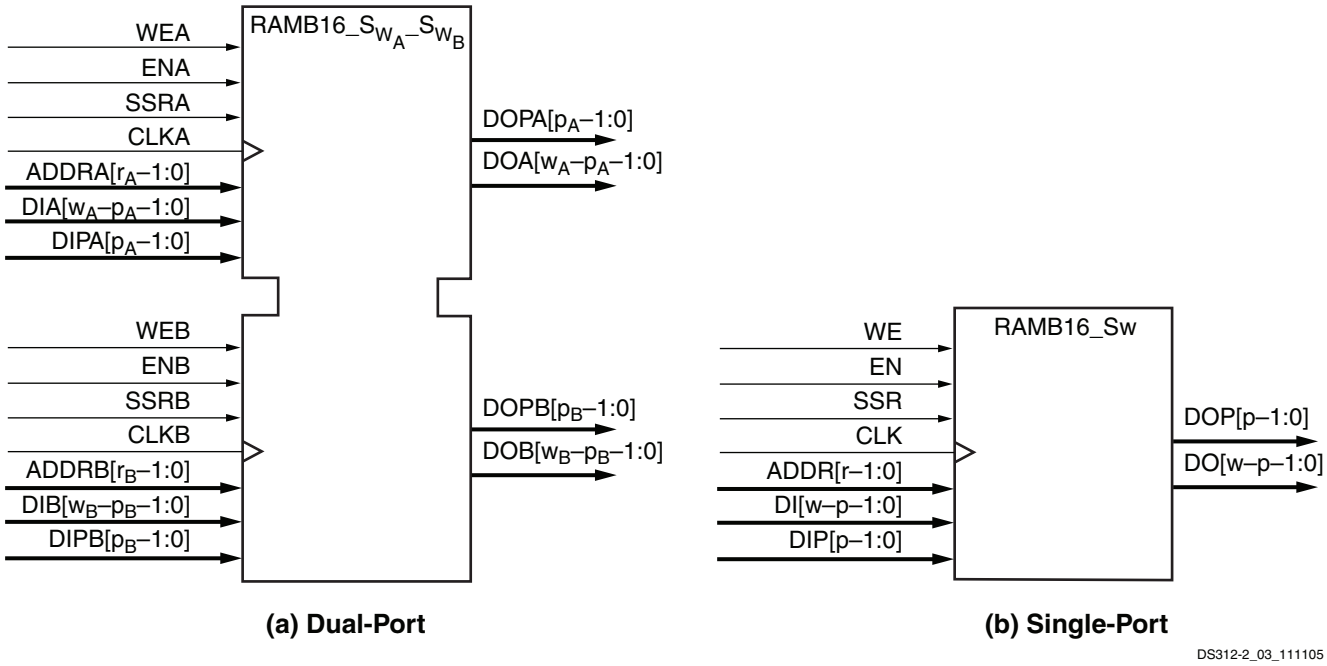
Figure 31: **Data Organization and Bus-matching Operation with Different Port Widths on Port A and Port B**

Block RAM Port Signal Definitions

Representations of the dual-port primitive RAMB16_S[w_A]_S[w_B] and the single-port primitive RAMB16_S[w] with their associated signals are shown in Figure 32a and Figure 32b, respectively. These signals are defined in Table 23. The control signals (WE, EN, CLK, and SSR) on the block RAM are active High. However, optional inverters on the control signals change the polarity of the active edge to active Low.

Design Note

Whenever a block RAM port is enabled (ENA or ENB = High), all address transitions must meet the data sheet setup and hold times with respect to the port clock (CLKA or CLKB), as shown in Table 103, page 138.This requirement must be met even if the RAM read output is of no interest.



Notes:

1. w_A and w_B are integers representing the total data path width (i.e., data bits plus parity bits) at Ports A and B, respectively.
2. p_A and p_B are integers that indicate the number of data path lines serving as parity bits.
3. r_A and r_B are integers representing the address bus width at ports A and B, respectively.
4. The control signals CLK, WE, EN, and SSR on both ports have the option of inverted polarity.

Figure 32: **Block RAM Primitives**

Table 23: **Block RAM Port Signals**

Signal Description	Port A Signal Name	Port B Signal Name	Direction	Function
Address Bus	ADDRA	ADDRB	Input	The Address Bus selects a memory location for read or write operations. The width (w) of the port's associated data path determines the number of available address lines (r), as per Table 22. Whenever a port is enabled (ENA or ENB = High), address transitions must meet the data sheet setup and hold times with respect to the port clock (CLKA or CLKB), as shown in Table 103, page 138.This requirement must be met even if the RAM read output is of no interest.
Data Input Bus	DIA	DIB	Input	Data at the DI input bus is written to the RAM location specified by the address input bus (ADDR) during the active edge of the CLK input, when the clock enable (EN) and write enable (WE) inputs are active. It is possible to configure a port's DI input bus width (w-p) based on Table 22. This selection applies to both the DI and DO paths of a given port.
Parity Data Input(s)	DIPA	DIPB	Input	Parity inputs represent additional bits included in the data input path. Although referred to herein as "parity" bits, the parity inputs and outputs have no special functionality for generating or checking parity and can be used as additional data bits. The number of parity bits 'p' included in the DI (same as for the DO bus) depends on a port's total data path width (w). See Table 22.
Data Output Bus	DOA	DOB	Output	Data is written to the DO output bus from the RAM location specified by the address input bus, ADDR. See the DI signal description for DO port width configurations. Basic data access occurs on the active edge of the CLK when WE is inactive and EN is active. The DO outputs mirror the data stored in the address ADDR memory location. Data access with WE active if the WRITE_MODE attribute is set to the value: WRITE_FIRST, which accesses data after the write takes place. READ_FIRST accesses data before the write occurs. A third attribute, NO_CHANGE, latches the DO outputs upon the assertion of WE. See Block RAM Data Operations for details on the WRITE_MODE attribute.
Parity Data Output(s)	DOPA	DOPB	Output	Parity outputs represent additional bits included in the data input path. The number of parity bits 'p' included in the DI bus (same as for the DO bus) depends on a port's total data path width (w). See the DIP signal description for configuration details.
Write Enable	WEA	WEB	Input	When asserted together with EN, this input enables the writing of data to the RAM. When WE is inactive with EN asserted, read operations are still possible. In this case, a latch passes data from the addressed memory location to the DO outputs.
Clock Enable	ENA	ENB	Input	When asserted, this input enables the CLK signal to perform read and write operations to the block RAM. When inactive, the block RAM does not perform any read or write operations.
Set/Reset	SSRA	SSRB	Input	When asserted, this pin forces the DO output latch to the value of the SRVAL attribute. It is synchronized to the CLK signal.
Clock	CLKA	CLKB	Input	This input accepts the clock signal to which read and write operations are synchronized. All associated port inputs are required to meet setup times with respect to the clock signal's active edge. The data output bus responds after a clock-to-out delay referenced to the clock signal's active edge.

Table 31: **Direct Clock Input and Optional External Feedback to Left-Edge DCMs (XC3S1200E and XC3S1600E)**

Diff. Clock		Single-Ended Pin Number by Package Type								Left Edge		
		VQ100	CP132	TQ144	PQ208	FT256	FG320	FG400	FG484	LHCLK	DCM/BUFGMUX	
											BUFGMUX_X0Y5	D
											BUFGMUX_X0Y4	C
Pair	P	P9	F3	P14	P22	H5	J5	K3	M5	LHCLK0	DCM_X0Y2	Clock Lines
	N	P10	F2	P15	P23	H6	J4	K2	L5	LHCLK1		
Pair	P	P11	F1	P16	P24	H3	J1	K7	L8	LHCLK2		
	N	P12	G1	P17	P25	H4	J2	L7	M8	LHCLK3		
											BUFGMUX_X0Y3	B
											BUFGMUX_X0Y2	A
											BUFGMUX_X0Y9	H
											BUFGMUX_X0Y8	G
Pair	P	P15	G3	P20	P28	J2	K3	M1	M1	LHCLK4	DCM_X0Y1	Clock Lines
	N	P16	H1	P21	P29	J3	K4	L1	N1	LHCLK5		
Pair	P	P17	H2	P22	P30	J5	K6	M3	M3	LHCLK6		
	N	P18	H3	P23	P31	J4	K5	L3	M4	LHCLK7		
											BUFGMUX_X0Y7	F
											BUFGMUX_X0Y6	E

Table 32: **Direct Clock Input and Optional External Feedback to Right-Edge DCMs (XC3S1200E and XC3S1600E)**

	Right Edge		Single-Ended Pin Number by Package Type								Diff. Clock	
	DCM/BUFGMUX	RHCLK	VQ100	CP132	TQ144	PQ208	FT256	FG320	FG400	FG484		
D	BUFGMUX_X3Y5											
C	BUFGMUX_X3Y4											
Clock Lines	DCM_X3Y2	RHCLK7	P68	G13	P94	P135	H11	J14	J20	L19	N	Pair
		RHCLK6	P67	G14	P93	P134	H12	J15	K20	L18	P	
		RHCLK5	P66	H12	P92	P133	H14	J16	K14	L21	N	Pair
		RHCLK4	P65	H13	P91	P132	H15	J17	K13	L20	P	
B	BUFGMUX_X3Y3											
A	BUFGMUX_X3Y2											
H	BUFGMUX_X3Y9											
G	BUFGMUX_X3Y8											
Clock Lines	DCM_X3Y1	RHCLK3	P63	J14	P88	P129	J13	K14	L14	M16	N	Pair
		RHCLK2	P62	J13	P87	P128	J14	K15	L15	M15	P	
		RHCLK1	P61	J12	P86	P127	J16	K12	L16	M22	N	Pair
		RHCLK0	P60	K14	P85	P126	K16	K13	M16	N22	P	
F	BUFGMUX_X3Y7											
E	BUFGMUX_X3Y6											

Every FPGA input provides a possible DCM clock input, but the path is not temperature and voltage compensated like the GCLKs. Alternatively, clock signals within the FPGA optionally provide a DCM clock input via a Global Clock Multiplexer Buffer (BUFGMUX). The global clock net connects directly to the CLKIN input. The internal and external connections are shown in Figure 42a and Figure 42c, respectively.

By contrast, the clock switch matrixes on the top and bottom edges receive signals from any of the five following sources: two GCLK pins, two DCM outputs, or one Double-Line interconnect.

Table 41 indicates permissible connections between clock inputs and BUFGMUX elements. The I0-input provides the best input path to a clock buffer. The I1-input provides the secondary input for the clock multiplexer function.

The four BUFGMUX elements on the top edge are paired together and share inputs from the eight global clock inputs along the top edge. Each BUFGMUX pair connects to four of the eight global clock inputs, as shown in Figure 45. This optionally allows differential inputs to the global clock inputs without wasting a BUFGMUX element.

Table 41: **Connections from Clock Inputs to BUFGMUX Elements and Associated Quadrant Clock**

Quadrant Clock Line[1]	Left-Half BUFGMUX			Top or Bottom BUFGMUX			Right-Half BUFGMUX		
	Location[2]	I0 Input	I1 Input	Location[2]	I0 Input	I1 Input	Location[2]	I0 Input	I1 Input
H	*X0Y9*	LHCLK7	LHCLK6	*X1Y10*	GCLK7 or GCLK11	GCLK6 or GCLK10	*X3Y9*	RHCLK3	RHCLK2
G	*X0Y8*	LHCLK6	LHCLK7	*X1Y11*	GCLK6 or GCLK10	GCLK7 or GCLK11	*X3Y8*	RHCLK2	RHCLK3
F	*X0Y7*	LHCLK5	LHCLK4	*X2Y10*	GCLK5 or GCLK9	GCLK4 or GCLK8	*X3Y7*	RHCLK1	RHCLK0
E	*X0Y6*	LHCLK4	LHCLK5	*X2Y11*	GCLK4 or GCLK8	GCLK5 or GCLK9	*X3Y6*	RHCLK0	RHCLK1
D	*X0Y5*	LHCLK3	LHCLK2	*X1Y0*	GCLK3 or GCLK15	GCLK2 or GCLK14	*X3Y5*	RHCLK7	RHCLK6
C	*X0Y4*	LHCLK2	LHCLK3	*X1Y1*	GCLK2 or GCLK14	GCLK3 or GCLK15	*X3Y4*	RHCLK6	RHCLK7
B	*X0Y3*	LHCLK1	LHCLK0	*X2Y0*	GCLK1 or GCLK13	GCLK0 or GCLK12	*X3Y3*	RHCLK5	RHCLK4
A	*X0Y2*	LHCLK0	LHCLK1	*X2Y1*	GCLK0 or GCLK12	GCLK1 or GCLK13	*X3Y2*	RHCLK4	RHCLK5

Notes:

1. See Quadrant Clock Routing for connectivity details for the eight quadrant clocks.
2. See Figure 45 for specific BUFGMUX locations, and Figure 47 for information on how BUFGMUX elements drive onto a specific clock line within a quadrant.

The configuration pins also operate at other voltages by setting VCCO_2 (and VCCO_1 in BPI mode) to either 3.3V or 1.8V. The change on the V_{CCO} supply also changes the I/O characteristics, including the effective IOSTANDARD. For example, with V_{CCO} = 3.3V, the output characteristics will be similar to those of LVCMOS33, and the current when driving High, I_{OH}, increases to approximately 12 to 16 mA, while the current when driving Low, I_{OL}, remains 8 mA. At V_{CCO} = 1.8V, the output characteristics will be similar to those of LVCMOS18, and the current when driving High, I_{OH}, decreases slightly to approximately 6 to 8 mA. Again, the current when driving Low, I_{OL}, remains 8 mA. The output voltages are determined by the V_{CCO} level, LVCMOS18 for 1.8V, LVCMOS25 for 2.5V, and LVCMOS33 for 3.3V. For more details see UG332.

CCLK Design Considerations

For additional information, refer to the “Configuration Pins and Behavior during Configuration” chapter in UG332.

The FPGA’s configuration process is controlled by the CCLK configuration clock. Consequently, signal integrity of CCLK is important to guarantee successful configuration. Poor CCLK signal integrity caused by ringing or reflections might cause double-clocking, causing the configuration process to fail.

Although the CCLK frequency is relatively low, Spartan-3E FPGA output edge rates are fast. Therefore, careful attention must be paid to the CCLK signal integrity on the printed circuit board. Signal integrity simulation with IBIS is recommended. For all configuration modes except JTAG, the signal integrity must be considered at every CCLK trace destination, including the FPGA’s CCLK pin.

This analysis is especially important when the FPGA re-uses the CCLK pin as a user-I/O after configuration. In these cases, there might be unrelated devices attached to CCLK, which add additional trace length and signal destinations.

In the Master Serial, SPI, and BPI configuration modes, the FPGA drives the CCLK pin and CCLK should be treated as a full bidirectional I/O pin for signal integrity analysis. In BPI mode, CCLK is only used in multi-FPGA daisy-chains.

The best signal integrity is ensured by following these basic PCB guidelines:

- Route the CCLK signal as a 50 Ω controlled-impedance transmission line.
- Route the CCLK signal without any branching. Do not use a “star” topology.
- Keep stubs, if required, shorter than 10 mm (0.4 inches).
- Terminate the end of the CCLK transmission line.

Design Considerations for the HSWAP, M[2:0], and VS[2:0] Pins

For additional information, refer to the “Configuration Pins and Behavior during Configuration” chapter in UG332.

Unlike previous Spartan FPGA families, nearly all of the Spartan-3E dual-purpose configuration pins are available as full-featured user I/O pins after successful configuration, when the DONE output goes High.

The HSWAP pin, the mode select pins (M[2:0]), and the variant-select pins (VS[2:0]) must have valid and stable logic values at the start of configuration. VS[2:0] are only used in the SPI configuration mode. The levels on the M[2:0] pins and VS[2:0] pins are sampled when the INIT_B pin returns High. See Figure 76 for a timing example.

The HSWAP pin defines whether FPGA user I/O pins have a pull-up resistor connected to their associated V_{CCO} supply pin during configuration or not, as shown Table 48. HSWAP must be valid at the start of configuration and remain constant throughout the configuration process.

Table 48: **HSWAP Behavior**

HSWAP Value	Description
0	Pull-up resistors connect to the associated V_{CCO} supply for all user-I/O or dual-purpose I/O pins during configuration. Pull-up resistors are active until configuration completes.
1	Pull-up resistors disabled during configuration. All user-I/O or dual-purpose I/O pins are in a high-impedance state.

The Configuration section provides detailed schematics for each configuration mode. The schematics indicate the required logic values for HSWAP, M[2:0], and VS[2:0] but do not specify how the application provides the logic Low or High value. The HSWAP, M[2:0], and VS[2:0] pins can be either dedicated or reused by the FPGA application.

Dedicating the HSWAP, M[2:0], and VS[2:0] Pins

If the HSWAP, M[2:0], and VS[2:0] pins are not required by the FPGA design after configuration, simply connect these pins directly to the V_{CCO} or GND supply rail shown in the appropriate configuration schematic.

Reusing HSWAP, M[2:0], and VS[2:0] After Configuration

To reuse the HSWAP, M[2:0], and VS[2:0] pin after configuration, use pull-up or pull-down resistors to define the logic values shown in the appropriate configuration schematic.

Table 53: **Variant Select Codes for Various SPI Serial Flash PROMs**

VS2	VS1	VS0	SPI Read Command	Dummy Bytes	SPI Serial Flash Vendor	SPI Flash Family	iMPACT Programming Support
1	1	1	FAST READ (0x0B) (see Figure 53)	1	STMicroelectronics (ST)	M25Pxx M25PExx/M45PExx	Yes
					Atmel	AT45DB 'D'-Series Data Flash	Yes
						AT26 / AT25(1)	
					Intel	S33	
					Spansion *(AMD, Fujitsu)*	S25FLxxxA	
					Winbond *(NexFlash)*	NX25 / W25	
					Macronix	MX25Lxxxx	
					Silicon Storage Technology (SST)	SST25LFxxxA SST25VFxxxA	
					Programmable Microelectronics Corp. (PMC)	Pm25LVxxx	
					AMIC Technology	A25L	
					Eon Silicon Solution, Inc.	EN25	
1	0	1	READ (0x03) (see Figure 53)	0	STMicroelectronics (ST)	M25Pxx M25PExx/M45PExx	Yes
					Spansion *(AMD, Fujitsu)*	S25FLxxxA	
					Winbond *(NexFlash)*	NX25 / W25	
					Macronix	MX25Lxxxx	
					Silicon Storage Technology (SST)	SST25LFxxxA SST25VFxxxA SST25VFxxx	
					Programmable Microelectronics Corp. (PMC)	Pm25LVxxx	
1	1	0	READ ARRAY (0xE8) (see Figure 54)	4	Atmel Corporation	AT45DB DataFlash *(use only 'C' or 'D' Series for Industrial temperature range)*	Yes
Others			Reserved				

Notes:
1. See iMPACT documentation for specific device support.

WRITER NOTE: Many of the URLs in this table are obsolete or otherwise broken.

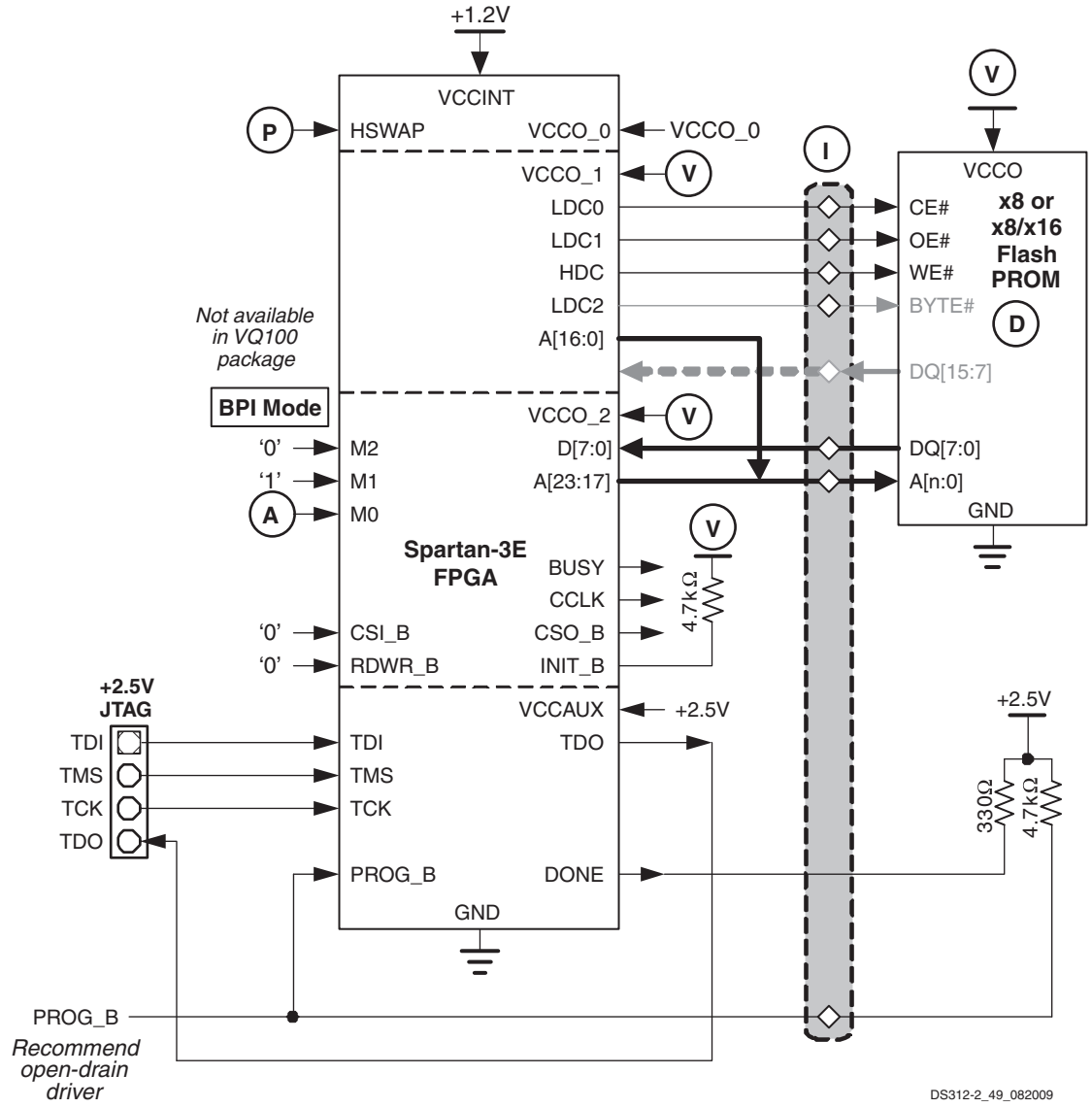


Figure 58: **Byte-wide Peripheral Interface (BPI) Mode Configured from Parallel NOR Flash PROMs**

(A) During configuration, the value of the M0 mode pin determines how the FPGA generates addresses, as shown Table 58. When M0 = 0, the FPGA generates addresses starting at 0 and increments the address on every falling CCLK edge. Conversely, when M0 = 1, the FPGA generates addresses starting at `0xFF_FFFF` (all ones) and decrements the address on every falling CCLK edge.

Table 58: **BPI Addressing Control**

M2	M1	M0	Start Address	Addressing
0	1	0	0	Incrementing
		1	`0xFF_FFFF`	Decrementing

General DC Characteristics for I/O Pins

Table 78: **General DC Characteristics of User I/O, Dual-Purpose, and Dedicated Pins**

Symbol	Description	Test Conditions	Min	Typ	Max	Units
I_L (3)	Leakage current at User I/O, Input-only, Dual-Purpose, and Dedicated pins	Driver is in a high-impedance state, V_{IN} = 0V or V_{CCO} max, sample-tested	–10	–	+10	µA
I_{RPU} (2)	Current through pull-up resistor at User I/O, Dual-Purpose, Input-only, and Dedicated pins	V_{IN} = 0V, V_{CCO} = 3.3V	–0.36	–	–1.24	mA
		V_{IN} = 0V, V_{CCO} = 2.5V	–0.22	–	–0.80	mA
		V_{IN} = 0V, V_{CCO} = 1.8V	–0.10	–	–0.42	mA
		V_{IN} = 0V, V_{CCO} = 1.5V	–0.06	–	–0.27	mA
		V_{IN} = 0V, V_{CCO} = 1.2V	–0.04	–	–0.22	mA
R_{PU} (2)	Equivalent pull-up resistor value at User I/O, Dual-Purpose, Input-only, and Dedicated pins (based on I_{RPU} per Note 2)	V_{IN} = 0V, V_{CCO} = 3.0V to 3.465V	2.4	–	10.8	kΩ
		V_{IN} = 0V, V_{CCO} = 2.3V to 2.7V	2.7	–	11.8	kΩ
		V_{IN} = 0V, V_{CCO} = 1.7V to 1.9V	4.3	–	20.2	kΩ
		V_{IN} = 0V, V_{CCO} =1.4V to 1.6V	5.0	–	25.9	kΩ
		V_{IN} = 0V, V_{CCO} = 1.14V to 1.26V	5.5	–	32.0	kΩ
I_{RPD} (2)	Current through pull-down resistor at User I/O, Dual-Purpose, Input-only, and Dedicated pins	V_{IN} = V_{CCO}	0.10	–	0.75	mA
R_{PD} (2)	Equivalent pull-down resistor value at User I/O, Dual-Purpose, Input-only, and Dedicated pins (based on I_{RPD} per Note 2)	V_{IN} = V_{CCO} = 3.0V to 3.465V	4.0	–	34.5	kΩ
		V_{IN} = V_{CCO} = 2.3V to 2.7V	3.0	–	27.0	kΩ
		V_{IN} = V_{CCO} = 1.7V to 1.9V	2.3	–	19.0	kΩ
		V_{IN} = V_{CCO} = 1.4V to 1.6V	1.8	–	16.0	kΩ
		V_{IN} = V_{CCO} = 1.14V to 1.26V	1.5	–	12.6	kΩ
I_{REF}	V_{REF} current per pin	All V_{CCO} levels	–10	–	+10	µA
C_{IN}	Input capacitance	–	–	–	10	pF
R_{DT}	Resistance of optional differential termination circuit within a differential I/O pair. Not available on Input-only pairs.	V_{OCM} Min ≤ V_{ICM} ≤ V_{OCM} Max V_{OD} Min ≤ V_{ID} ≤ V_{OD} Max V_{CCO} = 2.5V	–	120	–	Ω

Notes:

1. The numbers in this table are based on the conditions set forth in Table 77.
2. This parameter is based on characterization. The pull-up resistance R_{PU} = V_{CCO} / I_{RPU}. The pull-down resistance R_{PD} = V_{IN} / I_{RPD}.
3. For single-ended signals that are placed on a differential-capable I/O, V_{IN} of –0.2V to –0.5V is supported but can cause increased leakage between the two pins. See *Parasitic Leakage* in UG331, *Spartan-3 Generation FPGA User Guide*.

Table 90: **Propagation Times for the IOB Input Path**

Symbol	Description	Conditions	IFD_DELAY_VALUE=	Device	Speed Grade		Units
					-5	-4	
					Min	Min	
Propagation Times							
T_{IOPLI}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with no input delay programmed	LVCMOS25(2), IFD_DELAY_VALUE = 0	0	All	1.96	2.25	ns
T_{IOPLID}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with the input delay programmed	LVCMOS25(2), IFD_DELAY_VALUE = default software setting	2	XC3S100E	5.40	5.97	ns
			3	All Others	6.30	7.20	

Notes:

1. The numbers in this table are tested using the methodology presented in Table 95 and are based on the operating conditions set forth in Table 77 and Table 80.
2. This propagation time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. When this is true, *add* the appropriate Input adjustment from Table 91.

Table 91: **Input Timing Adjustments by IOSTANDARD**

Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
Single-Ended Standards			
LVTTL	0.42	0.43	ns
LVCMOS33	0.42	0.43	ns
LVCMOS25	0	0	ns
LVCMOS18	0.96	0.98	ns
LVCMOS15	0.62	0.63	ns
LVCMOS12	0.26	0.27	ns
PCI33_3	0.41	0.42	ns
PCI66_3	0.41	0.42	ns
HSTL_I_18	0.12	0.12	ns
HSTL_III_18	0.17	0.17	ns
SSTL18_I	0.30	0.30	ns
SSTL2_I	0.15	0.15	ns

Table 91: **Input Timing Adjustments by IOSTANDARD *(Cont'd)***

Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
Differential Standards			
LVDS_25	0.48	0.49	ns
BLVDS_25	0.39	0.39	ns
MINI_LVDS_25	0.48	0.49	ns
LVPECL_25	0.27	0.27	ns
RSDS_25	0.48	0.49	ns
DIFF_HSTL_I_18	0.48	0.49	ns
DIFF_HSTL_III_18	0.48	0.49	ns
DIFF_SSTL18_I	0.30	0.30	ns
DIFF_SSTL2_I	0.32	0.32	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 95 and are based on the operating conditions set forth in Table 77, Table 80, and Table 82.
2. These adjustments are used to convert input path times originally specified for the LVCMOS25 standard to times that correspond to other signal standards.

Master Serial and Slave Serial Mode Timing

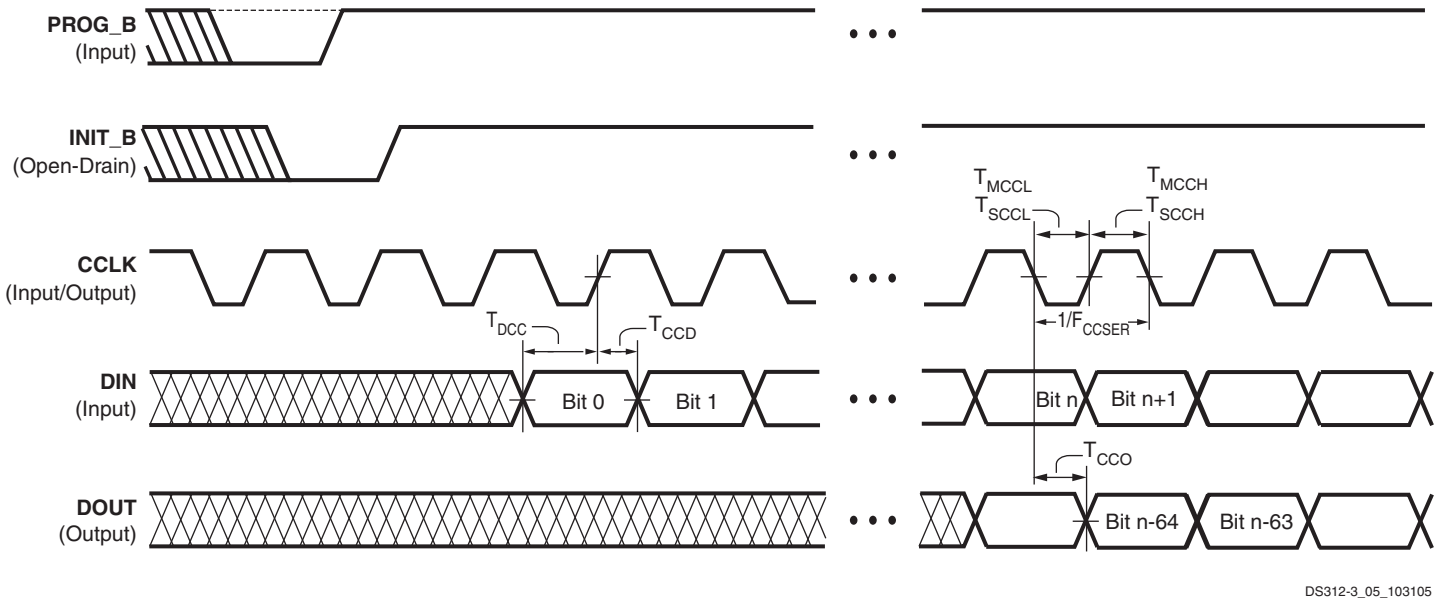


Figure 74: **Waveforms for Master Serial and Slave Serial Configuration**

Table 116: **Timing for the Master Serial and Slave Serial Configuration Modes**

Symbol	Description		Slave/ Master	All Speed Grades		Units
				Min	Max	
Clock-to-Output Times						
T_{CCO}	The time from the falling transition on the CCLK pin to data appearing at the DOUT pin		Both	1.5	10.0	ns
Setup Times						
T_{DCC}	The time from the setup of data at the DIN pin to the active edge of the CCLK pin		Both	11.0	-	ns
Hold Times						
T_{CCD}	The time from the active edge of the CCLK pin to the point when data is last held at the DIN pin		Both	0	-	ns
Clock Timing						
T_{CCH}	High pulse width at the CCLK input pin		Master	See Table 114		
			Slave	See Table 115		
T_{CCL}	Low pulse width at the CCLK input pin		Master	See Table 114		
			Slave	See Table 115		
F_{CCSER}	Frequency of the clock signal at the CCLK input pin	No bitstream compression	Slave	0	66(2)	MHz
		With bitstream compression		0	20	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 77.
2. For serial configuration with a daisy-chain of multiple FPGAs, the maximum limit is 25 MHz.

Mechanical Drawings

Detailed mechanical drawings for each package type are available from the Xilinx® web site at the specified location in Table 127.

Material Declaration Data Sheets (MDDS) are also available on the Xilinx web site for each package.

Table 127: **Xilinx Package Mechanical Drawings and Material Declaration Data Sheets**

Package	Package Drawing	MDDS
VQ100	Package Drawing	PK173_VQ100
VQG100		PK130_VQG100
CP132	Package Drawing	PK147_CP132
CPG132		PK101_CPG132
TQ144	Package Drawing	PK169_TQ144
TQG144		PK126_TQG144
PQ208	Package Drawing	PK166_PQ208
PQG208		PK123_PQG208
FT256	Package Drawing	PK158_FT256
FTG256		PK115_FTG256
FG320	Package Drawing	PK152_FG320
FGG320		PK106_FGG320
FG400	Package Drawing	PK182_FG400
FGG400		PK108_FGG400
FG484	Package Drawing	PK183_FG484
FGG484		PK110_FGG484

Package Pins by Type

Each package has three separate voltage supply inputs—VCCINT, VCCAUX, and VCCO—and a common ground return, GND. The numbers of pins dedicated to these functions vary by package, as shown in Table 128.

Table 128: **Power and Ground Supply Pins by Package**

Package	VCCINT	VCCAUX	VCCO	GND
VQ100	4	4	8	12
CP132	6	4	8	16
TQ144	4	4	9	13
PQ208	4	8	12	20
FT256	8	8	16	28
FG320	8	8	20	28
FG400	16	8	24	42
FG484	16	10	28	48

A majority of package pins are user-defined I/O or input pins. However, the numbers and characteristics of these I/O depend on the device type and the package in which it is available, as shown in Table 129. The table shows the maximum number of single-ended I/O pins available, assuming that all I/O-, INPUT-, DUAL-, VREF-, and CLK-type pins are used as general-purpose I/O. Likewise, the table shows the maximum number of differential pin-pairs available on the package. Finally, the table shows how the total maximum user-I/Os are distributed by pin type, including the number of unconnected—i.e., N.C.—pins on the device.

PQ208 Footprint (Left)

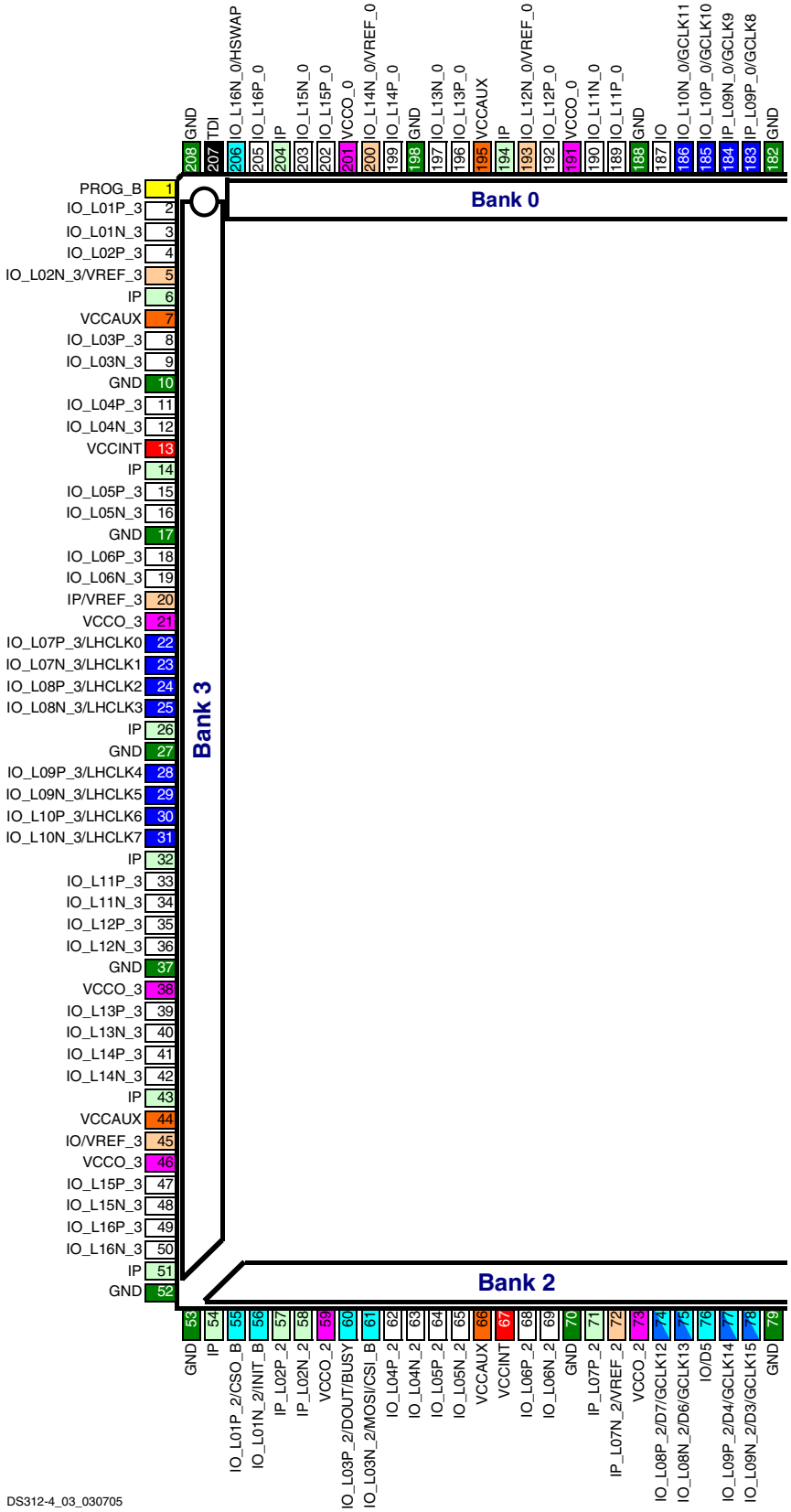


Figure 83: **PQ208 Footprint (Left)**

Table 143: **FT256 Package Pinout *(Cont'd)***

Bank	XC3S250E Pin Name	XC3S500E Pin Name	XC3S1200E Pin Name	FT256 Ball	Type
3	IO_L06P_3	IO_L06P_3	IO_L06P_3	G5	I/O
3	IO_L07N_3	IO_L07N_3	IO_L07N_3	G2	I/O
3	IO_L07P_3	IO_L07P_3	IO_L07P_3	G3	I/O
3	IO_L08N_3/LHCLK1	IO_L08N_3/LHCLK1	IO_L08N_3/LHCLK1	H6	LHCLK
3	IO_L08P_3/LHCLK0	IO_L08P_3/LHCLK0	IO_L08P_3/LHCLK0	H5	LHCLK
3	IO_L09N_3/LHCLK3/ IRDY2	IO_L09N_3/LHCLK3/ IRDY2	IO_L09N_3/LHCLK3/ IRDY2	H4	LHCLK
3	IO_L09P_3/LHCLK2	IO_L09P_3/LHCLK2	IO_L09P_3/LHCLK2	H3	LHCLK
3	IO_L10N_3/LHCLK5	IO_L10N_3/LHCLK5	IO_L10N_3/LHCLK5	J3	LHCLK
3	IO_L10P_3/LHCLK4/ TRDY2	IO_L10P_3/LHCLK4/ TRDY2	IO_L10P_3/LHCLK4/ TRDY2	J2	LHCLK
3	IO_L11N_3/LHCLK7	IO_L11N_3/LHCLK7	IO_L11N_3/LHCLK7	J4	LHCLK
3	IO_L11P_3/LHCLK6	IO_L11P_3/LHCLK6	IO_L11P_3/LHCLK6	J5	LHCLK
3	IO_L12N_3	IO_L12N_3	IO_L12N_3	K1	I/O
3	IO_L12P_3	IO_L12P_3	IO_L12P_3	J1	I/O
3	IO_L13N_3	IO_L13N_3	IO_L13N_3	K3	I/O
3	IO_L13P_3	IO_L13P_3	IO_L13P_3	K2	I/O
3	N.C. (◆)	IO_L14N_3/VREF_3	IO_L14N_3/VREF_3	L2	***250E:*** N.C. ***500E:*** VREF ***1200E:*** VREF
3	N.C. (◆)	IO_L14P_3	IO_L14P_3	L3	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O
3	IO_L15N_3	IO_L15N_3	IO_L15N_3	L5	I/O
3	IO_L15P_3	IO_L15P_3	IO_L15P_3	K5	I/O
3	IO_L16N_3	IO_L16N_3	IO_L16N_3	N1	I/O
3	IO_L16P_3	IO_L16P_3	IO_L16P_3	M1	I/O
3	N.C. (◆)	IO_L17N_3	IO_L17N_3	L4	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O
3	N.C. (◆)	IO_L17P_3	IO_L17P_3	M4	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O
3	IO_L18N_3	IO_L18N_3	IO_L18N_3	P1	I/O
3	IO_L18P_3	IO_L18P_3	IO_L18P_3	P2	I/O
3	IO_L19N_3	IO_L19N_3	IO_L19N_3	R1	I/O
3	IO_L19P_3	IO_L19P_3	IO_L19P_3	R2	I/O
3	IP	IP	IP	D2	INPUT
3	IP	IP	IP	F2	INPUT
3	IO	IO	IP	F5	***250E:*** I/O ***500E:*** I/O ***1200E:*** INPUT
3	IP	IP	IP	H1	INPUT
3	IP	IP	IP	J6	INPUT
3	IP	IP	IP	K4	INPUT
3	IP	IP	IP	M3	INPUT

Footprint Migration Differences

Table 147 summarizes any footprint and functionality differences between the XC3S250E, the XC3S500E, and the XC3S1200E FPGAs that may affect easy migration between devices in the FG256 package. There are 26 such balls. All other pins not listed in Table 147 unconditionally migrate between Spartan-3E devices available in the FT256 package.

The XC3S250E is duplicated on both the left and right sides of the table to show migrations to and from the XC3S500E and the XC3S1200E. The arrows indicate the direction for easy migration. A double-ended arrow (←→) indicates that the two pins have identical functionality. A left-facing arrow (←) indicates that the pin on the device on the right unconditionally migrates to the pin on the device on the left. It may be possible to migrate the opposite direction depending on the I/O configuration. For example, an I/O pin (Type = I/O) can migrate to an input-only pin (Type = INPUT) if the I/O pin is configured as an input.

Table 147: **FT256 Footprint Migration Differences**

FT256 Ball	Bank	XC3S250E Type	Migration	XC3S500E Type	Migration	XC3S1200E Type	Migration	XC3S250E Type
B6	0	INPUT	←→	INPUT	→	I/O	←	INPUT
B7	0	N.C.	→	I/O	←→	I/O	←	N.C.
B10	0	INPUT	←→	INPUT	→	I/O	←	INPUT
C7	0	N.C.	→	I/O	←→	I/O	←	N.C.
D16	1	VREF(I/O)	←	VREF(INPUT)	←→	VREF(INPUT)	→	VREF(I/O)
E13	1	N.C.	→	I/O	←→	I/O	←	N.C.
E16	1	N.C.	→	I/O	←→	I/O	←	N.C.
F3	3	N.C.	→	I/O	←→	I/O	←	N.C.
F4	3	N.C.	→	VREF	←→	VREF	←	N.C.
F5	3	I/O	←→	I/O	←	INPUT	→	I/O
L2	3	N.C.	→	VREF	←→	VREF	←	N.C.
L3	3	N.C.	→	I/O	←→	I/O	←	N.C.
L4	3	N.C.	→	I/O	←→	I/O	←	N.C.
L12	1	N.C.	→	I/O	←→	I/O	←	N.C.
L13	1	N.C.	→	I/O	←→	I/O	←	N.C.
M4	3	N.C.	→	I/O	←→	I/O	←	N.C.
M7	2	INPUT	←→	INPUT	→	I/O	←	INPUT
M14	1	I/O	←→	I/O	←	INPUT	→	I/O
N2	3	VREF(I/O)	←→	VREF(I/O)	←	VREF(INPUT)	→	VREF(I/O)
N7	2	N.C.	→	I/O	←→	I/O	←	N.C.
N14	1	N.C.	→	I/O	←→	I/O	←	N.C.
N15	1	N.C.	→	VREF	←→	VREF	←	N.C.
P7	2	N.C.	→	I/O	←→	I/O	←	N.C.
P10	2	N.C.	→	I/O	←→	I/O	←	N.C.
R10	2	N.C.	→	VREF	←→	VREF	←	N.C.
T12	2	INPUT	←→	INPUT	→	I/O	←	INPUT
DIFFERENCES			**19**		**7**		**26**	

Legend:

←→ This pin is identical on the device on the left and the right.

→ This pin can unconditionally migrate from the device on the left to the device on the right. Migration in the other direction may be possible depending on how the pin is configured for the device on the right.

← This pin can unconditionally migrate from the device on the right to the device on the left. Migration in the other direction may be possible depending on how the pin is configured for the device on the left.

FG320 Footprint

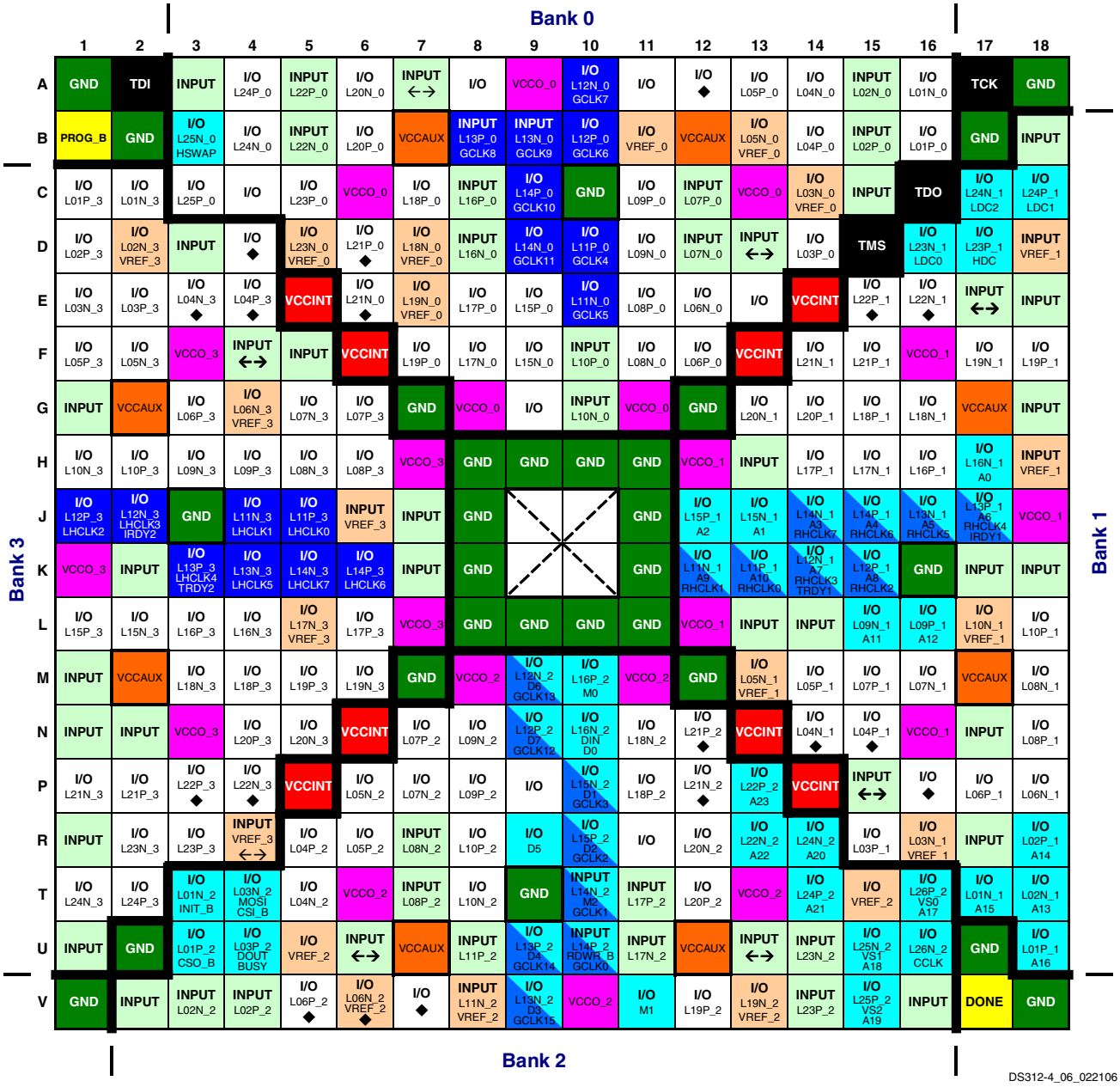


Figure 86: **FG320 Package Footprint (top view)**

102-120	**I/O:** Unrestricted, general-purpose user I/O	46	**DUAL:** Configuration pin, then possible user-I/O	20-21	**VREF:** User I/O or input voltage reference for bank
47-48	**INPUT:** Unrestricted, general-purpose input pin	16	**CLK:** User I/O, input, or global buffer input	20	**VCCO:** Output voltage supply for bank
2	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	8	**VCCINT:** Internal core supply voltage (+1.2V)
18	**N.C.:** Not connected. Only the XC3S500E has these pins (◆).	28	**GND:** Ground	8	**VCCAUX:** Auxiliary supply voltage (+2.5V)

FG400 Footprint

Right Half of Package (top view)

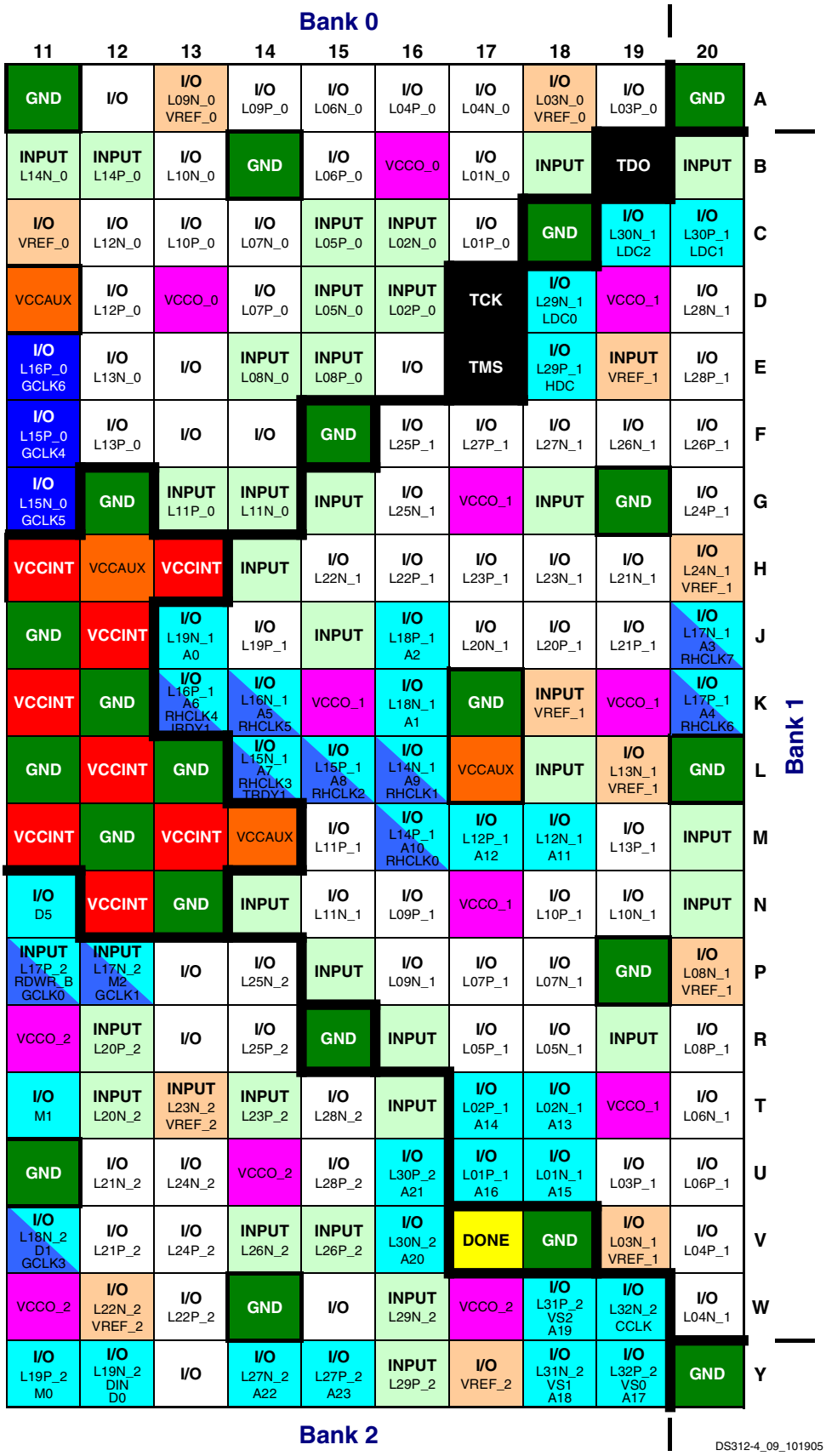


Table 154: **FG484 Package Pinout *(Cont'd)***

Bank	XC3S1600E Pin Name	FG484 Ball	Type
1	IO_L27N_1	J17	I/O
1	IO_L27P_1	J18	I/O
1	IO_L28N_1/VREF_1	H21	VREF
1	IO_L28P_1	H22	I/O
1	IO_L29N_1	H20	I/O
1	IO_L29P_1	H19	I/O
1	IO_L30N_1	H17	I/O
1	IO_L30P_1	G17	I/O
1	IO_L31N_1	F22	I/O
1	IO_L31P_1	G22	I/O
1	IO_L32N_1	F20	I/O
1	IO_L32P_1	G20	I/O
1	IO_L33N_1	G18	I/O
1	IO_L33P_1	G19	I/O
1	IO_L34N_1	D22	I/O
1	IO_L34P_1	E22	I/O
1	IO_L35N_1	F19	I/O
1	IO_L35P_1	F18	I/O
1	IO_L36N_1	E20	I/O
1	IO_L36P_1	E19	I/O
1	IO_L37N_1/LDC0	C21	DUAL
1	IO_L37P_1/HDC	C22	DUAL
1	IO_L38N_1/LDC2	B21	DUAL
1	IO_L38P_1/LDC1	B22	DUAL
1	IP	D20	INPUT
1	IP	F21	INPUT
1	IP	G16	INPUT
1	IP	H16	INPUT
1	IP	J16	INPUT
1	IP	J22	INPUT
1	IP	K20	INPUT
1	IP	L15	INPUT
1	IP	M18	INPUT
1	IP	N15	INPUT
1	IP	N21	INPUT
1	IP	P20	INPUT
1	IP	R15	INPUT
1	IP	T17	INPUT
1	IP	T20	INPUT
1	IP	U18	INPUT
1	IP/VREF_1	D21	VREF
1	IP/VREF_1	L17	VREF
1	VCCO_1	E21	VCCO
1	VCCO_1	H18	VCCO

Table 154: **FG484 Package Pinout *(Cont'd)***

Bank	XC3S1600E Pin Name	FG484 Ball	Type
1	VCCO_1	K21	VCCO
1	VCCO_1	L16	VCCO
1	VCCO_1	P21	VCCO
1	VCCO_1	R17	VCCO
1	VCCO_1	V21	VCCO
2	IO	Y8	I/O
2	IO	Y9	I/O
2	IO	AA10	I/O
2	IO	AB5	I/O
2	IO	AB13	I/O
2	IO	AB14	I/O
2	IO	AB16	I/O
2	IO	AB18	I/O
2	IO/D5	AB11	DUAL
2	IO/M1	AA12	DUAL
2	IO/VREF_2	AB4	VREF
2	IO/VREF_2	AB21	VREF
2	IO_L01N_2/INIT_B	AB3	DUAL
2	IO_L01P_2/CSO_B	AA3	DUAL
2	IO_L03N_2/MOSI/CSI_B	Y5	DUAL
2	IO_L03P_2/DOUT/BUSY	W5	DUAL
2	IO_L04N_2	W6	I/O
2	IO_L04P_2	V6	I/O
2	IO_L06N_2	W7	I/O
2	IO_L06P_2	Y7	I/O
2	IO_L07N_2	U7	I/O
2	IO_L07P_2	V7	I/O
2	IO_L09N_2/VREF_2	V8	VREF
2	IO_L09P_2	W8	I/O
2	IO_L10N_2	T8	I/O
2	IO_L10P_2	U8	I/O
2	IO_L11N_2	AB8	I/O
2	IO_L11P_2	AA8	I/O
2	IO_L12N_2	W9	I/O
2	IO_L12P_2	V9	I/O
2	IO_L13N_2/VREF_2	R9	VREF
2	IO_L13P_2	T9	I/O
2	IO_L14N_2	AB9	I/O
2	IO_L14P_2	AB10	I/O
2	IO_L16N_2	U10	I/O
2	IO_L16P_2	T10	I/O
2	IO_L17N_2	R10	I/O
2	IO_L17P_2	P10	I/O

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/01/05	1.0	Initial Xilinx release.
03/21/05	1.1	Added XC3S250E in the CP132 package to Table 129. Corrected number of differential I/O pairs on CP132. Added pinout and footprint information for the CP132, FG400, and FG484 packages. Removed IRDY and TRDY pins from the VQ100, TQ144, and PQ208 packages.
11/23/05	2.0	Corrected title of Table 153. Updated differential pair numbering for some pins in Bank 0 of the FG400 package, affecting Table 152 and Figure 87. Pin functionality and ball assignment were not affected. Added Package Thermal Characteristics section. Added package mass values to Table 125.
03/22/06	3.0	Included I/O pins, not just input-only pins under the VREF description in Table 124. Clarified that some global clock inputs are Input-only pins in Table 124. Added information on the XC3S100E in the CP132 package, affecting Table 129, Table 130, Table 133, Table 134, Table 136, and Figure 81. Ball A12 on the XC3S1600E in the FG320 package a full I/O pin, not an Input-only pin. Corrected the I/O counts for the XC3S1600E in the FG320 package, affecting Table 129, Table 150, Table 151, and Figure 86. Corrected pin type for XC3S1600E balls N14 and N15 in Table 148.
05/19/06	3.1	Minor text edits.
11/09/06	3.4	Added package thermal data for the XC3S100E in the CP132 package to Table 130. Corrected pin migration arrows for balls E17 and F4 between the XC3S500E and XC3S1600E in Table 151. Promoted Module 4 to Production status. Synchronized all modules to v3.4.
03/16/07	3.5	Minor formatting changes.
05/29/07	3.6	Corrected ‘Lxx’ to ‘Lxxy’ in Table 124. Noted that some GCLK and VREF pins are on INPUT pins in Table 124 and Table 129. Added link before Table 127 to Material Declaration Data Sheets.
04/18/08	3.7	Added XC3S500E VQG100 package. Added Material Declaration Data Sheet links in Table 127. Updated Thermal Characteristics in Table 130. Updated links.
08/26/09	3.8	Minor typographical updates.
10/29/12	4.0	Added Notice of Disclaimer. This product is not recommended for new designs. Updated the XC3S250E-FT256 in Table 129.

Notice of Disclaimer