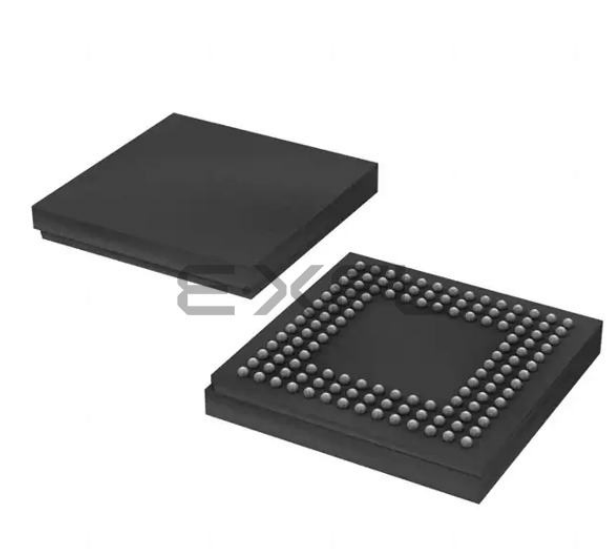

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	612
Number of Logic Elements/Cells	5508
Total RAM Bits	221184
Number of I/O	92
Number of Gates	250000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	132-TFBGA, CSPBGA
Supplier Device Package	132-CSPBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s250e-4cpg132c

Package Marking

Figure 2 provides a top marking example for Spartan-3E FPGAs in the quad-flat packages. Figure 3 shows the top marking for Spartan-3E FPGAs in BGA packages except the 132-ball chip-scale package (CP132 and CPG132). The markings for the BGA packages are nearly identical to those for the quad-flat packages, except that the marking is rotated with respect to the ball A1 indicator. Figure 4 shows the top marking for Spartan-3E FPGAs in the CP132 and CPG132 packages.

On the QFP and BGA packages, the optional numerical Stepping Code follows the Lot Code.

The "5C" and "4I" part combinations can have a dual mark of "5C/4I". Devices with a single mark are only guaranteed for the marked speed grade and temperature range. All "5C" and "4I" part combinations use the Stepping 1 production silicon.

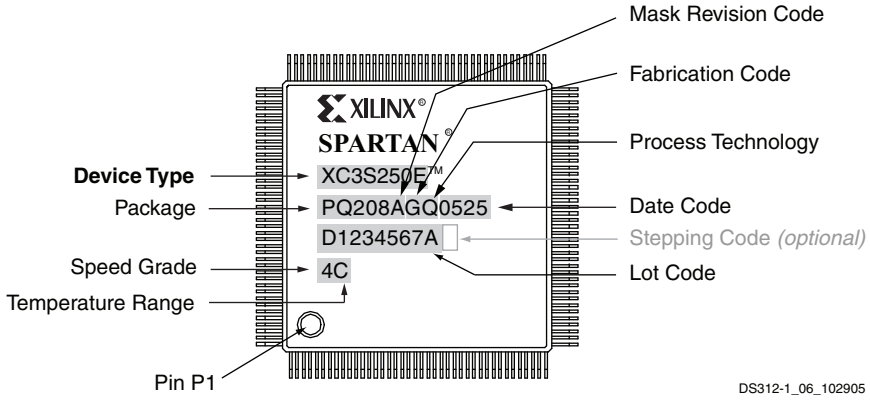

Figure 2: **Spartan-3E QFP Package Marking Example**

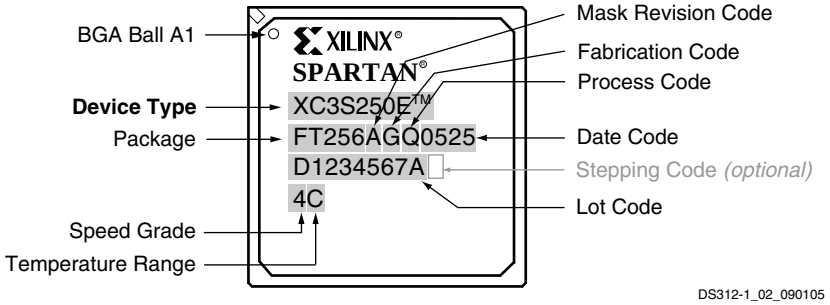

Figure 3: **Spartan-3E BGA Package Marking Example**

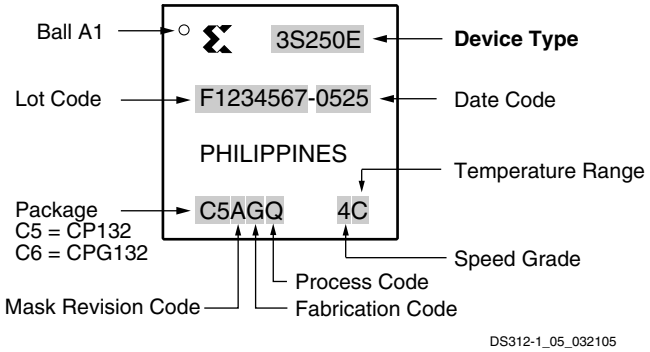

Figure 4: **Spartan-3E CP132 and CPG132 Package Marking Example**

Supply Voltages for the IOBs

The IOBs are powered by three supplies:

1. The V_{CCO} supplies, one for each of the FPGA's I/O banks, power the output drivers. The voltage on the V_{CCO} pins determines the voltage swing of the output signal.
2. V_{CCINT} is the main power supply for the FPGA's internal logic.
3. V_{CCAUX} is an auxiliary source of power, primarily to optimize the performance of various FPGA functions such as I/O switching.

I/O and Input-Only Pin Behavior During Power-On, Configuration, and User Mode

In this section, all behavior described for I/O pins also applies to input-only pins and dual-purpose I/O pins that are not actively involved in the currently-selected configuration mode.

All I/O pins have ESD clamp diodes to their respective V_{CCO} supply and from GND, as shown in Figure 5. The V_{CCINT} (1.2V), V_{CCAUX} (2.5V), and V_{CCO} supplies can be applied in any order. Before the FPGA can start its configuration process, V_{CCINT}, V_{CCO} Bank 2, and V_{CCAUX} must have reached their respective minimum recommended operating levels indicated in Table 74. At this time, all output drivers are in a high-impedance state. V_{CCO} Bank 2, V_{CCINT}, and V_{CCAUX} serve as inputs to the internal Power-On Reset circuit (POR).

A Low level applied to the HSWAP input enables pull-up resistors on user-I/O and input-only pins from power-on throughout configuration. A High level on HSWAP disables the pull-up resistors, allowing the I/Os to float. HSWAP contains an internal pull-up resistor and defaults to High if left floating. As soon as power is applied, the FPGA begins initializing its configuration memory. At the same time, the FPGA internally asserts the Global Set-Reset (GSR), which asynchronously resets all IOB storage elements to a default Low state. Also see Pin Behavior During Configuration.

Upon the completion of initialization and the beginning of configuration, INIT_B goes High, sampling the M0, M1, and M2 inputs to determine the configuration mode. Configuration data is then loaded into the FPGA. The I/O drivers remain in a high-impedance state (with or without pull-up resistors, as determined by the HSWAP input) throughout configuration.

At the end of configuration, the GSR net is released, placing the IOB registers in a Low state by default, unless the loaded design reverses the polarity of their respective SR inputs.

The Global Three State (GTS) net is released during Start-Up, marking the end of configuration and the beginning of design operation in the User mode. After the GTS net is released, all user I/Os go active while all unused I/Os are pulled down (PULLDOWN). The designer can control how the unused I/Os are terminated after GTS is released by setting the Bitstream Generator (BitGen) option UnusedPin to PULLUP, PULLDOWN, or FLOAT.

One clock cycle later (default), the Global Write Enable (GWE) net is released allowing the RAM and registers to change states. Once in User mode, any pull-up resistors enabled by HSWAP revert to the user settings and HSWAP is available as a general-purpose I/O. For more information on PULLUP and PULLDOWN, see Pull-Up and Pull-Down Resistors.

Behavior of Unused I/O Pins After Configuration

By default, the Xilinx ISE development software automatically configures all unused I/O pins as input pins with individual internal pull-down resistors to GND.

This default behavior is controlled by the ***UnusedPin*** bitstream generator (BitGen) option, as described in Table 69.

JTAG Boundary-Scan Capability

All Spartan-3E IOBs support boundary-scan testing compatible with IEEE 1149.1/1532 standards. During boundary-scan operations such as EXTEST and HIGHZ the pull-down resistor is active. See JTAG Mode for more information on programming via JTAG.

The wide multiplexers can be used by the automatic tools or instantiated in a design using a component such as the F5MUX. The symbol, signals, and function are described in Figure 21, Table 12, and Table 13. The description is similar for the F6MUX, F7MUX, and F8MUX. Each has versions with a general output, local output, or both.

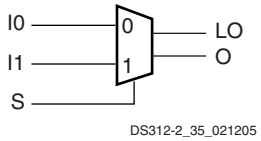

Figure 21: **F5MUX with Local and General Outputs**

Table 12: **F5MUX Inputs and Outputs**

Signal	Function
I0	Input selected when S is Low
I1	Input selected when S is High
S	Select input
LO	Local Output that connects to the F5 or FX CLB pins, which use local feedback to the FXIN inputs to the FiMUX for cascading
O	General Output that connects to the general-purpose combinatorial or registered outputs of the CLB

Table 13: **F5MUX Function**

Inputs			Outputs	
S	**I0**	**I1**	**O**	**LO**
0	1	X	1	1
0	0	X	0	0
1	X	1	1	1
1	X	0	0	0

There are a number of different conditions under which data can be accessed at the DO outputs. Basic data access always occurs when the WE input is inactive. Under this condition, data stored in the memory location addressed by the ADDR lines passes through a output latch to the DO outputs. The timing for basic data access is shown in the portions of Figure 33, Figure 34, and Figure 35 during which WE is Low.

Data also can be accessed on the DO outputs when asserting the WE input based on the value of the WRITE_MODE attribute as described in Table 26.

Table 26: **WRITE_MODE Effect on Data Output Latches During Write Operations**

Write Mode	Effect on Same Port	Effect on Opposite Port (dual-port only with same address)
WRITE_FIRST Read After Write	Data on DI and DIP inputs is written into specified RAM location and simultaneously appears on DO and DOP outputs.	Invalidates data on DO and DOP outputs.
READ_FIRST Read Before Write	Data from specified RAM location appears on DO and DOP outputs. Data on DI and DIP inputs is written into specified location.	Data from specified RAM location appears on DO and DOP outputs.
NO_CHANGE No Read on Write	Data on DO and DOP outputs remains unchanged. Data on DI and DIP inputs is written into specified location.	Invalidates data on DO and DOP outputs.

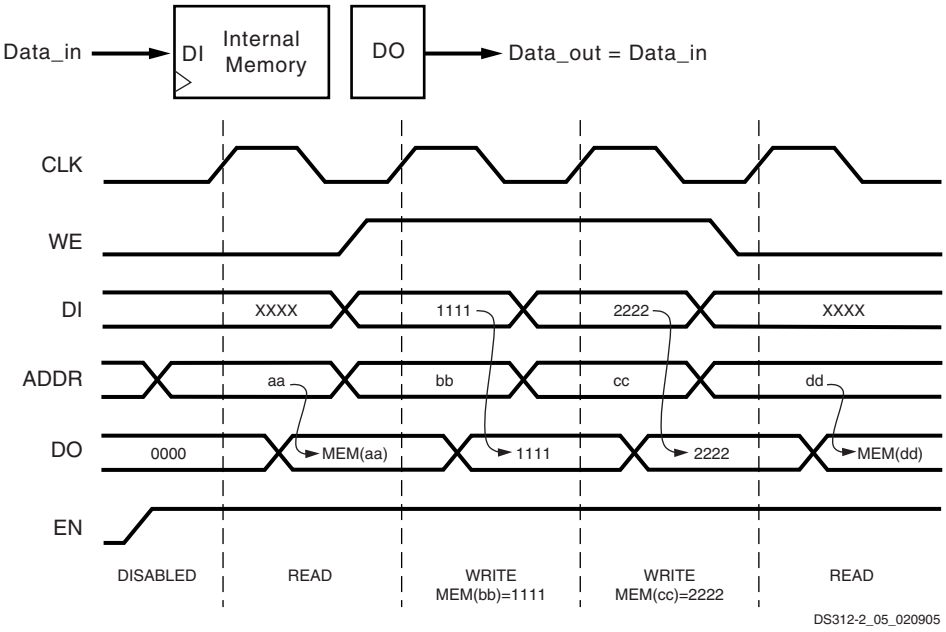

Figure 33: **Waveforms of Block RAM Data Operations with WRITE_FIRST Selected**

Setting the WRITE_MODE attribute to a value of WRITE_FIRST, data is written to the addressed memory location on an enabled active CLK edge and is also passed to the DO outputs. WRITE_FIRST timing is shown in the portion of Figure 33 during which WE is High.

Setting the WRITE_MODE attribute to a value of READ_FIRST, data already stored in the addressed location passes to the DO outputs before that location is overwritten with new data from the DI inputs on an enabled active CLK edge. READ_FIRST timing is shown in the portion of Figure 34 during which WE is High.

Configuration Bitstream Image Sizes

A specific Spartan-3E part type always requires a constant number of configuration bits, regardless of design complexity, as shown in Table 45. The configuration file size for a multiple-FPGA daisy-chain design roughly equals the sum of the individual file sizes.

Table 45: **Number of Bits to Program a Spartan-3E FPGA (Uncompressed Bitstreams)**

Spartan-3E FPGA	Number of Configuration Bits
XC3S100E	581,344
XC3S250E	1,353,728
XC3S500E	2,270,208
XC3S1200E	3,841,184
XC3S1600E	5,969,696

Pin Behavior During Configuration

For additional information, refer to the "Configuration Pins and Behavior during Configuration" chapter in UG332.

Table 46 shows how various pins behave during the FPGA configuration process. The actual behavior depends on the values applied to the M2, M1, and M0 mode select pins and the HSWAP pin. The mode select pins determine which of the I/O pins are borrowed during configuration and how they function. In JTAG configuration mode, no user-I/O pins are borrowed for configuration.

All user-I/O pins, input-only pins, and dual-purpose pins that are not actively involved in the currently-select configuration mode are high impedance (floating, three-stated, Hi-Z) during the configuration process. These pins are indicated in Table 46 as gray shaded table entries or cells.

The HSWAP input controls whether all user-I/O pins, input-only pins, and dual-purpose pins have a pull-up resistor to the supply rail or not. When HSWAP is Low, each pin has an internal pull-up resistor that is active throughout configuration. After configuration, pull-up and pull-down resistors are available in the FPGA application as described in Pull-Up and Pull-Down Resistors.

The yellow-shaded table entries or cells represent pins where the pull-up resistor is always enabled during configuration, regardless of the HSWAP input. The post-configuration behavior of these pins is defined by Bitstream Generator options as defined in Table 69.

Table 46: **Pin Behavior during Configuration**

Pin Name	Master Serial	SPI (Serial Flash)	BPI (Parallel NOR Flash)	JTAG	Slave Parallel	Slave Serial	I/O Bank[3]
IO* (user-I/O) IP* (input-only)							-
TDI	TDI	TDI	TDI	TDI	TDI	TDI	V_{CCAUX}
TMS	TMS	TMS	TMS	TMS	TMS	TMS	V_{CCAUX}
TCK	TCK	TCK	TCK	TCK	TCK	TCK	V_{CCAUX}
TDO	TDO	TDO	TDO	TDO	TDO	TDO	V_{CCAUX}
PROG_B	PROG_B	PROG_B	PROG_B	PROG_B	PROG_B	PROG_B	V_{CCAUX}
DONE	DONE	DONE	DONE	DONE	DONE	DONE	V_{CCAUX}
HSWAP	HSWAP	HSWAP	HSWAP	HSWAP	HSWAP	HSWAP	0
M2	0	0	0	1	1	1	2
M1	0	0	1	0	1	1	2
M0	0	1	0 = Up 1 = Down	1	0	1	2
CCLK	CCLK (I/O)	CCLK (I/O)	CCLK (I/O)		CCLK (I)	CCLK (I)	2
INIT_B	INIT_B	INIT_B	INIT_B		INIT_B	INIT_B	2
CSO_B		CSO_B	CSO_B		CSO_B		2
DOUT/BUSY	DOUT	DOUT	BUSY		BUSY	DOUT	2
MOSI/CSI_B		MOSI	CSI_B		CSI_B		2
D7			D7		D7		2
D6			D6		D6		2
D5			D5		D5		2
D4			D4		D4		2
D3			D3		D3		2
D2			D2		D2		2
D1			D1		D1		2

Master Serial Mode

For additional information, refer to the “Master Serial Mode” chapter in UG332.

In Master Serial mode (M[2:0] = <0:0:0>), the Spartan-3E FPGA configures itself from an attached Xilinx Platform Flash PROM, as illustrated in Figure 51. The FPGA supplies the CCLK output clock from its internal oscillator to the attached Platform Flash PROM. In response, the Platform Flash PROM supplies bit-serial data to the FPGA’s DIN input, and the FPGA accepts this data on each rising CCLK edge.

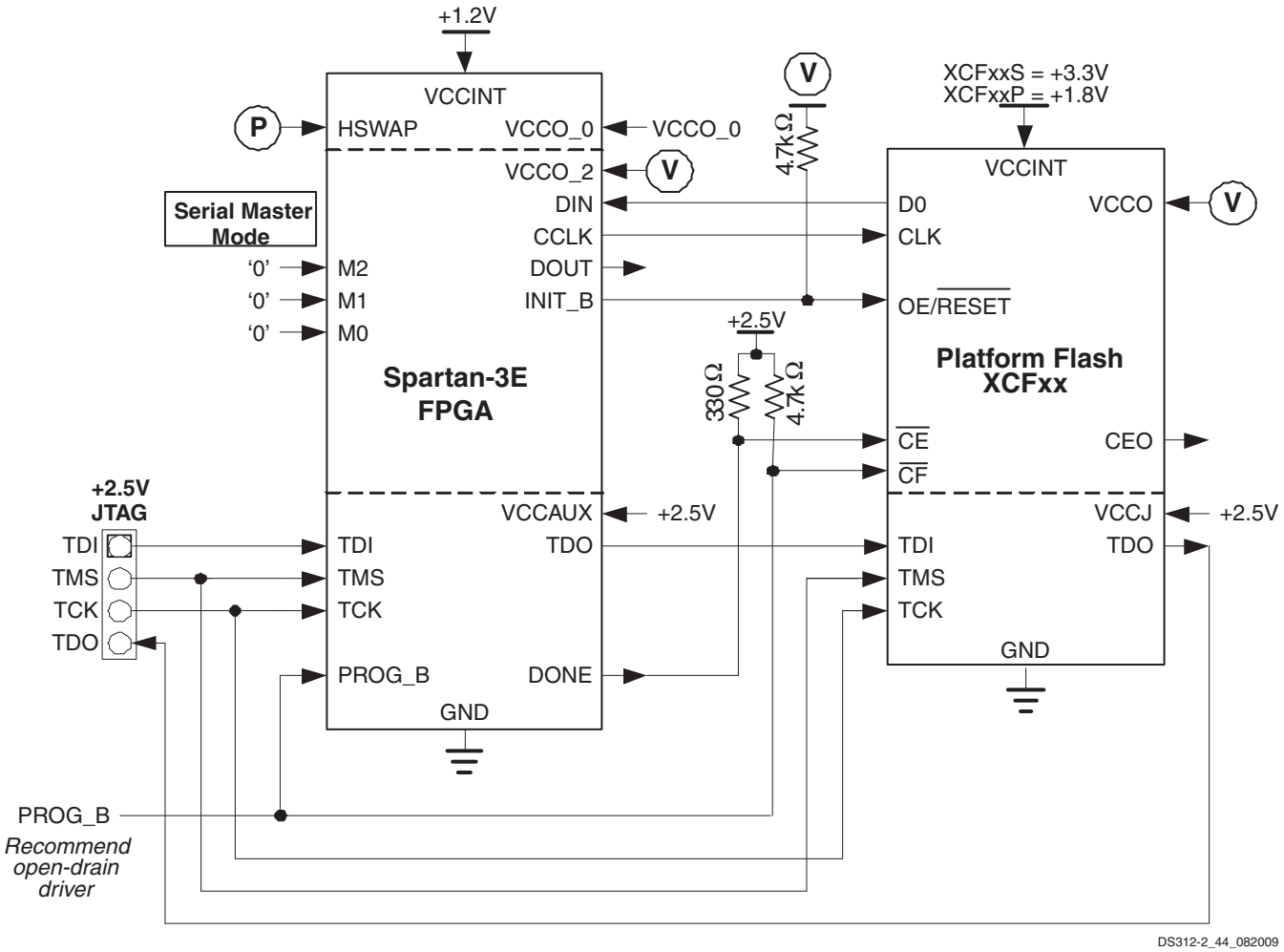

Figure 51: **Master Serial Mode using Platform Flash PROM**

All mode select pins, M[2:0], must be Low when sampled, when the FPGA’s INIT_B output goes High. After configuration, when the FPGA’s DONE output goes High, the mode select pins are available as full-featured user-I/O pins.

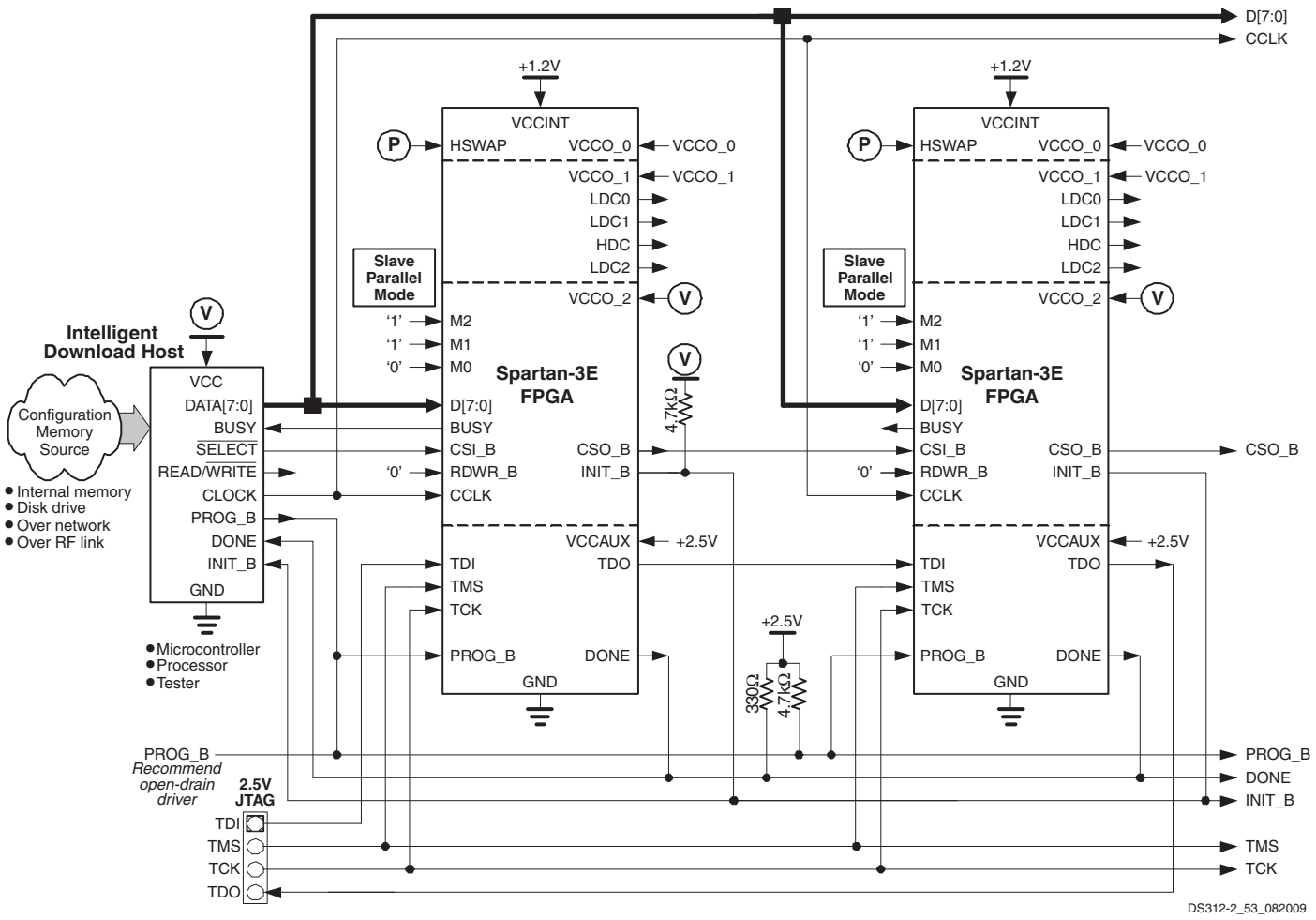

Figure 62: **Daisy-Chaining using Slave Parallel Mode**

Slave Serial Mode

For additional information, refer to the “Slave Serial Mode” chapter in UG332.

In Slave Serial mode (M[2:0] = <1:1:1>), an external host such as a microprocessor or microcontroller writes serial configuration data into the FPGA, using the synchronous serial interface shown in Figure 63. The serial configuration data is presented on the FPGA’s DIN input pin with sufficient setup time before each rising edge of the externally generated CCLK clock input.

The intelligent host starts the configuration process by pulsing PROG_B and monitoring that the INIT_B pin goes High, indicating that the FPGA is ready to receive its first data. The host then continues supplying data and clock signals until either the DONE pin goes High, indicating a successful configuration, or until the INIT_B pin goes Low, indicating a configuration error. The configuration process requires more clock cycles than indicated from the configuration file size. Additional clocks are required during the FPGA’s start-up sequence, especially if the FPGA is programmed to wait for selected Digital Clock Managers (DCMs) to lock to their respective clock inputs (see Start-Up, page 105).

FPGA passes configuration data via its DOUT output pin to the next FPGA on the falling CCLK edge.

Table 66: **Slave Serial Mode Connections**

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
HSWAP	Input	**User I/O Pull-Up Control**. When Low during configuration, enables pull-up resistors in all I/O pins to respective I/O bank V_{CCO} input. 0: Pull-up during configuration 1: No pull-ups	Drive at valid logic level throughout configuration.	User I/O
M[2:0]	Input	**Mode Select**. Selects the FPGA configuration mode. See Design Considerations for the HSWAP, M[2:0], and VS[2:0] Pins.	M2 = 1, M1 = 1, M0 = 1 Sampled when INIT_B goes High.	User I/O
DIN	Input	**Data Input**.	Serial data provided by host. FPGA captures data on rising CCLK edge.	User I/O
CCLK	Input	**Configuration Clock**. If CCLK PCB trace is long or has multiple connections, terminate this output to maintain signal integrity. See CCLK Design Considerations.	External clock.	User I/O
INIT_B	Open-drain bidirectional I/O	**Initialization Indicator**. Active Low. Goes Low at start of configuration during Initialization memory clearing process. Released at end of memory clearing, when mode select pins are sampled. In daisy-chain applications, this signal requires an external 4.7 kΩ pull-up resistor to VCCO_2.	Active during configuration. If CRC error detected during configuration, FPGA drives INIT_B Low.	User I/O. If unused in the application, drive INIT_B High.
DONE	Open-drain bidirectional I/O	**FPGA Configuration Done**. Low during configuration. Goes High when FPGA successfully completes configuration. Requires external 330 Ω pull-up resistor to 2.5V.	Low indicates that the FPGA is not yet configured.	Pulled High via external pull-up. When High, indicates that the FPGA successfully configured.
PROG_B	Input	**Program FPGA**. Active Low. When asserted Low for 500 ns or longer, forces the FPGA to restart its configuration process by clearing configuration memory and resetting the DONE and INIT_B pins once PROG_B returns High. Recommend external 4.7 kΩ pull-up resistor to 2.5V. Internal pull-up value may be weaker (see Table 78). If driving externally with a 3.3V output, use an open-drain or open-collector driver or use a current limiting series resistor.	Must be High to allow configuration to start.	Drive PROG_B Low and release to reprogram FPGA.

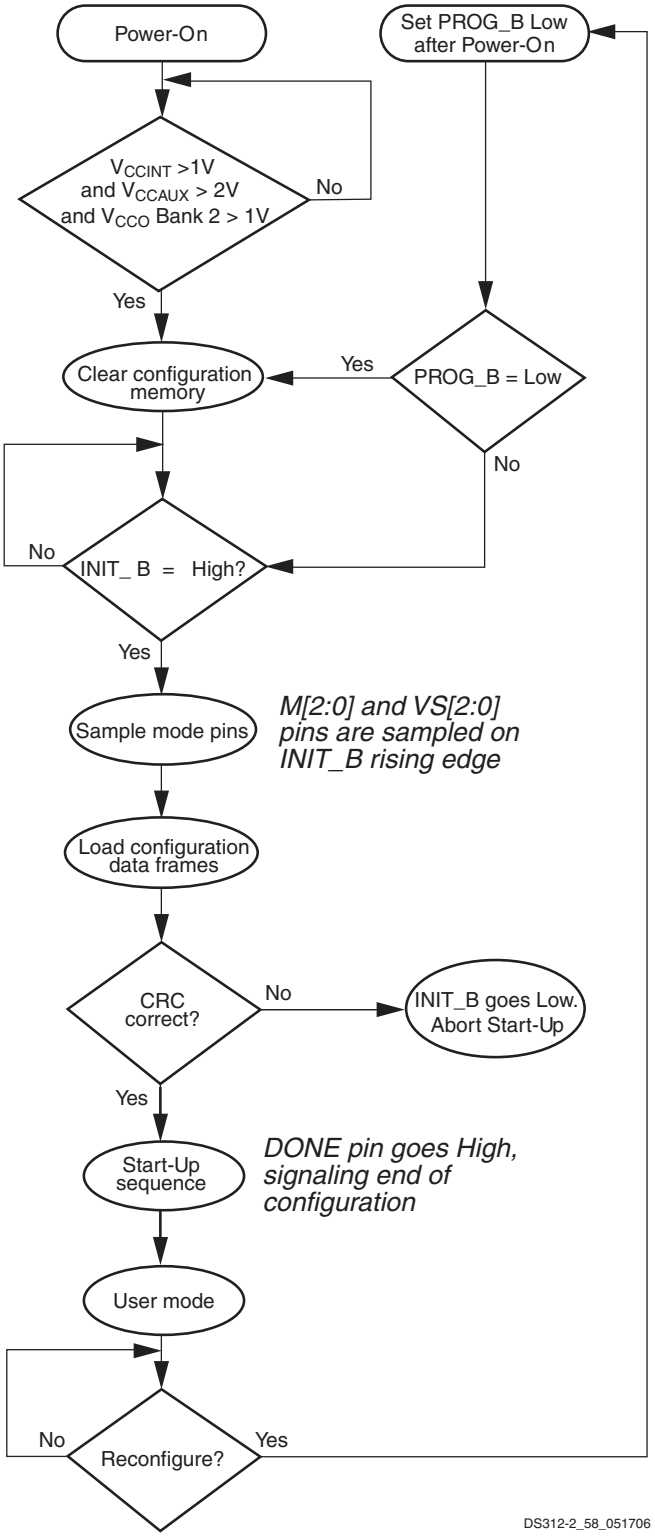

Figure 66: **General Configuration Process**

Start-Up

At the end of configuration, the FPGA automatically pulses the Global Set/Reset (GSR) signal, placing all flip-flops in a known state. After configuration completes, the FPGA switches over to the user application loaded into the FPGA. The sequence and timing of how the FPGA switches over is programmable as is the clock source controlling the sequence.

The default start-up sequence appears in Figure 68, where the Global Three-State signal (GTS) is released one clock cycle after DONE goes High. This sequence allows the DONE signal to enable or disable any external logic used during configuration before the user application in the FPGA starts driving output signals. One clock cycle later, the Global Write Enable (GWE) signal is released. This allows signals to propagate within the FPGA before any clocked storage elements such as flip-flops and block ROM are enabled.

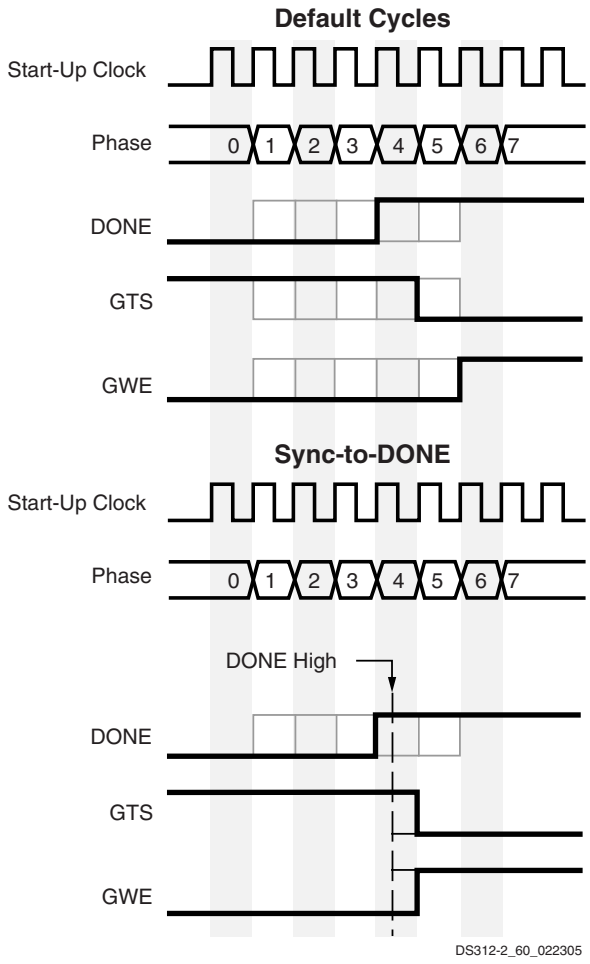

Figure 68: **Default Start-Up Sequence**

The function of the dual-purpose I/O pins, such as M[2:0], VS[2:0], HSWAP, and A[23:0], also changes when the DONE pin goes High. When DONE is High, these pins become user I/Os. Like all user-I/O pins, GTS controls when the dual-purpose pins can drive out.

The relative timing of configuration events is programmed via the Bitstream Generator (BitGen) options in the Xilinx development software. For example, the GTS and GWE events can be programmed to wait for all the DONE pins to High on all the devices in a multiple-FPGA daisy-chain, forcing the FPGAs to start synchronously. Similarly, the start-up sequence can be paused at any stage, waiting for selected DCMs to lock to their respective input clock signals. See also Stabilizing DCM Clocks Before User Mode.

By default, the start-up sequence is synchronized to CCLK. Alternatively, the start-up sequence can be synchronized to a user-specified clock from within the FPGA application using the STARTUP_SPARTAN3E library primitive and by setting the ***StartupClk*** bitstream generator option. The FPGA application can optionally assert the GSR and GTS signals via the STARTUP_SPARTAN3E primitive. For JTAG configuration, the start-up sequence can be synchronized to the TCK clock input.

Power Supply Specifications

Table 74: **Supply Voltage Thresholds for Power-On Reset**

Symbol	Description	Min	Max	Units
V_{CCINTT}	Threshold for the V_{CCINT} supply	0.4	1.0	V
V_{CCAUXT}	Threshold for the V_{CCAUX} supply	0.8	2.0	V
V_{CCO2T}	Threshold for the V_{CCO} Bank 2 supply	0.4	1.0	V

Notes:

1. V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies to the FPGA can be applied in any order. However, the FPGA's configuration source (Platform Flash, SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source. In Step 0 devices using the HSWAP internal pull-up, V_{CCINT} must be applied before V_{CCAUX}.
2. To ensure successful power-on, V_{CCINT}, V_{CCO} Bank 2, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 75: **Supply Voltage Ramp Rate**

Symbol	Description	Min	Max	Units
V_{CCINTR}	Ramp rate from GND to valid V_{CCINT} supply level	0.2	50	ms
V_{CCAUXR}	Ramp rate from GND to valid V_{CCAUX} supply level	0.2	50	ms
V_{CCO2R}	Ramp rate from GND to valid V_{CCO} Bank 2 supply level	0.2	50	ms

Notes:

1. V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies to the FPGA can be applied in any order. However, the FPGA's configuration source (Platform Flash, SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source. In Step 0 devices using the HSWAP internal pull-up, V_{CCINT} must be applied before V_{CCAUX}.
2. To ensure successful power-on, V_{CCINT}, V_{CCO} Bank 2, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 76: **Supply Voltage Levels Necessary for Preserving RAM Contents**

Symbol	Description	Min	Units
V_{DRINT}	V_{CCINT} level required to retain RAM data	1.0	V
V_{DRAUX}	V_{CCAUX} level required to retain RAM data	2.0	V

Notes:

1. RAM contents include configuration data.

Table 94: **Output Timing Adjustments for IOB**

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
Single-Ended Standards					
LVTTL	Slow	2 mA	5.20	5.41	ns
		4 mA	2.32	2.41	ns
		6 mA	1.83	1.90	ns
		8 mA	0.64	0.67	ns
		12 mA	0.68	0.70	ns
		16 mA	0.41	0.43	ns
	Fast	2 mA	4.80	5.00	ns
		4 mA	1.88	1.96	ns
		6 mA	1.39	1.45	ns
		8 mA	0.32	0.34	ns
		12 mA	0.28	0.30	ns
		16 mA	0.28	0.30	ns
LVCMOS33	Slow	2 mA	5.08	5.29	ns
		4 mA	1.82	1.89	ns
		6 mA	1.00	1.04	ns
		8 mA	0.66	0.69	ns
		12 mA	0.40	0.42	ns
		16 mA	0.41	0.43	ns
	Fast	2 mA	4.68	4.87	ns
		4 mA	1.46	1.52	ns
		6 mA	0.38	0.39	ns
		8 mA	0.33	0.34	ns
		12 mA	0.28	0.30	ns
		16 mA	0.28	0.30	ns
LVCMOS25	Slow	2 mA	4.04	4.21	ns
		4 mA	2.17	2.26	ns
		6 mA	1.46	1.52	ns
		8 mA	1.04	1.08	ns
		12 mA	0.65	0.68	ns
	Fast	2 mA	3.53	3.67	ns
		4 mA	1.65	1.72	ns
		6 mA	0.44	0.46	ns
		8 mA	0.20	0.21	ns
		12 mA	0	0	ns

Table 94: **Output Timing Adjustments for IOB *(Cont'd)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVCMOS18	Slow	2 mA	5.03	5.24	ns
		4 mA	3.08	3.21	ns
		6 mA	2.39	2.49	ns
		8 mA	1.83	1.90	ns
	Fast	2 mA	3.98	4.15	ns
		4 mA	2.04	2.13	ns
		6 mA	1.09	1.14	ns
		8 mA	0.72	0.75	ns
LVCMOS15	Slow	2 mA	4.49	4.68	ns
		4 mA	3.81	3.97	ns
		6 mA	2.99	3.11	ns
	Fast	2 mA	3.25	3.38	ns
		4 mA	2.59	2.70	ns
		6 mA	1.47	1.53	ns
LVCMOS12	Slow	2 mA	6.36	6.63	ns
	Fast	2 mA	4.26	4.44	ns
HSTL_I_18			0.33	0.34	ns
HSTL_III_18			0.53	0.55	ns
PCI33_3			0.44	0.46	ns
PCI66_3			0.44	0.46	ns
SSTL18_I			0.24	0.25	ns
SSTL2_I			–0.20	–0.20	ns
Differential Standards					
LVDS_25			–0.55	–0.55	ns
BLVDS_25			0.04	0.04	ns
MINI_LVDS_25			–0.56	–0.56	ns
LVPECL_25			Input Only		ns
RSDS_25			–0.48	–0.48	ns
DIFF_HSTL_I_18			0.42	0.42	ns
DIFF_HSTL_III_18			0.53	0.55	ns
DIFF_SSTL18_I			0.40	0.40	ns
DIFF_SSTL2_I			0.44	0.44	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 95 and are based on the operating conditions set forth in Table 77, Table 80, and Table 82.
2. These adjustments are used to convert output- and three-state-path times originally specified for the LVCMOS25 standard with 12 mA drive and Fast slew rate to times that correspond to other signal standards. Do not adjust times that measure when outputs go into a high-impedance state.

Table 99: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	-5		-4		Units
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{SHCKO}	Time from the active edge at the CLK input to data appearing on the distributed RAM output	-	2.05	-	2.35	ns
Setup Times						
T_{DS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the distributed RAM	0.40	-	0.46	-	ns
T_{AS}	Setup time of the F/G address inputs before the active transition at the CLK input of the distributed RAM	0.46	-	0.52	-	ns
T_{WS}	Setup time of the write enable input before the active transition at the CLK input of the distributed RAM	0.34	-	0.40	-	ns
Hold Times						
T_{DH}	Hold time of the BX, BY data inputs after the active transition at the CLK input of the distributed RAM	0.13	-	0.15	-	ns
T_{AH}, T_{WH}	Hold time of the F/G address inputs or the write enable input after the active transition at the CLK input of the distributed RAM	0	-	0	-	ns
Clock Pulse Width						
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	0.88	-	1.01	-	ns

Table 100: **CLB Shift Register Switching Characteristics**

Symbol	Description	-5		-4		Units
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{REG}	Time from the active edge at the CLK input to data appearing on the shift register output	-	3.62	-	4.16	ns
Setup Times						
T_{SRLDS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the shift register	0.41	-	0.46	-	ns
Hold Times						
T_{SRLDH}	Hold time of the BX or BY data input after the active transition at the CLK input of the shift register	0.14	-	0.16	-	ns
Clock Pulse Width						
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	0.88	-	1.01	-	ns

Clock Buffer/Multiplexer Switching Characteristics

Table 101: **Clock Distribution Switching Characteristics**

Description	Symbol	Maximum		Units
		Speed Grade		
		-5	-4	
Global clock buffer (BUFG, BUFGMUX, BUFGCE) I input to O-output delay	T_{GIO}	1.46	1.46	ns
Global clock multiplexer (BUFGMUX) select S-input setup to I0 and I1 inputs. Same as BUFGCE enable CE-input	T_{GSI}	0.55	0.63	ns
Frequency of signals distributed on global buffers (all sides)	F_{BUFG}	333	311	MHz

Table 117: **Timing for the Slave Parallel Configuration Mode *(Cont'd)***

Symbol	Description			All Speed Grades		Units
				Min	Max	
Clock Timing						
T_{CCH}	The High pulse width at the CCLK input pin			5	-	ns
T_{CCL}	The Low pulse width at the CCLK input pin			5	-	ns
F_{CCPAR}	Frequency of the clock signal at the CCLK input pin	No bitstream compression	Not using the BUSY pin(2)	0	50	MHz
			Using the BUSY pin	0	66	MHz
		With bitstream compression		0	20	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 77.
2. In the Slave Parallel mode, it is necessary to use the BUSY pin when the CCLK frequency exceeds this maximum specification.
3. Some Xilinx documents refer to Parallel modes as "SelectMAP" modes.

Footprint Migration Differences

Table 136 summarizes any footprint and functionality differences between the XC3S100E, the XC3S250E, and the XC3S500E FPGAs that may affect easy migration between devices in the CP132 package. There are 14 such balls. All other pins not listed in Table 136 unconditionally migrate between Spartan-3E devices available in the CP132 package.

The XC3S100E is duplicated on both the left and right sides of the table to show migrations to and from the XC3S250E and the XC3S500E. The arrows indicate the direction for easy migration. A double-ended arrow (←→) indicates that the two pins have identical functionality. A left-facing arrow (←) indicates that the pin on the device on the right unconditionally migrates to the pin on the device on the left. It may be possible to migrate the opposite direction depending on the I/O configuration. For example, an I/O pin (Type = I/O) can migrate to an input-only pin (Type = INPUT) if the I/O pin is configured as an input.

The XC3S100E FPGA in the CP132 package has four fewer BPI-mode address lines than the XC3S250E and XC3S500E.

Table 136: **CP132 Footprint Migration Differences**

CP132 Ball	Bank	XC3S100E Type	Migration	XC3S250E Type	Migration	XC3S500E Type	Migration	XC3S100E Type
A12	0	N.C.	→	I/O	←→	I/O	←	N.C.
B4	0	INPUT	→	I/O	←→	I/O	←	INPUT
B11	0	N.C.	→	I/O	←→	I/O	←	N.C.
B12	0	N.C.	→	I/O	←→	I/O	←	N.C.
C4	0	N.C.	→	I/O	←→	I/O	←	N.C.
C11	0	INPUT	→	I/O	←→	I/O	←	INPUT
D1	3	N.C.	→	I/O	←→	I/O	←	N.C.
D2	3	I/O	→	I/O (Diff)	←→	I/O (Diff)	←	I/O
K3	3	VREF(INPUT)	→	VREF(I/O)	←→	VREF(I/O)	←	VREF(INPUT)
M9	2	N.C.	→	DUAL	←→	DUAL	←	N.C.
M10	2	N.C.	→	DUAL	←→	DUAL	←	N.C.
N9	2	N.C.	→	DUAL	←→	DUAL	←	N.C.
N10	2	N.C.	→	DUAL	←→	DUAL	←	N.C.
P11	2	VREF(INPUT)	→	VREF(I/O)	←→	VREF(I/O)	←	VREF(INPUT)
DIFFERENCES			**14**		**0**		**14**	

Legend:

←→ This pin is identical on the device on the left and the right.

→ This pin can unconditionally migrate from the device on the left to the device on the right. Migration in the other direction may be possible depending on how the pin is configured for the device on the right.

← This pin can unconditionally migrate from the device on the right to the device on the left. Migration in the other direction may be possible depending on how the pin is configured for the device on the left.

Table 137: **TQ144 Package Pinout *(Cont'd)***

Bank	XC3S100E Pin Name	XC3S250E Pin Name	TQ144 Pin	Type
2	IP	IP	P38	INPUT
2	IP	IP	P41	INPUT
2	IP	IP	P69	INPUT
2	IP_L03N_2/VREF_2	IP_L03N_2/VREF_2	P48	VREF
2	IP_L03P_2	IP_L03P_2	P47	INPUT
2	IP_L06N_2/M2/GCLK1	IP_L06N_2/M2/GCLK1	P57	DUAL/GCLK
2	IP_L06P_2/RDWR_B/GCLK0	IP_L06P_2/RDWR_B/GCLK0	P56	DUAL/GCLK
2	VCCO_2	VCCO_2	P42	VCCO
2	VCCO_2	VCCO_2	P49	VCCO
2	VCCO_2	VCCO_2	P64	VCCO
3	IP/VREF_3	IO/VREF_3	P31	***100E:*** VREF(INPUT) ***250E:*** VREF(I/O)
3	IO_L01N_3	IO_L01N_3	P3	I/O
3	IO_L01P_3	IO_L01P_3	P2	I/O
3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	P5	VREF
3	IO_L02P_3	IO_L02P_3	P4	I/O
3	IO_L03N_3	IO_L03N_3	P8	I/O
3	IO_L03P_3	IO_L03P_3	P7	I/O
3	IO_L04N_3/LHCLK1	IO_L04N_3/LHCLK1	P15	LHCLK
3	IO_L04P_3/LHCLK0	IO_L04P_3/LHCLK0	P14	LHCLK
3	IO_L05N_3/LHCLK3/IRDY2	IO_L05N_3/LHCLK3	P17	LHCLK
3	IO_L05P_3/LHCLK2	IO_L05P_3/LHCLK2	P16	LHCLK
3	IO_L06N_3/LHCLK5	IO_L06N_3/LHCLK5	P21	LHCLK
3	IO_L06P_3/LHCLK4/TRDY2	IO_L06P_3/LHCLK4	P20	LHCLK
3	IO_L07N_3/LHCLK7	IO_L07N_3/LHCLK7	P23	LHCLK
3	IO_L07P_3/LHCLK6	IO_L07P_3/LHCLK6	P22	LHCLK
3	IO_L08N_3	IO_L08N_3	P26	I/O
3	IO_L08P_3	IO_L08P_3	P25	I/O
3	IO_L09N_3	IO_L09N_3	P33	I/O
3	IO_L09P_3	IO_L09P_3	P32	I/O
3	IO_L10N_3	IO_L10N_3	P35	I/O
3	IO_L10P_3	IO_L10P_3	P34	I/O
3	IP	IP	P6	INPUT
3	IO	IP	P10	***100E:*** I/O ***250E:*** INPUT
3	IP	IP	P18	INPUT
3	IP	IP	P24	INPUT
3	IO	IP	P29	***100E:*** I/O ***250E:*** INPUT
3	IP	IP	P36	INPUT
3	IP/VREF_3	IP/VREF_3	P12	VREF
3	VCCO_3	VCCO_3	P13	VCCO
3	VCCO_3	VCCO_3	P28	VCCO
GND	GND	GND	P11	GND
GND	GND	GND	P19	GND

PQ208: 208-pin Plastic Quad Flat Package

The 208-pin plastic quad flat package, PQ208, supports two different Spartan-3E FPGAs, including the XC3S250E and the XC3S500E.

Table 141 lists all the PQ208 package pins. They are sorted by bank number and then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at:

http://www.xilinx.com/support/documentation/data_sheets/s3e_pin.zip

Pinout Table

Table 141: **PQ208 Package Pinout**

Bank	XC3S250E XC3S500E Pin Name	PQ208 Pin	Type
0	IO	P187	I/O
0	IO/VREF_0	P179	VREF
0	IO_L01N_0	P161	I/O
0	IO_L01P_0	P160	I/O
0	IO_L02N_0/VREF_0	P163	VREF
0	IO_L02P_0	P162	I/O
0	IO_L03N_0	P165	I/O
0	IO_L03P_0	P164	I/O
0	IO_L04N_0/VREF_0	P168	VREF
0	IO_L04P_0	P167	I/O
0	IO_L05N_0	P172	I/O
0	IO_L05P_0	P171	I/O
0	IO_L07N_0/GCLK5	P178	GCLK
0	IO_L07P_0/GCLK4	P177	GCLK
0	IO_L08N_0/GCLK7	P181	GCLK
0	IO_L08P_0/GCLK6	P180	GCLK
0	IO_L10N_0/GCLK11	P186	GCLK
0	IO_L10P_0/GCLK10	P185	GCLK
0	IO_L11N_0	P190	I/O
0	IO_L11P_0	P189	I/O
0	IO_L12N_0/VREF_0	P193	VREF
0	IO_L12P_0	P192	I/O
0	IO_L13N_0	P197	I/O
0	IO_L13P_0	P196	I/O
0	IO_L14N_0/VREF_0	P200	VREF
0	IO_L14P_0	P199	I/O
0	IO_L15N_0	P203	I/O

Table 141: **PQ208 Package Pinout *(Cont'd)***

Bank	XC3S250E XC3S500E Pin Name	PQ208 Pin	Type
0	IO_L15P_0	P202	I/O
0	IO_L16N_0/HSWAP	P206	DUAL
0	IO_L16P_0	P205	I/O
0	IP	P159	INPUT
0	IP	P169	INPUT
0	IP	P194	INPUT
0	IP	P204	INPUT
0	IP_L06N_0	P175	INPUT
0	IP_L06P_0	P174	INPUT
0	IP_L09N_0/GCLK9	P184	GCLK
0	IP_L09P_0/GCLK8	P183	GCLK
0	VCCO_0	P176	VCCO
0	VCCO_0	P191	VCCO
0	VCCO_0	P201	VCCO
1	IO_L01N_1/A15	P107	DUAL
1	IO_L01P_1/A16	P106	DUAL
1	IO_L02N_1/A13	P109	DUAL
1	IO_L02P_1/A14	P108	DUAL
1	IO_L03N_1/VREF_1	P113	VREF
1	IO_L03P_1	P112	I/O
1	IO_L04N_1	P116	I/O
1	IO_L04P_1	P115	I/O
1	IO_L05N_1/A11	P120	DUAL
1	IO_L05P_1/A12	P119	DUAL
1	IO_L06N_1/VREF_1	P123	VREF
1	IO_L06P_1	P122	I/O
1	IO_L07N_1/A9/RHCLK1	P127	RHCLK/DUAL
1	IO_L07P_1/A10/RHCLK0	P126	RHCLK/DUAL
1	IO_L08N_1/A7/RHCLK3	P129	RHCLK/DUAL
1	IO_L08P_1/A8/RHCLK2	P128	RHCLK/DUAL
1	IO_L09N_1/A5/RHCLK5	P133	RHCLK/DUAL
1	IO_L09P_1/A6/RHCLK4	P132	RHCLK/DUAL
1	IO_L10N_1/A3/RHCLK7	P135	RHCLK/DUAL
1	IO_L10P_1/A4/RHCLK6	P134	RHCLK/DUAL
1	IO_L11N_1/A1	P138	DUAL
1	IO_L11P_1/A2	P137	DUAL
1	IO_L12N_1/A0	P140	DUAL
1	IO_L12P_1	P139	I/O
1	IO_L13N_1	P145	I/O
1	IO_L13P_1	P144	I/O
1	IO_L14N_1	P147	I/O
1	IO_L14P_1	P146	I/O

Table 143: **FT256 Package Pinout *(Cont'd)***

Bank	XC3S250E Pin Name	XC3S500E Pin Name	XC3S1200E Pin Name	FT256 Ball	Type
3	IO_L06P_3	IO_L06P_3	IO_L06P_3	G5	I/O
3	IO_L07N_3	IO_L07N_3	IO_L07N_3	G2	I/O
3	IO_L07P_3	IO_L07P_3	IO_L07P_3	G3	I/O
3	IO_L08N_3/LHCLK1	IO_L08N_3/LHCLK1	IO_L08N_3/LHCLK1	H6	LHCLK
3	IO_L08P_3/LHCLK0	IO_L08P_3/LHCLK0	IO_L08P_3/LHCLK0	H5	LHCLK
3	IO_L09N_3/LHCLK3/ IRDY2	IO_L09N_3/LHCLK3/ IRDY2	IO_L09N_3/LHCLK3/ IRDY2	H4	LHCLK
3	IO_L09P_3/LHCLK2	IO_L09P_3/LHCLK2	IO_L09P_3/LHCLK2	H3	LHCLK
3	IO_L10N_3/LHCLK5	IO_L10N_3/LHCLK5	IO_L10N_3/LHCLK5	J3	LHCLK
3	IO_L10P_3/LHCLK4/ TRDY2	IO_L10P_3/LHCLK4/ TRDY2	IO_L10P_3/LHCLK4/ TRDY2	J2	LHCLK
3	IO_L11N_3/LHCLK7	IO_L11N_3/LHCLK7	IO_L11N_3/LHCLK7	J4	LHCLK
3	IO_L11P_3/LHCLK6	IO_L11P_3/LHCLK6	IO_L11P_3/LHCLK6	J5	LHCLK
3	IO_L12N_3	IO_L12N_3	IO_L12N_3	K1	I/O
3	IO_L12P_3	IO_L12P_3	IO_L12P_3	J1	I/O
3	IO_L13N_3	IO_L13N_3	IO_L13N_3	K3	I/O
3	IO_L13P_3	IO_L13P_3	IO_L13P_3	K2	I/O
3	N.C. (◆)	IO_L14N_3/VREF_3	IO_L14N_3/VREF_3	L2	***250E:*** N.C. ***500E:*** VREF ***1200E:*** VREF
3	N.C. (◆)	IO_L14P_3	IO_L14P_3	L3	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O
3	IO_L15N_3	IO_L15N_3	IO_L15N_3	L5	I/O
3	IO_L15P_3	IO_L15P_3	IO_L15P_3	K5	I/O
3	IO_L16N_3	IO_L16N_3	IO_L16N_3	N1	I/O
3	IO_L16P_3	IO_L16P_3	IO_L16P_3	M1	I/O
3	N.C. (◆)	IO_L17N_3	IO_L17N_3	L4	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O
3	N.C. (◆)	IO_L17P_3	IO_L17P_3	M4	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O
3	IO_L18N_3	IO_L18N_3	IO_L18N_3	P1	I/O
3	IO_L18P_3	IO_L18P_3	IO_L18P_3	P2	I/O
3	IO_L19N_3	IO_L19N_3	IO_L19N_3	R1	I/O
3	IO_L19P_3	IO_L19P_3	IO_L19P_3	R2	I/O
3	IP	IP	IP	D2	INPUT
3	IP	IP	IP	F2	INPUT
3	IO	IO	IP	F5	***250E:*** I/O ***500E:*** I/O ***1200E:*** INPUT
3	IP	IP	IP	H1	INPUT
3	IP	IP	IP	J6	INPUT
3	IP	IP	IP	K4	INPUT
3	IP	IP	IP	M3	INPUT

Table 148: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S500E Pin Name	XC3S1200E Pin Name	XC3S1600E Pin Name	FG320 Ball	Type
GND	GND	GND	GND	K8	GND
GND	GND	GND	GND	K11	GND
GND	GND	GND	GND	K16	GND
GND	GND	GND	GND	L8	GND
GND	GND	GND	GND	L9	GND
GND	GND	GND	GND	L10	GND
GND	GND	GND	GND	L11	GND
GND	GND	GND	GND	M7	GND
GND	GND	GND	GND	M12	GND
GND	GND	GND	GND	T9	GND
GND	GND	GND	GND	U2	GND
GND	GND	GND	GND	U17	GND
GND	GND	GND	GND	V1	GND
GND	GND	GND	GND	V18	GND
VCCAUX	DONE	DONE	DONE	V17	CONFIG
VCCAUX	PROG_B	PROG_B	PROG_B	B1	CONFIG
VCCAUX	TCK	TCK	TCK	A17	JTAG
VCCAUX	TDI	TDI	TDI	A2	JTAG
VCCAUX	TDO	TDO	TDO	C16	JTAG
VCCAUX	TMS	TMS	TMS	D15	JTAG
VCCAUX	VCCAUX	VCCAUX	VCCAUX	B7	VCCAUX
VCCAUX	VCCAUX	VCCAUX	VCCAUX	B12	VCCAUX
VCCAUX	VCCAUX	VCCAUX	VCCAUX	G2	VCCAUX
VCCAUX	VCCAUX	VCCAUX	VCCAUX	G17	VCCAUX
VCCAUX	VCCAUX	VCCAUX	VCCAUX	M2	VCCAUX
VCCAUX	VCCAUX	VCCAUX	VCCAUX	M17	VCCAUX
VCCAUX	VCCAUX	VCCAUX	VCCAUX	U7	VCCAUX
VCCAUX	VCCAUX	VCCAUX	VCCAUX	U12	VCCAUX
VCCINT	VCCINT	VCCINT	VCCINT	E5	VCCINT
VCCINT	VCCINT	VCCINT	VCCINT	E14	VCCINT
VCCINT	VCCINT	VCCINT	VCCINT	F6	VCCINT
VCCINT	VCCINT	VCCINT	VCCINT	F13	VCCINT
VCCINT	VCCINT	VCCINT	VCCINT	N6	VCCINT
VCCINT	VCCINT	VCCINT	VCCINT	N13	VCCINT
VCCINT	VCCINT	VCCINT	VCCINT	P5	VCCINT
VCCINT	VCCINT	VCCINT	VCCINT	P14	VCCINT

User I/Os by Bank

Table 149 and Table 150 indicate how the available user-I/O pins are distributed between the four I/O banks on the FG320 package.

Table 149: **User I/Os Per Bank for XC3S500E in the FG320 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF(1)	CLK(2)
Top	0	58	29	14	1	6	8
Right	1	58	22	10	21	5	0(2)
Bottom	2	58	17	13	24	4	0(2)
Left	3	58	34	11	0	5	8
TOTAL		**232**	**102**	**48**	**46**	**20**	**16**

Notes:

1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

Table 150: **User I/Os Per Bank for XC3S1200E and XC3S1600E in the FG320 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF(1)	CLK(2)
Top	0	61	34	12	1	6	8
Right	1	63	25	12	21	5	0(2)
Bottom	2	63	23	11	24	5	0(2)
Left	3	63	38	12	0	5	8
TOTAL		**250**	**120**	**47**	**46**	**21**	**16**

Notes:

1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.