AMD Xilinx - XC3S250E-4FTG256C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	612
Number of Logic Elements/Cells	5508
Total RAM Bits	221184
Number of I/O	172
Number of Gates	250000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s250e-4ftg256c

The wide multiplexers can be used by the automatic tools or instantiated in a design using a component such as the F5MUX. The symbol, signals, and function are described in Figure 21, Table 12, and Table 13. The description is similar for the F6MUX, F7MUX, and F8MUX. Each has versions with a general output, local output, or both.

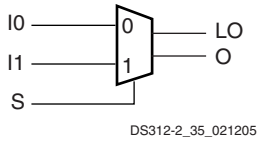

Figure 21: **F5MUX with Local and General Outputs**

Table 12: **F5MUX Inputs and Outputs**

Signal	Function
I0	Input selected when S is Low
I1	Input selected when S is High
S	Select input
LO	Local Output that connects to the F5 or FX CLB pins, which use local feedback to the FXIN inputs to the FiMUX for cascading
O	General Output that connects to the general-purpose combinatorial or registered outputs of the CLB

Table 13: **F5MUX Function**

Inputs			Outputs	
S	**I0**	**I1**	**O**	**LO**
0	1	X	1	1
0	0	X	0	0
1	X	1	1	1
1	X	0	0	0

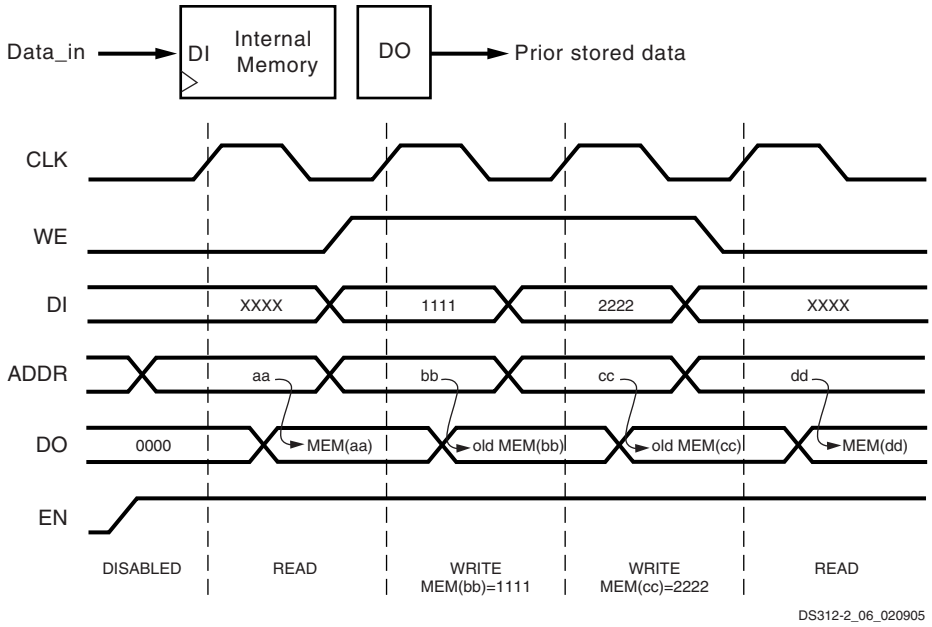

Figure 34: **Waveforms of Block RAM Data Operations with READ_FIRST Selected**

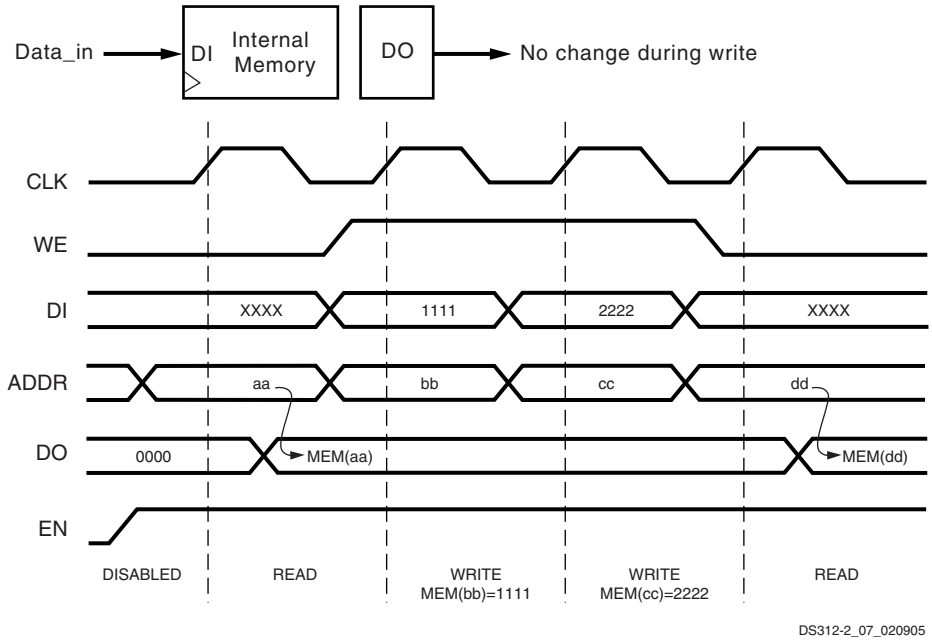

Figure 35: **Waveforms of Block RAM Data Operations with NO_CHANGE Selected**

Setting the WRITE_MODE attribute to a value of NO_CHANGE, puts the DO outputs in a latched state when asserting WE. Under this condition, the DO outputs retain the data driven just before WE is asserted. NO_CHANGE timing is shown in the portion of Figure 35 during which WE is High.

Table 31: **Direct Clock Input and Optional External Feedback to Left-Edge DCMs (XC3S1200E and XC3S1600E)**

Diff. Clock		Single-Ended Pin Number by Package Type								Left Edge		
		VQ100	CP132	TQ144	PQ208	FT256	FG320	FG400	FG484	LHCLK	DCM/BUFGMUX	
											BUFGMUX_X0Y5	D
											BUFGMUX_X0Y4	C
Pair	P	P9	F3	P14	P22	H5	J5	K3	M5	LHCLK0	DCM_X0Y2	Clock Lines
	N	P10	F2	P15	P23	H6	J4	K2	L5	LHCLK1		
Pair	P	P11	F1	P16	P24	H3	J1	K7	L8	LHCLK2		
	N	P12	G1	P17	P25	H4	J2	L7	M8	LHCLK3		
											BUFGMUX_X0Y3	B
											BUFGMUX_X0Y2	A
											BUFGMUX_X0Y9	H
											BUFGMUX_X0Y8	G
Pair	P	P15	G3	P20	P28	J2	K3	M1	M1	LHCLK4	DCM_X0Y1	Clock Lines
	N	P16	H1	P21	P29	J3	K4	L1	N1	LHCLK5		
Pair	P	P17	H2	P22	P30	J5	K6	M3	M3	LHCLK6		
	N	P18	H3	P23	P31	J4	K5	L3	M4	LHCLK7		
											BUFGMUX_X0Y7	F
											BUFGMUX_X0Y6	E

Table 32: **Direct Clock Input and Optional External Feedback to Right-Edge DCMs (XC3S1200E and XC3S1600E)**

	Right Edge		Single-Ended Pin Number by Package Type								Diff. Clock	
	DCM/BUFGMUX	RHCLK	VQ100	CP132	TQ144	PQ208	FT256	FG320	FG400	FG484		
D	BUFGMUX_X3Y5											
C	BUFGMUX_X3Y4											
Clock Lines	DCM_X3Y2	RHCLK7	P68	G13	P94	P135	H11	J14	J20	L19	N	Pair
		RHCLK6	P67	G14	P93	P134	H12	J15	K20	L18	P	
		RHCLK5	P66	H12	P92	P133	H14	J16	K14	L21	N	Pair
		RHCLK4	P65	H13	P91	P132	H15	J17	K13	L20	P	
B	BUFGMUX_X3Y3											
A	BUFGMUX_X3Y2											
H	BUFGMUX_X3Y9											
G	BUFGMUX_X3Y8											
Clock Lines	DCM_X3Y1	RHCLK3	P63	J14	P88	P129	J13	K14	L14	M16	N	Pair
		RHCLK2	P62	J13	P87	P128	J14	K15	L15	M15	P	
		RHCLK1	P61	J12	P86	P127	J16	K12	L16	M22	N	Pair
		RHCLK0	P60	K14	P85	P126	K16	K13	M16	N22	P	
F	BUFGMUX_X3Y7											
E	BUFGMUX_X3Y6											

Every FPGA input provides a possible DCM clock input, but the path is not temperature and voltage compensated like the GCLKs. Alternatively, clock signals within the FPGA optionally provide a DCM clock input via a Global Clock Multiplexer Buffer (BUFGMUX). The global clock net connects directly to the CLKIN input. The internal and external connections are shown in Figure 42a and Figure 42c, respectively.

Master Serial Mode

For additional information, refer to the “Master Serial Mode” chapter in UG332.

In Master Serial mode (M[2:0] = <0:0:0>), the Spartan-3E FPGA configures itself from an attached Xilinx Platform Flash PROM, as illustrated in Figure 51. The FPGA supplies the CCLK output clock from its internal oscillator to the attached Platform Flash PROM. In response, the Platform Flash PROM supplies bit-serial data to the FPGA’s DIN input, and the FPGA accepts this data on each rising CCLK edge.

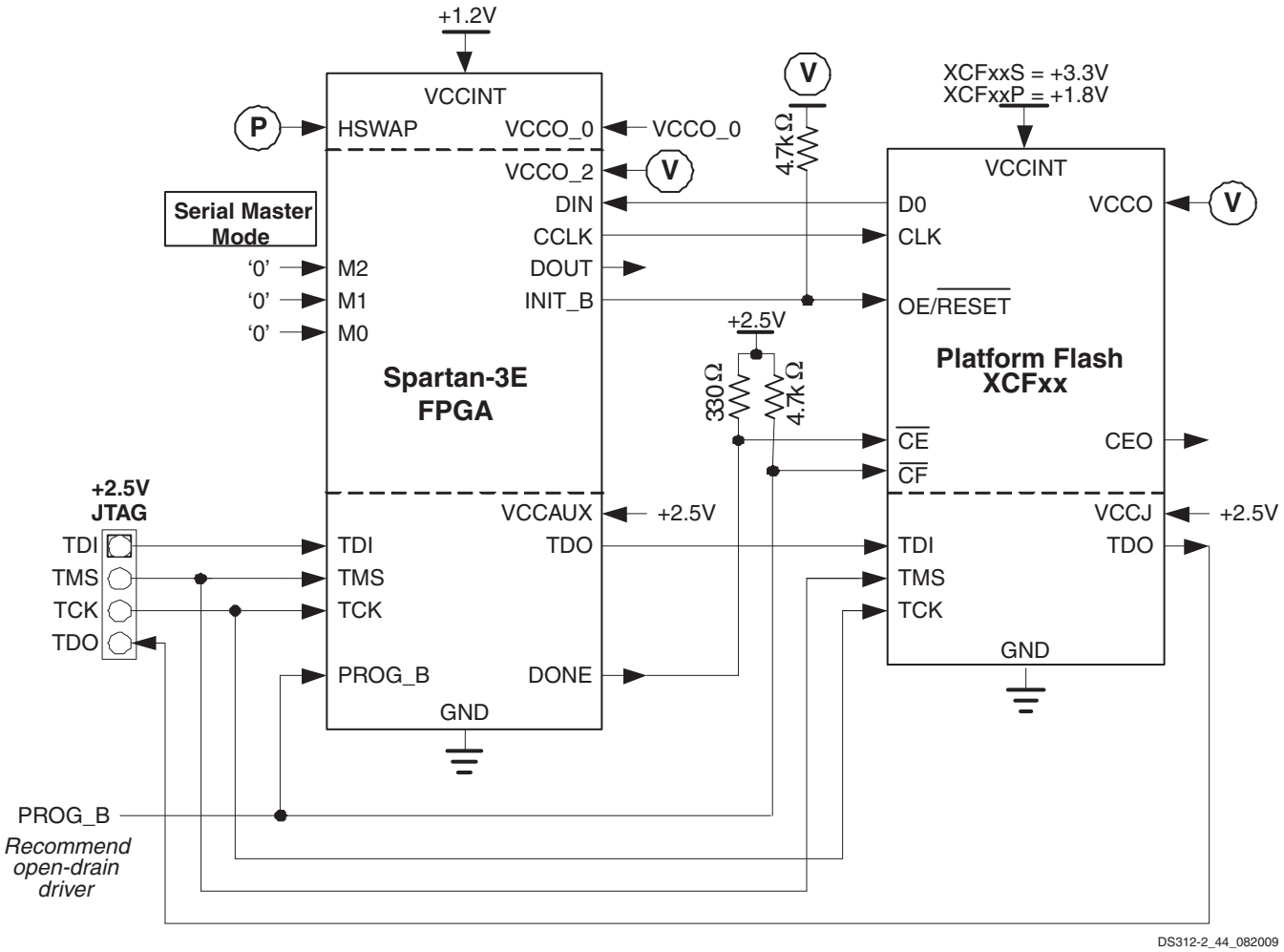

Figure 51: **Master Serial Mode using Platform Flash PROM**

All mode select pins, M[2:0], must be Low when sampled, when the FPGA’s INIT_B output goes High. After configuration, when the FPGA’s DONE output goes High, the mode select pins are available as full-featured user-I/O pins.

SPI Serial Flash Mode

For additional information, refer to the “Master SPI Mode” chapter in UG332.

In SPI Serial Flash mode (M[2:0] = <0:0:1>), the Spartan-3E FPGA configures itself from an attached industry-standard SPI serial Flash PROM, as illustrated in Figure 53 and Figure 54. The FPGA supplies the CCLK output clock from its internal oscillator to the clock input of the attached SPI Flash PROM.

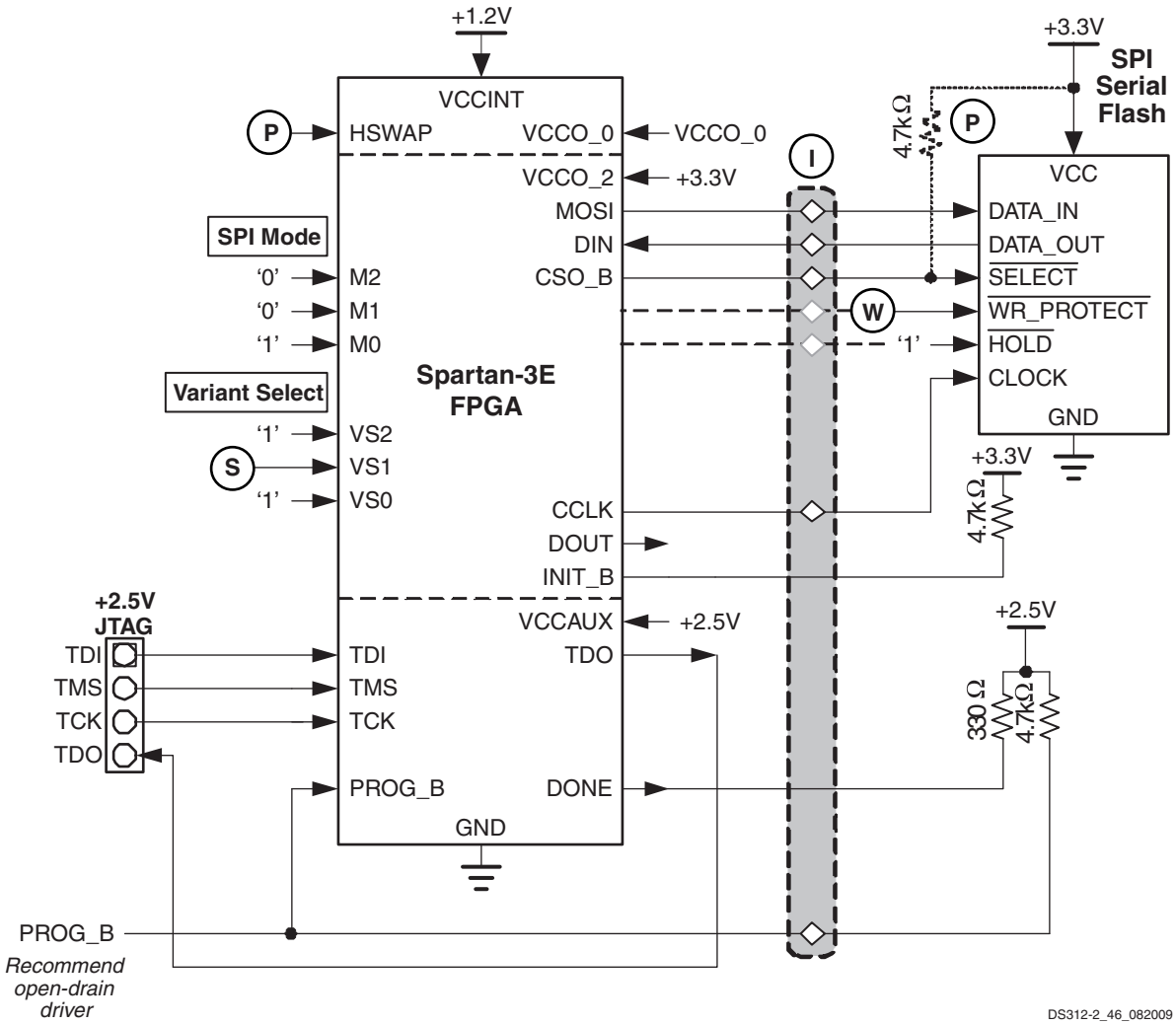

Figure 53: **SPI Flash PROM Interface for PROMs Supporting READ (0x03) and FAST_READ (0x0B) Commands**

Ⓢ Although SPI is a standard four-wire interface, various available SPI Flash PROMs use different command protocols. The FPGA’s variant select pins, VS[2:0], define how the FPGA communicates with the SPI Flash, including which SPI Flash command the FPGA issues to start the read operation and the number of dummy bytes inserted before the FPGA expects to receive valid data from the SPI Flash. Table 53 shows the available SPI Flash PROMs expected to operate with Spartan-3E FPGAs. Other compatible devices might work but have not been tested for suitability with Spartan-3E FPGAs. All other VS[2:0] values are reserved for future use. Consult the data sheet for the desired SPI Flash device to determine its suitability. The basic timing requirements and waveforms are provided in Serial Peripheral Interface (SPI) Configuration Timing in Module 3.

Figure 53 shows the general connection diagram for those SPI Flash PROMs that support the 0x03 READ command or the 0x0B FAST READ commands.

Figure 54 shows the connection diagram for Atmel DataFlash serial PROMs, which also use an SPI-based protocol. ‘B’-series DataFlash devices are limited to FPGA applications operating over the commercial temperature range. Industrial temperature range applications must use ‘C’- or ‘D’-series DataFlash devices, which have a shorter DataFlash select setup time, because of the faster FPGA CCLK frequency at cold temperatures.

Table 53: **Variant Select Codes for Various SPI Serial Flash PROMs**

VS2	VS1	VS0	SPI Read Command	Dummy Bytes	SPI Serial Flash Vendor	SPI Flash Family	iMPACT Programming Support
1	1	1	FAST READ (0x0B) (see Figure 53)	1	STMicroelectronics (ST)	M25Pxx M25PExx/M45PExx	Yes
					Atmel	AT45DB 'D'-Series Data Flash	Yes
						AT26 / AT25(1)	
					Intel	S33	
					Spansion *(AMD, Fujitsu)*	S25FLxxxA	
					Winbond *(NexFlash)*	NX25 / W25	
					Macronix	MX25Lxxxx	
					Silicon Storage Technology (SST)	SST25LFxxxA SST25VFxxxA	
					Programmable Microelectronics Corp. (PMC)	Pm25LVxxx	
					AMIC Technology	A25L	
					Eon Silicon Solution, Inc.	EN25	
1	0	1	READ (0x03) (see Figure 53)	0	STMicroelectronics (ST)	M25Pxx M25PExx/M45PExx	Yes
					Spansion *(AMD, Fujitsu)*	S25FLxxxA	
					Winbond *(NexFlash)*	NX25 / W25	
					Macronix	MX25Lxxxx	
					Silicon Storage Technology (SST)	SST25LFxxxA SST25VFxxxA SST25VFxxx	
					Programmable Microelectronics Corp. (PMC)	Pm25LVxxx	
1	1	0	READ ARRAY (0xE8) (see Figure 54)	4	Atmel Corporation	AT45DB DataFlash *(use only 'C' or 'D' Series for Industrial temperature range)*	Yes
Others			Reserved				

Notes:
1. See iMPACT documentation for specific device support.

WRITER NOTE: Many of the URLs in this table are obsolete or otherwise broken.

Table 59: **Byte-Wide Peripheral Interface (BPI) Connections *(Cont'd)***

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
DONE	Open-drain bidirectional I/O	**FPGA Configuration Done**. Low during configuration. Goes High when FPGA successfully completes configuration. Requires external 330 Ω pull-up resistor to 2.5V.	Low indicates that the FPGA is not yet configured.	Pulled High via external pull-up. When High, indicates that the FPGA is successfully configured.
PROG_B	Input	**Program FPGA**. Active Low. When asserted Low for 500 ns or longer, forces the FPGA to restart its configuration process by clearing configuration memory and resetting the DONE and INIT_B pins once PROG_B returns High. Recommend external 4.7 kΩ pull-up resistor to 2.5V. Internal pull-up value may be weaker (see Table 78). If driving externally with a 3.3V output, use an open-drain or open-collector driver or use a current limiting series resistor.	Must be High to allow configuration to start.	Drive PROG_B Low and release to reprogram FPGA. Hold PROG_B to force FPGA I/O pins into Hi-Z, allowing direct programming access to Flash PROM pins.

Voltage Compatibility

The FPGA's parallel Flash interface signals are within I/O Banks 1 and 2. The majority of parallel Flash PROMs use a single 3.3V supply voltage. Consequently, in most cases, the FPGA's VCCO_1 and VCCO_2 supply voltages must also be 3.3V to match the parallel Flash PROM. There are some 1.8V parallel Flash PROMs available and the FPGA interfaces with these devices if the VCCO_1 and VCCO_2 supplies are also 1.8V.

Power-On Precautions if PROM Supply is Last in Sequence

Like SPI Flash PROMs, parallel Flash PROMs typically require some amount of internal initialization time when the supply voltage reaches its minimum value.

The PROM supply voltage also connects to the FPGA's VCCO_2 supply input. In many systems, the PROM supply feeding the FPGA's VCCO_2 input is valid before the FPGA's other V_{CCINT} and V_{CCAUX} supplies, and consequently, there is no issue. However, if the PROM supply is last in the sequence, a potential race occurs between the FPGA and the parallel Flash PROM. See Power-On Precautions if 3.3V Supply is Last in Sequence for a similar description of the issue for SPI Flash PROMs.

Supported Parallel NOR Flash PROM Densities

Table 60 indicates the smallest usable parallel Flash PROM to program a single Spartan-3E FPGA. Parallel Flash density is specified in bits but addressed as bytes. The FPGA presents up to 24 address lines during configuration but not all are required for single FPGA applications. Table 60 shows the minimum required number of address lines between the FPGA and parallel Flash PROM. The actual number of address line required depends on the density of the attached parallel Flash PROM.

A multiple-FPGA daisy-chained application requires a parallel Flash PROM large enough to contain the sum of the FPGA file sizes. An application can also use a larger-density parallel Flash PROM to hold additional data beyond just FPGA configuration data. For example, the parallel Flash PROM can also contain the application code for a MicroBlaze RISC processor core implemented within the Spartan-3E FPGA. After configuration, the MicroBlaze processor can execute directly from external Flash or can copy the code to other, faster system memory before executing the code.

Table 60: **Number of Bits to Program a Spartan-3E FPGA and Smallest Parallel Flash PROM**

Spartan-3E FPGA	Uncompressed File Sizes (bits)	Smallest Usable Parallel Flash PROM	Minimum Required Address Lines
XC3S100E	581,344	1 Mbit	A[16:0]
XC3S250E	1,353,728	2 Mbit	A[17:0]
XC3S500E	2,270,208	4 Mbit	A[18:0]
XC3S1200E	3,841,184	4 Mbit	A[18:0]
XC3S1600E	5,969,696	8 Mbit	A[19:0]

Table 65: **Slave Parallel Mode Connections *(Cont'd)***

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
INIT_B	Open-drain bidirectional I/O	**Initialization Indicator**. Active Low. Goes Low at the start of configuration during the Initialization memory clearing process. Released at the end of memory clearing, when mode select pins are sampled. In daisy-chain applications, this signal requires an external 4.7 kΩ pull-up resistor to VCCO_2.	Active during configuration. If CRC error detected during configuration, FPGA drives INIT_B Low.	User I/O. If unused in the application, drive INIT_B High.
DONE	Open-drain bidirectional I/O	**FPGA Configuration Done**. Low during configuration. Goes High when FPGA successfully completes configuration. Requires external 330 Ω pull-up resistor to 2.5V.	Low indicates that the FPGA is not yet configured.	Pulled High via external pull-up. When High, indicates that the FPGA successfully configured.
PROG_B	Input	**Program FPGA**. Active Low. When asserted Low for 500 ns or longer, forces the FPGA to restart its configuration process by clearing configuration memory and resetting the DONE and INIT_B pins once PROG_B returns High. Recommend external 4.7 kΩ pull-up resistor to 2.5V. Internal pull-up value may be weaker (see Table 78). If driving externally with a 3.3V output, use an open-drain or open-collector driver or use a current limiting series resistor.	Must be High to allow configuration to start.	Drive PROG_B Low and release to reprogram FPGA.

Voltage Compatibility

Ⓥ Most Slave Parallel interface signals are within the FPGA's I/O Bank 2, supplied by the VCCO_2 supply input. The VCCO_2 voltage can be 1.8V, 2.5V, or 3.3V to match the requirements of the external host, ideally 2.5V. Using 1.8V or 3.3V requires additional design considerations as the DONE and PROG_B pins are powered by the FPGA's 2.5V V_{CCAUX} supply. See XAPP453: *The 3.3V Configuration of Spartan-3 FPGAs* for additional information.

Daisy-Chaining

If the application requires multiple FPGAs with different configurations, then configure the FPGAs using a daisy chain. Use Slave Parallel mode (M[2:0] = <1:1:0>) for all FPGAs in the daisy-chain. The schematic in Figure 62 is optimized for FPGA downloading and does not support the SelectMAP read interface. The FPGA's RDWR_B pin must be Low during configuration.

After the lead FPGA is filled with its configuration data, the lead FPGA enables the next FPGA in the daisy-chain by asserting is chip-select output, CSO_B.

Bitstream Generator (BitGen) Options

For additional information, refer to the "Configuration Bitstream Generator (BitGen) Settings" chapter in UG332.

Various Spartan-3E FPGA functions are controlled by specific bits in the configuration bitstream image. These values are specified when creating the bitstream image with the Bitstream Generator (BitGen) software.

Table 69 provides a list of all BitGen options for Spartan-3E FPGAs.

Table 69: **Spartan-3E FPGA Bitstream Generator (BitGen) Options**

Option Name	Pins/Function Affected	Values (***default***)	Description
ConfigRate	CCLK, Configuration	***1***, 3, 6, 12, 25, 50	Sets the approximate frequency, in MHz, of the internal oscillator using for Master Serial, SPI, and BPI configuration modes. The internal oscillator powers up at its lowest frequency, and the new setting is loaded as part of the configuration bitstream. The software default value is 1 (~1.5 MHz) starting with ISE 8.1, Service Pack 1.
StartupClk	Configuration, Startup	***Cclk***	***Default.*** The CCLK signal (internally or externally generated) controls the startup sequence when the FPGA transitions from configuration mode to the user mode. See Start-Up.
		UserClk	A clock signal from within the FPGA application controls the startup sequence when the FPGA transitions from configuration mode to the user mode. See Start-Up. The FPGA application supplies the user clock on the CLK pin on the STARTUP_SPARTAN3E primitive.
		Jtag	The JTAG TCK input controls the startup sequence when the FPGA transitions from the configuration mode to the user mode. See Start-Up.
UnusedPin	Unused I/O Pins	***Pulldown***	***Default.*** All unused I/O pins and input-only pins have a pull-down resistor to GND.
		Pullup	All unused I/O pins and input-only pins have a pull-up resistor to the VCCO_# supply for its associated I/O bank.
		Pullnone	All unused I/O pins and input-only pins are left floating (Hi-Z, high-impedance, three-state). Use external pull-up or pull-down resistors or logic to apply a valid signal level.
DONE_cycle	DONE pin, Configuration Startup	1, 2, 3, ***4***, 5, 6	Selects the Configuration Startup phase that activates the FPGA's DONE pin. See Start-Up.
GWE_cycle	All flip-flops, LUT RAMs, and SRL16 shift registers, Block RAM, Configuration Startup	1, 2, 3, 4, 5, ***6***	Selects the Configuration Startup phase that asserts the internal write-enable signal to all flip-flops, LUT RAMs and shift registers (SRL16). It also enables block RAM read and write operations. See Start-Up.
		Done	Waits for the DONE pin input to go High before asserting the internal write-enable signal to all flip-flops, LUT RAMs and shift registers (SRL16). Block RAM read and write operations are enabled at this time.
		Keep	Retains the current GWE_cycle setting for partial reconfiguration applications.
GTS_cycle	All I/O pins, Configuration	1, 2, 3, 4, ***5***, 6	Selects the Configuration Startup phase that releases the internal three-state control, holding all I/O buffers in high-impedance (Hi-Z). Output buffers actively drive, if so configured, after this point. See Start-Up.
		Done	Waits for the DONE pin input to go High before releasing the internal three-state control, holding all I/O buffers in high-impedance (Hi-Z). Output buffers actively drive, if so configured, after this point.
		Keep	Retains the current GTS_cycle setting for partial reconfiguration applications.
LCK_cycle	DCMs, Configuration Startup	***NoWait***	The FPGA does not wait for selected DCMs to lock before completing configuration.
		0, 1, 2, 3, 4, 5, 6	If one or more DCMs in the design have the STARTUP_WAIT attribute set to TRUE, the FPGA waits for such DCMs to acquire their respective input clock and assert their LOCKED output. This setting selects the Configuration Startup phase where the FPGA waits for the DCMs to lock.
DonePin	DONE pin	***Pullup***	Internally connects a pull-up resistor between DONE pin and V_{CCAUX}. An external 330 Ω pull-up resistor to V_{CCAUX} is still recommended.
		Pullnone	No internal pull-up resistor on DONE pin. An external 330 Ω pull-up resistor to V_{CCAUX} is required.

Voltage Regulators

Various power supply manufacturers offer complete power solutions for Xilinx FPGAs including some with integrated three-rail regulators specifically designed for Spartan-3 and Spartan-3E FPGAs. The Xilinx Power Corner website provides links to vendor solution guides and Xilinx power estimation and analysis tools.

Power Distribution System (PDS) Design and Decoupling/Bypass Capacitors

Good power distribution system (PDS) design is important for all FPGA designs, but especially so for high performance applications, greater than 100 MHz. Proper design results in better overall performance, lower clock and DCM jitter, and a generally more robust system. Before designing the printed circuit board (PCB) for the FPGA design, please review XAPP623: *Power Distribution System (PDS) Design: Using Bypass/Decoupling Capacitors*.

Power-On Behavior

For additional power-on behavior information, including I/O behavior before and during configuration, refer to the "Sequence of Events" chapter in UG332.

Spartan-3E FPGAs have a built-in Power-On Reset (POR) circuit that monitors the three power rails required to successfully configure the FPGA. At power-up, the POR circuit holds the FPGA in a reset state until the V_{CCINT}, V_{CCAUX}, and V_{CCO} Bank 2 supplies reach their respective input threshold levels (see Table 74 in Module 3). After all three supplies reach their respective thresholds, the POR reset is released and the FPGA begins its configuration process.

Supply Sequencing

Because the three FPGA supply inputs must be valid to release the POR reset and can be supplied in any order, there are no FPGA-specific voltage sequencing requirements. Applying the FPGA's V_{CCAUX} supply before the V_{CCINT} supply uses the least I_{CCINT} current.

Although the FPGA has no specific voltage sequence requirements, be sure to consider any potential sequencing requirement of the configuration device attached to the FPGA, such as an SPI serial Flash PROM, a parallel NOR Flash PROM, or a microcontroller. For example, Flash PROMs have a minimum time requirement before the PROM can be selected and this must be considered if the 3.3V supply is the last in the sequence. See Power-On Precautions if 3.3V Supply is Last in Sequence for more details.

When all three supplies are valid, the minimum current required to power-on the FPGA equals the worst-case quiescent current, specified in Table 79. Spartan-3E FPGAs do not require Power-On Surge (POS) current to successfully configure.

Surplus I_{CCINT} if V_{CCINT} Applied before V_{CCAUX}

If the V_{CCINT} supply is applied before the V_{CCAUX} supply, the FPGA might draw a surplus I_{CCINT} current in addition to the I_{CCINT} quiescent current levels specified in Table 79, page 118. The momentary additional I_{CCINT} surplus current might be a few hundred milliamperes under nominal conditions, significantly less than the instantaneous current consumed by the bypass capacitors at power-on. However, the surplus current immediately disappears when the V_{CCAUX} supply is applied, and, in response, the FPGA's I_{CCINT} quiescent current demand drops to the levels specified in Table 79. The FPGA does not use or require the surplus current to successfully power-on and configure. If applying V_{CCINT} before V_{CCAUX}, ensure that the regulator does not have a foldback feature that could inadvertently shut down in the presence of the surplus current.

Configuration Data Retention, Brown-Out

The FPGA's configuration data is stored in robust CMOS configuration latches. The data in these latches is retained even when the voltages drop to the minimum levels necessary to preserve RAM contents, as specified in Table 76.

If, after configuration, the V_{CCAUX} or V_{CCINT} supply drops below its data retention voltage, the current device configuration must be cleared using one of the following methods:

- Force the V_{CCAUX} or V_{CCINT} supply voltage below the minimum Power On Reset (POR) voltage threshold (Table 74).
- Assert PROG_B Low.

The POR circuit does not monitor the VCCO_2 supply after configuration. Consequently, dropping the VCCO_2 voltage does not reset the device by triggering a Power-On Reset (POR) event.

No Internal Charge Pumps or Free-Running Oscillators

Some system applications are sensitive to sources of analog noise. Spartan-3E FPGA circuitry is fully static and does not employ internal charge pumps.

The CCLK configuration clock is active during the FPGA configuration process. After configuration completes, the CCLK oscillator is automatically disabled unless the Bitstream Generator (BitGen) option ***Persist=Yes***.

Date	Version	Revision
03/16/07	3.5	Added information about new Spartan-3 Generation user guides (Design Documentation Available). Added cross-references to UG331: *Spartan-3 Generation FPGA User Guide* and to UG332: *Spartan-3 Generation Configuration User Guide*. Added note about possible JTAG configuration issues when the FPGA mode pins are set for Master mode and using software prior to ISE 9.1.01i (JTAG Mode). Removed a few lingering references to "weak" pull-up resistors, including in Figure 12. Removed vestigial references regarding the LDC[2:0] and HDC pins during Slave Parallel Mode configuration. These pins are not used in this configuration mode.
05/29/07	3.6	Added information about HSWAP and PCI differences between steppings to Table 71. Removed "Performance Differences between Global Buffers" to match improved specs in Module 3. Updated PROG_B pulse width descriptions to match specification in Module 3.
04/18/08	3.7	Corrected Figure 6 to show six taps and updated associated text. Added note for recommended pull-up on DONE in Table 55 and elsewhere. Added a caution regarding Persist of pins A20-A23. Updated Stepping description in Table 71 to note that only Stepping 1 is in production today. Updated links.
08/26/09	3.8	Added a frequency limitation to Equation 6. Added a new Equation 7 with a frequency limitation. Added a Spread Spectrum, page 56 paragraph. Added Table 42, page 60. Updated a Flash vendor name in Table 61, page 88. Removed the $\leq$ symbol from the flash read access times in Table 62, page 88. Revised the first paragraph in Configuration Sequence, page 101. Revised the first paragraph in Power-On Behavior, page 110. Revised the second paragraph in Production Stepping, page 111. Revised the first paragraph in Ordering a Later Stepping, page 111.
10/29/12	4.0	Added Notice of Disclaimer. This product is not recommended for new designs. Updated the design note section in VARIABLE Phase Shift Mode. Added the VQ100 to the Quadrant Clock Routing section.

Notice of Disclaimer

General Recommended Operating Conditions

Table 77: **General Recommended Operating Conditions**

Symbol	Description			Min	Nominal	Max	Units
T_J	Junction temperature	Commercial		0	–	85	°C
		Industrial		–40	–	100	°C
V_{CCINT}	Internal supply voltage			1.140	1.200	1.260	V
V_{CCO} (1)	Output driver supply voltage			1.100	-	3.465	V
V_{CCAUX}	Auxiliary supply voltage			2.375	2.500	2.625	V
V_{IN} (2,3)	Input voltage extremes to avoid turning on I/O protection diodes	I/O, Input-only, and Dual-Purpose pins (4)	IP or IO_#	–0.5	–	V_{CCO} + 0.5	V
			IO_Lxxy_# (5)	–0.5	–	V_{CCO} + 0.5	V
		Dedicated pins (6)		–0.5	–	V_{CCAUX} + 0.5	V
T_{IN}	Input signal transition time (7)			–	–	500	ns

Notes:

1. This V_{CCO} range spans the lowest and highest operating voltages for all supported I/O standards. Table 80 lists the recommended V_{CCO} range specific to each of the single-ended I/O standards, and Table 82 lists that specific to the differential standards.
2. Input voltages outside the recommended range require the I_{IK} input clamp diode rating is met and no more than 100 pins exceed the range simultaneously. Refer to Table 73.
3. See XAPP459: *Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins on Spartan-3 Families*.
4. Each of the User I/O and Dual-Purpose pins is associated with one of the four banks' V_{CCO} rails. Meeting the V_{IN} limit ensures that the internal diode junctions that exist between these pins and their associated V_{CCO} and GND rails do not turn on. The absolute maximum rating is provided in Table 73.
5. For single-ended signals that are placed on a differential-capable I/O, V_{IN} of –0.2V to –0.5V is supported but can cause increased leakage between the two pins. See *Parasitic Leakage* in UG331, *Spartan-3 Generation FPGA User Guide*.
6. All Dedicated pins (PROG_B, DONE, TCK, TDI, TDO, and TMS) draw power from the V_{CCAUX} rail (2.5V). Meeting the V_{IN} max limit ensures that the internal diode junctions that exist between each of these pins and the V_{CCAUX} and GND rails do not turn on.
7. Measured between 10% and 90% V_{CCO}. Follow Signal Integrity recommendations.

Switching Characteristics

All Spartan-3E FPGAs ship in two speed grades: -4 and the higher performance -5. Switching characteristics in this document may be designated as Advance, Preliminary, or Production, as shown in Table 84. Each category is defined as follows:

Advance: These specifications are based on simulations only and are typically available soon after establishing FPGA specifications. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These specifications are based on complete early silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting preliminary delays is greatly reduced compared to Advance data.

Production: These specifications are approved once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Software Version Requirements

Production-quality systems must use FPGA designs compiled using a speed file designated as PRODUCTION status. FPGAs designs using a less mature speed file designation should only be used during system prototyping or pre-production qualification. FPGA designs with speed files designated as Advance or Preliminary should not be used in a production-quality system.

Whenever a speed file designation changes, as a device matures toward Production status, rerun the latest Xilinx ISE software on the FPGA design to ensure that the FPGA design incorporates the latest timing information and software updates.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all Spartan-3E devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.**

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Timing parameters and their representative values are selected for inclusion below either because they are important as general design requirements or they indicate fundamental device performance characteristics. The Spartan-3E speed files (v1.27), part of the Xilinx Development Software, are the original source for many but not all of the values. The speed grade designations for these files are shown in Table 84. For more complete, more precise, and worst-case data, use the values reported by the Xilinx static timing analyzer (TRACE in the Xilinx development software) and back-annotated to the simulation netlist.

Table 84: **Spartan-3E v1.27 Speed Grade Designations**

Device	Advance	Preliminary	Production
XC3S100E			-MIN, -4, -5
XC3S250E			-MIN, -4, -5
XC3S500E			-MIN, -4, -5
XC3S1200E			-MIN, -4, -5
XC3S1600E			-MIN, -4, -5

Table 85 provides the history of the Spartan-3E speed files since all devices reached Production status.

Table 85: **Spartan-3E Speed File Version History**

Version	ISE Release	Description
1.27	9.2.03i	Added XA Automotive.
1.26	8.2.02i	Added -0/-MIN speed grade, which includes minimum values.
1.25	8.2.01i	Added XA Automotive devices to speed file. Improved model for left and right DCMs.
1.23	8.2i	Updated input setup/hold values based on default IFD_DELAY_VALUE settings.
1.21	8.1.03i	All Spartan-3E FPGAs and all speed grades elevated to Production status.

Simultaneously Switching Output Guidelines

This section provides guidelines for the recommended maximum allowable number of Simultaneous Switching Outputs (SSOs). These guidelines describe the maximum number of user I/O pins of a given output signal standard that should simultaneously switch in the same direction, while maintaining a safe level of switching noise. Meeting these guidelines for the stated test conditions ensures that the FPGA operates free from the adverse effects of ground and power bounce.

Ground or power bounce occurs when a large number of outputs simultaneously switch in the same direction. The output drive transistors all conduct current to a common voltage rail. Low-to-High transitions conduct to the V_{CCO} rail; High-to-Low transitions conduct to the GND rail. The resulting cumulative current transient induces a voltage difference across the inductance that exists between the die pad and the power supply or ground return. The inductance is associated with bonding wires, the package lead frame, and any other signal routing inside the package. Other variables contribute to SSO noise levels, including stray inductance on the PCB as well as capacitive loading at receivers. Any SSO-induced voltage consequently affects internal switching noise margins and ultimately signal quality.

Table 96 and Table 97 provide the essential SSO guidelines. For each device/package combination, Table 96 provides the number of equivalent V_{CCO}/GND pairs. The equivalent number of pairs is based on characterization and might not match the physical number of pairs. For each output signal standard and drive strength, Table 97 recommends the maximum number of SSOs, switching in the same direction, allowed per V_{CCO}/GND pair within an I/O bank. The guidelines in Table 97 are categorized by package style. Multiply the appropriate numbers from Table 96 and Table 97 to calculate the maximum number of SSOs allowed within an I/O bank. Exceeding these SSO guidelines might result in increased power or ground bounce, degraded signal integrity, or increased system jitter.

SSO_{MAX}/IO Bank = Table 96 x Table 97

The recommended maximum SSO values assumes that the FPGA is soldered on the printed circuit board and that the board uses sound design practices. The SSO values do not apply for FPGAs mounted in sockets, due to the lead inductance introduced by the socket.

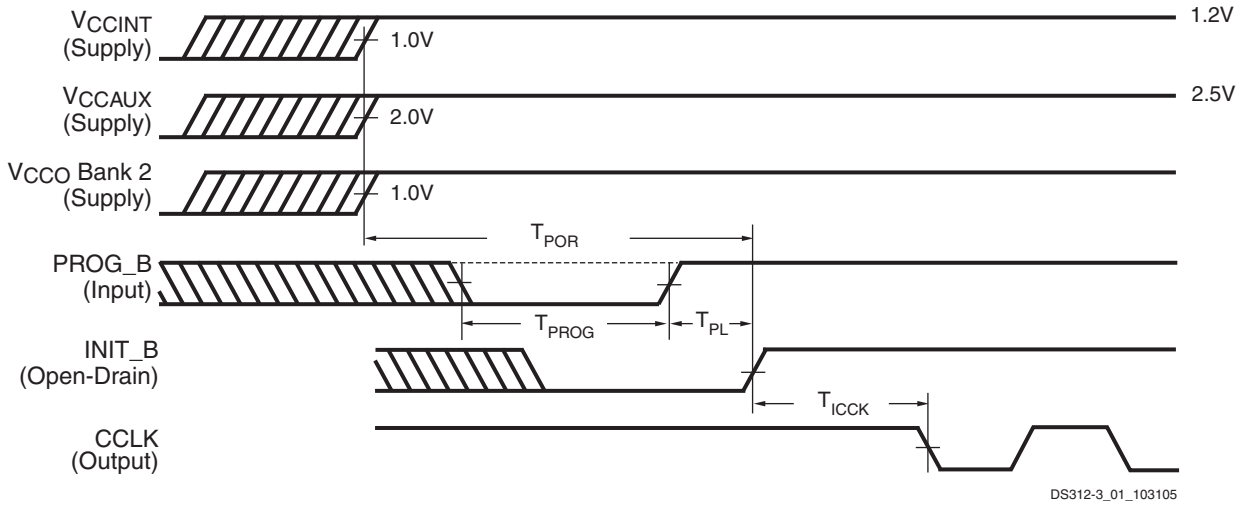
The number of SSOs allowed for quad-flat packages (VQ, TQ, PQ) is lower than for ball grid array packages (FG) due to the larger lead inductance of the quad-flat packages. The results for chip-scale packaging (CP132) are better than quad-flat packaging but not as high as for ball grid array packaging. Ball grid array packages are recommended for applications with a large number of simultaneously switching outputs.

Table 96: **Equivalent V_{CCO}/GND Pairs per Bank**

Device	Package Style *(including Pb-free)*							
	VQ100	CP132	TQ144	PQ208	FT256	FG320	FG400	FG484
XC3S100E	2	2	2	-	-	-	-	-
XC3S250E	2	2	2	3	4	-	-	-
XC3S500E	2	2	-	3	4	5	-	-
XC3S1200E	-	-	-	-	4	5	6	-
XC3S1600E	-	-	-	-	-	5	6	7

Configuration and JTAG Timing

General Configuration Power-On/Reconfigure Timing



Notes:

1. The V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies may be applied in any order.
2. The Low-going pulse on PROG_B is optional after power-on but necessary for reconfiguration without a power cycle.
3. The rising edge of INIT_B samples the voltage levels applied to the mode pins (M0 - M2).

Figure 73: **Waveforms for Power-On and the Beginning of Configuration**

Table 111: **Power-On Timing and the Beginning of Configuration**

Symbol	Description	Device	All Speed Grades		Units
			Min	Max	
T_{POR}(2)	The time from the application of V_{CCINT}, V_{CCAUX}, and V_{CCO} Bank 2 supply voltage ramps (whichever occurs last) to the rising transition of the INIT_B pin	XC3S100E	-	5	ms
		XC3S250E	-	5	ms
		XC3S500E	-	5	ms
		XC3S1200E	-	5	ms
		XC3S1600E	-	7	ms
T_{PROG}	The width of the low-going pulse on the PROG_B pin	All	0.5	-	µs
T_{PL}(2)	The time from the rising edge of the PROG_B pin to the rising transition on the INIT_B pin	XC3S100E	-	0.5	ms
		XC3S250E	-	0.5	ms
		XC3S500E	-	1	ms
		XC3S1200E	-	2	ms
		XC3S1600E	-	2	ms
T_{INIT}	Minimum Low pulse width on INIT_B output	All	250	-	ns
T_{ICCK}(3)	The time from the rising edge of the INIT_B pin to the generation of the configuration clock signal at the CCLK output pin	All	0.5	4.0	µs

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 77. This means power must be applied to all V_{CCINT}, V_{CCO}, and V_{CCAUX} lines.
2. Power-on reset and the clearing of configuration memory occurs during this period.
3. This specification applies only to the Master Serial, SPI, BPI-Up, and BPI-Down modes.

Table 133: **CP132 Package Pinout *(Cont'd)***

Bank	XC3S100E Pin Name	XC3S250E XC3S500E Pin Name	CP132 Ball	Type
2	N.C. (◆)	IO_L08P_2/A23	N9	***100E:*** N.C. ***Others:*** DUAL
2	N.C. (◆)	IO_L09N_2/A20	M10	***100E:*** N.C. ***Others:*** DUAL
2	N.C. (◆)	IO_L09P_2/A21	N10	***100E:*** N.C. ***Others:*** DUAL
2	IO_L10N_2/VS1/A18	IO_L10N_2/VS1/A18	M11	DUAL
2	IO_L10P_2/VS2/A19	IO_L10P_2/VS2/A19	N11	DUAL
2	IO_L11N_2/CCLK	IO_L11N_2/CCLK	N12	DUAL
2	IO_L11P_2/VS0/A17	IO_L11P_2/VS0/A17	P12	DUAL
2	IP/VREF_2	IP/VREF_2	N3	VREF
2	IP_L05N_2/M2/GCLK1	IP_L05N_2/M2/GCLK1	N6	DUAL/GCLK
2	IP_L05P_2/RDWR_B/GCLK0	IP_L05P_2/RDWR_B/GCLK0	M6	DUAL/GCLK
2	VCCO_2	VCCO_2	M8	VCCO
2	VCCO_2	VCCO_2	P3	VCCO
3	IO	IO	J3	I/O
3	IP/VREF_3	IO/VREF_3	K3	***100E:*** VREF(INPUT) ***Others:*** VREF(I/O)
3	IO_L01N_3	IO_L01N_3	B1	I/O
3	IO_L01P_3	IO_L01P_3	B2	I/O
3	IO_L02N_3	IO_L02N_3	C2	I/O
3	IO_L02P_3	IO_L02P_3	C3	I/O
3	N.C. (◆)	IO_L03N_3	D1	***100E:*** N.C. ***Others:*** I/O
3	IO	IO_L03P_3	D2	I/O
3	IO_L04N_3/LHCLK1	IO_L04N_3/LHCLK1	F2	LHCLK
3	IO_L04P_3/LHCLK0	IO_L04P_3/LHCLK0	F3	LHCLK
3	IO_L05N_3/LHCLK3/IRDY2	IO_L05N_3/LHCLK3/IRDY2	G1	LHCLK
3	IO_L05P_3/LHCLK2	IO_L05P_3/LHCLK2	F1	LHCLK
3	IO_L06N_3/LHCLK5	IO_L06N_3/LHCLK5	H1	LHCLK
3	IO_L06P_3/LHCLK4/TRDY2	IO_L06P_3/LHCLK4/TRDY2	G3	LHCLK
3	IO_L07N_3/LHCLK7	IO_L07N_3/LHCLK7	H3	LHCLK
3	IO_L07P_3/LHCLK6	IO_L07P_3/LHCLK6	H2	LHCLK
3	IO_L08N_3	IO_L08N_3	L2	I/O
3	IO_L08P_3	IO_L08P_3	L1	I/O
3	IO_L09N_3	IO_L09N_3	M1	I/O
3	IO_L09P_3	IO_L09P_3	L3	I/O
3	IP/VREF_3	IP/VREF_3	E2	VREF
3	VCCO_3	VCCO_3	E1	VCCO
3	VCCO_3	VCCO_3	J2	VCCO
GND	N.C. (GND)	GND	A4	GND
GND	GND	GND	A8	GND
GND	N.C. (GND)	GND	C1	GND
GND	GND	GND	C7	GND

FG320: 320-ball Fine-pitch Ball Grid Array

The 320-ball fine-pitch ball grid array package, FG320, supports three different Spartan-3E FPGAs, including the XC3S500E, the XC3S1200E, and the XC3S1600E, as shown in Table 148 and Figure 86.

The FG320 package is an 18 x 18 array of solder balls minus the four center balls.

Table 148 lists all the package pins. They are sorted by bank number and then by pin name of the largest device. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The highlighted rows indicate pinout differences between the XC3S500E, the XC3S1200E, and the XC3S1600E FPGAs. The XC3S500E has 18 unconnected balls, indicated as N.C. (No Connection) in Table 148 and with the black diamond character (◆) in Table 148 and Figure 86.

If the table row is highlighted in tan, then this is an instance where an unconnected pin on the XC3S500E FPGA maps to a VREF pin on the XC3S1200E and XC3S1600E FPGA. If the FPGA application uses an I/O standard that requires a VREF voltage reference, connect the highlighted pin to the VREF voltage supply, even though this does not actually connect to the XC3S500E FPGA. This VREF connection on the board allows future migration to the larger devices without modifying the printed-circuit board.

All other balls have nearly identical functionality on all three devices. Table 147 summarizes the Spartan-3E footprint migration differences for the FG320 package.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx web site at:

http://www.xilinx.com/support/documentation/data_sheets/s3e_pin.zip

Pinout Table

Table 148: **FG320 Package Pinout**

Bank	XC3S500E Pin Name	XC3S1200E Pin Name	XC3S1600E Pin Name	FG320 Ball	Type
0	IP	IO	IO	A7	**500E:** INPUT **1200E:** I/O **1600E:** I/O
0	IO	IO	IO	A8	I/O
0	IO	IO	IO	A11	I/O
0	N.C. (◆)	IO	IO	A12	**500E:** N.C. **1200E:** I/O **1600E:** I/O
0	IO	IO	IO	C4	I/O
0	IP	IO	IO	D13	**500E:** INPUT **1200E:** I/O **1600E:** I/O
0	IO	IO	IO	E13	I/O
0	IO	IO	IO	G9	I/O
0	IO/VREF_0	IO/VREF_0	IO/VREF_0	B11	VREF
0	IO_L01N_0	IO_L01N_0	IO_L01N_0	A16	I/O
0	IO_L01P_0	IO_L01P_0	IO_L01P_0	B16	I/O
0	IO_L03N_0/VREF_0	IO_L03N_0/VREF_0	IO_L03N_0/VREF_0	C14	VREF
0	IO_L03P_0	IO_L03P_0	IO_L03P_0	D14	I/O
0	IO_L04N_0	IO_L04N_0	IO_L04N_0	A14	I/O
0	IO_L04P_0	IO_L04P_0	IO_L04P_0	B14	I/O
0	IO_L05N_0/VREF_0	IO_L05N_0/VREF_0	IO_L05N_0/VREF_0	B13	VREF
0	IO_L05P_0	IO_L05P_0	IO_L05P_0	A13	I/O
0	IO_L06N_0	IO_L06N_0	IO_L06N_0	E12	I/O
0	IO_L06P_0	IO_L06P_0	IO_L06P_0	F12	I/O
0	IO_L08N_0	IO_L08N_0	IO_L08N_0	F11	I/O

Table 148: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S500E Pin Name	XC3S1200E Pin Name	XC3S1600E Pin Name	FG320 Ball	Type
0	VCCO_0	VCCO_0	VCCO_0	A9	VCCO
0	VCCO_0	VCCO_0	VCCO_0	C6	VCCO
0	VCCO_0	VCCO_0	VCCO_0	C13	VCCO
0	VCCO_0	VCCO_0	VCCO_0	G8	VCCO
0	VCCO_0	VCCO_0	VCCO_0	G11	VCCO
1	N.C. (◆)	IO	IO	P16	**500E:** N.C. **1200E:** I/O **1600E:** I/O
1	IO_L01N_1/A15	IO_L01N_1/A15	IO_L01N_1/A15	T17	DUAL
1	IO_L01P_1/A16	IO_L01P_1/A16	IO_L01P_1/A16	U18	DUAL
1	IO_L02N_1/A13	IO_L02N_1/A13	IO_L02N_1/A13	T18	DUAL
1	IO_L02P_1/A14	IO_L02P_1/A14	IO_L02P_1/A14	R18	DUAL
1	IO_L03N_1/VREF_1	IO_L03N_1/VREF_1	IO_L03N_1/VREF_1	R16	VREF
1	IO_L03P_1	IO_L03P_1	IO_L03P_1	R15	I/O
1	N.C. (◆)	IO_L04N_1	IO_L04N_1	N14	**500E:** N.C. **1200E:** I/O **1600E:** I/O
1	N.C. (◆)	IO_L04P_1	IO_L04P_1	N15	**500E:** N.C. **1200E:** I/O **1600E:** I/O
1	IO_L05N_1/VREF_1	IO_L05N_1/VREF_1	IO_L05N_1/VREF_1	M13	VREF
1	IO_L05P_1	IO_L05P_1	IO_L05P_1	M14	I/O
1	IO_L06N_1	IO_L06N_1	IO_L06N_1	P18	I/O
1	IO_L06P_1	IO_L06P_1	IO_L06P_1	P17	I/O
1	IO_L07N_1	IO_L07N_1	IO_L07N_1	M16	I/O
1	IO_L07P_1	IO_L07P_1	IO_L07P_1	M15	I/O
1	IO_L08N_1	IO_L08N_1	IO_L08N_1	M18	I/O
1	IO_L08P_1	IO_L08P_1	IO_L08P_1	N18	I/O
1	IO_L09N_1/A11	IO_L09N_1/A11	IO_L09N_1/A11	L15	DUAL
1	IO_L09P_1/A12	IO_L09P_1/A12	IO_L09P_1/A12	L16	DUAL
1	IO_L10N_1/VREF_1	IO_L10N_1/VREF_1	IO_L10N_1/VREF_1	L17	VREF
1	IO_L10P_1	IO_L10P_1	IO_L10P_1	L18	I/O
1	IO_L11N_1/A9/RHCLK1	IO_L11N_1/A9/RHCLK1	IO_L11N_1/A9/RHCLK1	K12	RHCLK/DUAL
1	IO_L11P_1/A10/RHCLK0	IO_L11P_1/A10/RHCLK0	IO_L11P_1/A10/RHCLK0	K13	RHCLK/DUAL
1	IO_L12N_1/A7/RHCLK3/ TRDY1	IO_L12N_1/A7/RHCLK3/ TRDY1	IO_L12N_1/A7/RHCLK3/ TRDY1	K14	RHCLK/DUAL
1	IO_L12P_1/A8/RHCLK2	IO_L12P_1/A8/RHCLK2	IO_L12P_1/A8/RHCLK2	K15	RHCLK/DUAL
1	IO_L13N_1/A5/RHCLK5	IO_L13N_1/A5/RHCLK5	IO_L13N_1/A5/RHCLK5	J16	RHCLK/DUAL
1	IO_L13P_1/A6/RHCLK4/ IRDY1	IO_L13P_1/A6/RHCLK4/ IRDY1	IO_L13P_1/A6/RHCLK4/ IRDY1	J17	RHCLK/DUAL
1	IO_L14N_1/A3/RHCLK7	IO_L14N_1/A3/RHCLK7	IO_L14N_1/A3/RHCLK7	J14	RHCLK/DUAL
1	IO_L14P_1/A4/RHCLK6	IO_L14P_1/A4/RHCLK6	IO_L14P_1/A4/RHCLK6	J15	RHCLK/DUAL
1	IO_L15N_1/A1	IO_L15N_1/A1	IO_L15N_1/A1	J13	DUAL
1	IO_L15P_1/A2	IO_L15P_1/A2	IO_L15P_1/A2	J12	DUAL
1	IO_L16N_1/A0	IO_L16N_1/A0	IO_L16N_1/A0	H17	DUAL
1	IO_L16P_1	IO_L16P_1	IO_L16P_1	H16	I/O

Footprint Migration Differences

Table 151 summarizes any footprint and functionality differences between the XC3S500E, the XC3S1200E, and the XC3S1600E FPGAs that may affect easy migration between devices available in the FG320 package. There are 26 such balls. All other pins not listed in Table 151 unconditionally migrate between Spartan-3E devices available in the FG320 package.

The XC3S500E is duplicated on both the left and right sides of the table to show migrations to and from the XC3S1200E and the XC3S1600E. The arrows indicate the direction for easy migration. A double-ended arrow (←→) indicates that the two pins have identical functionality. A left-facing arrow (←) indicates that the pin on the device on the right unconditionally migrates to the pin on the device on the left. It may be possible to migrate the opposite direction depending on the I/O configuration. For example, an I/O pin (Type = I/O) can migrate to an input-only pin (Type = INPUT) if the I/O pin is configured as an input.

Table 151: **FG320 Footprint Migration Differences**

Pin	Bank	XC3S500E	Migration	XC3S1200E	Migration	XC3S1600E	Migration	XC3S500E
A7	0	INPUT	→	I/O	←→	I/O	←	INPUT
A12	0	N.C.	→	I/O	←→	I/O	←	N.C.
D4	3	N.C.	→	I/O	←→	I/O	←	N.C.
D6	0	N.C.	→	I/O	←→	I/O	←	N.C.
D13	0	INPUT	→	I/O	←→	I/O	←	INPUT
E3	3	N.C.	→	I/O	←→	I/O	←	N.C.
E4	3	N.C.	→	I/O	←→	I/O	←	N.C.
E6	0	N.C.	→	I/O	←→	I/O	←	N.C.
E15	1	N.C.	→	I/O	←→	I/O	←	N.C.
E16	1	N.C.	→	I/O	←→	I/O	←	N.C.
E17	1	I/O	←	INPUT	←→	INPUT	→	I/O
F4	3	I/O	←	INPUT	←→	INPUT	→	I/O
N12	2	N.C.	→	I/O	←→	I/O	←	N.C.
N14	1	N.C.	→	I/O	←→	I/O	←	N.C.
N15	1	N.C.	→	I/O	←→	I/O	←	N.C.
P3	3	N.C.	→	I/O	←→	I/O	←	N.C.
P4	3	N.C.	→	I/O	←→	I/O	←	N.C.
P12	2	N.C.	→	I/O	←→	I/O	←	N.C.
P15	1	I/O	←	INPUT	←→	INPUT	→	I/O
P16	1	N.C.	→	I/O	←→	I/O	←	N.C.
R4	3	VREF(I/O)	←	VREF(INPUT)	←→	VREF(INPUT)	→	VREF(I/O)
U6	2	INPUT	→	I/O	←→	I/O	←	INPUT
U13	2	INPUT	→	I/O	←→	I/O	←	INPUT
V5	2	N.C.	→	I/O	←→	I/O	←	N.C.
V6	2	N.C.	→	VREF	←→	VREF	←	N.C.
V7	2	N.C.	→	I/O	←→	I/O	←	N.C.
DIFFERENCES			**26**		**0**		**26**	

Legend:

←→ This pin is identical on the device on the left and the right.

→ This pin can unconditionally migrate from the device on the left to the device on the right. Migration in the other direction may be possible depending on how the pin is configured for the device on the right.

← This pin can unconditionally migrate from the device on the right to the device on the left. Migration in the other direction may be possible depending on how the pin is configured for the device on the left.

FG484: 484-ball Fine-pitch Ball Grid Array

The 484-ball fine-pitch ball grid array, FG484, supports the XC3S1600E FPGA.

Table 154 lists all the FG484 package pins. They are sorted by bank number and then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at:

http://www.xilinx.com/support/documentation/data_sheets/s3e_pin.zip

Pinout Table

Table 154: **FG484 Package Pinout**

Bank	XC3S1600E Pin Name	FG484 Ball	Type
0	IO	B6	I/O
0	IO	B13	I/O
0	IO	C5	I/O
0	IO	C14	I/O
0	IO	E16	I/O
0	IO	F9	I/O
0	IO	F16	I/O
0	IO	G8	I/O
0	IO	H10	I/O
0	IO	H15	I/O
0	IO	J11	I/O
0	IO/VREF_0	G12	VREF
0	IO_L01N_0	C18	I/O
0	IO_L01P_0	C19	I/O
0	IO_L03N_0/VREF_0	A20	VREF
0	IO_L03P_0	A21	I/O
0	IO_L04N_0	A19	I/O
0	IO_L04P_0	A18	I/O
0	IO_L06N_0	C16	I/O
0	IO_L06P_0	D16	I/O
0	IO_L07N_0	A16	I/O
0	IO_L07P_0	A17	I/O
0	IO_L09N_0/VREF_0	B15	VREF
0	IO_L09P_0	C15	I/O
0	IO_L10N_0	G15	I/O
0	IO_L10P_0	F15	I/O
0	IO_L11N_0	D14	I/O
0	IO_L11P_0	E14	I/O
0	IO_L12N_0/VREF_0	A14	VREF
0	IO_L12P_0	A15	I/O
0	IO_L13N_0	H14	I/O
0	IO_L13P_0	G14	I/O
0	IO_L15N_0	G13	I/O
0	IO_L15P_0	F13	I/O
0	IO_L16N_0	J13	I/O
0	IO_L16P_0	H13	I/O
0	IO_L18N_0/GCLK5	E12	GCLK
0	IO_L18P_0/GCLK4	F12	GCLK
0	IO_L19N_0/GCLK7	C12	GCLK
0	IO_L19P_0/GCLK6	B12	GCLK
0	IO_L21N_0/GCLK11	B11	GCLK
0	IO_L21P_0/GCLK10	C11	GCLK
0	IO_L22N_0	D11	I/O
0	IO_L22P_0	E11	I/O
0	IO_L24N_0	A9	I/O
0	IO_L24P_0	A10	I/O
0	IO_L25N_0/VREF_0	D10	VREF
0	IO_L25P_0	C10	I/O
0	IO_L27N_0	H8	I/O
0	IO_L27P_0	H9	I/O
0	IO_L28N_0	C9	I/O
0	IO_L28P_0	B9	I/O
0	IO_L29N_0	E9	I/O
0	IO_L29P_0	D9	I/O
0	IO_L30N_0	B8	I/O
0	IO_L30P_0	A8	I/O
0	IO_L32N_0/VREF_0	F7	VREF
0	IO_L32P_0	F8	I/O
0	IO_L33N_0	A6	I/O
0	IO_L33P_0	A7	I/O
0	IO_L35N_0	A4	I/O
0	IO_L35P_0	A5	I/O
0	IO_L36N_0	E7	I/O
0	IO_L36P_0	D7	I/O
0	IO_L38N_0/VREF_0	D6	VREF
0	IO_L38P_0	D5	I/O
0	IO_L39N_0	B4	I/O
0	IO_L39P_0	B3	I/O
0	IO_L40N_0/HSWAP	D4	DUAL
0	IO_L40P_0	C4	I/O
0	IP	B19	INPUT