AMD Xilinx - XC3S250E-4FTG256I Datasheet

Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	612
Number of Logic Elements/Cells	5508
Total RAM Bits	221184
Number of I/O	172
Number of Gates	250000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s250e-4ftg256i

Design Documentation Available

The functionality of the Spartan®-3E FPGA family is now described and updated in the following documents. The topics covered in each guide are listed below.

- UG331: *Spartan-3 Generation FPGA User Guide*
  - Clocking Resources
  - Digital Clock Managers (DCMs)
  - Block RAM
  - Configurable Logic Blocks (CLBs)
    - Distributed RAM
    - SRL16 Shift Registers
    - Carry and Arithmetic Logic
  - I/O Resources
  - Embedded Multiplier Blocks
  - Programmable Interconnect
  - ISE® Design Tools
  - IP Cores
  - Embedded Processing and Control Solutions
  - Pin Types and Package Overview
  - Package Drawings
  - Powering FPGAs
  - Power Management
- UG332: *Spartan-3 Generation Configuration User Guide*
  - Configuration Overview
    - Configuration Pins and Behavior
    - Bitstream Sizes
  - Detailed Descriptions by Mode
    - Master Serial Mode using Xilinx® Platform Flash PROM
    - Master SPI Mode using Commodity SPI Serial Flash PROM
    - Master BPI Mode using Commodity Parallel NOR Flash PROM
    - Slave Parallel (SelectMAP) using a Processor
    - Slave Serial using a Processor
    - JTAG Mode
  - ISE iMPACT Programming Examples
  - MultiBoot Reconfiguration

Xilinx Alerts

Create a Xilinx user account and sign up to receive automatic e-mail notification whenever this data sheet or the associated user guides are updated.

Sign Up for Alerts on Xilinx.com
https://secure.xilinx.com/webreg/register.do?group=myprofile&languageID=1

Spartan-3E FPGA Starter Kit

For specific hardware examples, please see the Spartan-3E FPGA Starter Kit board web page, which has links to various design examples and the user guide.

- Spartan-3E FPGA Starter Kit Board page
  http://www.xilinx.com/s3estarter
- UG230: *Spartan-3E FPGA Starter Kit User Guide*

Double-Data-Rate Transmission

Double-Data-Rate (DDR) transmission describes the technique of synchronizing signals to both the rising and falling edges of the clock signal. Spartan-3E devices use register pairs in all three IOB paths to perform DDR operations.

The pair of storage elements on the IOB's Output path (OFF1 and OFF2), used as registers, combine with a special multiplexer to form a DDR D-type flip-flop (ODDR2). This primitive permits DDR transmission where output data bits are synchronized to both the rising and falling edges of a clock. DDR operation requires two clock signals (usually 50% duty cycle), one the inverted form of the other. These signals trigger the two registers in alternating fashion, as shown in Figure 7. The Digital Clock Manager (DCM) generates the two clock signals by mirroring an incoming signal, and then shifting it 180 degrees. This approach ensures minimal skew between the two signals. Alternatively, the inverter inside the IOB can be used to invert the clock signal, thus only using one clock line and both rising and falling edges of that clock line as the two clocks for the DDR flip-flops.

The storage-element pair on the Three-State path (TFF1 and TFF2) also can be combined with a local multiplexer to form a DDR primitive. This permits synchronizing the output enable to both the rising and falling edges of a clock. This DDR operation is realized in the same way as for the output path.

The storage-element pair on the input path (IFF1 and IFF2) allows an I/O to receive a DDR signal. An incoming DDR clock signal triggers one register, and the inverted clock signal triggers the other register. The registers take turns capturing bits of the incoming DDR data signal. The primitive to allow this functionality is called IDDR2.

Aside from high bandwidth data transfers, DDR outputs also can be used to reproduce, or *mirror*, a clock signal on the output. This approach is used to transmit clock and data signals together (source synchronously). A similar approach is used to reproduce a clock signal at multiple outputs. The advantage for both approaches is that skew across the outputs is minimal.

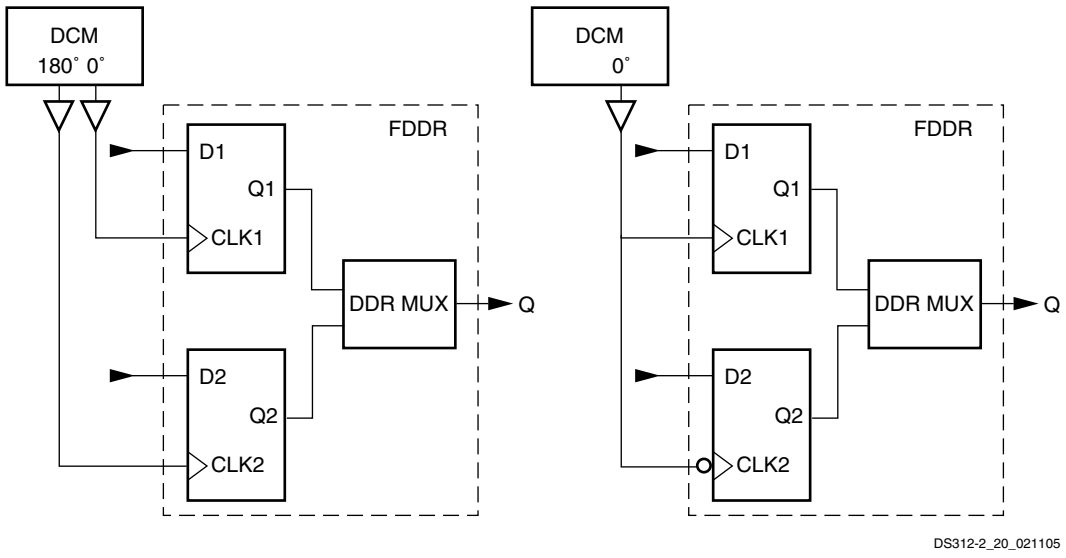

Figure 7: **Two Methods for Clocking the DDR Register**

Register Cascade Feature

In the Spartan-3E family, one of the IOBs in a differential pair can cascade its input storage elements with those in the other IOB as part of a differential pair. This is intended to make DDR operation at high speed much simpler to implement. The new DDR connections that are available are shown in Figure 5 (dashed lines), and are only available for routing between IOBs and are not accessible to the FPGA fabric. Note that this feature is only available when using the differential I/O standards LVDS, RSDS, and MINI_LVDS.

IDDR2

As a DDR input pair, the master IOB registers incoming data on the rising edge of ICLK1 (= D1) and the rising edge of ICLK2 (= D2), which is typically the same as the falling edge of ICLK1. This data is then transferred into the FPGA fabric. At some point, both signals must be brought into the same clock domain, typically ICLK1. This can be difficult at high frequencies because the available time is only one half of a clock cycle assuming a 50% duty cycle. See Figure 8 for a graphical illustration of this function.

Supply Voltages for the IOBs

The IOBs are powered by three supplies:

1. The V_{CCO} supplies, one for each of the FPGA's I/O banks, power the output drivers. The voltage on the V_{CCO} pins determines the voltage swing of the output signal.
2. V_{CCINT} is the main power supply for the FPGA's internal logic.
3. V_{CCAUX} is an auxiliary source of power, primarily to optimize the performance of various FPGA functions such as I/O switching.

I/O and Input-Only Pin Behavior During Power-On, Configuration, and User Mode

In this section, all behavior described for I/O pins also applies to input-only pins and dual-purpose I/O pins that are not actively involved in the currently-selected configuration mode.

All I/O pins have ESD clamp diodes to their respective V_{CCO} supply and from GND, as shown in Figure 5. The V_{CCINT} (1.2V), V_{CCAUX} (2.5V), and V_{CCO} supplies can be applied in any order. Before the FPGA can start its configuration process, V_{CCINT}, V_{CCO} Bank 2, and V_{CCAUX} must have reached their respective minimum recommended operating levels indicated in Table 74. At this time, all output drivers are in a high-impedance state. V_{CCO} Bank 2, V_{CCINT}, and V_{CCAUX} serve as inputs to the internal Power-On Reset circuit (POR).

A Low level applied to the HSWAP input enables pull-up resistors on user-I/O and input-only pins from power-on throughout configuration. A High level on HSWAP disables the pull-up resistors, allowing the I/Os to float. HSWAP contains an internal pull-up resistor and defaults to High if left floating. As soon as power is applied, the FPGA begins initializing its configuration memory. At the same time, the FPGA internally asserts the Global Set-Reset (GSR), which asynchronously resets all IOB storage elements to a default Low state. Also see Pin Behavior During Configuration.

Upon the completion of initialization and the beginning of configuration, INIT_B goes High, sampling the M0, M1, and M2 inputs to determine the configuration mode. Configuration data is then loaded into the FPGA. The I/O drivers remain in a high-impedance state (with or without pull-up resistors, as determined by the HSWAP input) throughout configuration.

At the end of configuration, the GSR net is released, placing the IOB registers in a Low state by default, unless the loaded design reverses the polarity of their respective SR inputs.

The Global Three State (GTS) net is released during Start-Up, marking the end of configuration and the beginning of design operation in the User mode. After the GTS net is released, all user I/Os go active while all unused I/Os are pulled down (PULLDOWN). The designer can control how the unused I/Os are terminated after GTS is released by setting the Bitstream Generator (BitGen) option UnusedPin to PULLUP, PULLDOWN, or FLOAT.

One clock cycle later (default), the Global Write Enable (GWE) net is released allowing the RAM and registers to change states. Once in User mode, any pull-up resistors enabled by HSWAP revert to the user settings and HSWAP is available as a general-purpose I/O. For more information on PULLUP and PULLDOWN, see Pull-Up and Pull-Down Resistors.

Behavior of Unused I/O Pins After Configuration

By default, the Xilinx ISE development software automatically configures all unused I/O pins as input pins with individual internal pull-down resistors to GND.

This default behavior is controlled by the ***UnusedPin*** bitstream generator (BitGen) option, as described in Table 69.

JTAG Boundary-Scan Capability

All Spartan-3E IOBs support boundary-scan testing compatible with IEEE 1149.1/1532 standards. During boundary-scan operations such as EXTEST and HIGHZ the pull-down resistor is active. See JTAG Mode for more information on programming via JTAG.

Carry and Arithmetic Logic

For additional information, refer to the “Using Carry and Arithmetic Logic” chapter in UG331.

The carry chain, together with various dedicated arithmetic logic gates, support fast and efficient implementations of math operations. The carry logic is automatically used for most arithmetic functions in a design. The gates and multiplexers of the carry and arithmetic logic can also be used for general-purpose logic, including simple wide Boolean functions.

The carry chain enters the slice as CIN and exits as COUT, controlled by several multiplexers. The carry chain connects directly from one CLB to the CLB above. The carry chain can be initialized at any point from the BX (or BY) inputs.

The dedicated arithmetic logic includes the exclusive-OR gates XORF and XORG (upper and lower portions of the slice, respectively) as well as the AND gates GAND and FAND (upper and lower portions, respectively). These gates work in conjunction with the LUTs to implement efficient arithmetic functions, including counters and multipliers, typically at two bits per slice. See Figure 22 and Table 14.

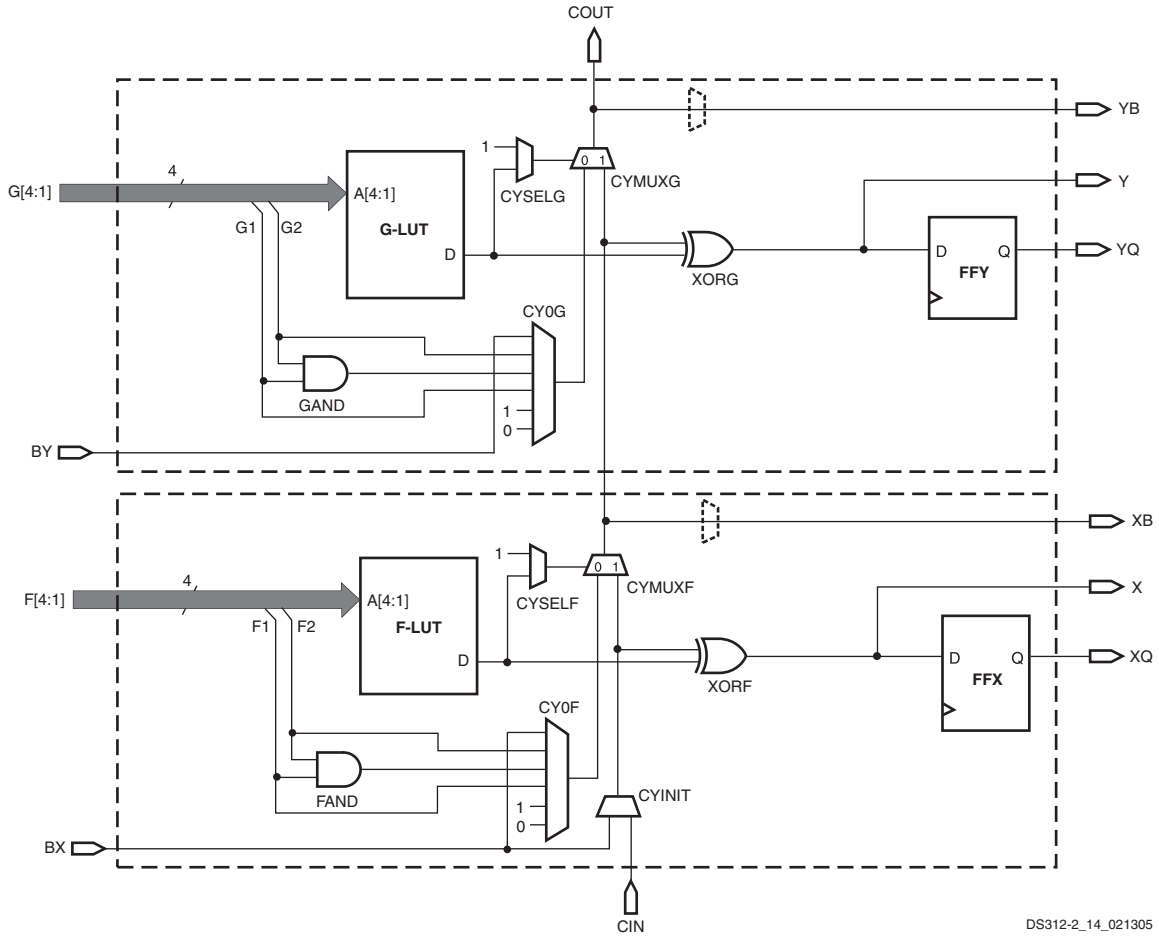

Figure 22: **Carry Logic**

Table 14: **Carry Logic Functions**

Function	Description
CYINIT	Initializes carry chain for a slice. Fixed selection of: · CIN carry input from the slice below · BX input
CY0F	Carry generation for bottom half of slice. Fixed selection of: · F1 or F2 inputs to the LUT (both equal 1 when a carry is to be generated) · FAND gate for multiplication · BX input for carry initialization · Fixed 1 or 0 input for use as a simple Boolean function

Status Logic

The Status Logic indicates the present state of the DCM and a means to reset the DCM to its initial known state. The Status Logic signals are described in Table 37.

In general, the Reset (RST) input is only asserted upon configuring the FPGA or when changing the CLKIN frequency. The RST signal must be asserted for three or more CLKIN cycles. A DCM reset does not affect attribute values (for example, CLKFX_MULTIPLY and CLKFX_DIVIDE). If not used, RST is tied to GND.

The eight bits of the STATUS bus are described in Table 38.

Table 37: **Status Logic Signals**

Signal	Direction	Description
RST	Input	A High resets the entire DCM to its initial power-on state. Initializes the DLL taps for a delay of zero. Sets the LOCKED output Low. This input is asynchronous.
STATUS[7:0]	Output	The bit values on the STATUS bus provide information regarding the state of DLL and PS operation
LOCKED	Output	Indicates that the CLKIN and CLKFB signals are in phase by going High. The two signals are out-of-phase when Low.

Table 38: **DCM Status Bus**

Bit	Name	Description
0	Reserved	-
1	CLKIN Stopped	When High, indicates that the CLKIN input signal is not toggling. When Low, indicates CLKIN is toggling. This bit functions only when the CLKFB input is connected.(1)
2	CLKFX Stopped	When High, indicates that the CLKFX output is not toggling. When Low, indicates the CLKFX output is toggling. This bit functions only when the CLKFX or CLKFX180 output are connected.
3-6	Reserved	-

Notes:

1. When only the DFS clock outputs but none of the DLL clock outputs are used, this bit does not go High when the CLKIN signal stops.

Stabilizing DCM Clocks Before User Mode

The STARTUP_WAIT attribute shown in Table 39 optionally delays the end of the FPGA's configuration process until after the DCM locks to its incoming clock frequency. This option ensures that the FPGA remains in the Startup phase of configuration until all clock outputs generated by the DCM are stable. When all DCMs that have their STARTUP_WAIT attribute set to TRUE assert the LOCKED signal, then the FPGA completes its configuration process and proceeds to user mode. The associated bitstream generator (BitGen) option ***LCK_cycle*** specifies one of the six cycles in the Startup phase. The selected cycle defines the point at which configuration stalls until all the LOCKED outputs go High. See Start-Up, page 105 for more information.

Table 39: **STARTUP_WAIT Attribute**

Attribute	Description	Values
STARTUP_WAIT	When TRUE, delays transition from configuration to user mode until DCM locks to the input clock.	TRUE, ***FALSE***

Spread Spectrum

DCMs accept typical spread spectrum clocks as long as they meet the input requirements. The DLL will track the frequency changes created by the spread spectrum clock to drive the global clocks to the FPGA logic. See XAPP469, *Spread-Spectrum Clocking Reception for Displays* for details.

(W) Table 54 shows the connections between the SPI Flash PROM and the FPGA's SPI configuration interface. Each SPI Flash PROM vendor uses slightly different signal naming. The SPI Flash PROM's write protect and hold controls are not used by the FPGA during configuration. However, the $\overline{\text{HOLD}}$ pin must be High during the configuration process. The PROM's write protect input must be High in order to write or program the Flash memory.

Table 54: **Example SPI Flash PROM Connections and Pin Naming**

SPI Flash Pin	FPGA Connection	STMicro	NexFlash	Silicon Storage Technology	Atmel DataFlash
DATA_IN	MOSI	D	DI	SI	SI
DATA_OUT	DIN	Q	DO	SO	SO
$\overline{\text{SELECT}}$	CSO_B	$\overline{\text{S}}$	$\overline{\text{CS}}$	CE#	$\overline{\text{CS}}$
CLOCK	CCLK	C	CLK	SCK	SCK
$\overline{\text{WR\_PROTECT}}$ (W)	Not required for FPGA configuration. Must be High to program SPI Flash. Optional connection to FPGA user I/O after configuration.	$\overline{\text{W}}$	$\overline{\text{WP}}$	WP#	$\overline{\text{WP}}$
$\overline{\text{HOLD}}$ (see Figure 53)	Not required for FPGA configuration but must be High during configuration. Optional connection to FPGA user I/O after configuration. Not applicable to Atmel DataFlash.	$\overline{\text{HOLD}}$	$\overline{\text{HOLD}}$	HOLD#	N/A
$\overline{\text{RESET}}$ (see Figure 54)	Only applicable to Atmel DataFlash. Not required for FPGA configuration but must be High during configuration. Optional connection to FPGA user I/O after configuration. Do not connect to FPGA's PROG_B as this will prevent direct programming of the DataFlash.	N/A	N/A	N/A	$\overline{\text{RESET}}$
RDY/$\overline{\text{BUSY}}$ (see Figure 54)	Only applicable to Atmel DataFlash and only available on certain packages. Not required for FPGA configuration. Output from DataFlash PROM. Optional connection to FPGA user I/O after configuration.	N/A	N/A	N/A	RDY/$\overline{\text{BUSY}}$

The mode select pins, M[2:0], and the variant select pins, VS[2:0] are sampled when the FPGA's INIT_B output goes High and must be at defined logic levels during this time. After configuration, when the FPGA's DONE output goes High, these pins are all available as full-featured user-I/O pins.

(P) Similarly, the FPGA's HSWAP pin must be Low to enable pull-up resistors on all user-I/O pins or High to disable the pull-up resistors. The HSWAP control must remain at a constant logic level throughout FPGA configuration. After configuration, when the FPGA's DONE output goes High, the HSWAP pin is available as full-featured user-I/O pin and is powered by the VCCO_0 supply.

In a single-FPGA application, the FPGA's DOUT pin is not used but is actively driving during the configuration process.

Table 55: **Serial Peripheral Interface (SPI) Connections**

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
HSWAP (P)	Input	**User I/O Pull-Up Control**. When Low during configuration, enables pull-up resistors in all I/O pins to respective I/O bank V_{CCO} input. 0: Pull-ups during configuration 1: No pull-ups	Drive at valid logic level throughout configuration.	User I/O
M[2:0]	Input	**Mode Select**. Selects the FPGA configuration mode. See Design Considerations for the HSWAP, M[2:0], and VS[2:0] Pins.	M2 = 0, M1 = 0, M0 = 1. Sampled when INIT_B goes High.	User I/O

Table 59: **Byte-Wide Peripheral Interface (BPI) Connections *(Cont'd)***

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
HDC	Output	PROM Write Enable	Connect to PROM write-enable input (WE#). FPGA drives this signal High throughout configuration.	User I/O
LDC2 (D)	Output	PROM Byte Mode	This signal is not used for x8 PROMs. For PROMs with a x8/x16 data width control, connect to PROM byte-mode input (BYTE#). See Precautions Using x8/x16 Flash PROMs. FPGA drives this signal Low throughout configuration.	User I/O. Drive this pin High after configuration to use a x8/x16 PROM in x16 mode.
A[23:0]	Output	Address	Connect to PROM address inputs. High-order address lines may not be available in all packages and not all may be required. Number of address lines required depends on the size of the attached Flash PROM. FPGA address generation controlled by M0 mode pin. Addresses presented on falling CCLK edge. Only 20 address lines are available in TQ144 package.	User I/O
D[7:0]	Input	Data Input	FPGA receives byte-wide data on these pins in response the address presented on A[23:0]. Data captured by FPGA on rising edge of CCLK.	User I/O. If bitstream option ***Persist=Yes***, becomes part of SelectMap parallel peripheral interface.
CSO_B	Output	**Chip Select Output**. Active Low.	Not used in single FPGA applications. In a daisy-chain configuration, this pin connects to the CSI_B pin of the next FPGA in the chain. If HSWAP = 1 in a multi-FPGA daisy-chain application, connect this signal to a 4.7 kΩ pull-up resistor to VCCO_2. Actively drives Low when selecting a downstream device in the chain.	User I/O
BUSY	Output	**Busy Indicator**. Typically only used after configuration, if bitstream option ***Persist=Yes***.	Not used during configuration but actively drives.	User I/O. If bitstream option ***Persist=Yes***, becomes part of SelectMap parallel peripheral interface.
CCLK	Output	**Configuration Clock**. Generated by FPGA internal oscillator. Frequency controlled by ***ConfigRate*** bitstream generator option. If CCLK PCB trace is long or has multiple connections, terminate this output to maintain signal integrity. See CCLK Design Considerations.	Not used in single FPGA applications but actively drives. In a daisy-chain configuration, drives the CCLK inputs of all other FPGAs in the daisy-chain.	User I/O. If bitstream option ***Persist=Yes***, becomes part of SelectMap parallel peripheral interface.
INIT_B	Open-drain bidirectional I/O	**Initialization Indicator**. Active Low. Goes Low at start of configuration during the Initialization memory clearing process. Released at the end of memory clearing, when the mode select pins are sampled. In daisy-chain applications, this signal requires an external 4.7 kΩ pull-up resistor to VCCO_2.	Active during configuration. If CRC error detected during configuration, FPGA drives INIT_B Low.	User I/O. If unused in the application, drive INIT_B High.

Compatible Flash Families

The Spartan-3E BPI configuration interface operates with a wide variety of x8 or x8/x16 parallel NOR Flash devices. Table 61 provides a few Flash memory families that operate with the Spartan-3E BPI interface. Consult the data sheet for the desired parallel NOR Flash to determine its suitability The basic timing requirements and waveforms are provided in Byte Peripheral Interface (BPI) Configuration Timing (Module 3).

Table 61: **Compatible Parallel NOR Flash Families**

Flash Vendor	Flash Memory Family
Numonyx	M29W, J3D StrataFlash
Atmel	AT29 / AT49
Spansion	S29
Macronix	MX29

CCLK Frequency

In BPI mode, the FPGA's internal oscillator generates the configuration clock frequency that controls all the interface timing. The FPGA starts configuration at its lowest frequency and increases its frequency for the remainder of the configuration process if so specified in the configuration bitstream. The maximum frequency is specified using the ***ConfigRate*** bitstream generator option.

Table 62: **Maximum ConfigRate Settings for Parallel Flash PROMs (Commercial Temperature Range)**

Flash Read Access Time	Maximum *ConfigRate* Setting
250 ns	3
115 ns	6
45 ns	12

Table 62 shows the maximum ***ConfigRate*** settings for various typical PROM read access times over the Commercial temperature operating range. See Byte Peripheral Interface (BPI) Configuration Timing (Module 3) and UG332 for more detailed information. Despite using slower ***ConfigRate*** settings, BPI mode is equally fast as the other configuration modes. In BPI mode, data is accessed at the ***ConfigRate*** frequency and internally serialized with an 8X clock frequency.

Using the BPI Interface after Configuration

After the FPGA successfully completes configuration, all pins connected to the parallel Flash PROM are available as user I/Os.

If not using the parallel Flash PROM after configuration, drive LDC0 High to disable the PROM's chip-select input. The remainder of the BPI pins then become available to the FPGA application, including all 24 address lines, the eight data lines, and the LDC2, LDC1, and HDC control pins.

Because all the interface pins are user I/Os after configuration, the FPGA application can continue to use the interface pins to communicate with the parallel Flash PROM. Parallel Flash PROMs are available in densities ranging from 1 Mbit up to 128 Mbits and beyond. However, a single Spartan-3E FPGA requires less than 6 Mbits for configuration. If desired, use a larger parallel Flash PROM to contain additional non-volatile application data, such as MicroBlaze processor code, or other user data, such as serial numbers and Ethernet MAC IDs. In such an example, the FPGA configures from parallel Flash PROM. Then using FPGA logic after configuration, a MicroBlaze processor embedded within the FPGA can either execute code directly from parallel Flash PROM or copy the code to external DDR SDRAM and execute from DDR SDRAM. Similarly, the FPGA application can store non-volatile application data within the parallel Flash PROM.

The FPGA configuration data is stored starting at either at location 0 or the top of memory (addresses all ones) or at both locations for MultiBoot mode. Store any additional data beginning in other available parallel Flash PROM sectors. Do not mix configuration data and user data in the same sector.

Similarly, the parallel Flash PROM interface can be expanded to additional parallel peripherals.

The address, data, and LDC1 (OE#) and HDC (WE#) control signals are common to all parallel peripherals. Connect the chip-select input on each additional peripheral to one of the FPGA user I/O pins. If HSWAP = 0 during configuration, the FPGA holds the chip-select line High via an internal pull-up resistor. If HSWAP = 1, connect the select line to +3.3V via an external 4.7 kΩ pull-up resistor to avoid spurious read or write operations. After configuration, drive the select line Low to select the desired peripheral. Refer to the individual peripheral data sheet for specific interface and communication protocol requirements.

The FPGA optionally supports a 16-bit peripheral interface by driving the LDC2 (BYTE#) control pin High after configuration. See Precautions Using x8/x16 Flash PROMs for additional information.

The FPGA provides up to 24 address lines during configuration, addressing up to 128 Mbits (16 Mbytes). If using a larger parallel PROM, connect the upper address lines to FPGA user I/O. During configuration, the upper address lines will be pulled High if HSWAP = 0. Otherwise, use external pull-up or pull-down resistors on these address lines to define their values during configuration.

Precautions Using x8/x16 Flash PROMs

(D) Most low- to mid-density PROMs are byte-wide (x8) only. Many higher-density Flash PROMs support both byte-wide (x8) and halfword-wide (x16) data paths and include a mode input called BYTE# that switches between x8 or x16. During configuration, Spartan-3E FPGAs only

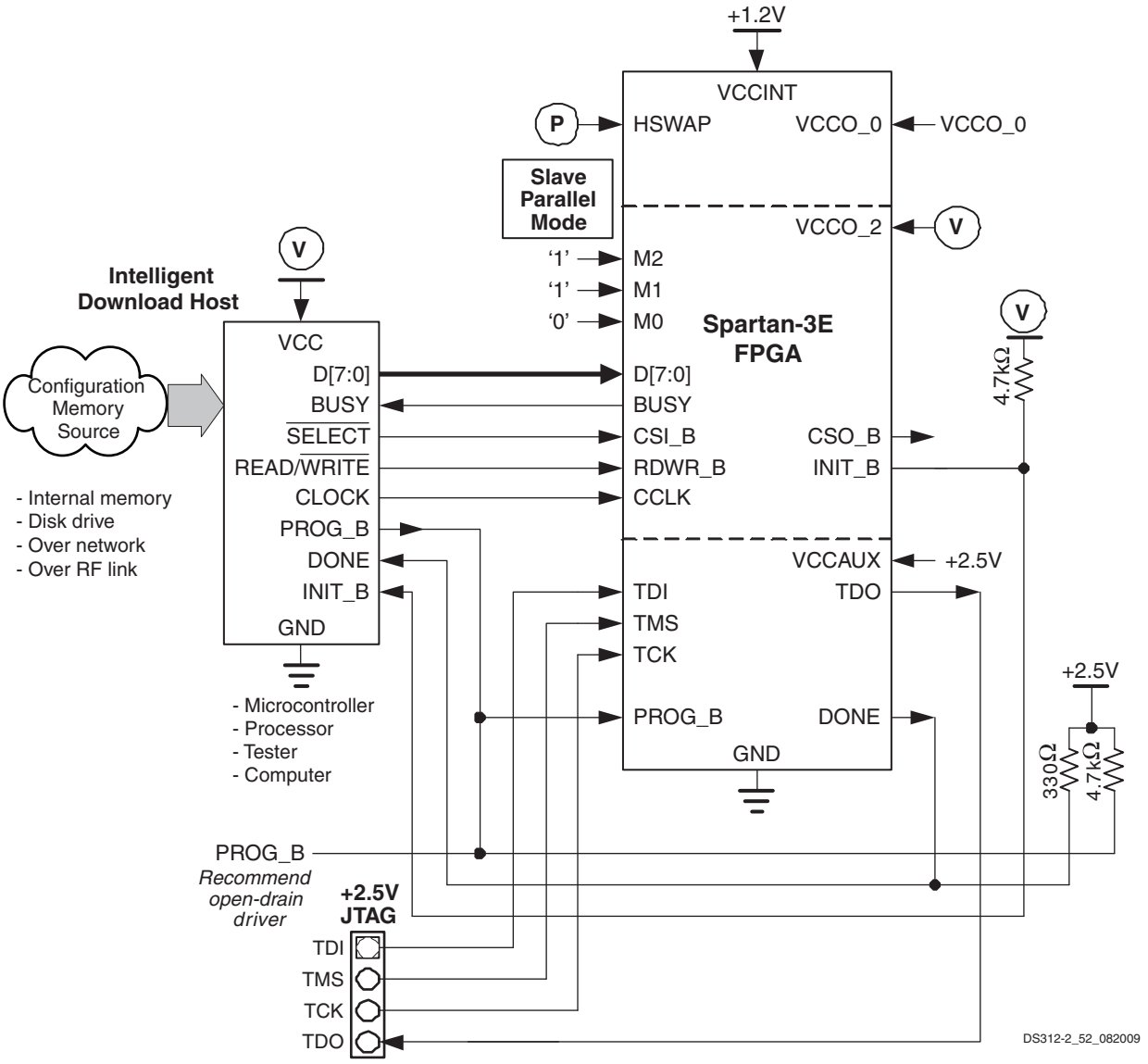

Figure 61: **Slave Parallel Configuration Mode**

Slave Parallel Mode

For additional information, refer to the "Slave Parallel (SelectMAP) Mode" chapter in UG332.

In Slave Parallel mode (M[2:0] = <1:1:0>), an external host, such as a microprocessor or microcontroller, writes byte-wide configuration data into the FPGA, using a typical peripheral interface as shown in Figure 61.

The external download host starts the configuration process by pulsing PROG_B and monitoring that the INIT_B pin goes High, indicating that the FPGA is ready to receive its first data. The host asserts the active-Low chip-select signal (CSI_B) and the active-Low Write signal (RDWR_B). The host then continues supplying data and clock signals until either the FPGA's DONE pin goes High, indicating a successful configuration, or until the FPGA's INIT_B pin goes Low, indicating a configuration error.

The FPGA captures data on the rising CCLK edge. If the CCLK frequency exceeds 50 MHz, then the host must also monitor the FPGA's BUSY output. If the FPGA asserts BUSY High, the host must hold the data for an additional clock cycle, until BUSY returns Low. If the CCLK frequency is 50 MHz or below, the BUSY pin may be ignored but actively drives during configuration.

The configuration process requires more clock cycles than indicated from the configuration file size. Additional clocks are required during the FPGA's start-up sequence, especially if the FPGA is programmed to wait for selected Digital Clock Managers (DCMs) to lock to their respective clock inputs (see Start-Up, page 105).

If the Slave Parallel interface is only used to configure the FPGA, never to read data back, then the RDWR_B signal

Switching Characteristics

All Spartan-3E FPGAs ship in two speed grades: -4 and the higher performance -5. Switching characteristics in this document may be designated as Advance, Preliminary, or Production, as shown in Table 84. Each category is defined as follows:

Advance: These specifications are based on simulations only and are typically available soon after establishing FPGA specifications. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These specifications are based on complete early silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting preliminary delays is greatly reduced compared to Advance data.

Production: These specifications are approved once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Software Version Requirements

Production-quality systems must use FPGA designs compiled using a speed file designated as PRODUCTION status. FPGAs designs using a less mature speed file designation should only be used during system prototyping or pre-production qualification. FPGA designs with speed files designated as Advance or Preliminary should not be used in a production-quality system.

Whenever a speed file designation changes, as a device matures toward Production status, rerun the latest Xilinx ISE software on the FPGA design to ensure that the FPGA design incorporates the latest timing information and software updates.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all Spartan-3E devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.**

Create a Xilinx user account and sign up to receive automatic e-mail notification whenever this data sheet or the associated user guides are updated.

Sign Up for Alerts on Xilinx.com
https://secure.xilinx.com/webreg/register.do?group=myprofile&languageID=1

Timing parameters and their representative values are selected for inclusion below either because they are important as general design requirements or they indicate fundamental device performance characteristics. The Spartan-3E speed files (v1.27), part of the Xilinx Development Software, are the original source for many but not all of the values. The speed grade designations for these files are shown in Table 84. For more complete, more precise, and worst-case data, use the values reported by the Xilinx static timing analyzer (TRACE in the Xilinx development software) and back-annotated to the simulation netlist.

Table 84: **Spartan-3E v1.27 Speed Grade Designations**

Device	Advance	Preliminary	Production
XC3S100E			-MIN, -4, -5
XC3S250E			-MIN, -4, -5
XC3S500E			-MIN, -4, -5
XC3S1200E			-MIN, -4, -5
XC3S1600E			-MIN, -4, -5

Table 85 provides the history of the Spartan-3E speed files since all devices reached Production status.

Table 85: **Spartan-3E Speed File Version History**

Version	ISE Release	Description
1.27	9.2.03i	Added XA Automotive.
1.26	8.2.02i	Added -0/-MIN speed grade, which includes minimum values.
1.25	8.2.01i	Added XA Automotive devices to speed file. Improved model for left and right DCMs.
1.23	8.2i	Updated input setup/hold values based on default IFD_DELAY_VALUE settings.
1.21	8.1.03i	All Spartan-3E FPGAs and all speed grades elevated to Production status.

I/O Timing

Table 86: **Pin-to-Pin Clock-to-Output Times for the IOB Output Path**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max[2]	Max[2]	
Clock-to-Output Times						
$T_{ICKOFDCM}$	When reading from the Output Flip-Flop (OFF), the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is used.	LVCMOS25[3], 12 mA output drive, Fast slew rate, with DCM[4]	XC3S100E	2.66	2.79	ns
			XC3S250E	3.00	3.45	ns
			XC3S500E	3.01	3.46	ns
			XC3S1200E	3.01	3.46	ns
			XC3S1600E	3.00	3.45	ns
T_{ICKOF}	When reading from OFF, the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is not used.	LVCMOS25[3], 12 mA output drive, Fast slew rate, without DCM	XC3S100E	5.60	5.92	ns
			XC3S250E	4.91	5.43	ns
			XC3S500E	4.98	5.51	ns
			XC3S1200E	5.36	5.94	ns
			XC3S1600E	5.45	6.05	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 95 and are based on the operating conditions set forth in Table 77 and Table 80.
2. For minimums, use the values reported by the Xilinx timing analyzer.
3. This clock-to-output time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or a standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. If the former is true, *add* the appropriate Input adjustment from Table 91. If the latter is true, *add* the appropriate Output adjustment from Table 94.
4. DCM output jitter is included in all measurements.

Table 95: **Test Methods for Timing Measurement at I/Os *(Cont'd)***

Signal Standard (IOSTANDARD)	Inputs			Outputs		Inputs and Outputs
	V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
DIFF_HSTL_I_18	-	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{ICM}
DIFF_HSTL_III_18	-	V_{REF} – 0.5	V_{REF} + 0.5	50	1.8	V_{ICM}
DIFF_SSTL18_I	-	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{ICM}
DIFF_SSTL2_I	-	V_{REF} – 0.5	V_{REF} + 0.5	50	1.25	V_{ICM}

Notes:

1. Descriptions of the relevant symbols are as follows:
   V_{REF} – The reference voltage for setting the input switching threshold
   V_{ICM} – The common mode input voltage
   V_M – Voltage of measurement point on signal transition
   V_L – Low-level test voltage at Input pin
   V_H – High-level test voltage at Input pin
   R_T – Effective termination resistance, which takes on a value of 1MΩ when no parallel termination is required
   V_T – Termination voltage
2. The load capacitance (C_L) at the Output pin is 0 pF for all signal standards.
3. According to the PCI specification.

The capacitive load (C_L) is connected between the output and GND. *The Output timing for all standards, as published in the speed files and the data sheet, is always based on a C_L value of zero.* High-impedance probes (less than 1 pF) are used for all measurements. Any delay that the test fixture might contribute to test measurements is subtracted from those measurements to produce the final timing numbers as published in the speed files and data sheet.

Using IBIS Models to Simulate Load Conditions in Application

IBIS models permit the most accurate prediction of timing delays for a given application. The parameters found in the IBIS model (V_{REF}, R_{REF}, and V_{MEAS}) correspond directly with the parameters used in Table 95 (V_T, R_T, and V_M). Do not confuse V_{REF} (the termination voltage) from the IBIS model with V_{REF} (the input-switching threshold) from the table. A fourth parameter, C_{REF}, is always zero. The four parameters describe all relevant output test conditions. IBIS models are found in the Xilinx development software as well as at the following link:

http://www.xilinx.com/support/download/index.htm

Delays for a given application are simulated according to its specific load conditions as follows:

1. Simulate the desired signal standard with the output driver connected to the test setup shown in Figure 72. Use parameter values V_T, R_T, and V_M from Table 95. C_{REF} is zero.
2. Record the time to V_M.
3. Simulate the same signal standard with the output driver connected to the PCB trace with load. Use the appropriate IBIS model (including V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} values) or capacitive value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. Add (or subtract) the increase (or decrease) in delay to (or from) the appropriate Output standard adjustment (Table 94) to yield the worst-case delay of the PCB trace.

18 x 18 Embedded Multiplier Timing

Table 102: **18 x 18 Embedded Multiplier Timing**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Combinatorial Delay						
T_{MULT}	Combinatorial multiplier propagation delay from the A and B inputs to the P outputs, assuming 18-bit inputs and a 36-bit product (AREG, BREG, and PREG registers unused)	-	4.34(1)	-	4.88(1)	ns
Clock-to-Output Times						
T_{MSCKP_P}	Clock-to-output delay from the active transition of the CLK input to valid data appearing on the P outputs when using the PREG register(2)	-	0.98	-	1.10	ns
T_{MSCKP_A} T_{MSCKP_B}	Clock-to-output delay from the active transition of the CLK input to valid data appearing on the P outputs when using either the AREG or BREG register(3)	-	4.42	-	4.97	ns
Setup Times						
T_{MSDCK_P}	Data setup time at the A or B input before the active transition at the CLK when using only the PREG output register (AREG, BREG registers unused)(2)	3.54	-	3.98	-	ns
T_{MSDCK_A}	Data setup time at the A input before the active transition at the CLK when using the AREG input register(3)	0.20	-	0.23	-	ns
T_{MSDCK_B}	Data setup time at the B input before the active transition at the CLK when using the BREG input register(3)	0.35	-	0.39	-	ns
Hold Times						
T_{MSCKD_P}	Data hold time at the A or B input after the active transition at the CLK when using only the PREG output register (AREG, BREG registers unused)(2)	–0.97	-	–0.97	-	ns
T_{MSCKD_A}	Data hold time at the A input after the active transition at the CLK when using the AREG input register(3)	0.03	-	0.04	-	ns
T_{MSCKD_B}	Data hold time at the B input after the active transition at the CLK when using the BREG input register(3)	0.04	-	0.05	-	ns
Clock Frequency						
F_{MULT}	Internal operating frequency for a two-stage 18x18 multiplier using the AREG and BREG input registers and the PREG output register(1)	0	270	0	240	MHz

Notes:

1. Combinatorial delay is less and pipelined performance is higher when multiplying input data with less than 18 bits.
2. The PREG register is typically used in both single-stage and two-stage pipelined multiplier implementations.
3. Input registers AREG or BREG are typically used when inferring a two-stage multiplier.

Configuration Clock (CCLK) Characteristics

Table 112: **Master Mode CCLK Output Period by *ConfigRate* Option Setting**

Symbol	Description	*ConfigRate* Setting	Temperature Range	Minimum	Maximum	Units
T_{CCLK1}	CCLK clock period by ***ConfigRate*** setting	1 *(power-on value and default value)*	Commercial	570	1,250	ns
			Industrial	485		ns
T_{CCLK3}		3	Commercial	285	625	ns
			Industrial	242		ns
T_{CCLK6}		6	Commercial	142	313	ns
			Industrial	121		ns
T_{CCLK12}		12	Commercial	71.2	157	ns
			Industrial	60.6		ns
T_{CCLK25}		25	Commercial	35.5	78.2	ns
			Industrial	30.3		ns
T_{CCLK50}		50	Commercial	17.8	39.1	ns
			Industrial	15.1		ns

Notes:

1. Set the ***ConfigRate*** option value when generating a configuration bitstream. See Bitstream Generator (BitGen) Options in Module 2.

Table 113: **Master Mode CCLK Output Frequency by *ConfigRate* Option Setting**

Symbol	Description	*ConfigRate* Setting	Temperature Range	Minimum	Maximum	Units
F_{CCLK1}	Equivalent CCLK clock frequency by ***ConfigRate*** setting	1 *(power-on value and default value)*	Commercial	0.8	1.8	MHz
			Industrial		2.1	MHz
F_{CCLK3}		3	Commercial	1.6	3.6	MHz
			Industrial		4.2	MHz
F_{CCLK6}		6	Commercial	3.2	7.1	MHz
			Industrial		8.3	MHz
F_{CCLK12}		12	Commercial	6.4	14.1	MHz
			Industrial		16.5	MHz
F_{CCLK25}		25	Commercial	12.8	28.1	MHz
			Industrial		33.0	MHz
F_{CCLK50}		50	Commercial	25.6	56.2	MHz
			Industrial		66.0	MHz

Table 114: **Master Mode CCLK Output Minimum Low and High Time**

Symbol	Description		*ConfigRate* Setting						Units
			1	3	6	12	25	50	
T_{MCCL}, T_{MCCH}	Master mode CCLK minimum Low and High time	Commercial	276	138	69	34.5	17.1	8.5	ns
		Industrial	235	117	58	29.3	14.5	7.3	ns

Table 115: **Slave Mode CCLK Input Low and High Time**

Symbol	Description	Min	Max	Units
T_{SCCL}, T_{SCCH}	CCLK Low and High time	5	∞	ns

Master Serial and Slave Serial Mode Timing

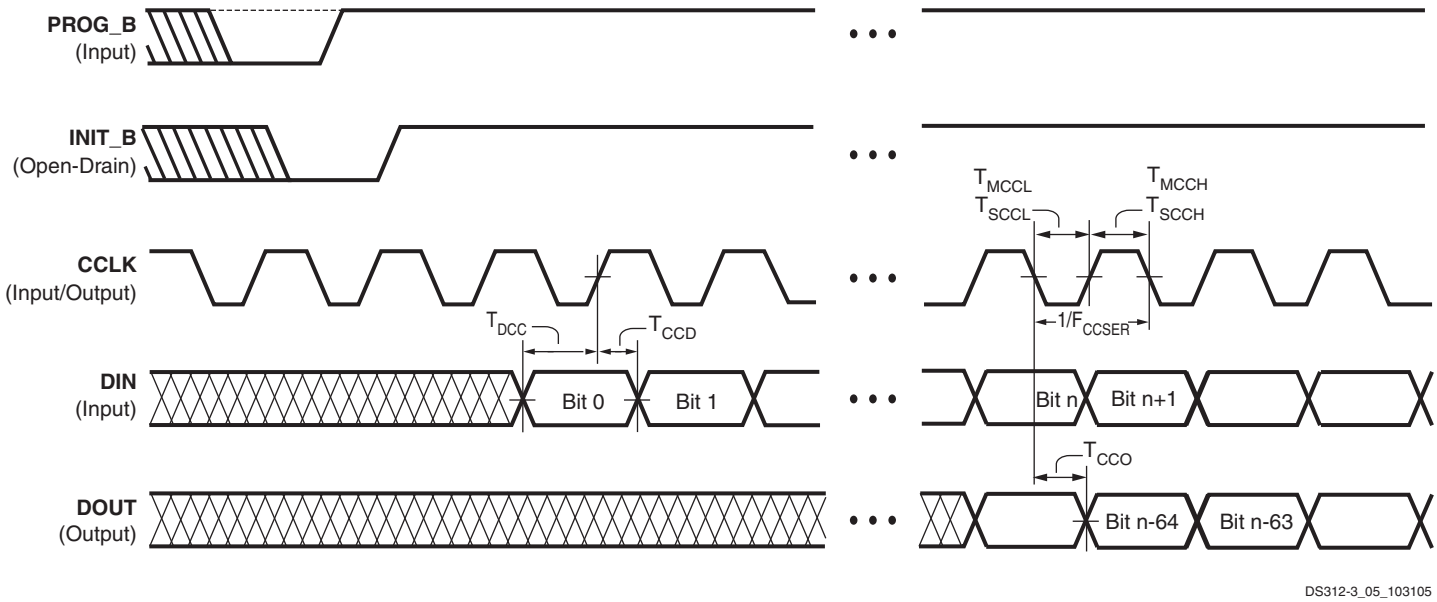

Figure 74: **Waveforms for Master Serial and Slave Serial Configuration**

Table 116: **Timing for the Master Serial and Slave Serial Configuration Modes**

Symbol	Description		Slave/ Master	All Speed Grades		Units
				Min	Max	
Clock-to-Output Times						
T_{CCO}	The time from the falling transition on the CCLK pin to data appearing at the DOUT pin		Both	1.5	10.0	ns
Setup Times						
T_{DCC}	The time from the setup of data at the DIN pin to the active edge of the CCLK pin		Both	11.0	-	ns
Hold Times						
T_{CCD}	The time from the active edge of the CCLK pin to the point when data is last held at the DIN pin		Both	0	-	ns
Clock Timing						
T_{CCH}	High pulse width at the CCLK input pin		Master	See Table 114		
			Slave	See Table 115		
T_{CCL}	Low pulse width at the CCLK input pin		Master	See Table 114		
			Slave	See Table 115		
F_{CCSER}	Frequency of the clock signal at the CCLK input pin	No bitstream compression	Slave	0	66(2)	MHz
		With bitstream compression		0	20	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 77.
2. For serial configuration with a daisy-chain of multiple FPGAs, the maximum limit is 25 MHz.

Table 117: **Timing for the Slave Parallel Configuration Mode *(Cont'd)***

Symbol	Description			All Speed Grades		Units
				Min	Max	
Clock Timing						
T_{CCH}	The High pulse width at the CCLK input pin			5	-	ns
T_{CCL}	The Low pulse width at the CCLK input pin			5	-	ns
F_{CCPAR}	Frequency of the clock signal at the CCLK input pin	No bitstream compression	Not using the BUSY pin(2)	0	50	MHz
			Using the BUSY pin	0	66	MHz
		With bitstream compression		0	20	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 77.
2. In the Slave Parallel mode, it is necessary to use the BUSY pin when the CCLK frequency exceeds this maximum specification.
3. Some Xilinx documents refer to Parallel modes as "SelectMAP" modes.

User I/Os by Bank

Table 134 shows how the 83 available user-I/O pins are distributed on the XC3S100E FPGA packaged in the CP132 package. Table 135 indicates how the 92 available user-I/O pins are distributed on the XC3S250E and the XC3S500E FPGAs in the CP132 package.

Table 134: **User I/Os Per Bank for the XC3S100E in the CP132 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF(1)	CLK(2)
Top	0	18	6	2	1	1	8
Right	1	23	0	0	21	2	0(2)
Bottom	2	22	0	0	20	2	0(2)
Left	3	20	10	0	0	2	8
TOTAL		**83**	**16**	**2**	**42**	**7**	**16**

Notes:

1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

Table 135: **User I/Os Per Bank for the XC3S250E and XC3S500E in the CP132 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF(1)	CLK(2)
Top	0	22	11	0	1	2	8
Right	1	23	0	0	21	2	0(2)
Bottom	2	26	0	0	24	2	0(2)
Left	3	21	11	0	0	2	8
TOTAL		**92**	**22**	**0**	**46**	**8**	**16**

Notes:

1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

TQ144 Footprint

Note pin 1 indicator in top-left corner and logo orientation.
Double arrows (↔) indicates a pinout migration difference between the XC3S100E and XC3S250E.

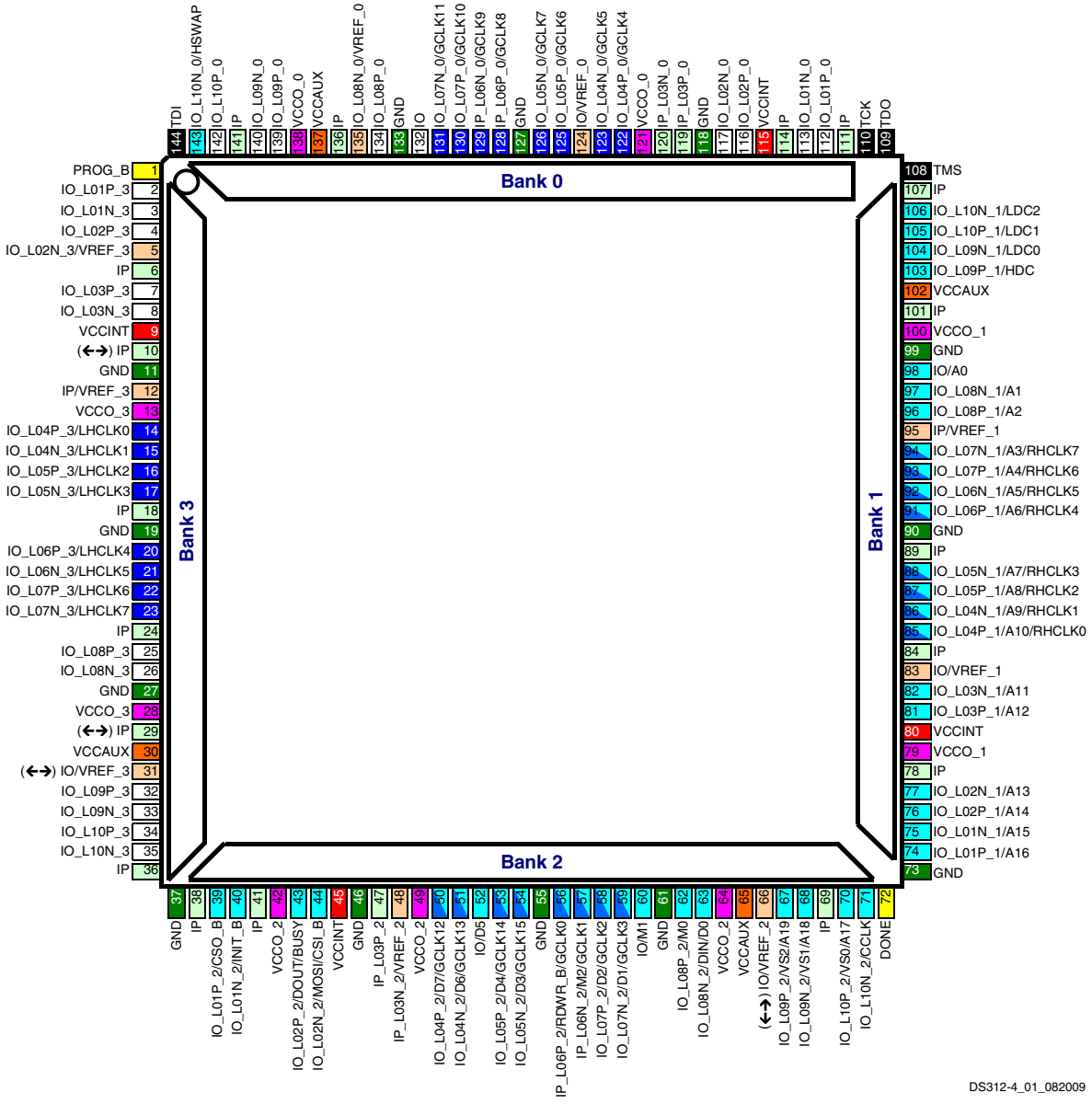

Figure 82: **TQ144 Package Footprint (top view)**

20	**I/O:** Unrestricted, general-purpose user I/O	42	**DUAL:** Configuration pin, then possible user I/O	9	**VREF:** User I/O or input voltage reference for bank
21	**INPUT:** Unrestricted, general-purpose input pin	16	**CLK:** User I/O, input, or global buffer input	9	**VCCO:** Output voltage supply for bank
2	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	4	**VCCINT:** Internal core supply voltage (+1.2V)
0	**N.C.:** Not connected	13	**GND:** Ground	4	**VCCAUX:** Auxiliary supply voltage (+2.5V)

User I/Os by Bank

Table 142 indicates how the 158 available user-I/O pins are distributed between the four I/O banks on the PQ208 package.

Footprint Migration Differences

The XC3S250E and XC3S500E FPGAs have identical footprints in the PQ208 package. Designs can migrate between the XC3S250E and XC3S500E without further consideration.

Table 142: **User I/Os Per Bank for the XC3S250E and XC3S500E in the PQ208 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF(1)	CLK(2)
Top	0	38	18	6	1	5	8
Right	1	40	9	7	21	3	0(2)
Bottom	2	40	8	6	24	2	0(2)
Left	3	40	23	6	0	3	8
TOTAL		**158**	**58**	**25**	**46**	**13**	**16**

Notes:

1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

FT256: 256-ball Fine-pitch, Thin Ball Grid Array

The 256-ball fine-pitch, thin ball grid array package, FT256, supports three different Spartan-3E FPGAs, including the XC3S250E, the XC3S500E, and the XC3S1200E.

Table 143 lists all the package pins. They are sorted by bank number and then by pin name of the largest device. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The highlighted rows indicate pinout differences between the XC3S250E, the XC3S500E, and the XC3S1200E FPGAs. The XC3S250E has 18 unconnected balls, indicated as N.C. (No Connection) in Table 143 and with the black diamond character (◆) in Table 143 and Figure 83.

If the table row is highlighted in tan, then this is an instance where an unconnected pin on the XC3S250E FPGA maps to a VREF pin on the XC3S500E and XC3S1200E FPGA. If the FPGA application uses an I/O standard that requires a VREF voltage reference, connect the highlighted pin to the VREF voltage supply, even though this does not actually connect to the XC3S250E FPGA. This VREF connection on the board allows future migration to the larger devices without modifying the printed-circuit board.

All other balls have nearly identical functionality on all three devices. Table 147 summarizes the Spartan-3E footprint migration differences for the FT256 package.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx web site at:

http://www.xilinx.com/support/documentation/data_sheets/s3e_pin.zip

Pinout Table

Table 143: **FT256 Package Pinout**

Bank	XC3S250E Pin Name	XC3S500E Pin Name	XC3S1200E Pin Name	FT256 Ball	Type
0	IO	IO	IO	A7	I/O
0	IO	IO	IO	A12	I/O
0	IO	IO	IO	B4	I/O
0	IP	IP	IO	B6	***250E:*** INPUT ***500E:*** INPUT ***1200E:*** I/O
0	IP	IP	IO	B10	***250E:*** INPUT ***500E:*** INPUT ***1200E:*** I/O
0	IO/VREF_0	IO/VREF_0	IO/VREF_0	D9	VREF
0	IO_L01N_0	IO_L01N_0	IO_L01N_0	A14	I/O
0	IO_L01P_0	IO_L01P_0	IO_L01P_0	B14	I/O
0	IO_L03N_0/VREF_0	IO_L03N_0/VREF_0	IO_L03N_0/VREF_0	A13	VREF
0	IO_L03P_0	IO_L03P_0	IO_L03P_0	B13	I/O
0	IO_L04N_0	IO_L04N_0	IO_L04N_0	E11	I/O
0	IO_L04P_0	IO_L04P_0	IO_L04P_0	D11	I/O
0	IO_L05N_0/VREF_0	IO_L05N_0/VREF_0	IO_L05N_0/VREF_0	B11	VREF
0	IO_L05P_0	IO_L05P_0	IO_L05P_0	C11	I/O
0	IO_L06N_0	IO_L06N_0	IO_L06N_0	E10	I/O
0	IO_L06P_0	IO_L06P_0	IO_L06P_0	D10	I/O
0	IO_L08N_0/GCLK5	IO_L08N_0/GCLK5	IO_L08N_0/GCLK5	F9	GCLK
0	IO_L08P_0/GCLK4	IO_L08P_0/GCLK4	IO_L08P_0/GCLK4	E9	GCLK
0	IO_L09N_0/GCLK7	IO_L09N_0/GCLK7	IO_L09N_0/GCLK7	A9	GCLK
0	IO_L09P_0/GCLK6	IO_L09P_0/GCLK6	IO_L09P_0/GCLK6	A10	GCLK
0	IO_L11N_0/GCLK11	IO_L11N_0/GCLK11	IO_L11N_0/GCLK11	D8	GCLK
0	IO_L11P_0/GCLK10	IO_L11P_0/GCLK10	IO_L11P_0/GCLK10	C8	GCLK
0	IO_L12N_0	IO_L12N_0	IO_L12N_0	F8	I/O