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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	612
Number of Logic Elements/Cells	5508
Total RAM Bits	221184
Number of I/O	108
Number of Gates	250000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s250e-4tq144c

Package Marking

Figure 2 provides a top marking example for Spartan-3E FPGAs in the quad-flat packages. Figure 3 shows the top marking for Spartan-3E FPGAs in BGA packages except the 132-ball chip-scale package (CP132 and CPG132). The markings for the BGA packages are nearly identical to those for the quad-flat packages, except that the marking is rotated with respect to the ball A1 indicator. Figure 4 shows the top marking for Spartan-3E FPGAs in the CP132 and CPG132 packages.

On the QFP and BGA packages, the optional numerical Stepping Code follows the Lot Code.

The "5C" and "4I" part combinations can have a dual mark of "5C/4I". Devices with a single mark are only guaranteed for the marked speed grade and temperature range. All "5C" and "4I" part combinations use the Stepping 1 production silicon.

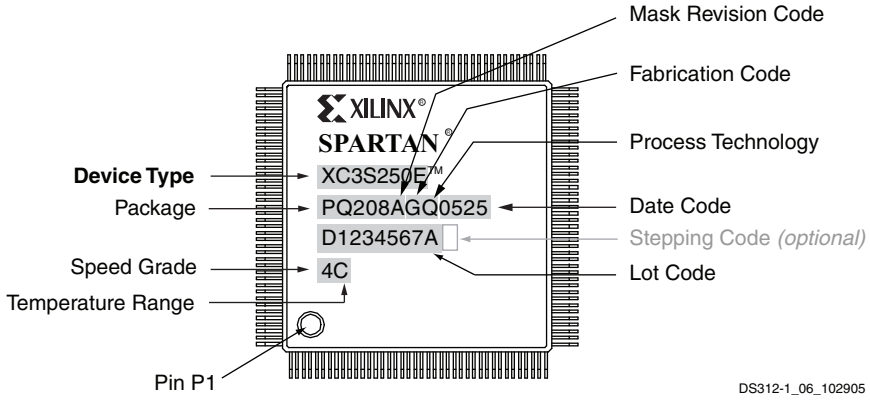

Figure 2: **Spartan-3E QFP Package Marking Example**

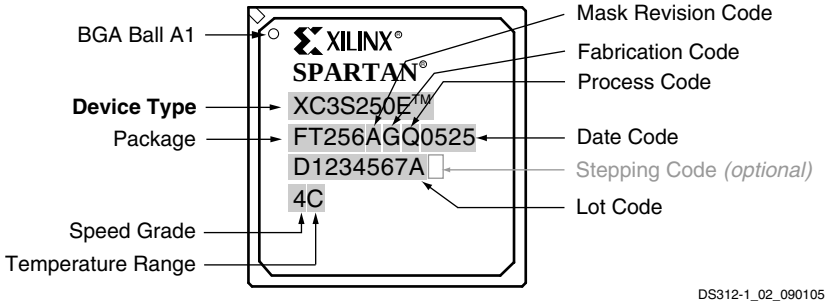

Figure 3: **Spartan-3E BGA Package Marking Example**

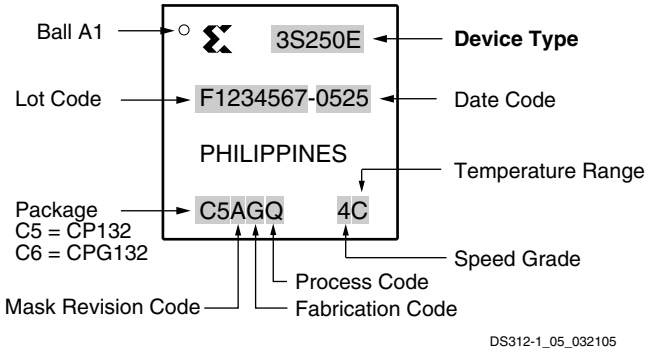

Figure 4: **Spartan-3E CP132 and CPG132 Package Marking Example**

Table 22: **Port Aspect Ratios**

Total Data Path Width (w bits)	DI/DO Data Bus Width (w-p bits)(1)	DIP/DOP Parity Bus Width (p bits)	ADDR Bus Width (r bits)(2)	DI/DO [w-p-1:0]	DIP/DOP [p-1:0]	ADDR [r-1:0]	No. of Addressable Locations (n)(3)	Block RAM Capacity (w*n bits)(4)
1	1	0	14	[0:0]	-	[13:0]	16,384	16,384
2	2	0	13	[1:0]	-	[12:0]	8,192	16,384
4	4	0	12	[3:0]	-	[11:0]	4,096	16,384
9	8	1	11	[7:0]	[0:0]	[10:0]	2,048	18,432
18	16	2	10	[15:0]	[1:0]	[9:0]	1,024	18,432
36	32	4	9	[31:0]	[3:0]	[8:0]	512	18,432

Notes:

1. The width of the total data path (w) is the sum of the DI/DO bus width (w-p) and any parity bits (p).
2. The width selection made for the DI/DO bus determines the number of address lines (r) according to the relationship expressed as: r = 14 – [log(w–p)/log9(2)].
3. The number of address lines delimits the total number (n) of addressable locations or depth according to the following equation: $n = 2^r$.
4. The product of w and n yields the total block RAM capacity.

If the data bus width of Port A differs from that of Port B, the block RAM automatically performs a bus-matching function as described in Figure 31. When data is written to a port with a narrow bus and then read from a port with a wide bus, the latter port effectively combines “narrow” words to form “wide” words. Similarly, when data is written into a port with a wide bus and then read from a port with a narrow bus, the latter port divides “wide” words to form “narrow” words. Parity bits are not available if the data port width is configured as x4, x2, or x1. For example, if a x36 data word (32 data, 4 parity) is addressed as two x18 halfwords (16 data, 2 parity), the parity bits associated with each data byte are mapped within the block RAM to the appropriate parity bits. The same effect happens when the x36 data word is mapped as four x9 words.

Dedicated Multipliers

For additional information, refer to the “Using Embedded Multipliers” chapter in UG331.

The Spartan-3E devices provide 4 to 36 dedicated multiplier blocks per device. The multipliers are located together with the block RAM in one or two columns depending on device density. See Arrangement of RAM Blocks on Die for details on the location of these blocks and their connectivity.

Operation

The multiplier blocks primarily perform two’s complement numerical multiplication but can also perform some less obvious applications, such as simple data storage and barrel shifting. Logic slices also implement efficient small multipliers and thereby supplement the dedicated multipliers. The Spartan-3E dedicated multiplier blocks have additional features beyond those provided in Spartan-3 FPGAs.

Each multiplier performs the principle operation P = A × B, where ‘A’ and ‘B’ are 18-bit words in two’s complement form, and ‘P’ is the full-precision 36-bit product, also in two’s complement form. The 18-bit inputs represent values ranging from $-131{,}072_{10}$ to $+131{,}071_{10}$ with a resulting product ranging from $-17{,}179{,}738{,}112_{10}$ to $+17{,}179{,}869{,}184_{10}$.

Implement multipliers with inputs less than 18 bits by sign-extending the inputs (i.e., replicating the most-significant bit). Wider multiplication operations are performed by combining the dedicated multipliers and slice-based logic in any viable combination or by time-sharing a single multiplier. Perform unsigned multiplication by restricting the inputs to the positive range. Tie the most-significant bit Low and represent the unsigned value in the remaining 17 lesser-significant bits.

Optional Pipeline Registers

As shown in Figure 36, each multiplier block has optional registers on each of the multiplier inputs and the output. The registers are named AREG, BREG, and PREG and can be used in any combination. The clock input is common to all the registers within a block, but each register has an independent clock enable and synchronous reset controls making them ideal for storing data samples and coefficients. When used for pipelining, the registers boost the multiplier clock rate, beneficial for higher performance applications.

Figure 36 illustrates the principle features of the multiplier block.

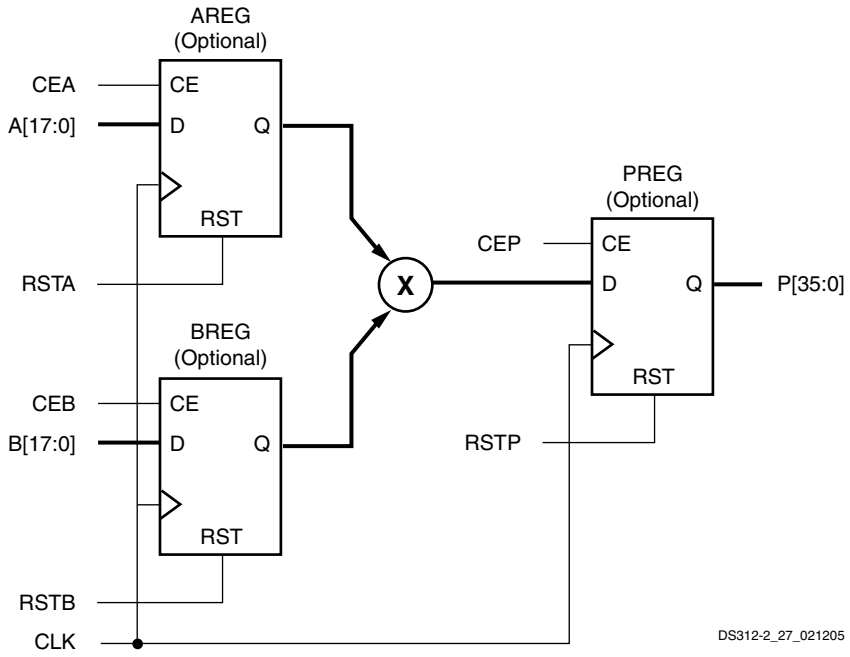

Figure 36: **Principle Ports and Functions of Dedicated Multiplier Blocks**

Use the MULT18X18SIO primitive shown in Figure 37 to instantiate a multiplier within a design. Although high-level logic synthesis software usually automatically infers a multiplier, adding the pipeline registers might require the MULT18X18SIO primitive. Connect the appropriate signals to the MULT18X18SIO multiplier ports and set the individual AREG, BREG, and PREG attributes to ‘1’ to insert the associated register, or to 0 to remove it and make the signal path combinatorial.

The connections for the bottom-edge BUFGMUX elements are similar to the top-edge connections (see Figure 46).

On the left and right edges, only two clock inputs feed each pair of BUFGMUX elements.

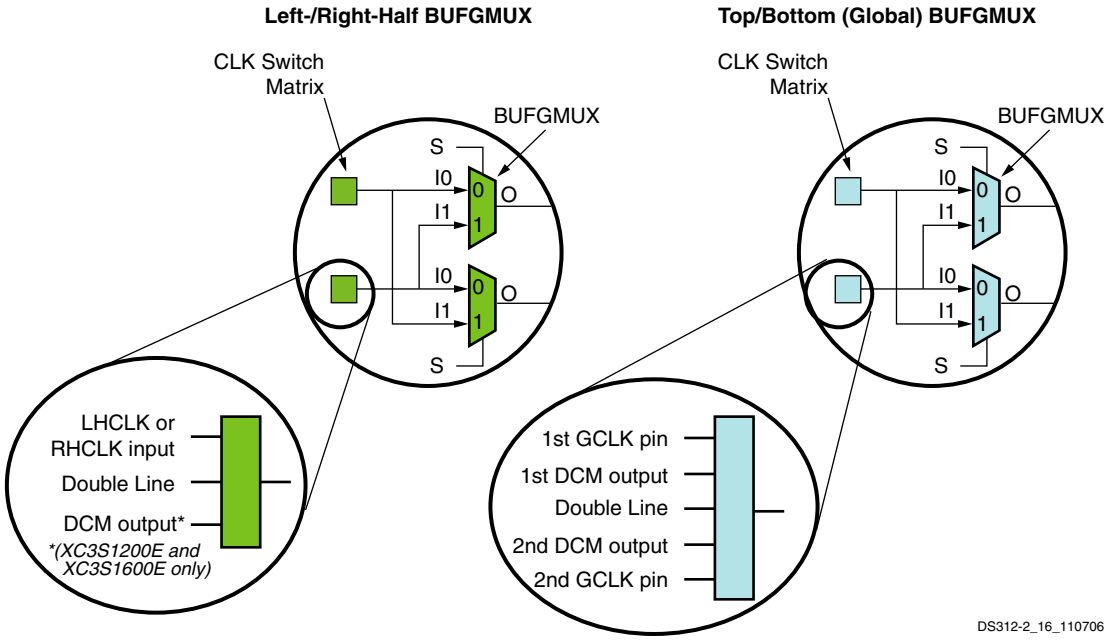

Figure 46: **Clock Switch Matrix to BUFGMUX Pair Connectivity**

Quadrant Clock Routing

The clock routing within the FPGA is quadrant-based, as shown in Figure 45. Each clock quadrant supports eight total clock signals, labeled 'A' through 'H' in Table 41 and Figure 47. The clock source for an individual clock line originates either from a global BUFGMUX element along the top and bottom edges or from a BUFGMUX element along the associated edge, as shown in Figure 47. The clock lines feed the synchronous resource elements (CLBs, IOBs, block RAM, multipliers, and DCMs) within the quadrant.

The four quadrants of the device are:

- Top Right (TR)
- Bottom Right (BR)
- Bottom Left (BL)
- Top Left (TL)

Note that the quadrant clock notation (TR, BR, BL, TL) is separate from that used for similar IOB placement constraints.

To estimate the quadrant location for a particular I/O, see the footprint diagrams in Module 4, Pinout Descriptions. For exact quadrant locations, use the floorplanning tool. In the QFP packages (VQ100, TQ144 and PQ208) the quadrant borders fall in the middle of each side of the package, at a GND pin. The clock inputs fall on the quadrant boundaries, as indicated in Table 42.

Table 42: **QFP Package Clock Quadrant Locations**

Clock Pins	Quadrant
GCLK[3:0]	BR
GCLK[7:4]	TR
GCLK[11:8]	TL
GCLK[15:12]	BL
RHCLK[3:0]	BR
RHCLK[7:4]	TR
LHCLK[3:0]	TL
LHCLK[7:4]	BL

In a few cases, a dedicated input is physically in one quadrant of the device but connects to a different clock quadrant:

- FT256, H16 is in clock quadrant BR
- FG320, K2 is in clock quadrant BL
- FG400, L8 is in clock quadrant TL and the I/O at N11 is in clock quadrant BL
- FG484, M2 is in clock quadrant TL and L15 is in clock quadrant BR

Configuration

For additional information on configuration, refer to UG332: *Spartan-3 Generation Configuration User Guide*.

Differences from Spartan-3 FPGAs

In general, Spartan-3E FPGA configuration modes are a superset to those available in Spartan-3 FPGAs. Two new modes added in Spartan-3E FPGAs provide a glueless configuration interface to industry-standard parallel NOR Flash and SPI serial Flash memories.

Configuration Process

The function of a Spartan-3E FPGA is defined by loading application-specific configuration data into the FPGA's internal, reprogrammable CMOS configuration latches (CCLs), similar to the way a microprocessor's function is defined by its application program. For FPGAs, this configuration process uses a subset of the device pins, some of which are dedicated to configuration; other pins are merely borrowed and returned to the application as general-purpose user I/Os after configuration completes.

Spartan-3E FPGAs offer several configuration options to minimize the impact of configuration on the overall system design. In some configuration modes, the FPGA generates a clock and loads itself from an external memory source, either serially or via a byte-wide data path. Alternatively, an external host such as a microprocessor downloads the FPGA's configuration data using a simple synchronous serial interface or via a byte-wide peripheral-style interface. Furthermore, multiple-FPGA designs share a single configuration memory source, creating a structure called a daisy chain.

Three FPGA pins—M2, M1, and M0—select the desired configuration mode. The mode pin settings appear in Table 44. The mode pin values are sampled during the start of configuration when the FPGA's INIT_B output goes High. After the FPGA completes configuration, the mode pins are available as user I/Os.

Table 44: **Spartan-3E Configuration Mode Options and Pin Settings**

	Master Serial	SPI	BPI	Slave Parallel	Slave Serial	JTAG
M[2:0] mode pin settings	<0:0:0>	<0:0:1>	<0:1:0>=Up <0:1:1>=Down	<1:1:0>	<1:1:1>	<1:0:1>
Data width	Serial	Serial	Byte-wide	Byte-wide	Serial	Serial
Configuration memory source	Xilinx Platform Flash	Industry-standard SPI serial Flash	Industry-standard parallel NOR Flash or Xilinx parallel Platform Flash	Any source via microcontroller, CPU, Xilinx parallel Platform Flash, etc.	Any source via microcontroller, CPU, Xilinx Platform Flash, etc.	Any source via microcontroller, CPU, System ACE™ CF, etc.
Clock source	Internal oscillator	Internal oscillator	Internal oscillator	External clock on CCLK pin	External clock on CCLK pin	External clock on TCK pin
Total I/O pins borrowed during configuration	8	13	46	21	8	0
Configuration mode for downstream daisy-chained FPGAs	Slave Serial	Slave Serial	Slave Parallel	Slave Parallel or Memory Mapped	Slave Serial	JTAG
Stand-alone FPGA applications (no external download host)	✓	✓	✓	Possible using XCFxxP Platform Flash, which optionally generates CCLK	Possible using XCFxxP Platform Flash, which optionally generates CCLK	
Uses low-cost, industry-standard Flash		✓	✓			
Supports optional MultiBoot, multi-configuration mode			✓			

Configuration Bitstream Image Sizes

A specific Spartan-3E part type always requires a constant number of configuration bits, regardless of design complexity, as shown in Table 45. The configuration file size for a multiple-FPGA daisy-chain design roughly equals the sum of the individual file sizes.

Table 45: **Number of Bits to Program a Spartan-3E FPGA (Uncompressed Bitstreams)**

Spartan-3E FPGA	Number of Configuration Bits
XC3S100E	581,344
XC3S250E	1,353,728
XC3S500E	2,270,208
XC3S1200E	3,841,184
XC3S1600E	5,969,696

Pin Behavior During Configuration

For additional information, refer to the "Configuration Pins and Behavior during Configuration" chapter in UG332.

Table 46 shows how various pins behave during the FPGA configuration process. The actual behavior depends on the values applied to the M2, M1, and M0 mode select pins and the HSWAP pin. The mode select pins determine which of the I/O pins are borrowed during configuration and how they function. In JTAG configuration mode, no user-I/O pins are borrowed for configuration.

All user-I/O pins, input-only pins, and dual-purpose pins that are not actively involved in the currently-select configuration mode are high impedance (floating, three-stated, Hi-Z) during the configuration process. These pins are indicated in Table 46 as gray shaded table entries or cells.

The HSWAP input controls whether all user-I/O pins, input-only pins, and dual-purpose pins have a pull-up resistor to the supply rail or not. When HSWAP is Low, each pin has an internal pull-up resistor that is active throughout configuration. After configuration, pull-up and pull-down resistors are available in the FPGA application as described in Pull-Up and Pull-Down Resistors.

The yellow-shaded table entries or cells represent pins where the pull-up resistor is always enabled during configuration, regardless of the HSWAP input. The post-configuration behavior of these pins is defined by Bitstream Generator options as defined in Table 69.

Table 46: **Pin Behavior during Configuration**

Pin Name	Master Serial	SPI (Serial Flash)	BPI (Parallel NOR Flash)	JTAG	Slave Parallel	Slave Serial	I/O Bank[3]
IO* (user-I/O) IP* (input-only)							-
TDI	TDI	TDI	TDI	TDI	TDI	TDI	V_{CCAUX}
TMS	TMS	TMS	TMS	TMS	TMS	TMS	V_{CCAUX}
TCK	TCK	TCK	TCK	TCK	TCK	TCK	V_{CCAUX}
TDO	TDO	TDO	TDO	TDO	TDO	TDO	V_{CCAUX}
PROG_B	PROG_B	PROG_B	PROG_B	PROG_B	PROG_B	PROG_B	V_{CCAUX}
DONE	DONE	DONE	DONE	DONE	DONE	DONE	V_{CCAUX}
HSWAP	HSWAP	HSWAP	HSWAP	HSWAP	HSWAP	HSWAP	0
M2	0	0	0	1	1	1	2
M1	0	0	1	0	1	1	2
M0	0	1	0 = Up 1 = Down	1	0	1	2
CCLK	CCLK (I/O)	CCLK (I/O)	CCLK (I/O)		CCLK (I)	CCLK (I)	2
INIT_B	INIT_B	INIT_B	INIT_B		INIT_B	INIT_B	2
CSO_B		CSO_B	CSO_B		CSO_B		2
DOUT/BUSY	DOUT	DOUT	BUSY		BUSY	DOUT	2
MOSI/CSI_B		MOSI	CSI_B		CSI_B		2
D7			D7		D7		2
D6			D6		D6		2
D5			D5		D5		2
D4			D4		D4		2
D3			D3		D3		2
D2			D2		D2		2
D1			D1		D1		2

Table 46: **Pin Behavior during Configuration *(Cont'd)***

Pin Name	Master Serial	SPI (Serial Flash)	BPI (Parallel NOR Flash)	JTAG	Slave Parallel	Slave Serial	I/O Bank[3]
D0/DIN	DIN	DIN	D0		D0	DIN	2
RDWR_B			RDWR_B		RDWR_B		2
A23			A23				2
A22			A22				2
A21			A21				2
A20			A20				2
A19/VS2		VS2	A19				2
A18/VS1		VS1	A18				2
A17/VS0		VS0	A17				2
A16			A16				1
A15			A15				1
A14			A14				1
A13			A13				1
A12			A12				1
A11			A11				1
A10			A10				1
A9			A9				1
A8			A8				1
A7			A7				1
A6			A6				1
A5			A5				1
A4			A4				1
A3			A3				1
A2			A2				1
A1			A1				1
A0			A0				1
LDC0			LDC0				1
LDC1			LDC1				1
LDC2			LDC2				1
HDC			HDC				1

Notes:
1. Gray shaded cells represent pins that are in a high-impedance state (Hi-Z, floating) during configuration. These pins have an optional internal pull-up resistor to their respective V_{CCO} supply pin that is active throughout configuration if the HSWAP input is Low.
2. Yellow shaded cells represent pins with an internal pull-up resistor to its respective voltage supply rail that is active during configuration, regardless of the HSWAP pin.
3. Note that dual-purpose outputs are supplied by V_{CCO}, and configuration inputs are supplied by V_{CCAUX}.

The HSWAP pin itself has a pull-up resistor enabled during configuration. However, the VCCO_0 supply voltage must be applied before the pull-up resistor becomes active. If the VCCO_0 supply ramps after the VCCO_2 power supply, do not let HSWAP float; tie HSWAP to the desired logic level externally.

Spartan-3E FPGAs have only six dedicated configuration pins, including the DONE and PROG_B pins, and the four JTAG boundary-scan pins: TDI, TDO, TMS, and TCK. All other configuration pins are dual-purpose I/O pins and are available to the FPGA application after the DONE pin goes High. See Start-Up for additional information.

Table 47 shows the default I/O standard setting for the various configuration pins during the configuration process. The configuration interface is designed primarily for 2.5V operation when the VCCO_2 (and VCCO_1 in BPI mode) connects to 2.5V.

Table 47: **Default I/O Standard Setting During Configuration (VCCO_2 = 2.5V)**

Pin(s)	I/O Standard	Output Drive	Slew Rate
All, including CCLK	LVCMOS25	8 mA	Slow

read operations at this time. Spartan-3E FPGAs issue the read command just once. If the SPI Flash is not ready, then the FPGA does not properly configure.

If the 3.3V supply is last in the sequence and does not ramp fast enough, or if the SPI Flash PROM cannot be ready when required by the FPGA, delay the FPGA configuration process by holding either the FPGA's PROG_B input or INIT_B input Low, as highlighted in Figure 54. Release the FPGA when the SPI Flash PROM is ready. For example, a simple R-C delay circuit attached to the INIT_B pin forces the FPGA to wait for a preselected amount of time. Alternately, a Power Good signal from the 3.3V supply or a system reset signal accomplishes the same purpose. Use an open-drain or open-collector output when driving PROG_B or INIT_B.

SPI Flash PROM Density Requirements

Table 57 shows the smallest usable SPI Flash PROM to program a single Spartan-3E FPGA. Commercially available SPI Flash PROMs range in density from 1 Mbit to 128 Mbits. A multiple-FPGA daisy-chained application requires a SPI Flash PROM large enough to contain the sum of the FPGA file sizes. An application can also use a larger-density SPI Flash PROM to hold additional data beyond just FPGA configuration data. For example, the SPI Flash PROM can also store application code for a MicroBlaze™ RISC processor core integrated in the Spartan-3E FPGA. See Using the SPI Flash Interface after Configuration.

Table 57: **Number of Bits to Program a Spartan-3E FPGA and Smallest SPI Flash PROM**

Device	Number of Configuration Bits	Smallest Usable SPI Flash PROM
XC3S100E	581,344	1 Mbit
XC3S250E	1,353,728	2 Mbit
XC3S500E	2,270,208	4 Mbit
XC3S1200E	3,841,184	4 Mbit
XC3S1600E	5,969,696	8 Mbit

CCLK Frequency

In SPI Flash mode, the FPGA's internal oscillator generates the configuration clock frequency. The FPGA provides this clock on its CCLK output pin, driving the PROM's clock input pin. The FPGA starts configuration at its lowest frequency and increases its frequency for the remainder of the configuration process if so specified in the configuration bitstream. The maximum frequency is specified using the ***ConfigRate*** bitstream generator option. The maximum frequency supported by the FPGA configuration logic depends on the timing for the SPI Flash device. Without examining the timing for a specific SPI Flash PROM, use ***ConfigRate*** = 12 or lower. SPI Flash PROMs that support the FAST READ command support higher data rates. Some such PROMs support up to ***ConfigRate*** = 25 and beyond but require careful data sheet analysis. See Serial Peripheral Interface (SPI) Configuration Timing for more detailed timing analysis.

Using the SPI Flash Interface after Configuration

After the FPGA successfully completes configuration, all of the pins connected to the SPI Flash PROM are available as user-I/O pins.

If not using the SPI Flash PROM after configuration, drive CSO_B High to disable the PROM. The MOSI, DIN, and CCLK pins are then available to the FPGA application.

Because all the interface pins are user I/O after configuration, the FPGA application can continue to use the SPI Flash interface pins to communicate with the SPI Flash PROM, as shown in Figure 56. SPI Flash PROMs offer random-accessible, byte-addressable, read/write, non-volatile storage to the FPGA application.

SPI Flash PROMs are available in densities ranging from 1 Mbit up to 128 Mbits. However, a single Spartan-3E FPGA requires less than 6 Mbits. If desired, use a larger SPI Flash PROM to contain additional non-volatile application data, such as MicroBlaze processor code, or other user data such as serial numbers and Ethernet MAC IDs. In the example shown in Figure 56, the FPGA configures from SPI Flash PROM. Then using FPGA logic after configuration, the FPGA copies MicroBlaze code from SPI Flash into external DDR SDRAM for code execution. Similarly, the FPGA application can store non-volatile application data within the SPI Flash PROM.

The FPGA configuration data is stored starting at location 0. Store any additional data beginning in the next available SPI Flash PROM sector or page. Do not mix configuration data and user data in the same sector or page.

Similarly, the SPI bus can be expanded to additional SPI peripherals. Because SPI is a common industry-standard interface, various SPI-based peripherals are available, such as analog-to-digital (A/D) converters, digital-to-analog (D/A) converters, CAN controllers, and temperature sensors. However, if sufficient I/O pins are available in the application, Xilinx recommends creating a separate SPI bus to control peripherals. Creating a second port reduces the loading on the CCLK and DIN pins, which are crucial for configuration.

The MOSI, DIN, and CCLK pins are common to all SPI peripherals. Connect the select input on each additional SPI peripheral to one of the FPGA user I/O pins. If HSWAP = 0 during configuration, the FPGA holds the select line High. If HSWAP = 1, connect the select line to +3.3V via an external 4.7 kΩ pull-up resistor to avoid spurious read or write operations. After configuration, drive the select line Low to select the desired SPI peripheral.

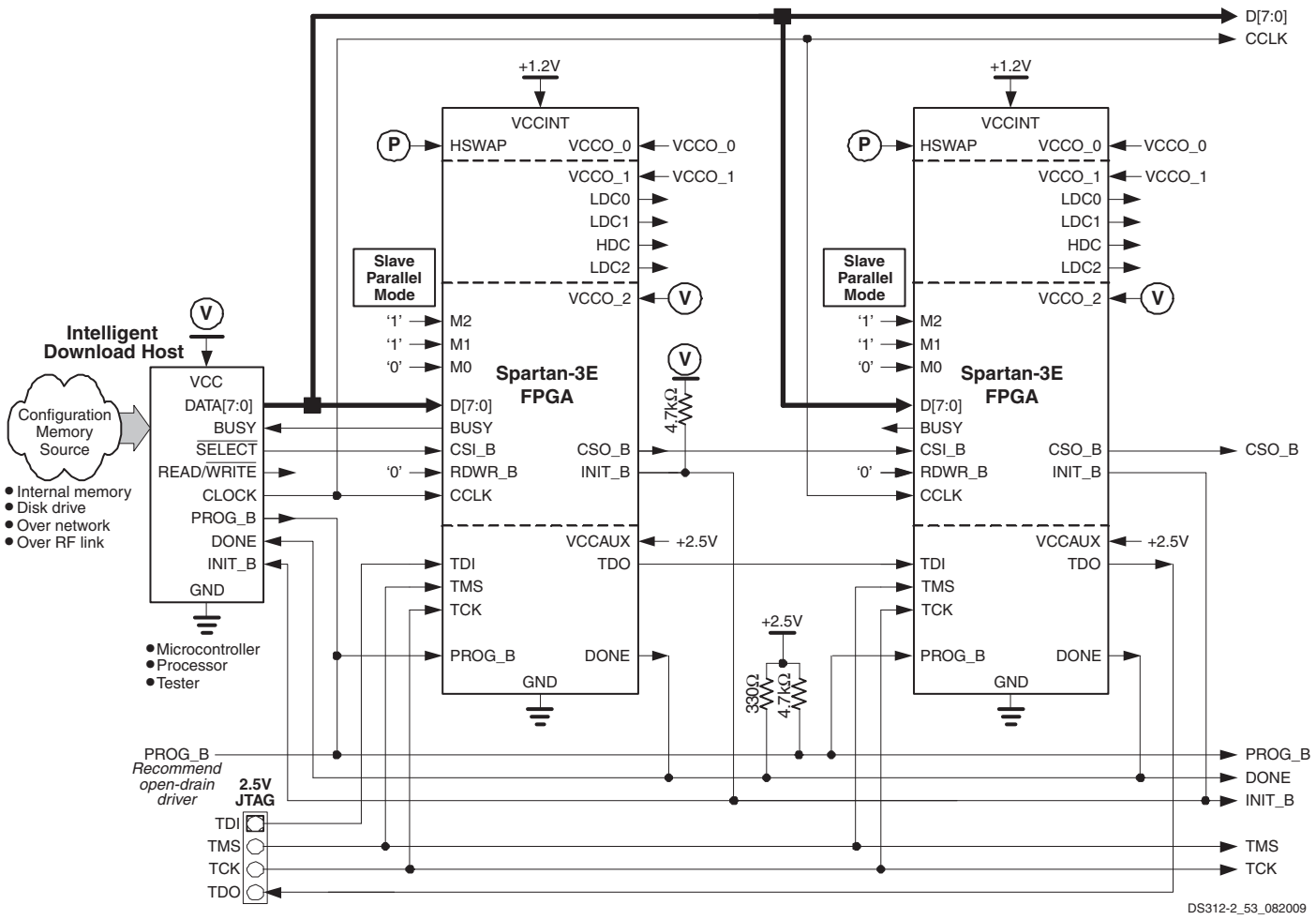

Figure 62: **Daisy-Chaining using Slave Parallel Mode**

Slave Serial Mode

For additional information, refer to the “Slave Serial Mode” chapter in UG332.

In Slave Serial mode (M[2:0] = <1:1:1>), an external host such as a microprocessor or microcontroller writes serial configuration data into the FPGA, using the synchronous serial interface shown in Figure 63. The serial configuration data is presented on the FPGA’s DIN input pin with sufficient setup time before each rising edge of the externally generated CCLK clock input.

The intelligent host starts the configuration process by pulsing PROG_B and monitoring that the INIT_B pin goes High, indicating that the FPGA is ready to receive its first data. The host then continues supplying data and clock signals until either the DONE pin goes High, indicating a successful configuration, or until the INIT_B pin goes Low, indicating a configuration error. The configuration process requires more clock cycles than indicated from the configuration file size. Additional clocks are required during the FPGA’s start-up sequence, especially if the FPGA is programmed to wait for selected Digital Clock Managers (DCMs) to lock to their respective clock inputs (see Start-Up, page 105).

Table 87: **Pin-to-Pin Setup and Hold Times for the IOB Input Path (System Synchronous)**

Symbol	Description	Conditions	IFD_DELAY_VALUE=	Device	Speed Grade		Units
					-5	-4	
					Min	Min	
Setup Times							
T_{PSDCM}	When writing to the Input Flip-Flop (IFF), the time from the setup of data at the Input pin to the active transition at a Global Clock pin. The DCM is used. No Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = 0, with DCM(3)	0	XC3S100E	2.65	2.98	ns
				XC3S250E	2.25	2.59	ns
				XC3S500E	2.25	2.59	ns
				XC3S1200E	2.25	2.58	ns
				XC3S1600E	2.25	2.59	ns
T_{PSFD}	When writing to IFF, the time from the setup of data at the Input pin to an active transition at the Global Clock pin. The DCM is not used. The Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = default software setting	2	XC3S100E	3.16	3.58	ns
			3	XC3S250E	3.44	3.91	ns
			3	XC3S500E	4.00	4.73	ns
			3	XC3S1200E	2.60	3.31	ns
			3	XC3S1600E	3.33	3.77	ns
Hold Times							
T_{PHDCM}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is used. No Input Delay is programmed.	LVCMOS25(4), IFD_DELAY_VALUE = 0, with DCM(3)	0	XC3S100E	–0.54	–0.52	ns
				XC3S250E	0.06	0.14	ns
				XC3S500E	0.07	0.14	ns
				XC3S1200E	0.07	0.15	ns
				XC3S1600E	0.06	0.14	ns
T_{PHFD}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is not used. The Input Delay is programmed.	LVCMOS25(4), IFD_DELAY_VALUE = default software setting	2	XC3S100E	–0.31	–0.24	ns
			3	XC3S250E	–0.32	–0.32	ns
			3	XC3S500E	–0.77	–0.77	ns
			3	XC3S1200E	0.13	0.16	ns
			3	XC3S1600E	–0.05	–0.03	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 95 and are based on the operating conditions set forth in Table 77 and Table 80.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, subtract the appropriate adjustment from Table 91. If this is true of the data Input, add the appropriate Input adjustment from the same table.
3. DCM output jitter is included in all measurements.
4. This hold time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, add the appropriate Input adjustment from Table 91. If this is true of the data Input, subtract the appropriate Input adjustment from the same table. When the hold time is negative, it is possible to change the data before the clock's active edge.

Table 88: **Setup and Hold Times for the IOB Input Path**

Symbol	Description	Conditions	IFD_DELAY_VALUE=	Device	Speed Grade		Units
					-5	-4	
					Min	Min	
Setup Times							
T_{IOPICK}	Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). No Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = 0	0	All	1.84	2.12	ns
$T_{IOPICKD}$	Time from the setup of data at the Input pin to the active transition at the IFF's ICLK input. The Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = default software setting	2	XC3S100E	6.12	7.01	ns
			3	All Others	6.76	7.72	
Hold Times							
T_{IOICKP}	Time from the active transition at the IFF's ICLK input to the point where data must be held at the Input pin. No Input Delay is programmed.	LVCMOS25(3), IFD_DELAY_VALUE = 0	0	All	–0.76	–0.76	ns
$T_{IOICKPD}$	Time from the active transition at the IFF's ICLK input to the point where data must be held at the Input pin. The Input Delay is programmed.	LVCMOS25(3), IFD_DELAY_VALUE = default software setting	2	XC3S100E	–3.93	–3.93	ns
			3	All Others	–3.50	–3.50	
Set/Reset Pulse Width							
T_{RPW_IOB}	Minimum pulse width to SR control input on IOB			All	1.57	1.80	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 95 and are based on the operating conditions set forth in Table 77 and Table 80.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, add the appropriate Input adjustment from Table 91.
3. These hold times require adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, subtract the appropriate Input adjustment from Table 91. When the hold time is negative, it is possible to change the data before the clock's active edge.

Table 89: **Sample Window (Source Synchronous)**

Symbol	Description	Max	Units
T_{SAMP}	Setup and hold capture window of an IOB input flip-flop	The input capture sample window value is highly specific to a particular application, device, package, I/O standard, I/O placement, DCM usage, and clock buffer. Please consult the appropriate Xilinx application note for application-specific values. • XAPP485: *1:7 Deserialization in Spartan-3E FPGAs at Speeds Up to 666 Mbps*	ps

Table 93: **Timing for the IOB Three-State Path**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max	Max	
Synchronous Output Enable/Disable Times						
T_{IOCKHZ}	Time from the active transition at the OTCLK input of the Three-state Flip-Flop (TFF) to when the Output pin enters the high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	1.49	1.71	ns
T_{IOCKON}(2)	Time from the active transition at TFF's OTCLK input to when the Output pin drives valid data		All	2.70	3.10	ns
Asynchronous Output Enable/Disable Times						
T_{GTS}	Time from asserting the Global Three State (GTS) input on the STARTUP_SPARTAN3E primitive to when the Output pin enters the high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	8.52	9.79	ns
Set/Reset Times						
T_{IOSRHZ}	Time from asserting TFF's SR input to when the Output pin enters a high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	2.11	2.43	ns
T_{IOSRON}(2)	Time from asserting TFF's SR input at TFF to when the Output pin drives valid data		All	3.32	3.82	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 95 and are based on the operating conditions set forth in Table 77 and Table 80.
2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from Table 94.
3. For minimum delays use the values reported by the Timing Analyzer.

Table 119: **Configuration Timing Requirements for Attached SPI Serial Flash**

Symbol	Description	Requirement	Units
T_{CCS}	SPI serial Flash PROM chip-select time	$T_{CCS} \leq T_{MCCL1} - T_{CCO}$	ns
T_{DSU}	SPI serial Flash PROM data input setup time	$T_{DSU} \leq T_{MCCL1} - T_{CCO}$	ns
T_{DH}	SPI serial Flash PROM data input hold time	$T_{DH} \leq T_{MCCH1}$	ns
T_V	SPI serial Flash PROM data clock-to-output time	$T_V \leq T_{MCCLn} - T_{DCC}$	ns
f_C or f_R	Maximum SPI serial Flash PROM clock frequency (also depends on specific read command used)	$f_C \geq \frac{1}{T_{CCLKn(min)}}$	MHz

Notes:

1. These requirements are for successful FPGA configuration in SPI mode, where the FPGA provides the CCLK frequency. The post configuration timing can be different to support the specific needs of the application loaded into the FPGA and the resulting clock source.
2. Subtract additional printed circuit board routing delay as required by the application.

TQ144 Footprint

Note pin 1 indicator in top-left corner and logo orientation.
Double arrows (↔) indicates a pinout migration difference between the XC3S100E and XC3S250E.

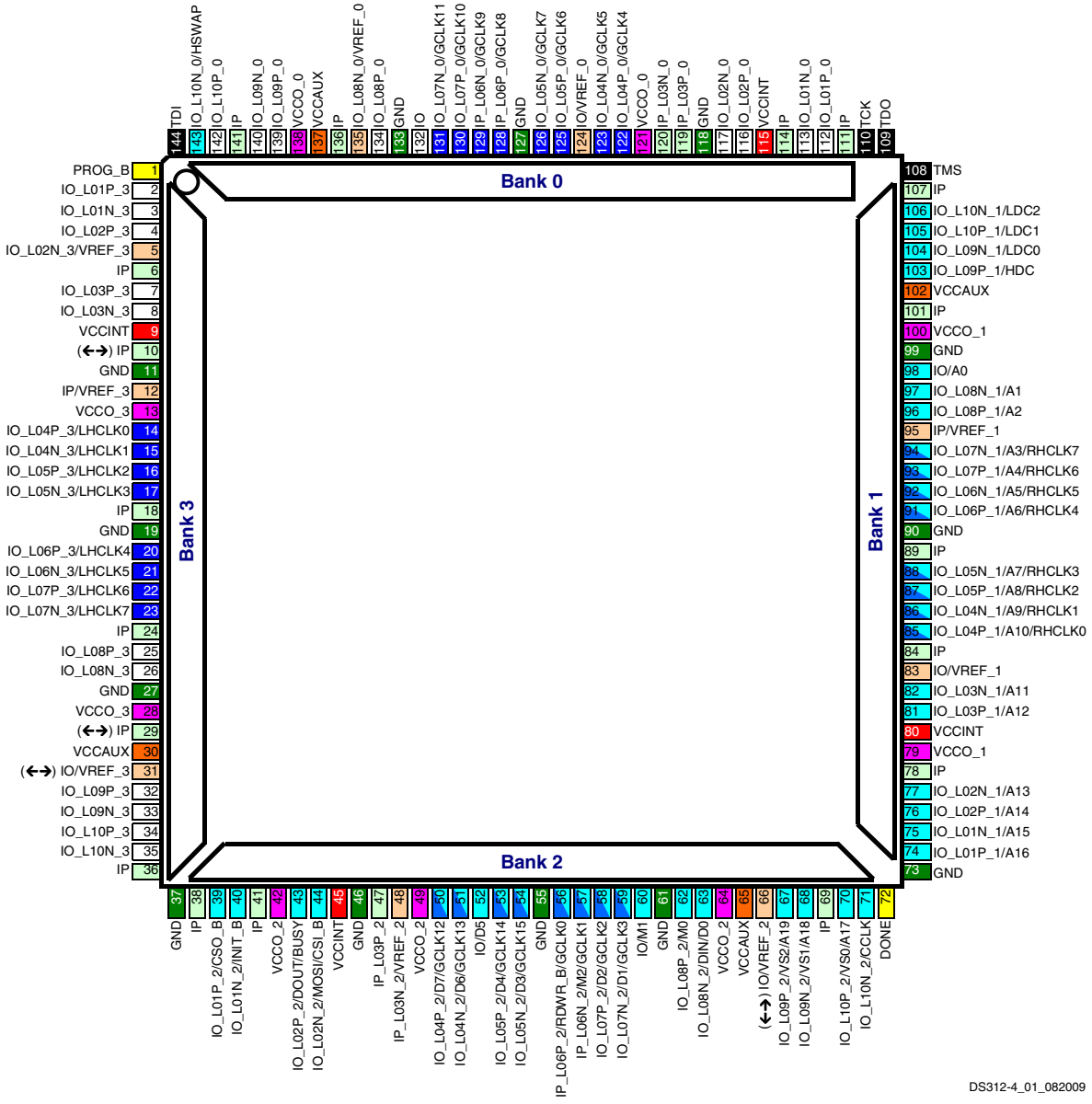

Figure 82: **TQ144 Package Footprint (top view)**

20	**I/O:** Unrestricted, general-purpose user I/O	42	**DUAL:** Configuration pin, then possible user I/O	9	**VREF:** User I/O or input voltage reference for bank
21	**INPUT:** Unrestricted, general-purpose input pin	16	**CLK:** User I/O, input, or global buffer input	9	**VCCO:** Output voltage supply for bank
2	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	4	**VCCINT:** Internal core supply voltage (+1.2V)
0	**N.C.:** Not connected	13	**GND:** Ground	4	**VCCAUX:** Auxiliary supply voltage (+2.5V)

PQ208: 208-pin Plastic Quad Flat Package

The 208-pin plastic quad flat package, PQ208, supports two different Spartan-3E FPGAs, including the XC3S250E and the XC3S500E.

Table 141 lists all the PQ208 package pins. They are sorted by bank number and then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at:

http://www.xilinx.com/support/documentation/data_sheets/s3e_pin.zip

Pinout Table

Table 141: **PQ208 Package Pinout**

Bank	XC3S250E XC3S500E Pin Name	PQ208 Pin	Type
0	IO	P187	I/O
0	IO/VREF_0	P179	VREF
0	IO_L01N_0	P161	I/O
0	IO_L01P_0	P160	I/O
0	IO_L02N_0/VREF_0	P163	VREF
0	IO_L02P_0	P162	I/O
0	IO_L03N_0	P165	I/O
0	IO_L03P_0	P164	I/O
0	IO_L04N_0/VREF_0	P168	VREF
0	IO_L04P_0	P167	I/O
0	IO_L05N_0	P172	I/O
0	IO_L05P_0	P171	I/O
0	IO_L07N_0/GCLK5	P178	GCLK
0	IO_L07P_0/GCLK4	P177	GCLK
0	IO_L08N_0/GCLK7	P181	GCLK
0	IO_L08P_0/GCLK6	P180	GCLK
0	IO_L10N_0/GCLK11	P186	GCLK
0	IO_L10P_0/GCLK10	P185	GCLK
0	IO_L11N_0	P190	I/O
0	IO_L11P_0	P189	I/O
0	IO_L12N_0/VREF_0	P193	VREF
0	IO_L12P_0	P192	I/O
0	IO_L13N_0	P197	I/O
0	IO_L13P_0	P196	I/O
0	IO_L14N_0/VREF_0	P200	VREF
0	IO_L14P_0	P199	I/O
0	IO_L15N_0	P203	I/O

Table 141: **PQ208 Package Pinout *(Cont'd)***

Bank	XC3S250E XC3S500E Pin Name	PQ208 Pin	Type
0	IO_L15P_0	P202	I/O
0	IO_L16N_0/HSWAP	P206	DUAL
0	IO_L16P_0	P205	I/O
0	IP	P159	INPUT
0	IP	P169	INPUT
0	IP	P194	INPUT
0	IP	P204	INPUT
0	IP_L06N_0	P175	INPUT
0	IP_L06P_0	P174	INPUT
0	IP_L09N_0/GCLK9	P184	GCLK
0	IP_L09P_0/GCLK8	P183	GCLK
0	VCCO_0	P176	VCCO
0	VCCO_0	P191	VCCO
0	VCCO_0	P201	VCCO
1	IO_L01N_1/A15	P107	DUAL
1	IO_L01P_1/A16	P106	DUAL
1	IO_L02N_1/A13	P109	DUAL
1	IO_L02P_1/A14	P108	DUAL
1	IO_L03N_1/VREF_1	P113	VREF
1	IO_L03P_1	P112	I/O
1	IO_L04N_1	P116	I/O
1	IO_L04P_1	P115	I/O
1	IO_L05N_1/A11	P120	DUAL
1	IO_L05P_1/A12	P119	DUAL
1	IO_L06N_1/VREF_1	P123	VREF
1	IO_L06P_1	P122	I/O
1	IO_L07N_1/A9/RHCLK1	P127	RHCLK/DUAL
1	IO_L07P_1/A10/RHCLK0	P126	RHCLK/DUAL
1	IO_L08N_1/A7/RHCLK3	P129	RHCLK/DUAL
1	IO_L08P_1/A8/RHCLK2	P128	RHCLK/DUAL
1	IO_L09N_1/A5/RHCLK5	P133	RHCLK/DUAL
1	IO_L09P_1/A6/RHCLK4	P132	RHCLK/DUAL
1	IO_L10N_1/A3/RHCLK7	P135	RHCLK/DUAL
1	IO_L10P_1/A4/RHCLK6	P134	RHCLK/DUAL
1	IO_L11N_1/A1	P138	DUAL
1	IO_L11P_1/A2	P137	DUAL
1	IO_L12N_1/A0	P140	DUAL
1	IO_L12P_1	P139	I/O
1	IO_L13N_1	P145	I/O
1	IO_L13P_1	P144	I/O
1	IO_L14N_1	P147	I/O
1	IO_L14P_1	P146	I/O

Table 141: **PQ208 Package Pinout *(Cont'd)***

Bank	XC3S250E XC3S500E Pin Name	PQ208 Pin	Type
3	IO_L14P_3	P41	I/O
3	IO_L15N_3	P48	I/O
3	IO_L15P_3	P47	I/O
3	IO_L16N_3	P50	I/O
3	IO_L16P_3	P49	I/O
3	IP	P6	INPUT
3	IP	P14	INPUT
3	IP	P26	INPUT
3	IP	P32	INPUT
3	IP	P43	INPUT
3	IP	P51	INPUT
3	IP/VREF_3	P20	VREF
3	VCCO_3	P21	VCCO
3	VCCO_3	P38	VCCO
3	VCCO_3	P46	VCCO
GND	GND	P10	GND
GND	GND	P17	GND
GND	GND	P27	GND
GND	GND	P37	GND
GND	GND	P52	GND
GND	GND	P53	GND
GND	GND	P70	GND
GND	GND	P79	GND
GND	GND	P85	GND
GND	GND	P95	GND
GND	GND	P105	GND
GND	GND	P121	GND
GND	GND	P131	GND
GND	GND	P141	GND
GND	GND	P156	GND
GND	GND	P173	GND
GND	GND	P182	GND
GND	GND	P188	GND
GND	GND	P198	GND
GND	GND	P208	GND
VCCAUX	DONE	P104	CONFIG
VCCAUX	PROG_B	P1	CONFIG
VCCAUX	TCK	P158	JTAG
VCCAUX	TDI	P207	JTAG
VCCAUX	TDO	P157	JTAG
VCCAUX	TMS	P155	JTAG
VCCAUX	VCCAUX	P7	VCCAUX
VCCAUX	VCCAUX	P44	VCCAUX

Table 141: **PQ208 Package Pinout *(Cont'd)***

Bank	XC3S250E XC3S500E Pin Name	PQ208 Pin	Type
VCCAUX	VCCAUX	P66	VCCAUX
VCCAUX	VCCAUX	P92	VCCAUX
VCCAUX	VCCAUX	P111	VCCAUX
VCCAUX	VCCAUX	P149	VCCAUX
VCCAUX	VCCAUX	P166	VCCAUX
VCCAUX	VCCAUX	P195	VCCAUX
VCCINT	VCCINT	P13	VCCINT
VCCINT	VCCINT	P67	VCCINT
VCCINT	VCCINT	P117	VCCINT
VCCINT	VCCINT	P170	VCCINT

PQ208 Footprint (Right)

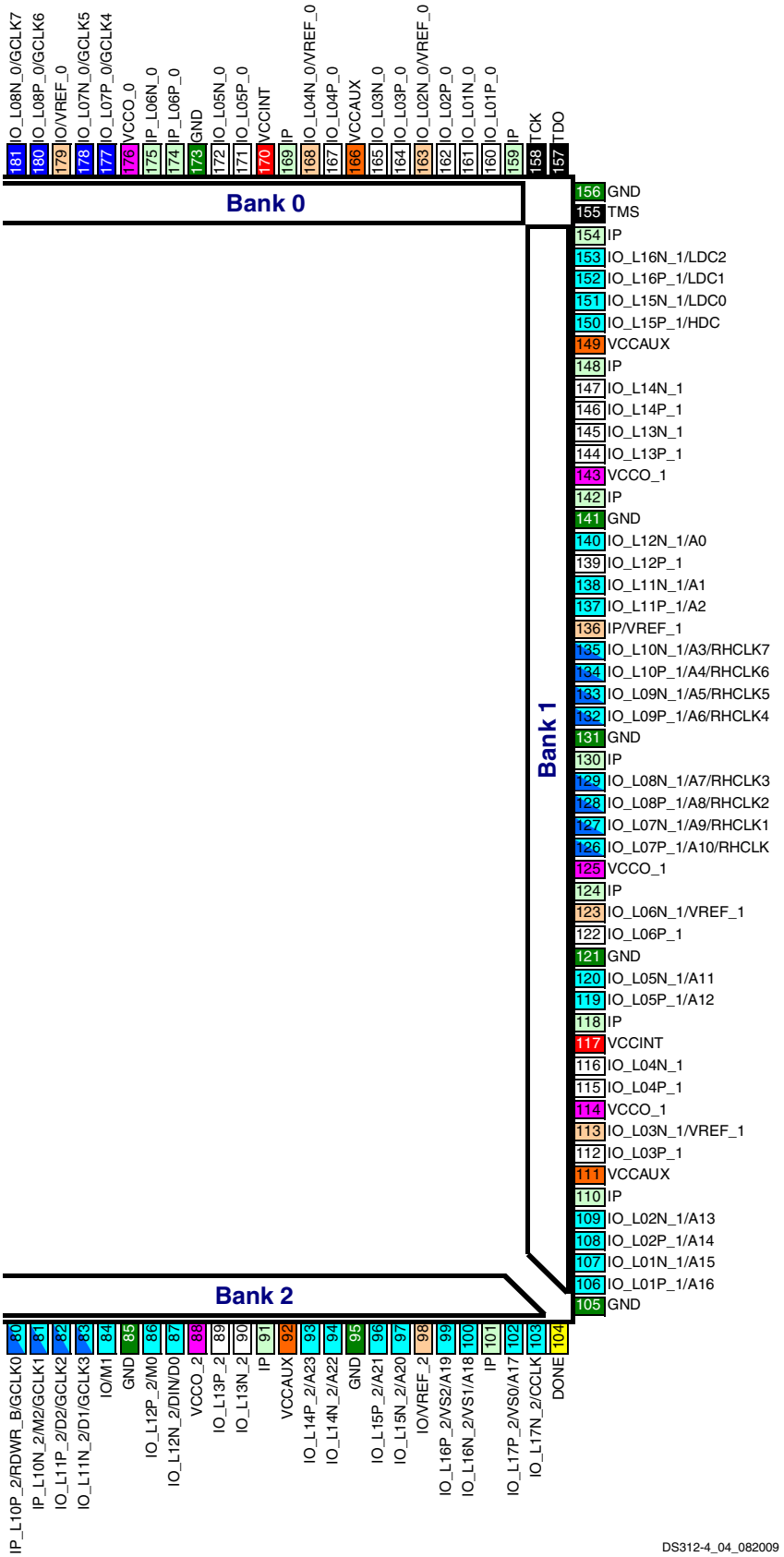

Figure 84: **PQ208 Footprint (Right)**

Table 148: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S500E Pin Name	XC3S1200E Pin Name	XC3S1600E Pin Name	FG320 Ball	Type
0	VCCO_0	VCCO_0	VCCO_0	A9	VCCO
0	VCCO_0	VCCO_0	VCCO_0	C6	VCCO
0	VCCO_0	VCCO_0	VCCO_0	C13	VCCO
0	VCCO_0	VCCO_0	VCCO_0	G8	VCCO
0	VCCO_0	VCCO_0	VCCO_0	G11	VCCO
1	N.C. (◆)	IO	IO	P16	**500E:** N.C. **1200E:** I/O **1600E:** I/O
1	IO_L01N_1/A15	IO_L01N_1/A15	IO_L01N_1/A15	T17	DUAL
1	IO_L01P_1/A16	IO_L01P_1/A16	IO_L01P_1/A16	U18	DUAL
1	IO_L02N_1/A13	IO_L02N_1/A13	IO_L02N_1/A13	T18	DUAL
1	IO_L02P_1/A14	IO_L02P_1/A14	IO_L02P_1/A14	R18	DUAL
1	IO_L03N_1/VREF_1	IO_L03N_1/VREF_1	IO_L03N_1/VREF_1	R16	VREF
1	IO_L03P_1	IO_L03P_1	IO_L03P_1	R15	I/O
1	N.C. (◆)	IO_L04N_1	IO_L04N_1	N14	**500E:** N.C. **1200E:** I/O **1600E:** I/O
1	N.C. (◆)	IO_L04P_1	IO_L04P_1	N15	**500E:** N.C. **1200E:** I/O **1600E:** I/O
1	IO_L05N_1/VREF_1	IO_L05N_1/VREF_1	IO_L05N_1/VREF_1	M13	VREF
1	IO_L05P_1	IO_L05P_1	IO_L05P_1	M14	I/O
1	IO_L06N_1	IO_L06N_1	IO_L06N_1	P18	I/O
1	IO_L06P_1	IO_L06P_1	IO_L06P_1	P17	I/O
1	IO_L07N_1	IO_L07N_1	IO_L07N_1	M16	I/O
1	IO_L07P_1	IO_L07P_1	IO_L07P_1	M15	I/O
1	IO_L08N_1	IO_L08N_1	IO_L08N_1	M18	I/O
1	IO_L08P_1	IO_L08P_1	IO_L08P_1	N18	I/O
1	IO_L09N_1/A11	IO_L09N_1/A11	IO_L09N_1/A11	L15	DUAL
1	IO_L09P_1/A12	IO_L09P_1/A12	IO_L09P_1/A12	L16	DUAL
1	IO_L10N_1/VREF_1	IO_L10N_1/VREF_1	IO_L10N_1/VREF_1	L17	VREF
1	IO_L10P_1	IO_L10P_1	IO_L10P_1	L18	I/O
1	IO_L11N_1/A9/RHCLK1	IO_L11N_1/A9/RHCLK1	IO_L11N_1/A9/RHCLK1	K12	RHCLK/DUAL
1	IO_L11P_1/A10/RHCLK0	IO_L11P_1/A10/RHCLK0	IO_L11P_1/A10/RHCLK0	K13	RHCLK/DUAL
1	IO_L12N_1/A7/RHCLK3/ TRDY1	IO_L12N_1/A7/RHCLK3/ TRDY1	IO_L12N_1/A7/RHCLK3/ TRDY1	K14	RHCLK/DUAL
1	IO_L12P_1/A8/RHCLK2	IO_L12P_1/A8/RHCLK2	IO_L12P_1/A8/RHCLK2	K15	RHCLK/DUAL
1	IO_L13N_1/A5/RHCLK5	IO_L13N_1/A5/RHCLK5	IO_L13N_1/A5/RHCLK5	J16	RHCLK/DUAL
1	IO_L13P_1/A6/RHCLK4/ IRDY1	IO_L13P_1/A6/RHCLK4/ IRDY1	IO_L13P_1/A6/RHCLK4/ IRDY1	J17	RHCLK/DUAL
1	IO_L14N_1/A3/RHCLK7	IO_L14N_1/A3/RHCLK7	IO_L14N_1/A3/RHCLK7	J14	RHCLK/DUAL
1	IO_L14P_1/A4/RHCLK6	IO_L14P_1/A4/RHCLK6	IO_L14P_1/A4/RHCLK6	J15	RHCLK/DUAL
1	IO_L15N_1/A1	IO_L15N_1/A1	IO_L15N_1/A1	J13	DUAL
1	IO_L15P_1/A2	IO_L15P_1/A2	IO_L15P_1/A2	J12	DUAL
1	IO_L16N_1/A0	IO_L16N_1/A0	IO_L16N_1/A0	H17	DUAL
1	IO_L16P_1	IO_L16P_1	IO_L16P_1	H16	I/O

Table 152: **FG400 Package Pinout *(Cont'd)***

Bank	XC3S1200E XC3S1600E Pin Name	FG400 Ball	Type
1	IP	L18	INPUT
1	IP	M20	INPUT
1	IP	N14	INPUT
1	IP	N20	INPUT
1	IP	P15	INPUT
1	IP	R16	INPUT
1	IP	R19	INPUT
1	IP/VREF_1	E19	VREF
1	IP/VREF_1	K18	VREF
1	VCCO_1	D19	VCCO
1	VCCO_1	G17	VCCO
1	VCCO_1	K15	VCCO
1	VCCO_1	K19	VCCO
1	VCCO_1	N17	VCCO
1	VCCO_1	T19	VCCO
2	IO	P8	I/O
2	IO	P13	I/O
2	IO	R9	I/O
2	IO	R13	I/O
2	IO	W15	I/O
2	IO	Y5	I/O
2	IO	Y7	I/O
2	IO	Y13	I/O
2	IO/D5	N11	DUAL
2	IO/M1	T11	DUAL
2	IO/VREF_2	Y3	VREF
2	IO/VREF_2	Y17	VREF
2	IO_L01N_2/INIT_B	V4	DUAL
2	IO_L01P_2/CSO_B	U4	DUAL
2	IO_L03N_2/MOSI/CSI_B	V5	DUAL
2	IO_L03P_2/DOUT/BUSY	U5	DUAL
2	IO_L04N_2	Y4	I/O
2	IO_L04P_2	W4	I/O
2	IO_L06N_2	T6	I/O
2	IO_L06P_2	T5	I/O
2	IO_L07N_2	U7	I/O
2	IO_L07P_2	V7	I/O
2	IO_L09N_2/VREF_2	R7	VREF
2	IO_L09P_2	T7	I/O
2	IO_L10N_2	V8	I/O
2	IO_L10P_2	W8	I/O
2	IO_L12N_2	U9	I/O
2	IO_L12P_2	V9	I/O

Table 152: **FG400 Package Pinout *(Cont'd)***

Bank	XC3S1200E XC3S1600E Pin Name	FG400 Ball	Type
2	IO_L13N_2	Y8	I/O
2	IO_L13P_2	Y9	I/O
2	IO_L15N_2/D6/GCLK13	W10	DUAL/ GCLK
2	IO_L15P_2/D7/GCLK12	W9	DUAL/ GCLK
2	IO_L16N_2/D3/GCLK15	P10	DUAL/ GCLK
2	IO_L16P_2/D4/GCLK14	R10	DUAL/ GCLK
2	IO_L18N_2/D1/GCLK3	V11	DUAL/ GCLK
2	IO_L18P_2/D2/GCLK2	V10	DUAL/ GCLK
2	IO_L19N_2/DIN/D0	Y12	DUAL
2	IO_L19P_2/M0	Y11	DUAL
2	IO_L21N_2	U12	I/O
2	IO_L21P_2	V12	I/O
2	IO_L22N_2/VREF_2	W12	VREF
2	IO_L22P_2	W13	I/O
2	IO_L24N_2	U13	I/O
2	IO_L24P_2	V13	I/O
2	IO_L25N_2	P14	I/O
2	IO_L25P_2	R14	I/O
2	IO_L27N_2/A22	Y14	DUAL
2	IO_L27P_2/A23	Y15	DUAL
2	IO_L28N_2	T15	I/O
2	IO_L28P_2	U15	I/O
2	IO_L30N_2/A20	V16	DUAL
2	IO_L30P_2/A21	U16	DUAL
2	IO_L31N_2/VS1/A18	Y18	DUAL
2	IO_L31P_2/VS2/A19	W18	DUAL
2	IO_L32N_2/CCLK	W19	DUAL
2	IO_L32P_2/VS0/A17	Y19	DUAL
2	IP	T16	INPUT
2	IP	W3	INPUT
2	IP_L02N_2	Y2	INPUT
2	IP_L02P_2	W2	INPUT
2	IP_L05N_2	V6	INPUT
2	IP_L05P_2	U6	INPUT
2	IP_L08N_2	Y6	INPUT
2	IP_L08P_2	W6	INPUT
2	IP_L11N_2	R8	INPUT
2	IP_L11P_2	T8	INPUT
2	IP_L14N_2/VREF_2	T10	VREF

Table 154: **FG484 Package Pinout *(Cont'd)***

Bank	XC3S1600E Pin Name	FG484 Ball	Type
GND	GND	E10	GND
GND	GND	E13	GND
GND	GND	F6	GND
GND	GND	F17	GND
GND	GND	G2	GND
GND	GND	G21	GND
GND	GND	J4	GND
GND	GND	J9	GND
GND	GND	J12	GND
GND	GND	J14	GND
GND	GND	J19	GND
GND	GND	K10	GND
GND	GND	K12	GND
GND	GND	L2	GND
GND	GND	L6	GND
GND	GND	L9	GND
GND	GND	L13	GND
GND	GND	M10	GND
GND	GND	M14	GND
GND	GND	M17	GND
GND	GND	M21	GND
GND	GND	N11	GND
GND	GND	N13	GND
GND	GND	P4	GND
GND	GND	P9	GND
GND	GND	P11	GND
GND	GND	P14	GND
GND	GND	P19	GND
GND	GND	T2	GND
GND	GND	T21	GND
GND	GND	U6	GND
GND	GND	U17	GND
GND	GND	V10	GND
GND	GND	V13	GND
GND	GND	Y3	GND
GND	GND	Y20	GND
GND	GND	AA7	GND
GND	GND	AA16	GND

Table 154: **FG484 Package Pinout *(Cont'd)***

Bank	XC3S1600E Pin Name	FG484 Ball	Type
GND	GND	AB1	GND
GND	GND	AB12	GND
GND	GND	AB22	GND
VCCAUX	DONE	AA21	CONFIG
VCCAUX	PROG_B	B1	CONFIG
VCCAUX	TCK	E17	JTAG
VCCAUX	TDI	B2	JTAG
VCCAUX	TDO	B20	JTAG
VCCAUX	TMS	D19	JTAG
VCCAUX	VCCAUX	D12	VCCAUX
VCCAUX	VCCAUX	E5	VCCAUX
VCCAUX	VCCAUX	E18	VCCAUX
VCCAUX	VCCAUX	K14	VCCAUX
VCCAUX	VCCAUX	L4	VCCAUX
VCCAUX	VCCAUX	M19	VCCAUX
VCCAUX	VCCAUX	N9	VCCAUX
VCCAUX	VCCAUX	V5	VCCAUX
VCCAUX	VCCAUX	V18	VCCAUX
VCCAUX	VCCAUX	W11	VCCAUX
VCCINT	VCCINT	J10	VCCINT
VCCINT	VCCINT	K9	VCCINT
VCCINT	VCCINT	K11	VCCINT
VCCINT	VCCINT	K13	VCCINT
VCCINT	VCCINT	L10	VCCINT
VCCINT	VCCINT	L11	VCCINT
VCCINT	VCCINT	L12	VCCINT
VCCINT	VCCINT	L14	VCCINT
VCCINT	VCCINT	M9	VCCINT
VCCINT	VCCINT	M11	VCCINT
VCCINT	VCCINT	M12	VCCINT
VCCINT	VCCINT	M13	VCCINT
VCCINT	VCCINT	N10	VCCINT
VCCINT	VCCINT	N12	VCCINT
VCCINT	VCCINT	N14	VCCINT
VCCINT	VCCINT	P13	VCCINT

User I/Os by Bank

Table 155 indicates how the 304 available user-I/O pins are distributed between the four I/O banks on the FG484 package.