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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	612
Number of Logic Elements/Cells	5508
Total RAM Bits	221184
Number of I/O	108
Number of Gates	250000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s250e-4tqg144i

Storage Element Functions

There are three pairs of storage elements in each IOB, one pair for each of the three paths. It is possible to configure each of these storage elements as an edge-triggered D-type flip-flop (FD) or a level-sensitive latch (LD).

The storage-element pair on either the Output path or the Three-State path can be used together with a special multiplexer to produce Double-Data-Rate (DDR) transmission. This is accomplished by taking data synchronized to the clock signal's rising edge and converting it to bits synchronized on both the rising and the falling edge. The combination of two registers and a multiplexer is referred to as a Double-Data-Rate D-type flip-flop (ODDR2).

Table 4 describes the signal paths associated with the storage element.

Table 4: **Storage Element Signal Description**

Storage Element Signal	Description	Function
D	Data input	Data at this input is stored on the active edge of CK and enabled by CE. For latch operation when the input is enabled, data passes directly to the output Q.
Q	Data output	The data on this output reflects the state of the storage element. For operation as a latch in transparent mode, Q mirrors the data at D.
CK	Clock input	Data is loaded into the storage element on this input's active edge with CE asserted.
CE	Clock Enable input	When asserted, this input enables CK. If not connected, CE defaults to the asserted state.
SR	Set/Reset input	This input forces the storage element into the state specified by the SRHIGH/SRLOW attributes. The SYNC/ASYNC attribute setting determines if the SR input is synchronized to the clock or not. If both SR and REV are active at the same time, the storage element gets a value of 0.
REV	Reverse input	This input is used together with SR. It forces the storage element into the state opposite from what SR does. The SYNC/ASYNC attribute setting determines whether the REV input is synchronized to the clock or not. If both SR and REV are active at the same time, the storage element gets a value of 0.

As shown in Figure 5, the upper registers in both the output and three-state paths share a common clock. The OTCLK1 clock signal drives the CK clock inputs of the upper registers on the output and three-state paths. Similarly, OTCLK2 drives the CK inputs for the lower registers on the output and three-state paths. The upper and lower registers on the input path have independent clock lines: ICLK1 and ICLK2.

The OCE enable line controls the CE inputs of the upper and lower registers on the output path. Similarly, TCE controls the CE inputs for the register pair on the three-state path and ICE does the same for the register pair on the input path.

The Set/Reset (SR) line entering the IOB controls all six registers, as is the Reverse (REV) line.

In addition to the signal polarity controls described in IOB Overview, each storage element additionally supports the controls described in Table 5.

Table 5: **Storage Element Options**

Option Switch	Function	Specificity
FF/Latch	Chooses between an edge-triggered flip-flop or a level-sensitive latch	Independent for each storage element
SYNC/ASYNC	Determines whether the SR set/reset control is synchronous or asynchronous	Independent for each storage element
SRHIGH/SRLOW	Determines whether SR acts as a Set, which forces the storage element to a logic 1 (SRHIGH) or a Reset, which forces a logic 0 (SRLOW)	Independent for each storage element, except when using ODDR2. In the latter case, the selection for the upper element will apply to both elements.
INIT1/INIT0	When Global Set/Reset (GSR) is asserted or after configuration this option specifies the initial state of the storage element, either set (INIT1) or reset (INIT0). By default, choosing SRLOW also selects INIT0; choosing SRHIGH also selects INIT1.	Independent for each storage element, except when using ODDR2, which uses two IOBs. In the ODDR2 case, selecting INIT0 for one IOBs applies to both elements within the IOB, although INIT1 could be selected for the elements in the other IOB.

Dedicated Multipliers

For additional information, refer to the “Using Embedded Multipliers” chapter in UG331.

The Spartan-3E devices provide 4 to 36 dedicated multiplier blocks per device. The multipliers are located together with the block RAM in one or two columns depending on device density. See Arrangement of RAM Blocks on Die for details on the location of these blocks and their connectivity.

Operation

The multiplier blocks primarily perform two’s complement numerical multiplication but can also perform some less obvious applications, such as simple data storage and barrel shifting. Logic slices also implement efficient small multipliers and thereby supplement the dedicated multipliers. The Spartan-3E dedicated multiplier blocks have additional features beyond those provided in Spartan-3 FPGAs.

Each multiplier performs the principle operation P = A × B, where ‘A’ and ‘B’ are 18-bit words in two’s complement form, and ‘P’ is the full-precision 36-bit product, also in two’s complement form. The 18-bit inputs represent values ranging from $-131,072_{10}$ to $+131,071_{10}$ with a resulting product ranging from $-17,179,738,112_{10}$ to $+17,179,869,184_{10}$.

Implement multipliers with inputs less than 18 bits by sign-extending the inputs (i.e., replicating the most-significant bit). Wider multiplication operations are performed by combining the dedicated multipliers and slice-based logic in any viable combination or by time-sharing a single multiplier. Perform unsigned multiplication by restricting the inputs to the positive range. Tie the most-significant bit Low and represent the unsigned value in the remaining 17 lesser-significant bits.

Optional Pipeline Registers

As shown in Figure 36, each multiplier block has optional registers on each of the multiplier inputs and the output. The registers are named AREG, BREG, and PREG and can be used in any combination. The clock input is common to all the registers within a block, but each register has an independent clock enable and synchronous reset controls making them ideal for storing data samples and coefficients. When used for pipelining, the registers boost the multiplier clock rate, beneficial for higher performance applications.

Figure 36 illustrates the principle features of the multiplier block.

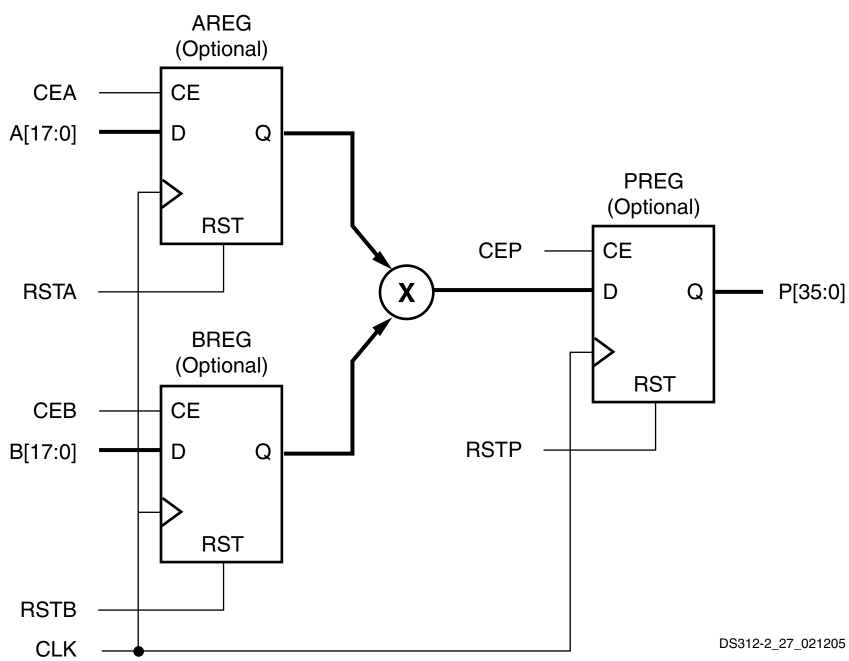

Figure 36: **Principle Ports and Functions of Dedicated Multiplier Blocks**

Use the MULT18X18SIO primitive shown in Figure 37 to instantiate a multiplier within a design. Although high-level logic synthesis software usually automatically infers a multiplier, adding the pipeline registers might require the MULT18X18SIO primitive. Connect the appropriate signals to the MULT18X18SIO multiplier ports and set the individual AREG, BREG, and PREG attributes to ‘1’ to insert the associated register, or to 0 to remove it and make the signal path combinatorial.

VARIABLE Phase Shift Mode

In VARIABLE phase shift mode, the FPGA application dynamically adjusts the fine phase shift value using three inputs to the PS unit (PSEN, PSCLK, and PSINCDEC), as defined in Table 36 and shown in Figure 40.

Table 36: **Signals for Variable Phase Mode**

Signal	Direction	Description
PSEN(1)	Input	Enables the Phase Shift unit for variable phase adjustment.
PSCLK(1)	Input	Clock to synchronize phase shift adjustment.
PSINCDEC(1)	Input	When High, increments the current phase shift value. When Low, decrements the current phase shift value. This signal is synchronized to the PSCLK signal.
PSDONE	Output	Goes High to indicate that the present phase adjustment is complete and PS unit is ready for next phase adjustment request. This signal is synchronized to the PSCLK signal.

Notes:

1. This input supports either a true or inverted polarity.

The FPGA application uses the three PS inputs on the Phase Shift unit to dynamically and incrementally increase or decrease the phase shift amount on all nine DCM clock outputs.

To adjust the current phase shift value, the PSEN enable signal must be High to enable the PS unit. Coincidently, PSINCDEC must be High to increment the current phase shift amount or Low to decrement the current amount. All VARIABLE phase shift operations are controlled by the PSCLK input, which can be the CLKIN signal or any other clock signal.

Design Note

The VARIABLE phase shift feature operates differently from the Spartan-3 DCM; use the DCM_SP primitive, not the DCM primitive.

DCM_DELAY_STEP

DCM_DELAY_STEP is the finest delay resolution available in the PS unit. Its value is provided at the bottom of Table 105 in Module 3. For each enabled PSCLK cycle that PSINCDEC is High, the PS unit adds one DCM_ DELAY_STEP of phase shift to all nine DCM outputs. Similarly, for each enabled PSCLK cycle that PSINCDEC is Low, the PS unit subtracts one DCM_ DELAY_STEP of phase shift from all nine DCM outputs.

Because each DCM_DELAY_STEP has a minimum and maximum value, the actual phase shift delay for the present phase increment/decrement value (VALUE) falls within the minimum and maximum values according to Equation 4 and Equation 5.

$$T_{PS}(Max) = VALUE \bullet \text{DCM\_DELAY\_STEP\_MAX} \quad \textit{Eq 4}$$

$$T_{PS}(Min) = VALUE \bullet \text{DCM\_DELAY\_STEP\_MIN} \quad \textit{Eq 5}$$

The maximum variable phase shift steps, MAX_STEPS, is described in Equation 6 or Equation 7, for a given CLKIN input period, T_{CLKIN}, in nanoseconds. To convert this to a phase shift range measured in time and not steps, use MAX_STEPS derived in Equation 6 and Equation 7 for VALUE in Equation 4 and Equation 5.

If CLKIN < 60 MHz:

$$\text{MAX\_STEPS} = \pm[INTEGER(10 \bullet (T_{CLKIN} - 3))] \quad \textit{Eq 6}$$

If CLKIN ≥ 60 MHz:

$$\text{MAX\_STEPS} = \pm[INTEGER(15 \bullet (T_{CLKIN} - 3))] \quad \textit{Eq 7}$$

The phase adjustment might require as many as 100 CLKIN cycles plus 3 PSCLK cycles to take effect, at which point the DCM's PSDONE output goes High for one PSCLK cycle. This pulse indicates that the PS unit completed the previous adjustment and is now ready for the next request.

Asserting the Reset (RST) input returns the phase shift to zero.

By contrast, the clock switch matrixes on the top and bottom edges receive signals from any of the five following sources: two GCLK pins, two DCM outputs, or one Double-Line interconnect.

Table 41 indicates permissible connections between clock inputs and BUFGMUX elements. The I0-input provides the best input path to a clock buffer. The I1-input provides the secondary input for the clock multiplexer function.

The four BUFGMUX elements on the top edge are paired together and share inputs from the eight global clock inputs along the top edge. Each BUFGMUX pair connects to four of the eight global clock inputs, as shown in Figure 45. This optionally allows differential inputs to the global clock inputs without wasting a BUFGMUX element.

Table 41: **Connections from Clock Inputs to BUFGMUX Elements and Associated Quadrant Clock**

Quadrant Clock Line(1)	Left-Half BUFGMUX			Top or Bottom BUFGMUX			Right-Half BUFGMUX		
	Location(2)	I0 Input	I1 Input	Location(2)	I0 Input	I1 Input	Location(2)	I0 Input	I1 Input
H	*X0Y9*	LHCLK7	LHCLK6	*X1Y10*	GCLK7 or GCLK11	GCLK6 or GCLK10	*X3Y9*	RHCLK3	RHCLK2
G	*X0Y8*	LHCLK6	LHCLK7	*X1Y11*	GCLK6 or GCLK10	GCLK7 or GCLK11	*X3Y8*	RHCLK2	RHCLK3
F	*X0Y7*	LHCLK5	LHCLK4	*X2Y10*	GCLK5 or GCLK9	GCLK4 or GCLK8	*X3Y7*	RHCLK1	RHCLK0
E	*X0Y6*	LHCLK4	LHCLK5	*X2Y11*	GCLK4 or GCLK8	GCLK5 or GCLK9	*X3Y6*	RHCLK0	RHCLK1
D	*X0Y5*	LHCLK3	LHCLK2	*X1Y0*	GCLK3 or GCLK15	GCLK2 or GCLK14	*X3Y5*	RHCLK7	RHCLK6
C	*X0Y4*	LHCLK2	LHCLK3	*X1Y1*	GCLK2 or GCLK14	GCLK3 or GCLK15	*X3Y4*	RHCLK6	RHCLK7
B	*X0Y3*	LHCLK1	LHCLK0	*X2Y0*	GCLK1 or GCLK13	GCLK0 or GCLK12	*X3Y3*	RHCLK5	RHCLK4
A	*X0Y2*	LHCLK0	LHCLK1	*X2Y1*	GCLK0 or GCLK12	GCLK1 or GCLK13	*X3Y2*	RHCLK4	RHCLK5

Notes:
1. See Quadrant Clock Routing for connectivity details for the eight quadrant clocks.
2. See Figure 45 for specific BUFGMUX locations, and Figure 47 for information on how BUFGMUX elements drive onto a specific clock line within a quadrant.

Table 46: **Pin Behavior during Configuration *(Cont'd)***

Pin Name	Master Serial	SPI (Serial Flash)	BPI (Parallel NOR Flash)	JTAG	Slave Parallel	Slave Serial	I/O Bank(3)
D0/DIN	DIN	DIN	D0		D0	DIN	2
RDWR_B			RDWR_B		RDWR_B		2
A23			A23				2
A22			A22				2
A21			A21				2
A20			A20				2
A19/VS2		VS2	A19				2
A18/VS1		VS1	A18				2
A17/VS0		VS0	A17				2
A16			A16				1
A15			A15				1
A14			A14				1
A13			A13				1
A12			A12				1
A11			A11				1
A10			A10				1
A9			A9				1
A8			A8				1
A7			A7				1
A6			A6				1
A5			A5				1
A4			A4				1
A3			A3				1
A2			A2				1
A1			A1				1
A0			A0				1
LDC0			LDC0				1
LDC1			LDC1				1
LDC2			LDC2				1
HDC			HDC				1

Notes:
1. Gray shaded cells represent pins that are in a high-impedance state (Hi-Z, floating) during configuration. These pins have an optional internal pull-up resistor to their respective V_{CCO} supply pin that is active throughout configuration if the HSWAP input is Low.
2. Yellow shaded cells represent pins with an internal pull-up resistor to its respective voltage supply rail that is active during configuration, regardless of the HSWAP pin.
3. Note that dual-purpose outputs are supplied by V_{CCO}, and configuration inputs are supplied by V_{CCAUX}.

The HSWAP pin itself has a pull-up resistor enabled during configuration. However, the VCCO_0 supply voltage must be applied before the pull-up resistor becomes active. If the VCCO_0 supply ramps after the VCCO_2 power supply, do not let HSWAP float; tie HSWAP to the desired logic level externally.

Spartan-3E FPGAs have only six dedicated configuration pins, including the DONE and PROG_B pins, and the four JTAG boundary-scan pins: TDI, TDO, TMS, and TCK. All other configuration pins are dual-purpose I/O pins and are available to the FPGA application after the DONE pin goes High. See Start-Up for additional information.

Table 47 shows the default I/O standard setting for the various configuration pins during the configuration process. The configuration interface is designed primarily for 2.5V operation when the VCCO_2 (and VCCO_1 in BPI mode) connects to 2.5V.

Table 47: **Default I/O Standard Setting During Configuration (VCCO_2 = 2.5V)**

Pin(s)	I/O Standard	Output Drive	Slew Rate
All, including CCLK	LVCMOS25	8 mA	Slow

(W) Table 54 shows the connections between the SPI Flash PROM and the FPGA's SPI configuration interface. Each SPI Flash PROM vendor uses slightly different signal naming. The SPI Flash PROM's write protect and hold controls are not used by the FPGA during configuration. However, the $\overline{\text{HOLD}}$ pin must be High during the configuration process. The PROM's write protect input must be High in order to write or program the Flash memory.

Table 54: **Example SPI Flash PROM Connections and Pin Naming**

SPI Flash Pin	FPGA Connection	STMicro	NexFlash	Silicon Storage Technology	Atmel DataFlash
DATA_IN	MOSI	D	DI	SI	SI
DATA_OUT	DIN	Q	DO	SO	SO
$\overline{\text{SELECT}}$	CSO_B	$\overline{\text{S}}$	$\overline{\text{CS}}$	CE#	$\overline{\text{CS}}$
CLOCK	CCLK	C	CLK	SCK	SCK
$\overline{\text{WR\_PROTECT}}$ (W)	Not required for FPGA configuration. Must be High to program SPI Flash. Optional connection to FPGA user I/O after configuration.	$\overline{\text{W}}$	$\overline{\text{WP}}$	WP#	$\overline{\text{WP}}$
$\overline{\text{HOLD}}$ (see Figure 53)	Not required for FPGA configuration but must be High during configuration. Optional connection to FPGA user I/O after configuration. Not applicable to Atmel DataFlash.	$\overline{\text{HOLD}}$	$\overline{\text{HOLD}}$	HOLD#	N/A
$\overline{\text{RESET}}$ (see Figure 54)	Only applicable to Atmel DataFlash. Not required for FPGA configuration but must be High during configuration. Optional connection to FPGA user I/O after configuration. Do not connect to FPGA's PROG_B as this will prevent direct programming of the DataFlash.	N/A	N/A	N/A	$\overline{\text{RESET}}$
RDY/$\overline{\text{BUSY}}$ (see Figure 54)	Only applicable to Atmel DataFlash and only available on certain packages. Not required for FPGA configuration. Output from DataFlash PROM. Optional connection to FPGA user I/O after configuration.	N/A	N/A	N/A	RDY/$\overline{\text{BUSY}}$

The mode select pins, M[2:0], and the variant select pins, VS[2:0] are sampled when the FPGA's INIT_B output goes High and must be at defined logic levels during this time. After configuration, when the FPGA's DONE output goes High, these pins are all available as full-featured user-I/O pins.

(P) Similarly, the FPGA's HSWAP pin must be Low to enable pull-up resistors on all user-I/O pins or High to disable the pull-up resistors. The HSWAP control must remain at a constant logic level throughout FPGA configuration. After configuration, when the FPGA's DONE output goes High, the HSWAP pin is available as full-featured user-I/O pin and is powered by the VCCO_0 supply.

In a single-FPGA application, the FPGA's DOUT pin is not used but is actively driving during the configuration process.

Table 55: **Serial Peripheral Interface (SPI) Connections**

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
HSWAP (P)	Input	**User I/O Pull-Up Control**. When Low during configuration, enables pull-up resistors in all I/O pins to respective I/O bank V_{CCO} input. 0: Pull-ups during configuration 1: No pull-ups	Drive at valid logic level throughout configuration.	User I/O
M[2:0]	Input	**Mode Select**. Selects the FPGA configuration mode. See Design Considerations for the HSWAP, M[2:0], and VS[2:0] Pins.	M2 = 0, M1 = 0, M0 = 1. Sampled when INIT_B goes High.	User I/O

Daisy-Chaining

If the application requires multiple FPGAs with different configurations, then configure the FPGAs using a daisy chain, as shown in Figure 57. Daisy-chaining from a single SPI serial Flash PROM is supported in Stepping 1 devices. It is not supported in Stepping 0 devices. Use SPI Flash mode (M[2:0] = <0:0:1>) for the FPGA connected to the Platform Flash PROM and Slave Serial mode (M[2:0] = <1:1:1>) for all other FPGAs in the daisy-chain. After the master FPGA—the FPGA on the left in the diagram—finishes loading its configuration data from the SPI Flash PROM, the master device uses its DOUT output pin to supply data to the next device in the daisy-chain, on the falling CCLK edge.

Design Note

SPI mode daisy chains are supported only in Stepping 1 silicon versions.

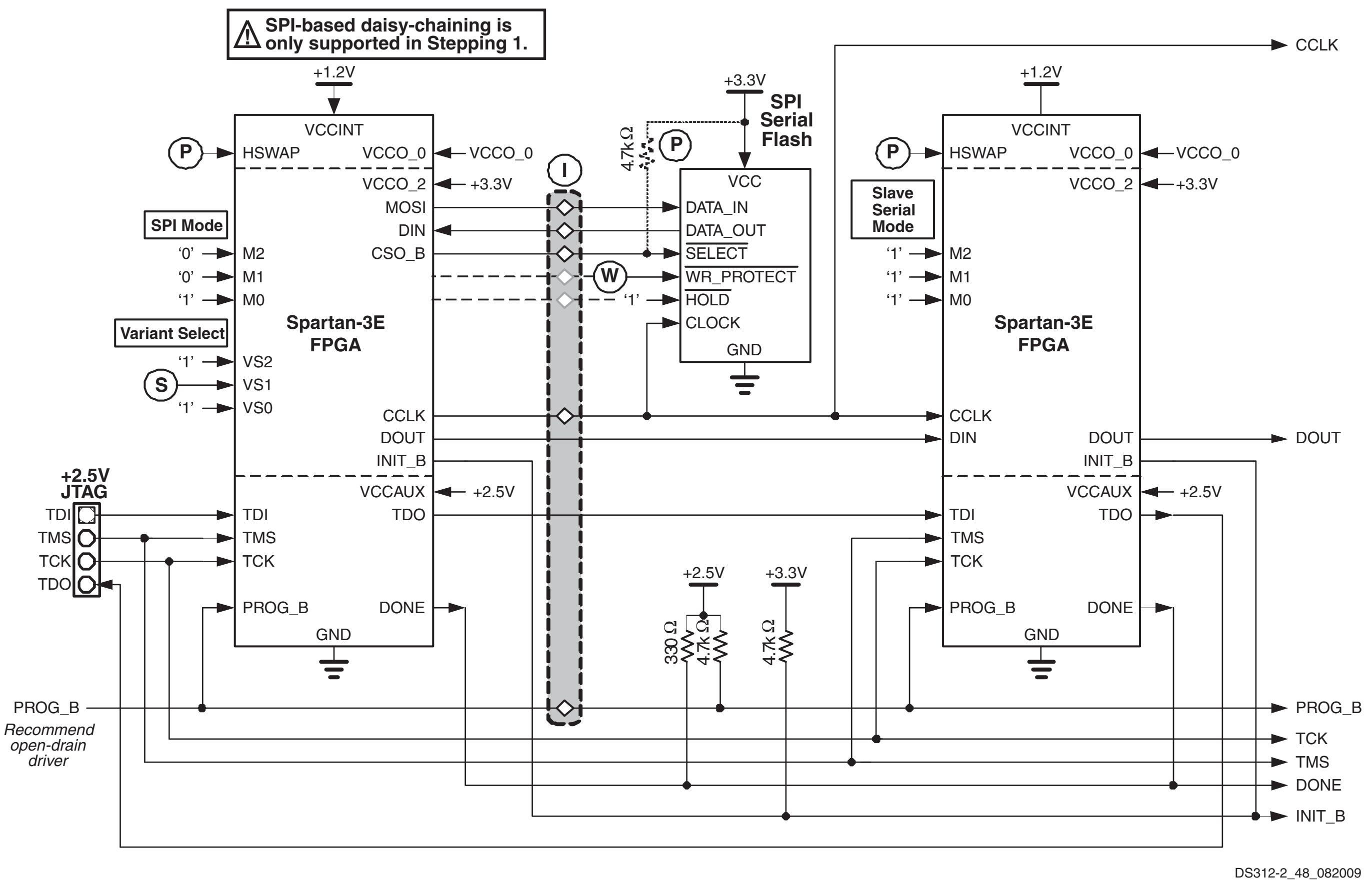

Figure 57: **Daisy-Chaining from SPI Flash Mode (Stepping 1)**

Programming Support

For successful daisy-chaining, the ***DONE_cycle*** configuration option must be set to cycle 5 or sooner. The default cycle is 4. See Table 69 and the Start-Up section for additional information.

(I) In production applications, the SPI Flash PROM is usually pre-programmed before it is mounted on the printed circuit board. The Xilinx ISE development software produces industry-standard programming files that can be used with third-party gang programmers. Consult your specific SPI Flash vendor for recommended production programming solutions.

In-system programming support is available from some third-party PROM programmers using a socket adapter with attached wires. To gain access to the SPI Flash signals, drive the FPGA's PROG_B input Low with an open-drain driver. This action places all FPGA I/O pins, including those attached to the SPI Flash, in high-impedance (Hi-Z). If the HSWAP input is Low, the I/Os have pull-up resistors to the V_{CCO} input on their respective I/O bank. The external programming hardware then has direct access to the SPI Flash pins. The programming access points are highlighted in the gray box in Figure 53, Figure 54, and Figure 57.

Beginning with the Xilinx ISE 8.2i software release, the iMPACT programming utility provides direct, in-system prototype programming support for STMicro M25P-series

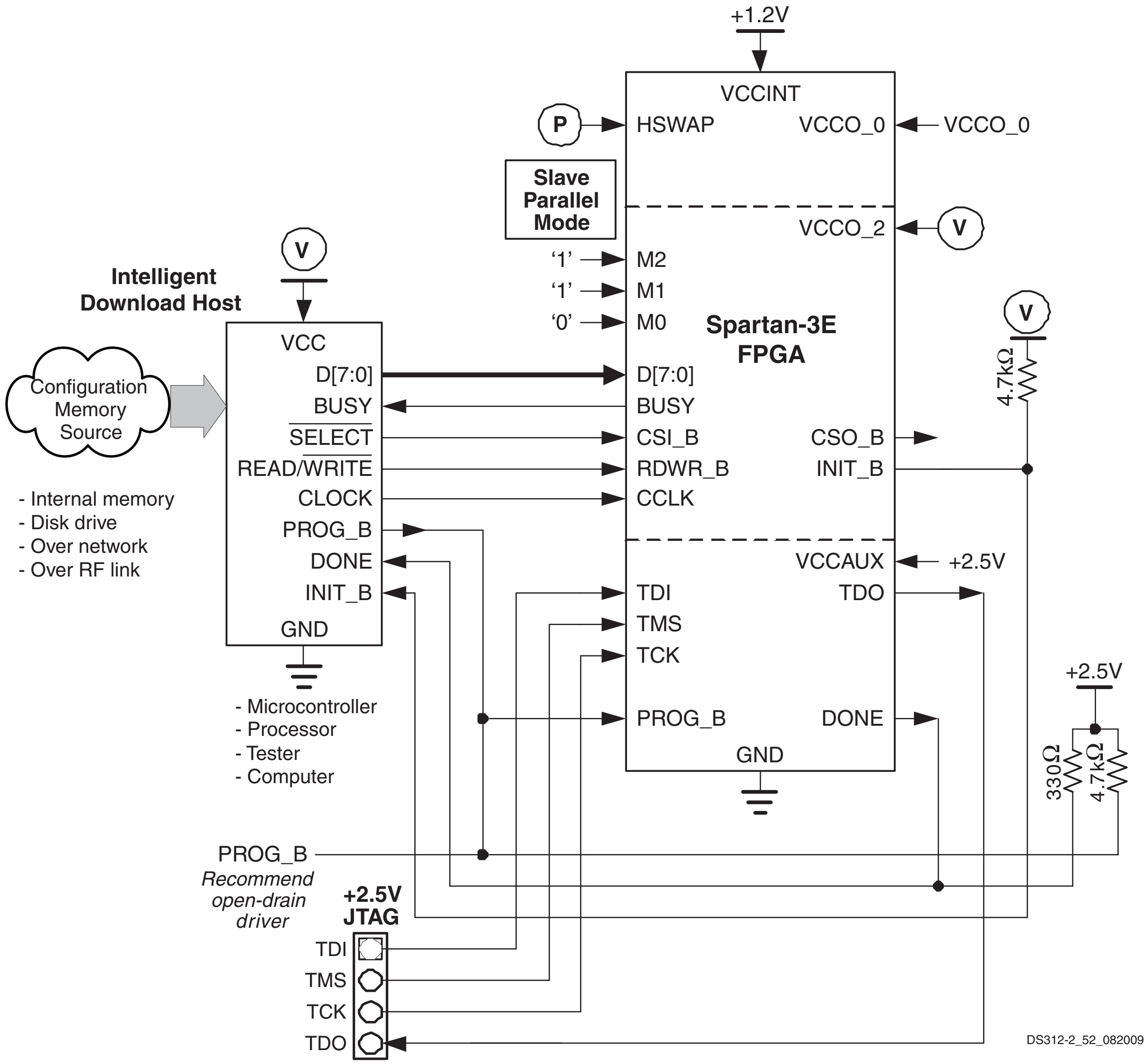

Figure 61: **Slave Parallel Configuration Mode**

Slave Parallel Mode

For additional information, refer to the “Slave Parallel (SelectMAP) Mode” chapter in UG332.

In Slave Parallel mode (M[2:0] = <1:1:0>), an external host, such as a microprocessor or microcontroller, writes byte-wide configuration data into the FPGA, using a typical peripheral interface as shown in Figure 61.

The external download host starts the configuration process by pulsing PROG_B and monitoring that the INIT_B pin goes High, indicating that the FPGA is ready to receive its first data. The host asserts the active-Low chip-select signal (CSI_B) and the active-Low Write signal (RDWR_B). The host then continues supplying data and clock signals until either the FPGA's DONE pin goes High, indicating a successful configuration, or until the FPGA's INIT_B pin goes Low, indicating a configuration error.

The FPGA captures data on the rising CCLK edge. If the CCLK frequency exceeds 50 MHz, then the host must also monitor the FPGA's BUSY output. If the FPGA asserts BUSY High, the host must hold the data for an additional clock cycle, until BUSY returns Low. If the CCLK frequency is 50 MHz or below, the BUSY pin may be ignored but actively drives during configuration.

The configuration process requires more clock cycles than indicated from the configuration file size. Additional clocks are required during the FPGA's start-up sequence, especially if the FPGA is programmed to wait for selected Digital Clock Managers (DCMs) to lock to their respective clock inputs (see Start-Up, page 105).

If the Slave Parallel interface is only used to configure the FPGA, never to read data back, then the RDWR_B signal

General Recommended Operating Conditions

Table 77: **General Recommended Operating Conditions**

Symbol	Description			Min	Nominal	Max	Units
T_J	Junction temperature	Commercial		0	–	85	°C
		Industrial		–40	–	100	°C
V_{CCINT}	Internal supply voltage			1.140	1.200	1.260	V
V_{CCO}[1]	Output driver supply voltage			1.100	-	3.465	V
V_{CCAUX}	Auxiliary supply voltage			2.375	2.500	2.625	V
V_{IN}[2,3]	Input voltage extremes to avoid turning on I/O protection diodes	I/O, Input-only, and Dual-Purpose pins [4]	IP or IO_#	–0.5	–	V_{CCO} + 0.5	V
			IO_Lxxy_#[5]	–0.5	–	V_{CCO} + 0.5	V
		Dedicated pins[6]		–0.5	–	V_{CCAUX} + 0.5	V
T_{IN}	Input signal transition time[7]			–	–	500	ns

Notes:

1. This V_{CCO} range spans the lowest and highest operating voltages for all supported I/O standards. Table 80 lists the recommended V_{CCO} range specific to each of the single-ended I/O standards, and Table 82 lists that specific to the differential standards.
2. Input voltages outside the recommended range require the I_{IK} input clamp diode rating is met and no more than 100 pins exceed the range simultaneously. Refer to Table 73.
3. See XAPP459: *Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins on Spartan-3 Families*.
4. Each of the User I/O and Dual-Purpose pins is associated with one of the four banks' V_{CCO} rails. Meeting the V_{IN} limit ensures that the internal diode junctions that exist between these pins and their associated V_{CCO} and GND rails do not turn on. The absolute maximum rating is provided in Table 73.
5. For single-ended signals that are placed on a differential-capable I/O, V_{IN} of –0.2V to –0.5V is supported but can cause increased leakage between the two pins. See *Parasitic Leakage* in UG331, *Spartan-3 Generation FPGA User Guide*.
6. All Dedicated pins (PROG_B, DONE, TCK, TDI, TDO, and TMS) draw power from the V_{CCAUX} rail (2.5V). Meeting the V_{IN} max limit ensures that the internal diode junctions that exist between each of these pins and the V_{CCAUX} and GND rails do not turn on.
7. Measured between 10% and 90% V_{CCO}. Follow Signal Integrity recommendations.

Table 107: **Switching Characteristics for the DFS**

Symbol	Description		Device	Speed Grade -5 Min	Speed Grade -5 Max	Speed Grade -4 Min	Speed Grade -4 Max	Units
Output Frequency Ranges								
CLKOUT_FREQ_FX_LF	Frequency for the CLKFX and CLKFX180 outputs, low frequencies	Stepping 0	XC3S100E XC3S250E XC3S500E XC3S1600E	N/A	N/A	5	90	MHz
CLKOUT_FREQ_FX_HF	Frequency for the CLKFX and CLKFX180 outputs, high frequencies					220	307	MHz
CLKOUT_FREQ_FX	Frequency for the CLKFX and CLKFX180 outputs	Stepping 0	XC3S1200E			5	307	MHz
		Stepping 1	All	5	333		311	MHz
Output Clock Jitter(2,3)								
CLKOUT_PER_JITT_FX	Period jitter at the CLKFX and CLKFX180 outputs.		All	Typ	Max	Typ	Max	
		CLKIN ≤ 20 MHz		Note 6				ps
		CLKIN > 20 MHz		±[1% of CLKFX period + 100]	±[1% of CLKFX period + 200]	±[1% of CLKFX period + 100]	±[1% of CLKFX period + 200]	ps
Duty Cycle(4,5)								
CLKOUT_DUTY_CYCLE_FX	Duty cycle precision for the CLKFX and CLKFX180 outputs, including the BUFGMUX and clock tree duty-cycle distortion		All	-	±[1% of CLKFX period + 400]	-	±[1% of CLKFX period + 400]	ps
Phase Alignment(5)								
CLKOUT_PHASE_FX	Phase offset between the DFS CLKFX output and the DLL CLK0 output when both the DFS and DLL are used		All	-	±200	-	±200	ps
CLKOUT_PHASE_FX180	Phase offset between the DFS CLKFX180 output and the DLL CLK0 output when both the DFS and DLL are used		All	-	±[1% of CLKFX period + 300]	-	±[1% of CLKFX period + 300]	ps
Lock Time								
LOCK_FX(2)	The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX and CLKFX180 signals are valid. If using both the DLL and the DFS, use the longer locking time.	5 MHz ≤ F_{CLKIN} ≤ 15 MHz	All	-	5	-	5	ms
		F_{CLKIN} > 15 MHz		-	450	-	450	µs

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 77 and Table 106.
2. For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
3. Maximum output jitter is characterized within a reasonable noise environment (150 ps input period jitter, 40 SSOs and 25% CLB switching). Output jitter strongly depends on the environment, including the number of SSOs, the output drive strength, CLB utilization, CLB switching activities, switching frequency, power supply and PCB design. The actual maximum output jitter depends on the system application.
4. The CLKFX and CLKFX180 outputs always have an approximate 50% duty cycle.
5. Some duty-cycle and alignment specifications include 1% of the CLKFX output period or 0.01 UI.

   Example: The data sheet specifies a maximum jitter of ±[1% of CLKFX period + 300]. Assume the CLKFX output frequency is 100 MHz. The equivalent CLKFX period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 300 ps] = ±400 ps.
6. Use the Spartan-3A Jitter Calculator (www.xilinx.com/support/documentation/data_sheets/s3a_jitter_calc.zip) to estimate DFS output jitter. Use the Clocking Wizard to determine jitter for a specific design.

Byte Peripheral Interface (BPI) Configuration Timing

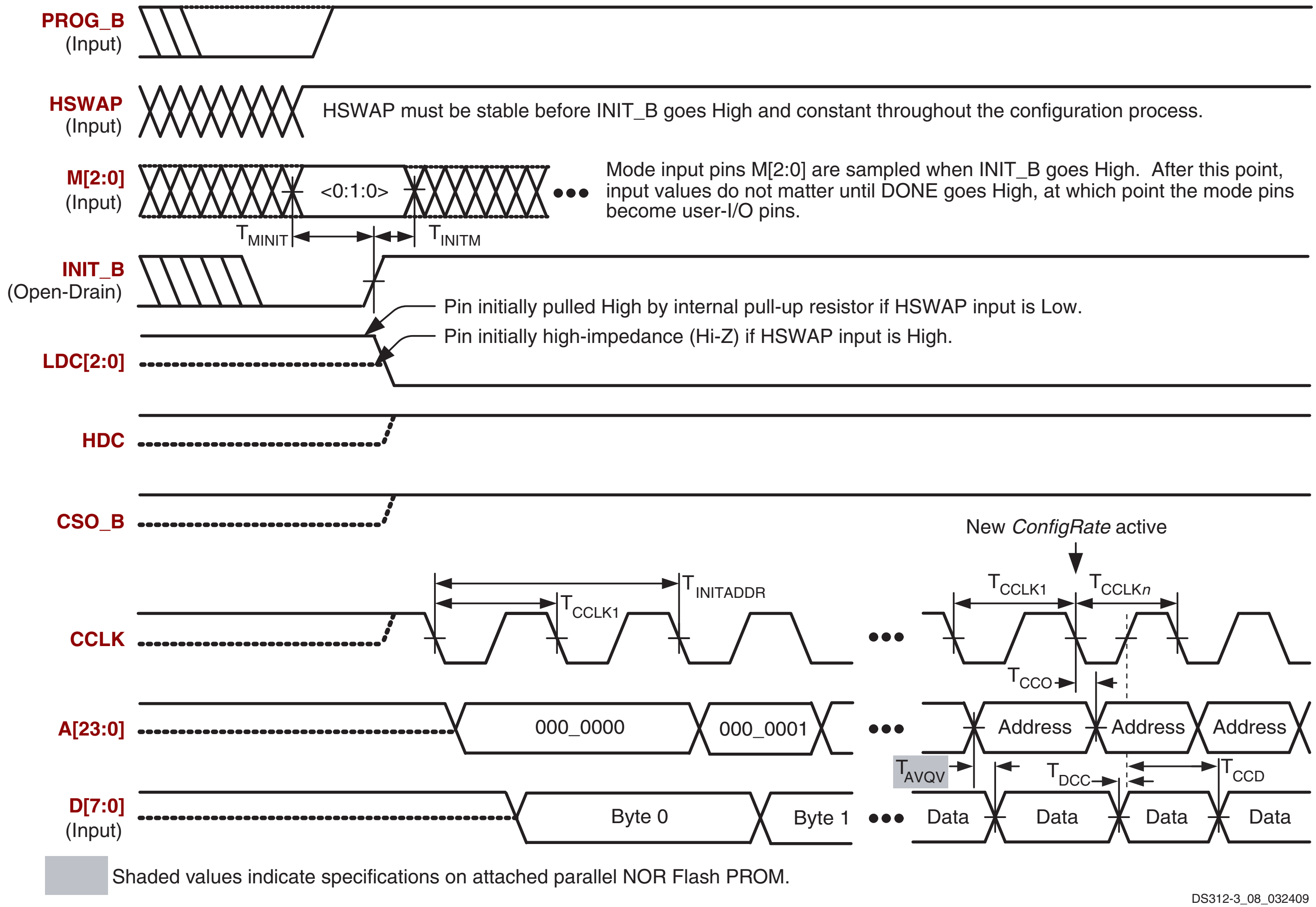

Figure 77: **Waveforms for Byte-wide Peripheral Interface (BPI) Configuration (BPI-DN mode shown)**

Table 120: **Timing for Byte-wide Peripheral Interface (BPI) Configuration Mode**

Symbol	Description		Minimum	Maximum	Units
T_{CCLK1}	Initial CCLK clock period		See Table 112		
T_{CCLKn}	CCLK clock period after FPGA loads ConfigRate setting		See Table 112		
T_{MINIT}	Setup time on CSI_B, RDWR_B, and M[2:0] mode pins before the rising edge of INIT_B		50	-	ns
T_{INITM}	Hold time on CSI_B, RDWR_B, and M[2:0] mode pins after the rising edge of INIT_B		0	-	ns
$T_{INITADDR}$	Minimum period of initial A[23:0] address cycle; LDC[2:0] and HDC are asserted and valid	BPI-UP: (M[2:0] = <0:1:0>)	5	5	T_{CCLK1} cycles
		BPI-DN: (M[2:0] = <0:1:1>)	2	2	
T_{CCO}	Address A[23:0] outputs valid after CCLK falling edge		See Table 116		
T_{DCC}	Setup time on D[7:0] data inputs before CCLK rising edge		See Table 116		
T_{CCD}	Hold time on D[7:0] data inputs after CCLK rising edge		See Table 116		

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/01/05	1.0	Initial Xilinx release.
11/23/05	2.0	Added AC timing information and additional DC specifications.
03/22/06	3.0	Upgraded data sheet status to Preliminary. Finalized production timing parameters. All speed grades for all Spartan-3E FPGAs are now Production status using the v1.21 speed files, as shown in Table 84. Expanded description in Note 2, Table 78. Updated pin-to-pin and clock-to-output timing based on final characterization, shown in Table 86. Updated system-synchronous input setup and hold times based on final characterization, shown in Table 87 and Table 88. Updated other I/O timing in Table 90. Provided input and output adjustments for LVPECL_25, DIFF_SSTL and DIFF_HSTL I/O standards that supersede the v1.21 speed file values, in Table 91 and Table 94. Reduced I/O three-state and set/reset delays in Table 93. Added XC3S100E FPGA in CP132 package to Table 96. Increased T_{AS} slice flip-flop timing by 100 ps in Table 98. Updated distributed RAM timing in Table 99 and SRL16 timing in Table 100. Updated global clock timing, removed left/right clock buffer limits in Table 101. Updated block RAM timing in Table 103. Added DCM parameters for remainder of Step 0 device; added improved Step 1 DCM performance to Table 104, Table 105, Table 106, and Table 107. Added minimum INIT_B pulse width specification, T_{INIT}, in Table 111. Increased data hold time for Slave Parallel mode to 1.0 ns (T_{SMCCD}) in Table 117. Improved the DCM performance for the XC3S1200E, Stepping 0 in Table 104, Table 105, Table 106, and Table 107. Corrected links in Table 118 and Table 120. Added MultiBoot timing specifications to Table 122.
04/07/06	3.1	Improved SSO limits for LVDS_25, MINI_LVDS_25, and RSDS_25 I/O standards in the QFP packages (Table 97). Removed potentially confusing Note 2 from Table 78.
05/19/06	3.2	Clarified that 100 mV of hysteresis applies to LVCMOS33 and LVCMOS25 I/O standards (Note 4, Table 80). Other minor edits.
05/30/06	3.2.1	Corrected various typos and incorrect links.
11/09/06	3.4	Improved absolute maximum voltage specifications in Table 73, providing additional overshoot allowance. Widened the recommended voltage range for PCI and PCI-X standards in Table 80. Clarified Note 2, Table 83. Improved various timing specifications for v1.26 speed file. Added Table 85 to summarize the history of speed file releases after which time all devices became Production status. Added absolute minimum values for Table 86, Table 92, and Table 93. Updated pin-to-pin setup and hold timing based on default IFD_DELAY_VALUE settings in Table 87, Table 88, and Table 90. Added Table 89 about source-synchronous input capture sample window. Promoted Module 3 to Production status. Synchronized all modules to v3.4.
03/16/07	3.5	Based on extensive 90 nm production data, improved (reduced) the maximum quiescent current limits for the I_{CCINTQ}, I_{CCAUXQ}, and I_{CCOQ} specifications in Table 79 by an average of 50%.
05/29/07	3.6	Added note to Table 74 and Table 75 regarding HSWAP in step 0 devices. Updated t_{RPW_CLB} in Table 98 to match value in speed file. Improved CLKOUT_FREQ_CLK90 to 200 MHz for Stepping 1 in Table 105.
04/18/08	3.7	Clarified that Stepping 0 was offered only for -4C and removed Stepping 0 -5 specifications. Added reference to XAPP459 in Table 73 and Table 77. Improved recommended max V_{CCO} to 3.465V (3.3V + 5%) in Table 77. Removed minimum input capacitance from Table 78. Updated Recommended Operating Conditions for LVCMOS and PCI I/O standards in Table 80. Removed Absolute Minimums from Table 86, Table 92 and Table 93 and added footnote recommending use of Timing Analyzer for minimum values. Updated T_{PSFD} and T_{PHFD} in Table 87 to match current speed file. Update T_{RPW_IOB} in Table 88 to match current speed file and CLB equivalent spec. Added XC3S500E VQG100 to Table 96. Replaced $T_{MULCKID}$ with T_{MSCKD} for A, B, and P registers in Table 102. Updated CLKOUT_PER_JITT_FX in Table 107. Updated MAX_STEPS equation in Table 109. Updated Figure 77 and Table 120 to correct CCLK active edge. Updated links.

User I/Os by Bank

Table 134 shows how the 83 available user-I/O pins are distributed on the XC3S100E FPGA packaged in the CP132 package. Table 135 indicates how the 92 available user-I/O pins are distributed on the XC3S250E and the XC3S500E FPGAs in the CP132 package.

Table 134: **User I/Os Per Bank for the XC3S100E in the CP132 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF(1)	CLK(2)
Top	0	18	6	2	1	1	8
Right	1	23	0	0	21	2	0(2)
Bottom	2	22	0	0	20	2	0(2)
Left	3	20	10	0	0	2	8
TOTAL		**83**	**16**	**2**	**42**	**7**	**16**

Notes:
1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

Table 135: **User I/Os Per Bank for the XC3S250E and XC3S500E in the CP132 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF(1)	CLK(2)
Top	0	22	11	0	1	2	8
Right	1	23	0	0	21	2	0(2)
Bottom	2	26	0	0	24	2	0(2)
Left	3	21	11	0	0	2	8
TOTAL		**92**	**22**	**0**	**46**	**8**	**16**

Notes:
1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

PQ208 Footprint (Right)

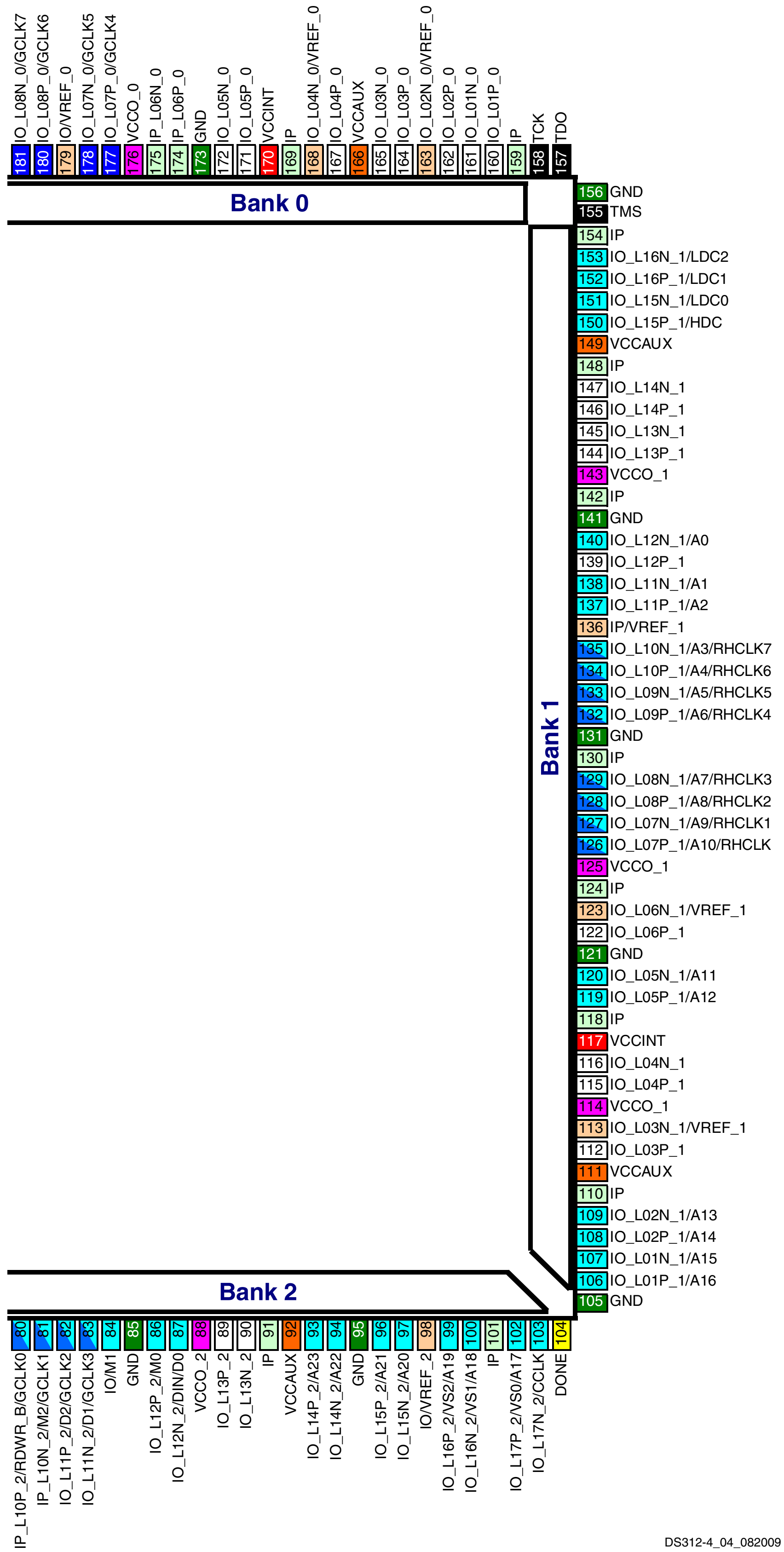

Figure 84: **PQ208 Footprint (Right)**

FG320: 320-ball Fine-pitch Ball Grid Array

The 320-ball fine-pitch ball grid array package, FG320, supports three different Spartan-3E FPGAs, including the XC3S500E, the XC3S1200E, and the XC3S1600E, as shown in Table 148 and Figure 86.

The FG320 package is an 18 x 18 array of solder balls minus the four center balls.

Table 148 lists all the package pins. They are sorted by bank number and then by pin name of the largest device. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The highlighted rows indicate pinout differences between the XC3S500E, the XC3S1200E, and the XC3S1600E FPGAs. The XC3S500E has 18 unconnected balls, indicated as N.C. (No Connection) in Table 148 and with the black diamond character (◆) in Table 148 and Figure 86.

If the table row is highlighted in tan, then this is an instance where an unconnected pin on the XC3S500E FPGA maps to a VREF pin on the XC3S1200E and XC3S1600E FPGA. If the FPGA application uses an I/O standard that requires a VREF voltage reference, connect the highlighted pin to the VREF voltage supply, even though this does not actually connect to the XC3S500E FPGA. This VREF connection on the board allows future migration to the larger devices without modifying the printed-circuit board.

All other balls have nearly identical functionality on all three devices. Table 147 summarizes the Spartan-3E footprint migration differences for the FG320 package.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx web site at:

http://www.xilinx.com/support/documentation/data_sheets/s3e_pin.zip

Pinout Table

Table 148: **FG320 Package Pinout**

Bank	XC3S500E Pin Name	XC3S1200E Pin Name	XC3S1600E Pin Name	FG320 Ball	Type
0	IP	IO	IO	A7	**500E:** INPUT **1200E:** I/O **1600E:** I/O
0	IO	IO	IO	A8	I/O
0	IO	IO	IO	A11	I/O
0	N.C. (◆)	IO	IO	A12	**500E:** N.C. **1200E:** I/O **1600E:** I/O
0	IO	IO	IO	C4	I/O
0	IP	IO	IO	D13	**500E:** INPUT **1200E:** I/O **1600E:** I/O
0	IO	IO	IO	E13	I/O
0	IO	IO	IO	G9	I/O
0	IO/VREF_0	IO/VREF_0	IO/VREF_0	B11	VREF
0	IO_L01N_0	IO_L01N_0	IO_L01N_0	A16	I/O
0	IO_L01P_0	IO_L01P_0	IO_L01P_0	B16	I/O
0	IO_L03N_0/VREF_0	IO_L03N_0/VREF_0	IO_L03N_0/VREF_0	C14	VREF
0	IO_L03P_0	IO_L03P_0	IO_L03P_0	D14	I/O
0	IO_L04N_0	IO_L04N_0	IO_L04N_0	A14	I/O
0	IO_L04P_0	IO_L04P_0	IO_L04P_0	B14	I/O
0	IO_L05N_0/VREF_0	IO_L05N_0/VREF_0	IO_L05N_0/VREF_0	B13	VREF
0	IO_L05P_0	IO_L05P_0	IO_L05P_0	A13	I/O
0	IO_L06N_0	IO_L06N_0	IO_L06N_0	E12	I/O
0	IO_L06P_0	IO_L06P_0	IO_L06P_0	F12	I/O
0	IO_L08N_0	IO_L08N_0	IO_L08N_0	F11	I/O

Table 148: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S500E Pin Name	XC3S1200E Pin Name	XC3S1600E Pin Name	FG320 Ball	Type
3	N.C. (◆)	IO_L04N_3	IO_L04N_3	E3	**500E:** N.C. **1200E:** I/O **1600E:** I/O
3	N.C. (◆)	IO_L04P_3	IO_L04P_3	E4	**500E:** N.C. **1200E:** I/O **1600E:** I/O
3	IO_L05N_3	IO_L05N_3	IO_L05N_3	F2	I/O
3	IO_L05P_3	IO_L05P_3	IO_L05P_3	F1	I/O
3	IO_L06N_3/VREF_3	IO_L06N_3/VREF_3	IO_L06N_3/VREF_3	G4	VREF
3	IO_L06P_3	IO_L06P_3	IO_L06P_3	G3	I/O
3	IO_L07N_3	IO_L07N_3	IO_L07N_3	G5	I/O
3	IO_L07P_3	IO_L07P_3	IO_L07P_3	G6	I/O
3	IO_L08N_3	IO_L08N_3	IO_L08N_3	H5	I/O
3	IO_L08P_3	IO_L08P_3	IO_L08P_3	H6	I/O
3	IO_L09N_3	IO_L09N_3	IO_L09N_3	H3	I/O
3	IO_L09P_3	IO_L09P_3	IO_L09P_3	H4	I/O
3	IO_L10N_3	IO_L10N_3	IO_L10N_3	H1	I/O
3	IO_L10P_3	IO_L10P_3	IO_L10P_3	H2	I/O
3	IO_L11N_3/LHCLK1	IO_L11N_3/LHCLK1	IO_L11N_3/LHCLK1	J4	LHCLK
3	IO_L11P_3/LHCLK0	IO_L11P_3/LHCLK0	IO_L11P_3/LHCLK0	J5	LHCLK
3	IO_L12N_3/LHCLK3/ IRDY2	IO_L12N_3/LHCLK3/ IRDY2	IO_L12N_3/LHCLK3/ IRDY2	J2	LHCLK
3	IO_L12P_3/LHCLK2	IO_L12P_3/LHCLK2	IO_L12P_3/LHCLK2	J1	LHCLK
3	IO_L13N_3/LHCLK5	IO_L13N_3/LHCLK5	IO_L13N_3/LHCLK5	K4	LHCLK
3	IO_L13P_3/LHCLK4/ TRDY2	IO_L13P_3/LHCLK4/ TRDY2	IO_L13P_3/LHCLK4/ TRDY2	K3	LHCLK
3	IO_L14N_3/LHCLK7	IO_L14N_3/LHCLK7	IO_L14N_3/LHCLK7	K5	LHCLK
3	IO_L14P_3/LHCLK6	IO_L14P_3/LHCLK6	IO_L14P_3/LHCLK6	K6	LHCLK
3	IO_L15N_3	IO_L15N_3	IO_L15N_3	L2	I/O
3	IO_L15P_3	IO_L15P_3	IO_L15P_3	L1	I/O
3	IO_L16N_3	IO_L16N_3	IO_L16N_3	L4	I/O
3	IO_L16P_3	IO_L16P_3	IO_L16P_3	L3	I/O
3	IO_L17N_3/VREF_3	IO_L17N_3/VREF_3	IO_L17N_3/VREF_3	L5	VREF
3	IO_L17P_3	IO_L17P_3	IO_L17P_3	L6	I/O
3	IO_L18N_3	IO_L18N_3	IO_L18N_3	M3	I/O
3	IO_L18P_3	IO_L18P_3	IO_L18P_3	M4	I/O
3	IO_L19N_3	IO_L19N_3	IO_L19N_3	M6	I/O
3	IO_L19P_3	IO_L19P_3	IO_L19P_3	M5	I/O
3	IO_L20N_3	IO_L20N_3	IO_L20N_3	N5	I/O
3	IO_L20P_3	IO_L20P_3	IO_L20P_3	N4	I/O
3	IO_L21N_3	IO_L21N_3	IO_L21N_3	P1	I/O
3	IO_L21P_3	IO_L21P_3	IO_L21P_3	P2	I/O
3	N.C. (◆)	IO_L22N_3	IO_L22N_3	P4	**500E:** N.C. **1200E:** I/O **1600E:** I/O

Table 148: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S500E Pin Name	XC3S1200E Pin Name	XC3S1600E Pin Name	FG320 Ball	Type
3	N.C. (◆)	IO_L22P_3	IO_L22P_3	P3	**500E:** N.C. **1200E:** I/O **1600E:** I/O
3	IO_L23N_3	IO_L23N_3	IO_L23N_3	R2	I/O
3	IO_L23P_3	IO_L23P_3	IO_L23P_3	R3	I/O
3	IO_L24N_3	IO_L24N_3	IO_L24N_3	T1	I/O
3	IO_L24P_3	IO_L24P_3	IO_L24P_3	T2	I/O
3	IP	IP	IP	D3	INPUT
3	IO	IP	IP	F4	**500E:** I/O **1200E:** INPUT **1600E:** INPUT
3	IP	IP	IP	F5	INPUT
3	IP	IP	IP	G1	INPUT
3	IP	IP	IP	J7	INPUT
3	IP	IP	IP	K2	INPUT
3	IP	IP	IP	K7	INPUT
3	IP	IP	IP	M1	INPUT
3	IP	IP	IP	N1	INPUT
3	IP	IP	IP	N2	INPUT
3	IP	IP	IP	R1	INPUT
3	IP	IP	IP	U1	INPUT
3	IP/VREF_3	IP/VREF_3	IP/VREF_3	J6	VREF
3	IO/VREF_3	IP/VREF_3	IP/VREF_3	R4	**500E:** VREF(I/O) **1200E:** VREF(INPUT) **1600E:** VREF(INPUT)
3	VCCO_3	VCCO_3	VCCO_3	F3	VCCO
3	VCCO_3	VCCO_3	VCCO_3	H7	VCCO
3	VCCO_3	VCCO_3	VCCO_3	K1	VCCO
3	VCCO_3	VCCO_3	VCCO_3	L7	VCCO
3	VCCO_3	VCCO_3	VCCO_3	N3	VCCO
GND	GND	GND	GND	A1	GND
GND	GND	GND	GND	A18	GND
GND	GND	GND	GND	B2	GND
GND	GND	GND	GND	B17	GND
GND	GND	GND	GND	C10	GND
GND	GND	GND	GND	G7	GND
GND	GND	GND	GND	G12	GND
GND	GND	GND	GND	H8	GND
GND	GND	GND	GND	H9	GND
GND	GND	GND	GND	H10	GND
GND	GND	GND	GND	H11	GND
GND	GND	GND	GND	J3	GND
GND	GND	GND	GND	J8	GND
GND	GND	GND	GND	J11	GND

User I/Os by Bank

Table 149 and Table 150 indicate how the available user-I/O pins are distributed between the four I/O banks on the FG320 package.

Table 149: **User I/Os Per Bank for XC3S500E in the FG320 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF[1]	CLK[2]
Top	0	58	29	14	1	6	8
Right	1	58	22	10	21	5	0[2]
Bottom	2	58	17	13	24	4	0[2]
Left	3	58	34	11	0	5	8
TOTAL		**232**	**102**	**48**	**46**	**20**	**16**

Notes:
1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

Table 150: **User I/Os Per Bank for XC3S1200E and XC3S1600E in the FG320 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF[1]	CLK[2]
Top	0	61	34	12	1	6	8
Right	1	63	25	12	21	5	0[2]
Bottom	2	63	23	11	24	5	0[2]
Left	3	63	38	12	0	5	8
TOTAL		**250**	**120**	**47**	**46**	**21**	**16**

Notes:
1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

FG400 Footprint

Right Half of Package (top view)

Bank 0

	11	12	13	14	15	16	17	18	19	20
A	GND	I/O	I/O L09N_0 VREF_0	I/O L09P_0	I/O L06N_0	I/O L04P_0	I/O L04N_0	I/O L03N_0 VREF_0	I/O L03P_0	GND
B	INPUT L14N_0	INPUT L14P_0	I/O L10N_0	GND	I/O L06P_0	VCCO_0	I/O L01N_0	INPUT	TDO	INPUT
C	I/O VREF_0	I/O L12N_0	I/O L10P_0	I/O L07N_0	INPUT L05P_0	INPUT L02N_0	I/O L01P_0	GND	I/O L30N_1 LDC2	I/O L30P_1 LDC1
D	VCCAUX	I/O L12P_0	VCCO_0	I/O L07P_0	INPUT L05N_0	INPUT L02P_0	TCK	I/O L29N_1 LDC0	VCCO_1	I/O L28N_1
E	I/O L16P_0 GCLK6	I/O L13N_0	I/O	INPUT L08N_0	INPUT L08P_0	I/O	TMS	I/O L29P_1 HDC	INPUT VREF_1	I/O L28P_1
F	I/O L15P_0 GCLK4	I/O L13P_0	I/O	I/O	GND	I/O L25P_1	I/O L27P_1	I/O L27N_1	I/O L26N_1	I/O L26P_1
G	I/O L15N_0 GCLK5	GND	INPUT L11P_0	INPUT L11N_0	INPUT	I/O L25N_1	VCCO_1	INPUT	GND	I/O L24P_1
H	VCCINT	VCCAUX	VCCINT	INPUT	I/O L22N_1	I/O L22P_1	I/O L23P_1	I/O L23N_1	I/O L21N_1	I/O L24N_1 VREF_1
J	GND	VCCINT	I/O L19N_1 A0	I/O L19P_1	INPUT	I/O L18P_1 A2	I/O L20N_1	I/O L20P_1	I/O L21P_1	I/O L17N_1 A3 RHCLK7
K	VCCINT	GND	I/O L16P_1 A6 RHCLK4 IRDY1	I/O L16N_1 A5 RHCLK5	VCCO_1	I/O L18N_1 A1	GND	INPUT VREF_1	VCCO_1	I/O L17P_1 A4 RHCLK6
L	GND	VCCINT	GND	I/O L15N_1 A7 RHCLK3 TRDY1	I/O L15P_1 A8 RHCLK2	I/O L14N_1 A9 RHCLK1	VCCAUX	INPUT	I/O L13N_1 VREF_1	GND
M	VCCINT	GND	VCCINT	VCCAUX	I/O L11P_1	I/O L14P_1 A10 RHCLK0	I/O L12P_1 A12	I/O L12N_1 A11	I/O L13P_1	INPUT
N	I/O D5	VCCINT	GND	INPUT	I/O L11N_1	I/O L09P_1	VCCO_1	I/O L10P_1	I/O L10N_1	INPUT
P	INPUT L17P_2 RDWR_B GCLK0	INPUT L17N_2 M2 GCLK1	I/O	I/O L25N_2	INPUT	I/O L09N_1	I/O L07P_1	I/O L07N_1	GND	I/O L08N_1 VREF_1
R	VCCO_2	INPUT L20P_2	I/O	I/O L25P_2	GND	INPUT	I/O L05P_1	I/O L05N_1	INPUT	I/O L08P_1
T	I/O M1	INPUT L20N_2	INPUT L23N_2 VREF_2	INPUT L23P_2	I/O L28N_2	INPUT	I/O L02P_1 A14	I/O L02N_1 A13	VCCO_1	I/O L06N_1
U	GND	I/O L21N_2	I/O L24N_2	VCCO_2	I/O L28P_2	I/O L30P_2 A21	I/O L01P_1 A16	I/O L01N_1 A15	I/O L03P_1	I/O L06P_1
V	I/O L18N_2 D1 GCLK3	I/O L21P_2	I/O L24P_2	INPUT L26N_2	INPUT L26P_2	I/O L30N_2 A20	DONE	GND	I/O L03N_1 VREF_1	I/O L04P_1
W	VCCO_2	I/O L22N_2 VREF_2	I/O L22P_2	GND	I/O	INPUT L29N_2	VCCO_2	I/O L31P_2 VS2 A19	I/O L32N_2 CCLK	I/O L04N_1
Y	I/O L19P_2 M0	I/O L19N_2 DIN D0	I/O	I/O L27N_2 A22	I/O L27P_2 A23	INPUT L29P_2	I/O VREF_2	I/O L31N_2 VS1 A18	I/O L32P_2 VS0 A17	GND

Bank 1

Bank 2

DS312-4_09_101905

Table 154: **FG484 Package Pinout *(Cont'd)***

Bank	XC3S1600E Pin Name	FG484 Ball	Type
2	IO_L19N_2/D6/GCLK13	U11	DUAL/ GCLK
2	IO_L19P_2/D7/GCLK12	V11	DUAL/ GCLK
2	IO_L20N_2/D3/GCLK15	T11	DUAL/ GCLK
2	IO_L20P_2/D4/GCLK14	R11	DUAL/ GCLK
2	IO_L22N_2/D1/GCLK3	W12	DUAL/ GCLK
2	IO_L22P_2/D2/GCLK2	Y12	DUAL/ GCLK
2	IO_L23N_2/DIN/D0	U12	DUAL
2	IO_L23P_2/M0	V12	DUAL
2	IO_L25N_2	Y13	I/O
2	IO_L25P_2	W13	I/O
2	IO_L26N_2/VREF_2	U14	VREF
2	IO_L26P_2	U13	I/O
2	IO_L27N_2	T14	I/O
2	IO_L27P_2	R14	I/O
2	IO_L28N_2	Y14	I/O
2	IO_L28P_2	AA14	I/O
2	IO_L29N_2	W14	I/O
2	IO_L29P_2	V14	I/O
2	IO_L30N_2	AB15	I/O
2	IO_L30P_2	AA15	I/O
2	IO_L32N_2	W15	I/O
2	IO_L32P_2	Y15	I/O
2	IO_L33N_2	U16	I/O
2	IO_L33P_2	V16	I/O
2	IO_L35N_2/A22	AB17	DUAL
2	IO_L35P_2/A23	AA17	DUAL
2	IO_L36N_2	W17	I/O
2	IO_L36P_2	Y17	I/O
2	IO_L38N_2/A20	Y18	DUAL
2	IO_L38P_2/A21	W18	DUAL
2	IO_L39N_2/VS1/A18	AA20	DUAL
2	IO_L39P_2/VS2/A19	AB20	DUAL
2	IO_L40N_2/CCLK	W19	DUAL
2	IO_L40P_2/VS0/A17	Y19	DUAL
2	IP	V17	INPUT
2	IP	AB2	INPUT
2	IP_L02N_2	AA4	INPUT
2	IP_L02P_2	Y4	INPUT
2	IP_L05N_2	Y6	INPUT
2	IP_L05P_2	AA6	INPUT

Table 154: **FG484 Package Pinout *(Cont'd)***

Bank	XC3S1600E Pin Name	FG484 Ball	Type
2	IP_L08N_2	AB7	INPUT
2	IP_L08P_2	AB6	INPUT
2	IP_L15N_2	Y10	INPUT
2	IP_L15P_2	W10	INPUT
2	IP_L18N_2/VREF_2	AA11	VREF
2	IP_L18P_2	Y11	INPUT
2	IP_L21N_2/M2/GCLK1	P12	DUAL/ GCLK
2	IP_L21P_2/RDWR_B/ GCLK0	R12	DUAL/ GCLK
2	IP_L24N_2	R13	INPUT
2	IP_L24P_2	T13	INPUT
2	IP_L31N_2/VREF_2	T15	VREF
2	IP_L31P_2	U15	INPUT
2	IP_L34N_2	Y16	INPUT
2	IP_L34P_2	W16	INPUT
2	IP_L37N_2	AA19	INPUT
2	IP_L37P_2	AB19	INPUT
2	VCCO_2	T12	VCCO
2	VCCO_2	U9	VCCO
2	VCCO_2	V15	VCCO
2	VCCO_2	AA5	VCCO
2	VCCO_2	AA9	VCCO
2	VCCO_2	AA13	VCCO
2	VCCO_2	AA18	VCCO
3	IO_L01N_3	C1	I/O
3	IO_L01P_3	C2	I/O
3	IO_L02N_3/VREF_3	D2	VREF
3	IO_L02P_3	D3	I/O
3	IO_L03N_3	E3	I/O
3	IO_L03P_3	E4	I/O
3	IO_L04N_3	E1	I/O
3	IO_L04P_3	D1	I/O
3	IO_L05N_3	F4	I/O
3	IO_L05P_3	F3	I/O
3	IO_L06N_3	G5	I/O
3	IO_L06P_3	G4	I/O
3	IO_L07N_3	F1	I/O
3	IO_L07P_3	G1	I/O
3	IO_L08N_3/VREF_3	G6	VREF
3	IO_L08P_3	G7	I/O
3	IO_L09N_3	H4	I/O
3	IO_L09P_3	H5	I/O
3	IO_L10N_3	H2	I/O
3	IO_L10P_3	H3	I/O