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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	612
Number of Logic Elements/Cells	5508
Total RAM Bits	221184
Number of I/O	66
Number of Gates	250000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s250e-4vq100c

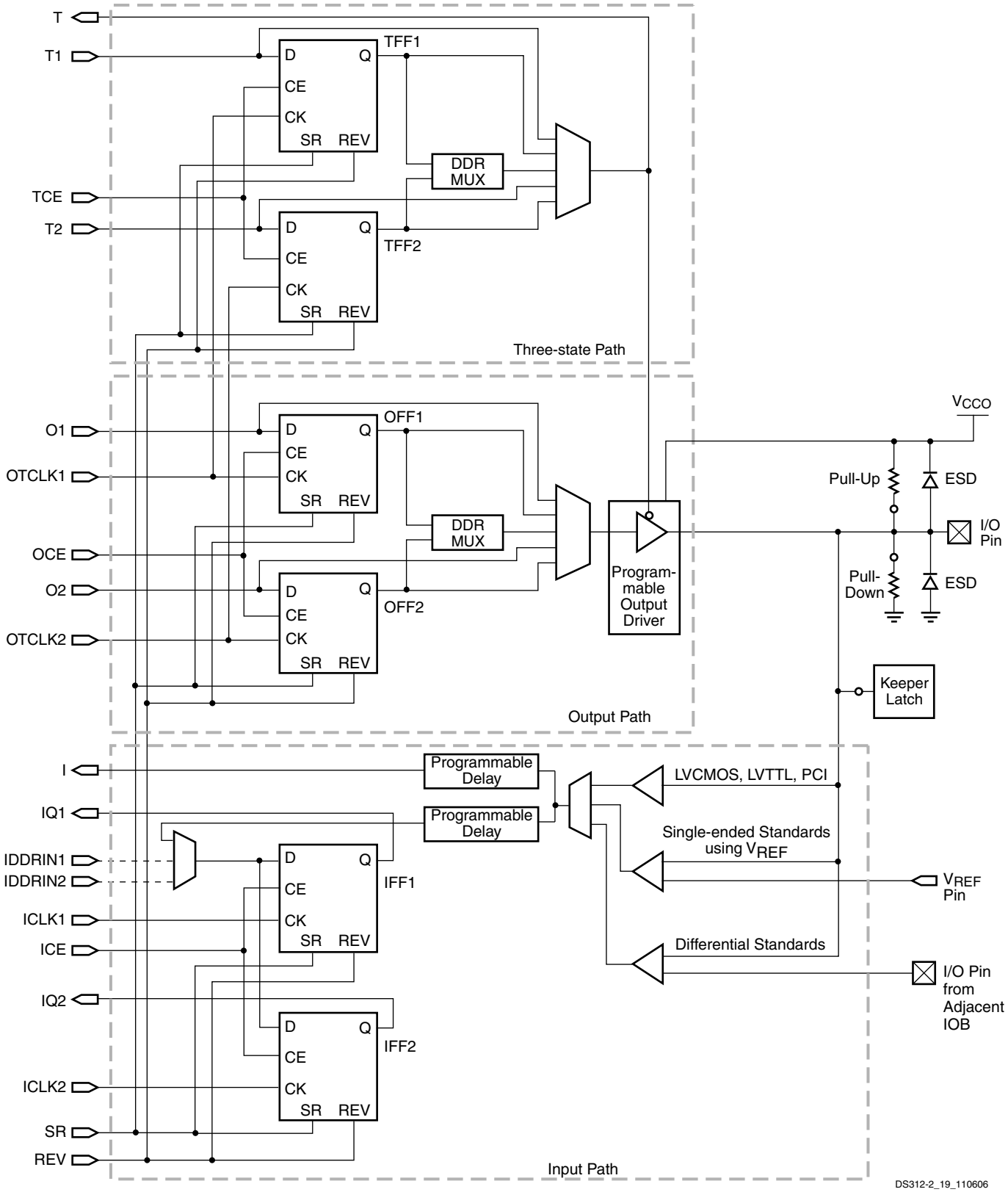


Figure 5: **Simplified IOB Diagram**

Input Delay Functions

Each IOB has a programmable delay block that optionally delays the input signal. In Figure 6, the signal path has a coarse delay element that can be bypassed. The input signal then feeds a 6-tap delay line. The coarse and tap delays vary; refer to timing reports for specific delay values. All six taps are available via a multiplexer for use as an asynchronous input directly into the FPGA fabric. In this way, the delay is programmable in 12 steps. Three of the six taps are also available via a multiplexer to the D inputs of the synchronous storage elements. The delay inserted in the path to the storage element can be varied in six steps. The first, coarse delay element is common to both asynchronous and synchronous paths, and must be either used or not used for both paths.

The delay values are set up in the silicon once at configuration time—they are non-modifiable in device operation.

The primary use for the input delay element is to adjust the input delay path to ensure that there is no hold time requirement when using the input flip-flop(s) with a global clock. The default value is chosen automatically by the Xilinx software tools as the value depends on device size and the specific device edge where the flip-flop resides. The value set by the Xilinx ISE software is indicated in the Map report generated by the implementation tools, and the resulting effects on input timing are reported using the Timing Analyzer tool.

If the design uses a DCM in the clock path, then the delay element can be safely set to zero because the Delay-Locked Loop (DLL) compensation automatically ensures that there is still no input hold time requirement.

Both asynchronous and synchronous values can be modified, which is useful where extra delay is required on clock or data inputs, for example, in interfaces to various types of RAM.

These delay values are defined through the IBUF_DELAY_VALUE and the IFD_DELAY_VALUE parameters. The default IBUF_DELAY_VALUE is 0, bypassing the delay elements for the asynchronous input. The user can set this parameter to 0-12. The default IFD_DELAY_VALUE is AUTO. IBUF_DELAY_VALUE and IFD_DELAY_VALUE are independent for each input. If the same input pin uses both registered and non-registered input paths, both parameters can be used, but they must both be in the same half of the total delay (both either bypassing or using the coarse delay element).

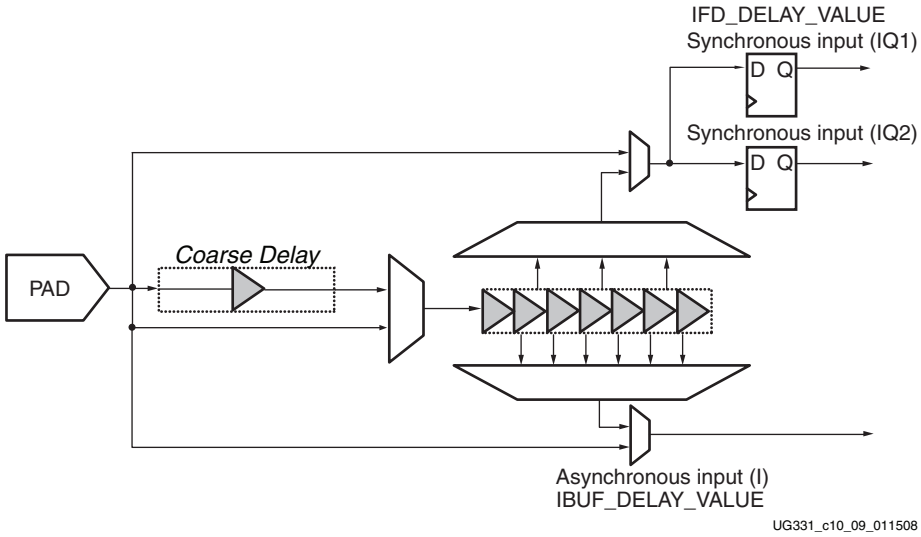


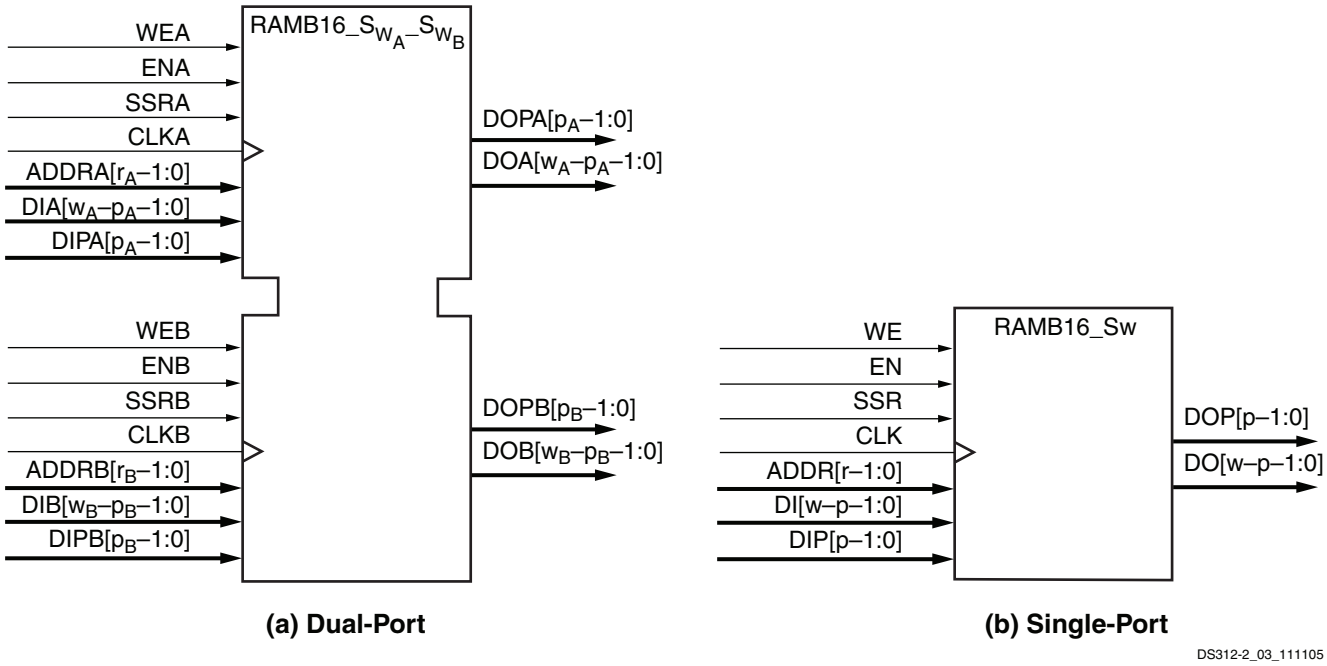
Figure 6: **Programmable Fixed Input Delay Elements**

Block RAM Port Signal Definitions

Representations of the dual-port primitive RAMB16_S[w_A]_S[w_B] and the single-port primitive RAMB16_S[w] with their associated signals are shown in Figure 32a and Figure 32b, respectively. These signals are defined in Table 23. The control signals (WE, EN, CLK, and SSR) on the block RAM are active High. However, optional inverters on the control signals change the polarity of the active edge to active Low.

Design Note

Whenever a block RAM port is enabled (ENA or ENB = High), all address transitions must meet the data sheet setup and hold times with respect to the port clock (CLKA or CLKB), as shown in Table 103, page 138.This requirement must be met even if the RAM read output is of no interest.



Notes:

1. w_A and w_B are integers representing the total data path width (i.e., data bits plus parity bits) at Ports A and B, respectively.
2. p_A and p_B are integers that indicate the number of data path lines serving as parity bits.
3. r_A and r_B are integers representing the address bus width at ports A and B, respectively.
4. The control signals CLK, WE, EN, and SSR on both ports have the option of inverted polarity.

Figure 32: **Block RAM Primitives**

Table 46: **Pin Behavior during Configuration *(Cont'd)***

Pin Name	Master Serial	SPI (Serial Flash)	BPI (Parallel NOR Flash)	JTAG	Slave Parallel	Slave Serial	I/O Bank[3]
D0/DIN	DIN	DIN	D0		D0	DIN	2
RDWR_B			RDWR_B		RDWR_B		2
A23			A23				2
A22			A22				2
A21			A21				2
A20			A20				2
A19/VS2		VS2	A19				2
A18/VS1		VS1	A18				2
A17/VS0		VS0	A17				2
A16			A16				1
A15			A15				1
A14			A14				1
A13			A13				1
A12			A12				1
A11			A11				1
A10			A10				1
A9			A9				1
A8			A8				1
A7			A7				1
A6			A6				1
A5			A5				1
A4			A4				1
A3			A3				1
A2			A2				1
A1			A1				1
A0			A0				1
LDC0			LDC0				1
LDC1			LDC1				1
LDC2			LDC2				1
HDC			HDC				1

Notes:
1. Gray shaded cells represent pins that are in a high-impedance state (Hi-Z, floating) during configuration. These pins have an optional internal pull-up resistor to their respective V_{CCO} supply pin that is active throughout configuration if the HSWAP input is Low.
2. Yellow shaded cells represent pins with an internal pull-up resistor to its respective voltage supply rail that is active during configuration, regardless of the HSWAP pin.
3. Note that dual-purpose outputs are supplied by V_{CCO}, and configuration inputs are supplied by V_{CCAUX}.

The HSWAP pin itself has a pull-up resistor enabled during configuration. However, the VCCO_0 supply voltage must be applied before the pull-up resistor becomes active. If the VCCO_0 supply ramps after the VCCO_2 power supply, do not let HSWAP float; tie HSWAP to the desired logic level externally.

Spartan-3E FPGAs have only six dedicated configuration pins, including the DONE and PROG_B pins, and the four JTAG boundary-scan pins: TDI, TDO, TMS, and TCK. All other configuration pins are dual-purpose I/O pins and are available to the FPGA application after the DONE pin goes High. See Start-Up for additional information.

Table 47 shows the default I/O standard setting for the various configuration pins during the configuration process. The configuration interface is designed primarily for 2.5V operation when the VCCO_2 (and VCCO_1 in BPI mode) connects to 2.5V.

Table 47: **Default I/O Standard Setting During Configuration (VCCO_2 = 2.5V)**

Pin(s)	I/O Standard	Output Drive	Slew Rate
All, including CCLK	LVCMOS25	8 mA	Slow

Table 55: **Serial Peripheral Interface (SPI) Connections *(Cont'd)***

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
VS[2:0] Ⓢ	Input	**Variant Select**. Instructs the FPGA how to communicate with the attached SPI Flash PROM. See Design Considerations for the HSWAP, M[2:0], and VS[2:0] Pins.	Must be at the logic levels shown in Table 53. Sampled when INIT_B goes High.	User I/O
MOSI	Output	**Serial Data Output**.	FPGA sends SPI Flash memory read commands and starting address to the PROM's serial data input.	User I/O
DIN	Input	**Serial Data Input**.	FPGA receives serial data from PROM's serial data output.	User I/O
CSO_B	Output	**Chip Select Output**. Active Low.	Connects to the SPI Flash PROM's chip-select input. If HSWAP = 1, connect this signal to a 4.7 kΩ pull-up resistor to 3.3V.	Drive CSO_B High after configuration to disable the SPI Flash and reclaim the MOSI, DIN, and CCLK pins. Optionally, re-use this pin and MOSI, DIN, and CCLK to continue communicating with SPI Flash.
CCLK	Output	**Configuration Clock**. Generated by FPGA internal oscillator. Frequency controlled by ***ConfigRate*** bitstream generator option. If CCLK PCB trace is long or has multiple connections, terminate this output to maintain signal integrity. See CCLK Design Considerations.	Drives PROM's clock input.	User I/O
DOUT	Output	**Serial Data Output**.	Actively drives. Not used in single-FPGA designs. In a daisy-chain configuration, this pin connects to DIN input of the next FPGA in the chain.	User I/O
INIT_B	Open-drain bidirectional I/O	**Initialization Indicator**. Active Low. Goes Low at start of configuration during Initialization memory clearing process. Released at end of memory clearing, when mode select pins are sampled. In daisy-chain applications, this signal requires an external 4.7 kΩ pull-up resistor to VCCO_2.	Active during configuration. If SPI Flash PROM requires > 2 ms to awake after powering on, hold INIT_B Low until PROM is ready. If CRC error detected during configuration, FPGA drives INIT_B Low.	User I/O. If unused in the application, drive INIT_B High.
DONE	Open-drain bidirectional I/O	**FPGA Configuration Done**. Low during configuration. Goes High when FPGA successfully completes configuration. Requires external 330 Ω pull-up resistor to 2.5V.	Low indicates that the FPGA is not yet configured.	Pulled High via external pull-up. When High, indicates that the FPGA successfully configured.
PROG_B	Input	**Program FPGA**. Active Low. When asserted Low for 500 ns or longer, forces the FPGA to restart its configuration process by clearing configuration memory and resetting the DONE and INIT_B pins once PROG_B returns High. Recommend external 4.7 kΩ pull-up resistor to 2.5V. Internal pull-up value may be weaker (see Table 78). If driving externally with a 3.3V output, use an open-drain or open-collector driver or use a current limiting series resistor.	Must be High to allow configuration to start.	Drive PROG_B Low and release to reprogram FPGA. Hold PROG_B to force FPGA I/O pins into Hi-Z, allowing direct programming access to SPI Flash PROM pins.

After the FPGA configures itself using BPI mode from one end of the parallel Flash PROM, then the FPGA can trigger a MultiBoot event and reconfigure itself from the opposite end of the parallel Flash PROM. MultiBoot is only available when using BPI mode and only for applications with a single Spartan-3E FPGA.

By default, MultiBoot mode is disabled. To trigger a MultiBoot event, assert a Low pulse lasting at least 300 ns on the MultiBoot Trigger (MBT) input to the STARTUP_SPARTAN3E library primitive. When the MBT signal returns High after the 300 ns or longer pulse, the FPGA automatically reconfigures from the opposite end of the parallel Flash memory.

Figure 60 shows an example usage. At power up, the FPGA loads itself from the attached parallel Flash PROM. In this example, the M0 mode pin is Low so the FPGA starts at address 0 and increments through the Flash PROM memory locations. After the FPGA completes configuration, the application initially loaded into the FPGA performs a board-level or system test using FPGA logic. If the test is successful, the FPGA then triggers a MultiBoot event, causing the FPGA to reconfigure from the opposite end of the Flash PROM memory. This second configuration contains the FPGA application for normal operation.

Similarly, the general FPGA application could trigger another MultiBoot event at any time to reload the diagnostics design, and so on.

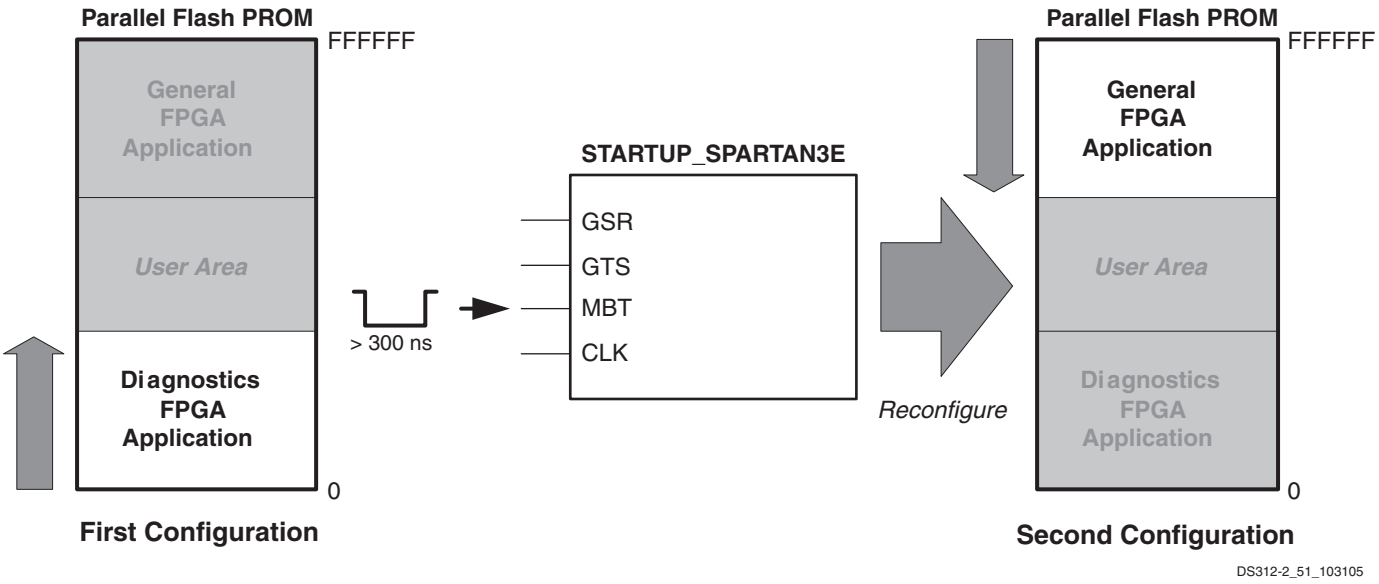


Figure 60: **Use MultiBoot to Load Alternate Configuration Images**

In another potential application, the initial design loaded into the FPGA image contains a “golden” or “fail-safe” configuration image, which then communicates with the outside world and checks for a newer image. If there is a new configuration revision and the new image verifies as good, the “golden” configuration triggers a MultiBoot event to load the new image.

When a MultiBoot event is triggered, the FPGA then again drives its configuration pins as described in Table 59. However, the FPGA does not assert the PROG_B pin. The system design must ensure that no other device drives on these same pins during the reconfiguration process. The FPGA’s DONE, LDC[2:0], or HDC pins can temporarily disable any conflicting drivers during reconfiguration.

Asserting the PROG_B pin Low overrides the MultiBoot feature and forces the FPGA to reconfigure starting from the end of memory defined by the mode pins, shown in Table 58.

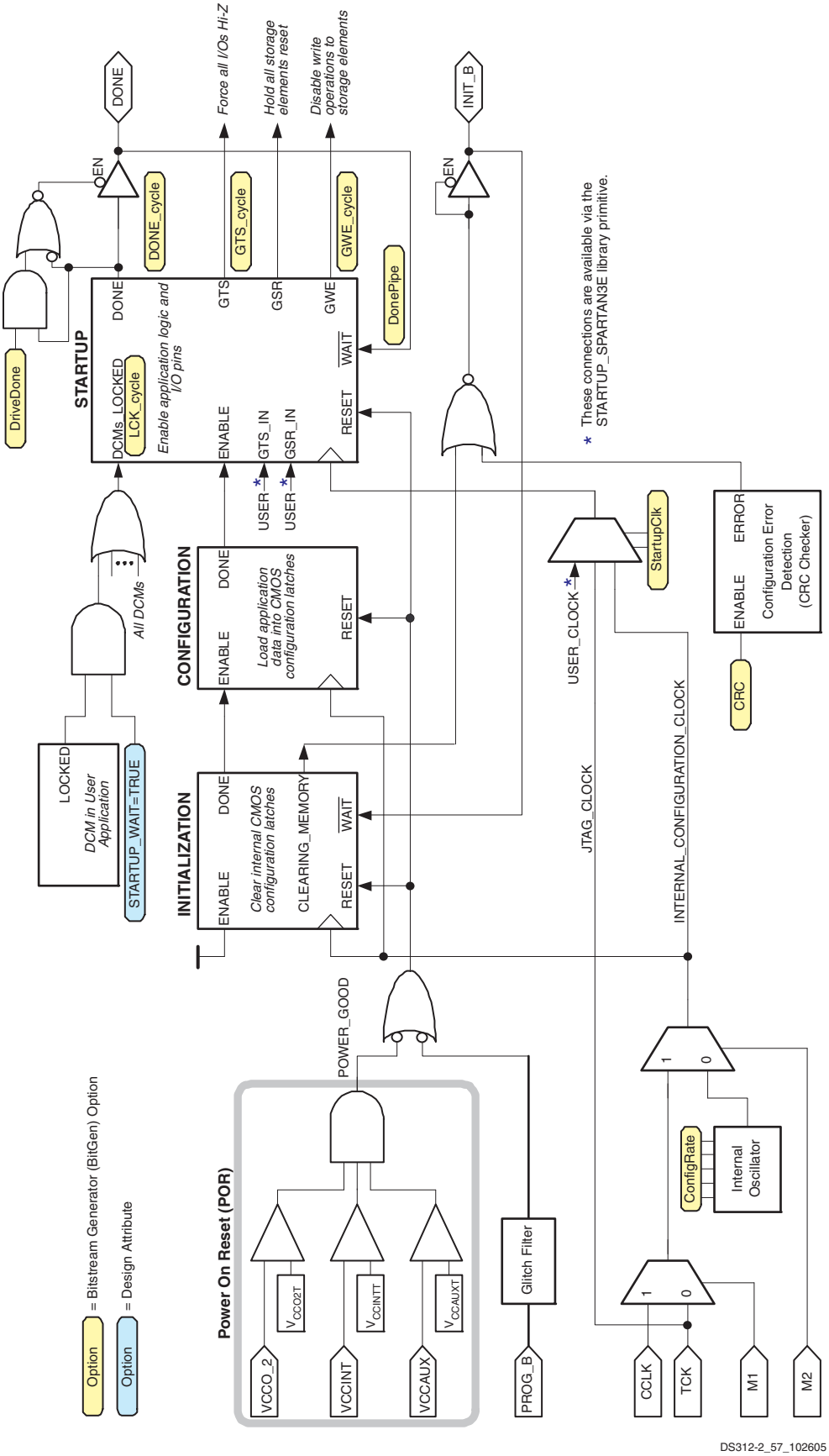


Figure 66: **Generalized Spartan-3E FPGA Configuration Logic Block Diagram**

Bitstream Generator (BitGen) Options

For additional information, refer to the "Configuration Bitstream Generator (BitGen) Settings" chapter in UG332.

Various Spartan-3E FPGA functions are controlled by specific bits in the configuration bitstream image. These values are specified when creating the bitstream image with the Bitstream Generator (BitGen) software.

Table 69 provides a list of all BitGen options for Spartan-3E FPGAs.

Table 69: **Spartan-3E FPGA Bitstream Generator (BitGen) Options**

Option Name	Pins/Function Affected	Values (***default***)	Description
ConfigRate	CCLK, Configuration	***1***, 3, 6, 12, 25, 50	Sets the approximate frequency, in MHz, of the internal oscillator using for Master Serial, SPI, and BPI configuration modes. The internal oscillator powers up at its lowest frequency, and the new setting is loaded as part of the configuration bitstream. The software default value is 1 (~1.5 MHz) starting with ISE 8.1, Service Pack 1.
StartupClk	Configuration, Startup	***Cclk***	***Default.*** The CCLK signal (internally or externally generated) controls the startup sequence when the FPGA transitions from configuration mode to the user mode. See Start-Up.
		UserClk	A clock signal from within the FPGA application controls the startup sequence when the FPGA transitions from configuration mode to the user mode. See Start-Up. The FPGA application supplies the user clock on the CLK pin on the STARTUP_SPARTAN3E primitive.
		Jtag	The JTAG TCK input controls the startup sequence when the FPGA transitions from the configuration mode to the user mode. See Start-Up.
UnusedPin	Unused I/O Pins	***Pulldown***	***Default.*** All unused I/O pins and input-only pins have a pull-down resistor to GND.
		Pullup	All unused I/O pins and input-only pins have a pull-up resistor to the VCCO_# supply for its associated I/O bank.
		Pullnone	All unused I/O pins and input-only pins are left floating (Hi-Z, high-impedance, three-state). Use external pull-up or pull-down resistors or logic to apply a valid signal level.
DONE_cycle	DONE pin, Configuration Startup	1, 2, 3, ***4***, 5, 6	Selects the Configuration Startup phase that activates the FPGA's DONE pin. See Start-Up.
GWE_cycle	All flip-flops, LUT RAMs, and SRL16 shift registers, Block RAM, Configuration Startup	1, 2, 3, 4, 5, ***6***	Selects the Configuration Startup phase that asserts the internal write-enable signal to all flip-flops, LUT RAMs and shift registers (SRL16). It also enables block RAM read and write operations. See Start-Up.
		Done	Waits for the DONE pin input to go High before asserting the internal write-enable signal to all flip-flops, LUT RAMs and shift registers (SRL16). Block RAM read and write operations are enabled at this time.
		Keep	Retains the current GWE_cycle setting for partial reconfiguration applications.
GTS_cycle	All I/O pins, Configuration	1, 2, 3, 4, ***5***, 6	Selects the Configuration Startup phase that releases the internal three-state control, holding all I/O buffers in high-impedance (Hi-Z). Output buffers actively drive, if so configured, after this point. See Start-Up.
		Done	Waits for the DONE pin input to go High before releasing the internal three-state control, holding all I/O buffers in high-impedance (Hi-Z). Output buffers actively drive, if so configured, after this point.
		Keep	Retains the current GTS_cycle setting for partial reconfiguration applications.
LCK_cycle	DCMs, Configuration Startup	***NoWait***	The FPGA does not wait for selected DCMs to lock before completing configuration.
		0, 1, 2, 3, 4, 5, 6	If one or more DCMs in the design have the STARTUP_WAIT attribute set to TRUE, the FPGA waits for such DCMs to acquire their respective input clock and assert their LOCKED output. This setting selects the Configuration Startup phase where the FPGA waits for the DCMs to lock.
DonePin	DONE pin	***Pullup***	Internally connects a pull-up resistor between DONE pin and V_{CCAUX}. An external 330 Ω pull-up resistor to V_{CCAUX} is still recommended.
		Pullnone	No internal pull-up resistor on DONE pin. An external 330 Ω pull-up resistor to V_{CCAUX} is required.

Table 69: **Spartan-3E FPGA Bitstream Generator (BitGen) Options *(Cont'd)***

Option Name	Pins/Function Affected	Values (***default***)	Description
DriveDone	DONE pin	***No***	When configuration completes, the DONE pin stops driving Low and relies on an external 330 Ω pull-up resistor to V_{CCAUX} for a valid logic High.
		Yes	When configuration completes, the DONE pin actively drives High. When using this option, an external pull-up resistor is no longer required. Only one device in an FPGA daisy-chain should use this setting.
DonePipe	DONE pin	***No***	The input path from DONE pin input back to the Startup sequencer is not pipelined.
		Yes	This option adds a pipeline register stage between the DONE pin input and the Startup sequencer. Used for high-speed daisy-chain configurations when DONE cannot rise in a single CCLK cycle. Releases GWE and GTS signals on the first rising edge of StartupClk after the DONE pin input goes High.
ProgPin	PROG_B pin	***Pullup***	Internally connects a pull-up resistor or between PROG_B pin and V_{CCAUX}. An external 4.7 kΩ pull-up resistor to V_{CCAUX} is still recommended since the internal pull-up value may be weaker (see Table 78).
		Pullnone	No internal pull-up resistor on PROG_B pin. An external 4.7 kΩ pull-up resistor to V_{CCAUX} is required.
TckPin	JTAG TCK pin	***Pullup***	Internally connects a pull-up resistor between JTAG TCK pin and V_{CCAUX}.
		Pulldown	Internally connects a pull-down resistor between JTAG TCK pin and GND.
		Pullnone	No internal pull-up resistor on JTAG TCK pin.
TdiPin	JTAG TDI pin	***Pullup***	Internally connects a pull-up resistor between JTAG TDI pin and V_{CCAUX}.
		Pulldown	Internally connects a pull-down resistor between JTAG TDI pin and GND.
		Pullnone	No internal pull-up resistor on JTAG TDI pin.
TdoPin	JTAG TDO pin	***Pullup***	Internally connects a pull-up resistor between JTAG TDO pin and V_{CCAUX}.
		Pulldown	Internally connects a pull-down resistor between JTAG TDO pin and GND.
		Pullnone	No internal pull-up resistor on JTAG TDO pin.
TmsPin	JTAG TMS pin	***Pullup***	Internally connects a pull-up resistor between JTAG TMS pin and V_{CCAUX}.
		Pulldown	Internally connects a pull-down resistor between JTAG TMS pin and GND.
		Pullnone	No internal pull-up resistor on JTAG TMS pin.
UserID	JTAG User ID register	User string	The 32-bit JTAG User ID register value is loaded during configuration. The default value is all ones, `0xFFFF_FFFF` hexadecimal. To specify another value, enter an 8-character hexadecimal value.
Security	JTAG, SelectMAP, Readback, Partial reconfiguration	***None***	Readback and limited partial reconfiguration are available via the JTAG port or via the SelectMAP interface, if the ***Persist*** option is set to ***Yes***.
		Level1	Readback function is disabled. Limited partial reconfiguration is still available via the JTAG port or via the SelectMAP interface, if the ***Persist*** option is set to ***Yes***.
		Level2	Readback function is disabled. Limited partial reconfiguration is disabled.
CRC	Configuration	**Enable**	***Default.*** Enable CRC checking on the FPGA bitstream. If error detected, FPGA asserts INIT_B Low and DONE pin stays Low.
		Disable	Turn off CRC checking.
Persist	SelectMAP interface pins, BPI mode, Slave mode, Configuration	***No***	All BPI and Slave mode configuration pins are available as user-I/O after configuration.
		Yes	This option is required for Readback and partial reconfiguration using the SelectMAP interface. The SelectMAP interface pins (see Slave Parallel Mode) are reserved after configuration and are not available as user-I/O.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/01/05	1.0	Initial Xilinx release.
03/21/05	1.1	Updated Figure 45. Modified title on Table 39 and Table 45.
11/23/05	2.0	Updated values of On-Chip Differential Termination resistors. Updated Table 7. Updated configuration bitstream sizes for XC3S250E through XC3S1600E in Table 45, Table 51, Table 57, and Table 60. Added DLL Performance Differences Between Steppings. Added Stepping 0 Limitations when Reprogramming via JTAG if FPGA Set for BPI Configuration. Added Stepping 0 limitations when Daisy-Chaining in SPI configuration mode. Added Multiplier/Block RAM Interaction section. Updated Digital Clock Managers (DCMs) section, especially Phase Shifter (PS) portion. Corrected and enhanced the clock infrastructure diagram in Figure 45 and Table 41. Added CCLK Design Considerations section. Added Design Considerations for the HSWAP, M[2:0], and VS[2:0] Pins section. Added Spansion, Winbond, and Macronix to list of SPI Flash vendors in Table 53 and Table 56. Clarified that SPI mode configuration supports Atmel 'C'- and 'D'-series DataFlash. Updated the Programming Support section for SPI Flash PROMs. Added Power-On Precautions if PROM Supply is Last in Sequence, Compatible Flash Families, and BPI Mode Interaction with Right and Bottom Edge Global Clock Inputs sections to BPI configuration mode topic. Updated and amplified Powering Spartan-3E FPGAs section. Added Production Stepping section.
03/22/06	3.0	Upgraded data sheet status to Preliminary. Updated Input Delay Functions and Figure 6. Added clarification that Input-only pins also have Pull-Up and Pull-Down Resistors. Added design note about address setup and hold requirements to Block RAM. Added warning message about software differences between ISE 8.1i, Service Pack 3 and earlier software to FIXED Phase Shift Mode and VARIABLE Phase Shift Mode. Added message about using GCLK1 in DLL Clock Input Connections and Clock Inputs. Updated Figure 45. Added additional information on HSWAP behavior to Pin Behavior During Configuration. Highlighted which pins have configuration pull-up resistors unaffected by HSWAP in Table 46. Updated bitstream image sizes for the XC3S1200E and XC3S1600E in Table 45, Table 51, Table 57, and Table 60. Clarified that 'B'-series Atmel DataFlash SPI PROMs can be used in Commercial temperature range applications in Table 53 and Figure 54. Updated Figure 56. Updated Dynamically Loading Multiple Configuration Images Using MultiBoot Option section. Added design note about BPI daisy-chaining software support to BPI Daisy-Chaining section. Updated JTAG revision codes in Table 67. Added No Internal Charge Pumps or Free-Running Oscillators. Updated information on production stepping differences in Table 71. Updated Software Version Requirements.
04/10/06	3.1	Updated JTAG User ID information. Clarified Note 1, Figure 5. Clarified that Figure 45 shows electrical connectivity and corrected left- and right-edge DCM coordinates. Updated Table 30, Table 31, and Table 32 to show the specific clock line driven by the associated BUFGMUX primitive. Corrected the coordinate locations for the associated BUFGMUX primitives in Table 31 and Table 32. Updated Table 41 to show that the I0-input is the preferred connection to a BUFGMUX.
05/19/06	3.2	Made further clarifying changes to Figure 46, showing both direct inputs to BUFGMUX primitives and to DCMs. Added Atmel AT45DBxxxD-series DataFlash serial PROMs to Table 53. Added details that intermediate FPGAs in a BPI-mode, multi-FPGA configuration daisy-chain must be from either the Spartan-3E or the Virtex-5 FPGA families (see BPI Daisy-Chaining). Added Using JTAG Interface to Communicate to a Configured FPGA Design. Minor updates to Figure 66 and Figure 67. Clarified which Spartan-3E FPGA product options support the Readback feature, shown in Table 68.
05/30/06	3.2.1	Corrected various typos and incorrect links.
10/02/06	3.3	Clarified that the block RAM Readback feature is available either on the -5 speed grade or the Industrial temperature range.
11/09/06	3.4	Updated the description of the Input Delay Functions. The ODDR2 flip-flop with C0 or C1 Alignment is no longer supported. Updated Figure 5. Updated Table 6 for improved PCI input voltage tolerance. Replaced missing text in Clock Buffers/Multiplexers. Updated SPI Flash devices in Table 53. Updated parallel NOR Flash devices in Table 61. Direct, SPI Flash in-system Programming Support was added beginning with ISE 8.1i iMPACT software for STMicro and Atmel SPI PROMs. Updated Table 71 and Table 72 as Stepping 1 is in full production. Freshened various hyper links. Promoted Module 2 to Production status.

DC Electrical Characteristics

In this section, specifications may be designated as Advance, Preliminary, or Production. These terms are defined as follows:

Advance: Initial estimates are based on simulation, early characterization, and/or extrapolation from the characteristics of other families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on characterization. Further changes are not expected.

Production: These specifications are approved once the silicon has been characterized over numerous production lots. Parameter values are considered stable with no future changes expected.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all Spartan®-3E devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.**

Absolute Maximum Ratings

Stresses beyond those listed under Table 73, Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to absolute maximum conditions for extended periods of time adversely affects device reliability.

Table 73: **Absolute Maximum Ratings**

Symbol	Description	Conditions		Min	Max	Units
V_{CCINT}	Internal supply voltage			–0.5	1.32	V
V_{CCAUX}	Auxiliary supply voltage			–0.5	3.00	V
V_{CCO}	Output driver supply voltage			–0.5	3.75	V
V_{REF}	Input reference voltage			–0.5	V_{CCO} + 0.5 (1)	V
V_{IN} (1,2,3,4)	Voltage applied to all User I/O pins and Dual-Purpose pins	Driver in a high-impedance state	Commercial	–0.95	4.4	V
			Industrial	–0.85	4.3	V
	Voltage applied to all Dedicated pins		All temp. ranges	–0.5	V_{CCAUX} + 0.5 (3)	V
I_{IK}	Input clamp current per I/O pin	–0.5 V < V_{IN} < (V_{CCO} + 0.5 V)		–	±100	mA
V_{ESD}	Electrostatic Discharge Voltage	Human body model		–	±2000	V
		Charged device model		–	±500	V
		Machine model		–	±200	V
T_J	Junction temperature			–	125	°C
T_{STG}	Storage temperature			–65	150	°C

Notes:

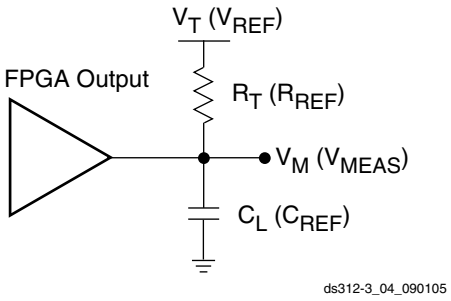
1. Each of the User I/O and Dual-Purpose pins is associated with one of the four banks' V_{CCO} rails. Keeping V_{IN} within 500 mV of the associated V_{CCO} rails or ground rail ensures that the internal diode junctions do not turn on. Table 77 specifies the V_{CCO} range used to evaluate the maximum V_{IN} voltage.
2. Input voltages outside the -0.5V to V_{CCO} + 0.5V (or V_{CCAUX} + 0.5V) voltage range are require the I_{IK} input diode clamp diode rating is met and no more than 100 pins exceed the range simultaneously. Prolonged exposure to such current may compromise device reliability. A sustained current of 10 mA will not compromise device reliability. See XAPP459: *Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins on Spartan-3 Families* for more details.
3. All Dedicated pins (PROG_B, DONE, TCK, TDI, TDO, and TMS) draw power from the V_{CCAUX} rail (2.5V). Meeting the V_{IN} max limit ensures that the internal diode junctions that exist between each of these pins and the V_{CCAUX} rail do not turn on. Table 77 specifies the V_{CCAUX} range used to evaluate the maximum V_{IN} voltage. As long as the V_{IN} max specification is met, oxide stress is not possible.
4. See XAPP459: *Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins on Spartan-3 Families*.
5. For soldering guidelines, see UG112: *Device Packaging and Thermal Characteristics* and XAPP427: *Implementation and Solder Reflow Guidelines for Pb-Free Packages*.

Timing Measurement Methodology

When measuring timing parameters at the programmable I/Os, different signal standards call for different test conditions. Table 95 lists the conditions to use for each standard.

The method for measuring Input timing is as follows: A signal that swings between a Low logic level of V_L and a High logic level of V_H is applied to the Input under test. Some standards also require the application of a bias voltage to the V_{REF} pins of a given bank to properly set the input-switching threshold. The measurement point of the Input signal (V_M) is commonly located halfway between V_L and V_H.

The Output test setup is shown in Figure 72. A termination voltage V_T is applied to the termination resistor R_T, the other end of which is connected to the Output. For each standard, R_T and V_T generally take on the standard values recommended for minimizing signal reflections. If the standard does not ordinarily use terminations (e.g., LVCMOS, LVTTL), then R_T is set to 1MΩ to indicate an open connection, and V_T is set to zero. The same measurement point (V_M) that was used at the Input is also used at the Output.



Notes:

1. The names shown in parentheses are used in the IBIS file.

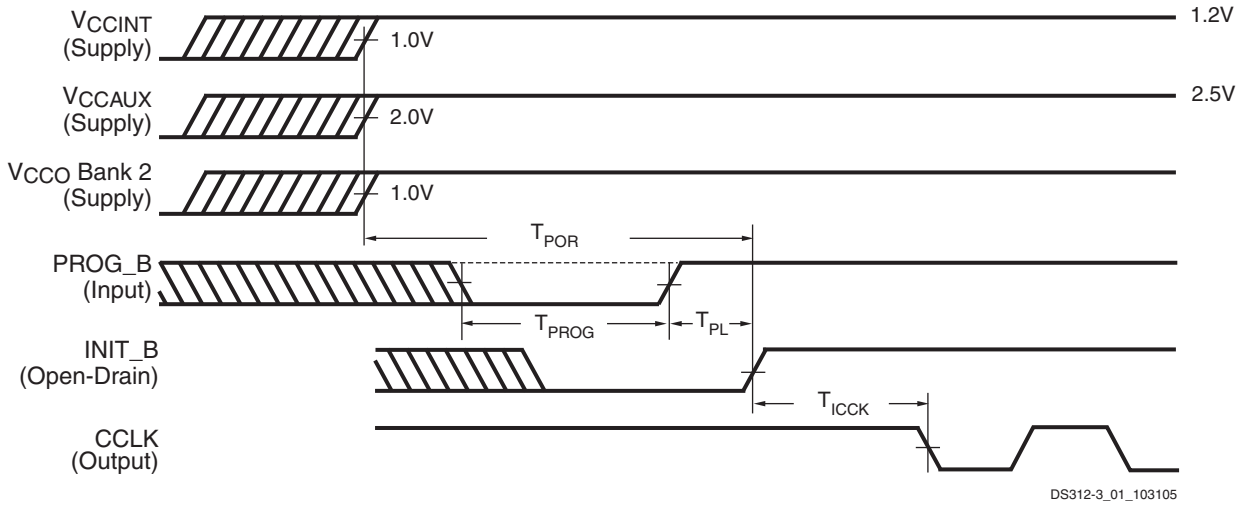
Figure 72: **Output Test Setup**

Table 95: **Test Methods for Timing Measurement at I/Os**

Signal Standard (IOSTANDARD)		Inputs			Outputs		Inputs and Outputs
		V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
Single-Ended							
LVTTL		-	0	3.3	1M	0	1.4
LVCMOS33		-	0	3.3	1M	0	1.65
LVCMOS25		-	0	2.5	1M	0	1.25
LVCMOS18		-	0	1.8	1M	0	0.9
LVCMOS15		-	0	1.5	1M	0	0.75
LVCMOS12		-	0	1.2	1M	0	0.6
PCI33_3	Rising	-	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
PCI66_3	Rising	-	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
HSTL_I_18		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
HSTL_III_18		1.1	V_{REF} – 0.5	V_{REF} + 0.5	50	1.8	V_{REF}
SSTL18_I		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
SSTL2_I		1.25	V_{REF} – 0.75	V_{REF} + 0.75	50	1.25	V_{REF}
Differential							
LVDS_25		-	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
BLVDS_25		-	V_{ICM} – 0.125	V_{ICM} + 0.125	1M	0	V_{ICM}
MINI_LVDS_25		-	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
LVPECL_25		-	V_{ICM} – 0.3	V_{ICM} + 0.3	1M	0	V_{ICM}
RSDS_25		-	V_{ICM} – 0.1	V_{ICM} + 0.1	50	1.2	V_{ICM}

Configuration and JTAG Timing

General Configuration Power-On/Reconfigure Timing



Notes:

1. The V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies may be applied in any order.
2. The Low-going pulse on PROG_B is optional after power-on but necessary for reconfiguration without a power cycle.
3. The rising edge of INIT_B samples the voltage levels applied to the mode pins (M0 - M2).

Figure 73: **Waveforms for Power-On and the Beginning of Configuration**

Table 111: **Power-On Timing and the Beginning of Configuration**

Symbol	Description	Device	All Speed Grades		Units
			Min	Max	
T_{POR}(2)	The time from the application of V_{CCINT}, V_{CCAUX}, and V_{CCO} Bank 2 supply voltage ramps (whichever occurs last) to the rising transition of the INIT_B pin	XC3S100E	-	5	ms
		XC3S250E	-	5	ms
		XC3S500E	-	5	ms
		XC3S1200E	-	5	ms
		XC3S1600E	-	7	ms
T_{PROG}	The width of the low-going pulse on the PROG_B pin	All	0.5	-	µs
T_{PL}(2)	The time from the rising edge of the PROG_B pin to the rising transition on the INIT_B pin	XC3S100E	-	0.5	ms
		XC3S250E	-	0.5	ms
		XC3S500E	-	1	ms
		XC3S1200E	-	2	ms
		XC3S1600E	-	2	ms
T_{INIT}	Minimum Low pulse width on INIT_B output	All	250	-	ns
T_{ICCK}(3)	The time from the rising edge of the INIT_B pin to the generation of the configuration clock signal at the CCLK output pin	All	0.5	4.0	µs

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 77. This means power must be applied to all V_{CCINT}, V_{CCO}, and V_{CCAUX} lines.
2. Power-on reset and the clearing of configuration memory occurs during this period.
3. This specification applies only to the Master Serial, SPI, BPI-Up, and BPI-Down modes.

VQ100 Footprint

In Figure 80, note pin 1 indicator in top-left corner and logo orientation.

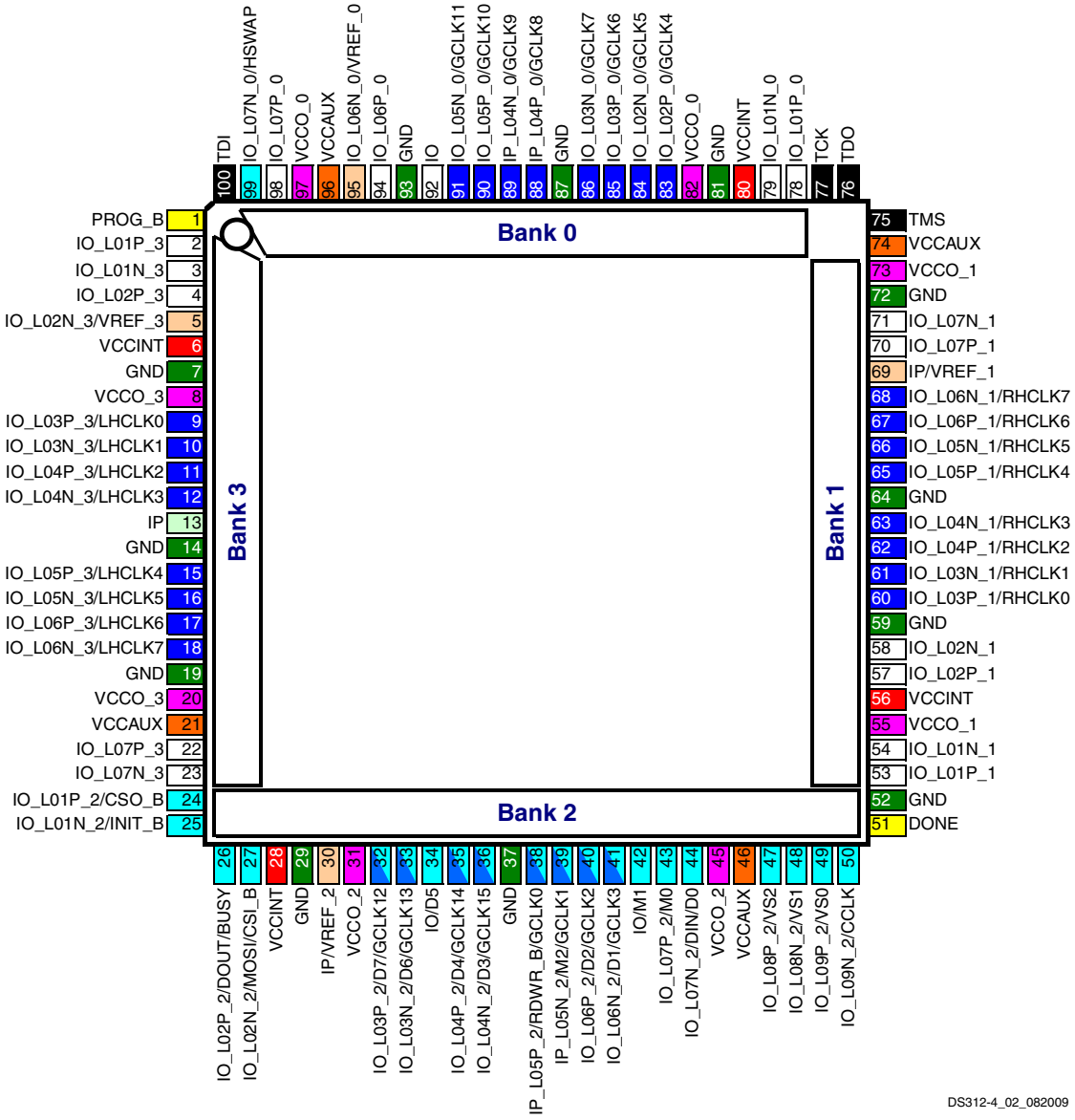


Figure 80: **VQ100 Package Footprint (top view)**

16	**I/O:** Unrestricted, general-purpose user I/O	21	**DUAL:** Configuration pin, then possible user-I/O	4	**VREF:** User I/O or input voltage reference for bank
1	**INPUT:** Unrestricted, general-purpose input pin	24	**CLK:** User I/O, input, or global buffer input	8	**VCCO:** Output voltage supply for bank
2	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	4	**VCCINT:** Internal core supply voltage (+1.2V)
0	**N.C.:** Not connected	12	**GND:** Ground	4	**VCCAUX:** Auxiliary supply voltage (+2.5V)

CP132 Footprint

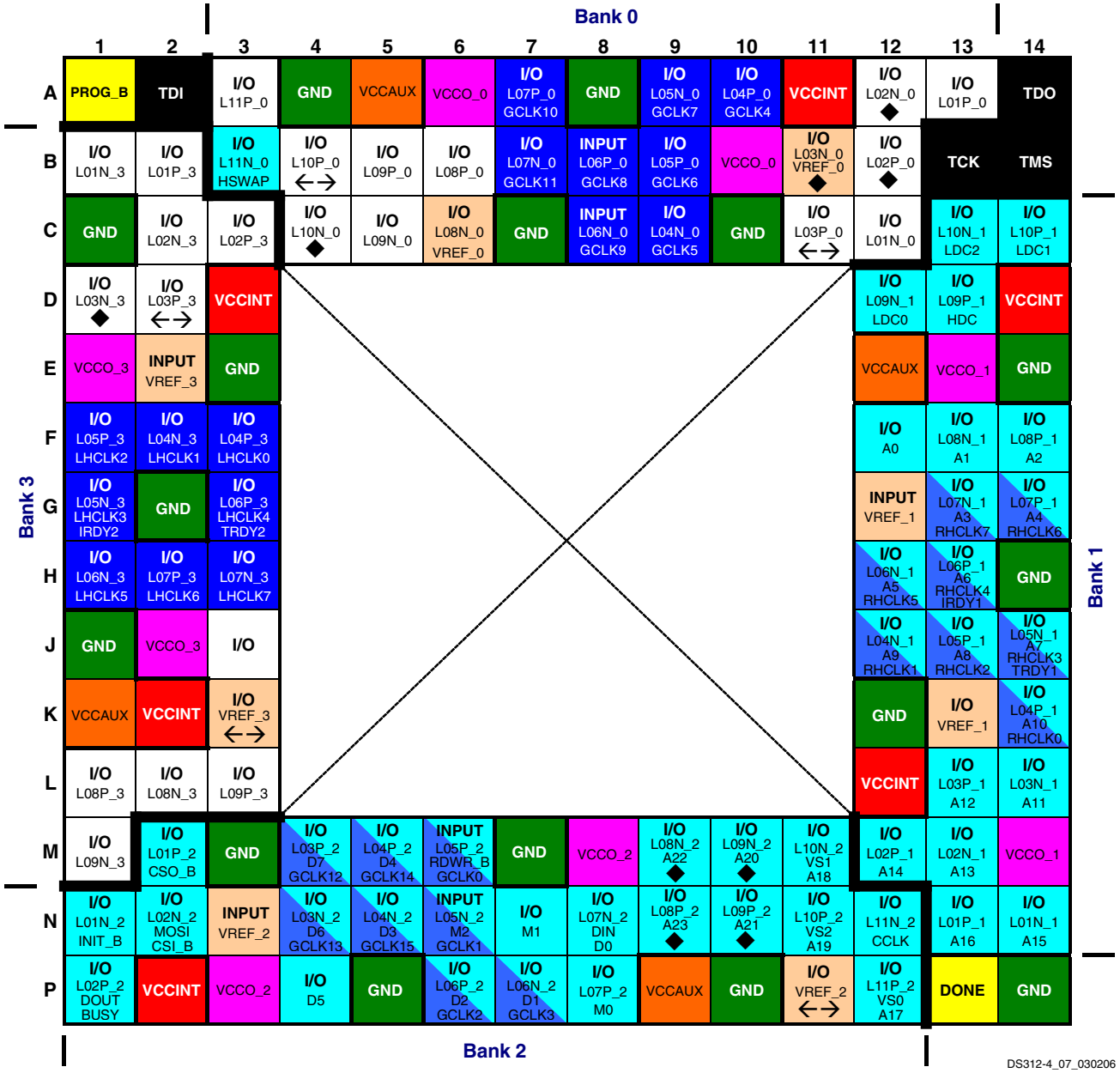


Figure 81: **CP132 Package Footprint (top view)**

16-22	**I/O:** Unrestricted, general-purpose user I/O	42-46	**DUAL:** Configuration pin, then possible user I/O	7-8	**VREF:** User I/O or input voltage reference for bank
0-2	**INPUT:** Unrestricted, general-purpose input pin	16	**CLK:** User I/O, input, or global buffer input	8	**VCCO:** Output voltage supply for bank
2	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	6	**VCCINT:** Internal core supply voltage (+1.2V)
9	**N.C.:** Unconnected balls on the XC3S100E FPGA (◆)	16	**GND:** Ground	4	**VCCAUX:** Auxiliary supply voltage (+2.5V)

PQ208: 208-pin Plastic Quad Flat Package

The 208-pin plastic quad flat package, PQ208, supports two different Spartan-3E FPGAs, including the XC3S250E and the XC3S500E.

Table 141 lists all the PQ208 package pins. They are sorted by bank number and then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at:

http://www.xilinx.com/support/documentation/data_sheets/s3e_pin.zip

Pinout Table

Table 141: **PQ208 Package Pinout**

Bank	XC3S250E XC3S500E Pin Name	PQ208 Pin	Type
0	IO	P187	I/O
0	IO/VREF_0	P179	VREF
0	IO_L01N_0	P161	I/O
0	IO_L01P_0	P160	I/O
0	IO_L02N_0/VREF_0	P163	VREF
0	IO_L02P_0	P162	I/O
0	IO_L03N_0	P165	I/O
0	IO_L03P_0	P164	I/O
0	IO_L04N_0/VREF_0	P168	VREF
0	IO_L04P_0	P167	I/O
0	IO_L05N_0	P172	I/O
0	IO_L05P_0	P171	I/O
0	IO_L07N_0/GCLK5	P178	GCLK
0	IO_L07P_0/GCLK4	P177	GCLK
0	IO_L08N_0/GCLK7	P181	GCLK
0	IO_L08P_0/GCLK6	P180	GCLK
0	IO_L10N_0/GCLK11	P186	GCLK
0	IO_L10P_0/GCLK10	P185	GCLK
0	IO_L11N_0	P190	I/O
0	IO_L11P_0	P189	I/O
0	IO_L12N_0/VREF_0	P193	VREF
0	IO_L12P_0	P192	I/O
0	IO_L13N_0	P197	I/O
0	IO_L13P_0	P196	I/O
0	IO_L14N_0/VREF_0	P200	VREF
0	IO_L14P_0	P199	I/O
0	IO_L15N_0	P203	I/O

Table 141: **PQ208 Package Pinout *(Cont'd)***

Bank	XC3S250E XC3S500E Pin Name	PQ208 Pin	Type
0	IO_L15P_0	P202	I/O
0	IO_L16N_0/HSWAP	P206	DUAL
0	IO_L16P_0	P205	I/O
0	IP	P159	INPUT
0	IP	P169	INPUT
0	IP	P194	INPUT
0	IP	P204	INPUT
0	IP_L06N_0	P175	INPUT
0	IP_L06P_0	P174	INPUT
0	IP_L09N_0/GCLK9	P184	GCLK
0	IP_L09P_0/GCLK8	P183	GCLK
0	VCCO_0	P176	VCCO
0	VCCO_0	P191	VCCO
0	VCCO_0	P201	VCCO
1	IO_L01N_1/A15	P107	DUAL
1	IO_L01P_1/A16	P106	DUAL
1	IO_L02N_1/A13	P109	DUAL
1	IO_L02P_1/A14	P108	DUAL
1	IO_L03N_1/VREF_1	P113	VREF
1	IO_L03P_1	P112	I/O
1	IO_L04N_1	P116	I/O
1	IO_L04P_1	P115	I/O
1	IO_L05N_1/A11	P120	DUAL
1	IO_L05P_1/A12	P119	DUAL
1	IO_L06N_1/VREF_1	P123	VREF
1	IO_L06P_1	P122	I/O
1	IO_L07N_1/A9/RHCLK1	P127	RHCLK/DUAL
1	IO_L07P_1/A10/RHCLK0	P126	RHCLK/DUAL
1	IO_L08N_1/A7/RHCLK3	P129	RHCLK/DUAL
1	IO_L08P_1/A8/RHCLK2	P128	RHCLK/DUAL
1	IO_L09N_1/A5/RHCLK5	P133	RHCLK/DUAL
1	IO_L09P_1/A6/RHCLK4	P132	RHCLK/DUAL
1	IO_L10N_1/A3/RHCLK7	P135	RHCLK/DUAL
1	IO_L10P_1/A4/RHCLK6	P134	RHCLK/DUAL
1	IO_L11N_1/A1	P138	DUAL
1	IO_L11P_1/A2	P137	DUAL
1	IO_L12N_1/A0	P140	DUAL
1	IO_L12P_1	P139	I/O
1	IO_L13N_1	P145	I/O
1	IO_L13P_1	P144	I/O
1	IO_L14N_1	P147	I/O
1	IO_L14P_1	P146	I/O

Table 141: **PQ208 Package Pinout *(Cont'd)***

Bank	XC3S250E XC3S500E Pin Name	PQ208 Pin	Type
3	IO_L14P_3	P41	I/O
3	IO_L15N_3	P48	I/O
3	IO_L15P_3	P47	I/O
3	IO_L16N_3	P50	I/O
3	IO_L16P_3	P49	I/O
3	IP	P6	INPUT
3	IP	P14	INPUT
3	IP	P26	INPUT
3	IP	P32	INPUT
3	IP	P43	INPUT
3	IP	P51	INPUT
3	IP/VREF_3	P20	VREF
3	VCCO_3	P21	VCCO
3	VCCO_3	P38	VCCO
3	VCCO_3	P46	VCCO
GND	GND	P10	GND
GND	GND	P17	GND
GND	GND	P27	GND
GND	GND	P37	GND
GND	GND	P52	GND
GND	GND	P53	GND
GND	GND	P70	GND
GND	GND	P79	GND
GND	GND	P85	GND
GND	GND	P95	GND
GND	GND	P105	GND
GND	GND	P121	GND
GND	GND	P131	GND
GND	GND	P141	GND
GND	GND	P156	GND
GND	GND	P173	GND
GND	GND	P182	GND
GND	GND	P188	GND
GND	GND	P198	GND
GND	GND	P208	GND
VCCAUX	DONE	P104	CONFIG
VCCAUX	PROG_B	P1	CONFIG
VCCAUX	TCK	P158	JTAG
VCCAUX	TDI	P207	JTAG
VCCAUX	TDO	P157	JTAG
VCCAUX	TMS	P155	JTAG
VCCAUX	VCCAUX	P7	VCCAUX
VCCAUX	VCCAUX	P44	VCCAUX

Table 141: **PQ208 Package Pinout *(Cont'd)***

Bank	XC3S250E XC3S500E Pin Name	PQ208 Pin	Type
VCCAUX	VCCAUX	P66	VCCAUX
VCCAUX	VCCAUX	P92	VCCAUX
VCCAUX	VCCAUX	P111	VCCAUX
VCCAUX	VCCAUX	P149	VCCAUX
VCCAUX	VCCAUX	P166	VCCAUX
VCCAUX	VCCAUX	P195	VCCAUX
VCCINT	VCCINT	P13	VCCINT
VCCINT	VCCINT	P67	VCCINT
VCCINT	VCCINT	P117	VCCINT
VCCINT	VCCINT	P170	VCCINT

Table 148: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S500E Pin Name	XC3S1200E Pin Name	XC3S1600E Pin Name	FG320 Ball	Type
0	IO_L08P_0	IO_L08P_0	IO_L08P_0	E11	I/O
0	IO_L09N_0	IO_L09N_0	IO_L09N_0	D11	I/O
0	IO_L09P_0	IO_L09P_0	IO_L09P_0	C11	I/O
0	IO_L11N_0/GCLK5	IO_L11N_0/GCLK5	IO_L11N_0/GCLK5	E10	GCLK
0	IO_L11P_0/GCLK4	IO_L11P_0/GCLK4	IO_L11P_0/GCLK4	D10	GCLK
0	IO_L12N_0/GCLK7	IO_L12N_0/GCLK7	IO_L12N_0/GCLK7	A10	GCLK
0	IO_L12P_0/GCLK6	IO_L12P_0/GCLK6	IO_L12P_0/GCLK6	B10	GCLK
0	IO_L14N_0/GCLK11	IO_L14N_0/GCLK11	IO_L14N_0/GCLK11	D9	GCLK
0	IO_L14P_0/GCLK10	IO_L14P_0/GCLK10	IO_L14P_0/GCLK10	C9	GCLK
0	IO_L15N_0	IO_L15N_0	IO_L15N_0	F9	I/O
0	IO_L15P_0	IO_L15P_0	IO_L15P_0	E9	I/O
0	IO_L17N_0	IO_L17N_0	IO_L17N_0	F8	I/O
0	IO_L17P_0	IO_L17P_0	IO_L17P_0	E8	I/O
0	IO_L18N_0/VREF_0	IO_L18N_0/VREF_0	IO_L18N_0/VREF_0	D7	VREF
0	IO_L18P_0	IO_L18P_0	IO_L18P_0	C7	I/O
0	IO_L19N_0/VREF_0	IO_L19N_0/VREF_0	IO_L19N_0/VREF_0	E7	VREF
0	IO_L19P_0	IO_L19P_0	IO_L19P_0	F7	I/O
0	IO_L20N_0	IO_L20N_0	IO_L20N_0	A6	I/O
0	IO_L20P_0	IO_L20P_0	IO_L20P_0	B6	I/O
0	N.C. (◆)	IO_L21N_0	IO_L21N_0	E6	**500E:** N.C. **1200E:** I/O **1600E:** I/O
0	N.C. (◆)	IO_L21P_0	IO_L21P_0	D6	**500E:** N.C. **1200E:** I/O **1600E:** I/O
0	IO_L23N_0/VREF_0	IO_L23N_0/VREF_0	IO_L23N_0/VREF_0	D5	VREF
0	IO_L23P_0	IO_L23P_0	IO_L23P_0	C5	I/O
0	IO_L24N_0	IO_L24N_0	IO_L24N_0	B4	I/O
0	IO_L24P_0	IO_L24P_0	IO_L24P_0	A4	I/O
0	IO_L25N_0/HSWAP	IO_L25N_0/HSWAP	IO_L25N_0/HSWAP	B3	DUAL
0	IO_L25P_0	IO_L25P_0	IO_L25P_0	C3	I/O
0	IP	IP	IP	A3	INPUT
0	IP	IP	IP	C15	INPUT
0	IP_L02N_0	IP_L02N_0	IP_L02N_0	A15	INPUT
0	IP_L02P_0	IP_L02P_0	IP_L02P_0	B15	INPUT
0	IP_L07N_0	IP_L07N_0	IP_L07N_0	D12	INPUT
0	IP_L07P_0	IP_L07P_0	IP_L07P_0	C12	INPUT
0	IP_L10N_0	IP_L10N_0	IP_L10N_0	G10	INPUT
0	IP_L10P_0	IP_L10P_0	IP_L10P_0	F10	INPUT
0	IP_L13N_0/GCLK9	IP_L13N_0/GCLK9	IP_L13N_0/GCLK9	B9	GCLK
0	IP_L13P_0/GCLK8	IP_L13P_0/GCLK8	IP_L13P_0/GCLK8	B8	GCLK
0	IP_L16N_0	IP_L16N_0	IP_L16N_0	D8	INPUT
0	IP_L16P_0	IP_L16P_0	IP_L16P_0	C8	INPUT
0	IP_L22N_0	IP_L22N_0	IP_L22N_0	B5	INPUT
0	IP_L22P_0	IP_L22P_0	IP_L22P_0	A5	INPUT

Table 154: **FG484 Package Pinout *(Cont'd)***

Bank	XC3S1600E Pin Name	FG484 Ball	Type
GND	GND	E10	GND
GND	GND	E13	GND
GND	GND	F6	GND
GND	GND	F17	GND
GND	GND	G2	GND
GND	GND	G21	GND
GND	GND	J4	GND
GND	GND	J9	GND
GND	GND	J12	GND
GND	GND	J14	GND
GND	GND	J19	GND
GND	GND	K10	GND
GND	GND	K12	GND
GND	GND	L2	GND
GND	GND	L6	GND
GND	GND	L9	GND
GND	GND	L13	GND
GND	GND	M10	GND
GND	GND	M14	GND
GND	GND	M17	GND
GND	GND	M21	GND
GND	GND	N11	GND
GND	GND	N13	GND
GND	GND	P4	GND
GND	GND	P9	GND
GND	GND	P11	GND
GND	GND	P14	GND
GND	GND	P19	GND
GND	GND	T2	GND
GND	GND	T21	GND
GND	GND	U6	GND
GND	GND	U17	GND
GND	GND	V10	GND
GND	GND	V13	GND
GND	GND	Y3	GND
GND	GND	Y20	GND
GND	GND	AA7	GND
GND	GND	AA16	GND

Table 154: **FG484 Package Pinout *(Cont'd)***

Bank	XC3S1600E Pin Name	FG484 Ball	Type
GND	GND	AB1	GND
GND	GND	AB12	GND
GND	GND	AB22	GND
VCCAUX	DONE	AA21	CONFIG
VCCAUX	PROG_B	B1	CONFIG
VCCAUX	TCK	E17	JTAG
VCCAUX	TDI	B2	JTAG
VCCAUX	TDO	B20	JTAG
VCCAUX	TMS	D19	JTAG
VCCAUX	VCCAUX	D12	VCCAUX
VCCAUX	VCCAUX	E5	VCCAUX
VCCAUX	VCCAUX	E18	VCCAUX
VCCAUX	VCCAUX	K14	VCCAUX
VCCAUX	VCCAUX	L4	VCCAUX
VCCAUX	VCCAUX	M19	VCCAUX
VCCAUX	VCCAUX	N9	VCCAUX
VCCAUX	VCCAUX	V5	VCCAUX
VCCAUX	VCCAUX	V18	VCCAUX
VCCAUX	VCCAUX	W11	VCCAUX
VCCINT	VCCINT	J10	VCCINT
VCCINT	VCCINT	K9	VCCINT
VCCINT	VCCINT	K11	VCCINT
VCCINT	VCCINT	K13	VCCINT
VCCINT	VCCINT	L10	VCCINT
VCCINT	VCCINT	L11	VCCINT
VCCINT	VCCINT	L12	VCCINT
VCCINT	VCCINT	L14	VCCINT
VCCINT	VCCINT	M9	VCCINT
VCCINT	VCCINT	M11	VCCINT
VCCINT	VCCINT	M12	VCCINT
VCCINT	VCCINT	M13	VCCINT
VCCINT	VCCINT	N10	VCCINT
VCCINT	VCCINT	N12	VCCINT
VCCINT	VCCINT	N14	VCCINT
VCCINT	VCCINT	P13	VCCINT

User I/Os by Bank

Table 155 indicates how the 304 available user-I/O pins are distributed between the four I/O banks on the FG484 package.

AUTOMOTIVE APPLICATIONS DISCLAIMER

XILINX PRODUCTS ARE NOT DESIGNED OR INTENDED TO BE FAIL-SAFE, OR FOR USE IN ANY APPLICATION REQUIRING FAIL-SAFE PERFORMANCE, SUCH AS APPLICATIONS RELATED TO: (I) THE DEPLOYMENT OF AIRBAGS, (II) CONTROL OF A VEHICLE, UNLESS THERE IS A FAIL-SAFE OR REDUNDANCY FEATURE (WHICH DOES NOT INCLUDE USE OF SOFTWARE IN THE XILINX DEVICE TO IMPLEMENT THE REDUNDANCY) AND A WARNING SIGNAL UPON FAILURE TO THE OPERATOR, OR (III) USES THAT COULD LEAD TO DEATH OR PERSONAL INJURY. CUSTOMER ASSUMES THE SOLE RISK AND LIABILITY OF ANY USE OF XILINX PRODUCTS IN SUCH APPLICATIONS.