AMD Xilinx - XC3S250E-4VQ100I Datasheet

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	612
Number of Logic Elements/Cells	5508
Total RAM Bits	221184
Number of I/O	66
Number of Gates	250000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s250e-4vq100i

IOBs Organized into Banks

The Spartan-3E architecture organizes IOBs into four I/O banks as shown in Figure 13. Each bank maintains separate V_{CCO} and V_{REF} supplies. The separate supplies allow each bank to independently set V_{CCO}. Similarly, the V_{REF} supplies can be set for each bank. Refer to Table 6 and Table 7 for V_{CCO} and V_{REF} requirements.

When working with Spartan-3E devices, most of the differential I/O standards are compatible and can be combined within any given bank. Each bank can support any two of the following differential standards: LVDS_25 outputs, MINI_LVDS_25 outputs, and RSDS_25 outputs. As an example, LVDS_25 outputs, RSDS_25 outputs, and any other differential inputs while using on-chip differential termination are a valid combination. A combination not allowed is a single bank with LVDS_25 outputs, RSDS_25 outputs, and MINI_LVDS_25 outputs.

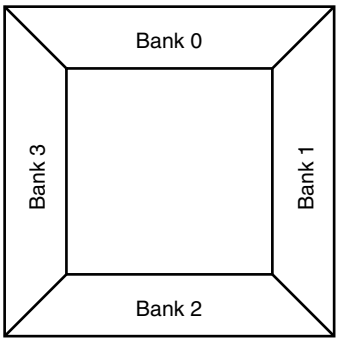

Figure 13: **Spartan-3E I/O Banks (top view)**

I/O Banking Rules

When assigning I/Os to banks, these V_{CCO} rules must be followed:

1. All V_{CCO} pins on the FPGA must be connected even if a bank is unused.
2. All V_{CCO} lines associated within a bank must be set to the same voltage level.
3. The V_{CCO} levels used by all standards assigned to the I/Os of any given bank must agree. The Xilinx development software checks for this. Table 6 and Table 7 describe how different standards use the V_{CCO} supply.
4. If a bank does not have any V_{CCO} requirements, connect V_{CCO} to an available voltage, such as 2.5V or 3.3V. Some configuration modes might place additional V_{CCO} requirements. Refer to Configuration for more information.

If any of the standards assigned to the Inputs of the bank use V_{REF}, then the following additional rules must be observed:

1. All V_{REF} pins must be connected within a bank.
2. All V_{REF} lines associated with the bank must be set to the same voltage level.
3. The V_{REF} levels used by all standards assigned to the Inputs of the bank must agree. The Xilinx development software checks for this. Table 6 describes how different standards use the V_{REF} supply.

If V_{REF} is not required to bias the input switching thresholds, all associated V_{REF} pins within the bank can be used as user I/Os or input pins.

Package Footprint Compatibility

Sometimes, applications outgrow the logic capacity of a specific Spartan-3E FPGA. Fortunately, the Spartan-3E family is designed so that multiple part types are available in pin-compatible package footprints, as described in Module 4, Pinout Descriptions. In some cases, there are subtle differences between devices available in the same footprint. These differences are outlined for each package, such as pins that are unconnected on one device but connected on another in the same package or pins that are dedicated inputs on one package but full I/O on another. When designing the printed circuit board (PCB), plan for potential future upgrades and package migration.

The Spartan-3E family is not pin-compatible with any previous Xilinx FPGA family.

Dedicated Inputs

Dedicated Inputs are IOBs used only as inputs. Pin names designate a Dedicated Input if the name starts with *IP*, for example, IP or IP_Lxxx_x. Dedicated inputs retain the full functionality of the IOB for input functions with a single exception for differential inputs (IP_Lxxx_x). For the differential Dedicated Inputs, the on-chip differential termination is not available. To replace the on-chip differential termination, choose a differential pair that supports outputs (IO_Lxxx_x) or use an external 100Ω termination resistor on the board.

ESD Protection

Clamp diodes protect all device pads against damage from Electro-Static Discharge (ESD) as well as excessive voltage transients. Each I/O has two clamp diodes: one diode extends P-to-N from the pad to V_{CCO} and a second diode extends N-to-P from the pad to GND. During operation, these diodes are normally biased in the off state. These clamp diodes are always connected to the pad, regardless of the signal standard selected. The presence of diodes limits the ability of Spartan-3E I/Os to tolerate high signal voltages. The V_{IN} absolute maximum rating in Table 73 of Module 3, DC and Switching Characteristics specifies the voltage range that I/Os can tolerate.

The SLICEM pair supports two additional functions:

- Two 16x1 distributed RAM blocks, RAM16
- Two 16-bit shift registers, SRL16

Each of these elements is described in more detail in the following sections.

Logic Cells

The combination of a LUT and a storage element is known as a "Logic Cell". The additional features in a slice, such as the wide multiplexers, carry logic, and arithmetic gates, add to the capacity of a slice, implementing logic that would otherwise require additional LUTs. Benchmarks have shown that the overall slice is equivalent to 2.25 simple logic cells. This calculation provides the equivalent logic cell count shown in Table 9.

Slice Details

Figure 15 is a detailed diagram of the SLICEM. It represents a superset of the elements and connections to be found in all slices. The dashed and gray lines (blue when viewed in color) indicate the resources found only in the SLICEM and not in the SLICEL.

Each slice has two halves, which are differentiated as top and bottom to keep them distinct from the upper and lower slices in a CLB. The control inputs for the clock (CLK), Clock Enable (CE), Slice Write Enable (SLICEWE1), and Reset/Set (RS) are shared in common between the two halves.

The LUTs located in the top and bottom portions of the slice are referred to as "G" and "F", respectively, or the "G-LUT" and the "F-LUT". The storage elements in the top and bottom portions of the slice are called FFY and FFX, respectively.

Each slice has two multiplexers with F5MUX in the bottom portion of the slice and FiMUX in the top portion. Depending on the slice, the FiMUX takes on the name F6MUX, F7MUX, or F8MUX, according to its position in the multiplexer chain. The lower SLICEL and SLICEM both have an F6MUX. The upper SLICEM has an F7MUX, and the upper SLICEL has an F8MUX.

The carry chain enters the bottom of the slice as CIN and exits at the top as COUT. Five multiplexers control the chain: CYINIT, CY0F, and CYMUXF in the bottom portion and CY0G and CYMUXG in the top portion. The dedicated arithmetic logic includes the exclusive-OR gates XORF and XORG (bottom and top portions of the slice, respectively) as well as the AND gates FAND and GAND (bottom and top portions, respectively).

See Table 10 for a description of all the slice input and output signals.

Table 10: **Slice Inputs and Outputs**

Name	Location	Direction	Description
F[4:1]	SLICEL/M Bottom	Input	F-LUT and FAND inputs
G[4:1]	SLICEL/M Top	Input	G-LUT and GAND inputs or Write Address (SLICEM)
BX	SLICEL/M Bottom	Input	Bypass to or output (SLICEM) or storage element, or control input to F5MUX, input to carry logic, or data input to RAM (SLICEM)
BY	SLICEL/M Top	Input	Bypass to or output (SLICEM) or storage element, or control input to FiMUX, input to carry logic, or data input to RAM (SLICEM)
BXOUT	SLICEM Bottom	Output	BX bypass output
BYOUT	SLICEM Top	Output	BY bypass output
ALTDIG	SLICEM Top	Input	Alternate data input to RAM
DIG	SLICEM Top	Output	ALTDIG or SHIFTIN bypass output
SLICEWE1	SLICEM Common	Input	RAM Write Enable
F5	SLICEL/M Bottom	Output	Output from F5MUX; direct feedback to FiMUX
FXINA	SLICEL/M Top	Input	Input to FiMUX; direct feedback from F5MUX or another FiMUX
FXINB	SLICEL/M Top	Input	Input to FiMUX; direct feedback from F5MUX or another FiMUX
Fi	SLICEL/M Top	Output	Output from FiMUX; direct feedback to another FiMUX
CE	SLICEL/M Common	Input	FFX/Y Clock Enable
SR	SLICEL/M Common	Input	FFX/Y Set or Reset or RAM Write Enable (SLICEM)
CLK	SLICEL/M Common	Input	FFX/Y Clock or RAM Clock (SLICEM)
SHIFTIN	SLICEM Top	Input	Data input to G-LUT RAM

Carry and Arithmetic Logic

For additional information, refer to the “Using Carry and Arithmetic Logic” chapter in UG331.

The carry chain, together with various dedicated arithmetic logic gates, support fast and efficient implementations of math operations. The carry logic is automatically used for most arithmetic functions in a design. The gates and multiplexers of the carry and arithmetic logic can also be used for general-purpose logic, including simple wide Boolean functions.

The carry chain enters the slice as CIN and exits as COUT, controlled by several multiplexers. The carry chain connects directly from one CLB to the CLB above. The carry chain can be initialized at any point from the BX (or BY) inputs.

The dedicated arithmetic logic includes the exclusive-OR gates XORF and XORG (upper and lower portions of the slice, respectively) as well as the AND gates GAND and FAND (upper and lower portions, respectively). These gates work in conjunction with the LUTs to implement efficient arithmetic functions, including counters and multipliers, typically at two bits per slice. See Figure 22 and Table 14.

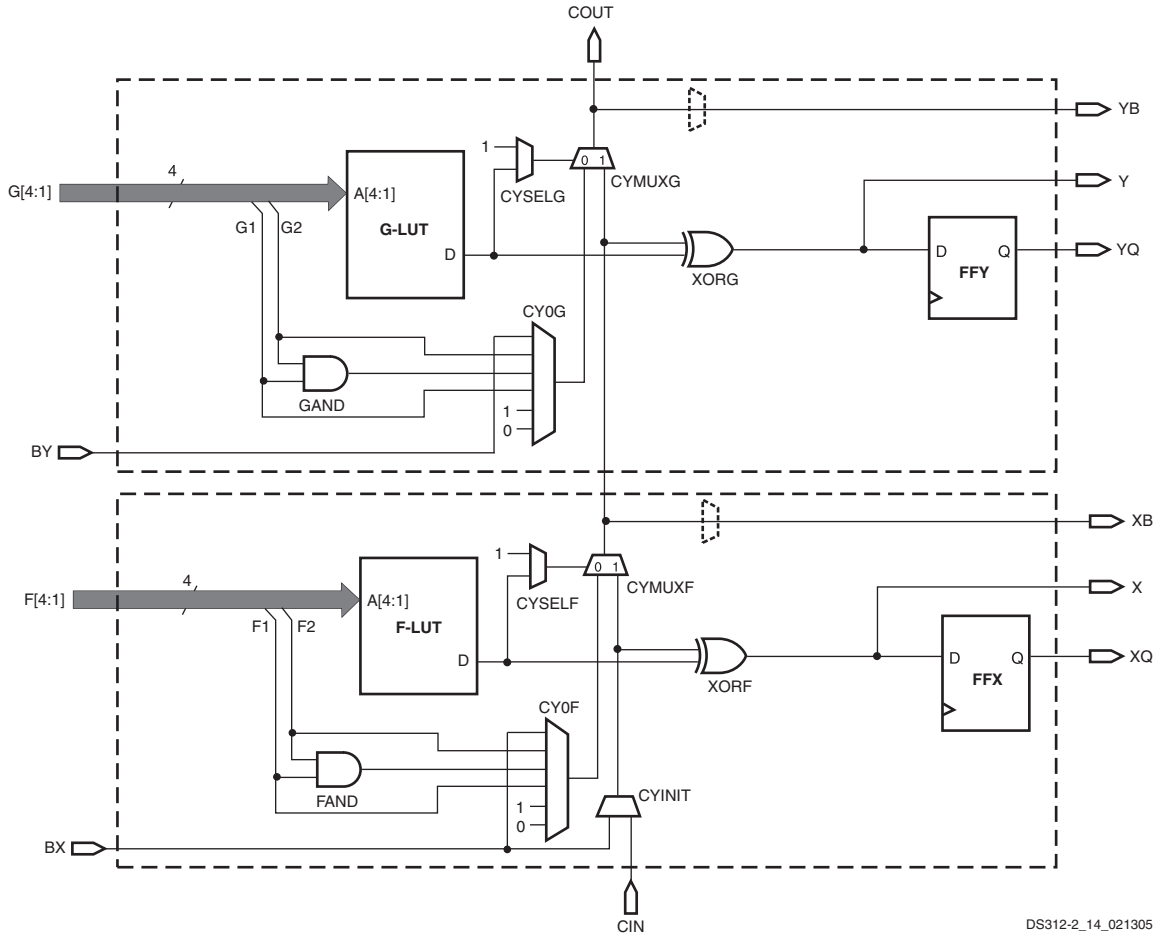

Figure 22: **Carry Logic**

Table 14: **Carry Logic Functions**

Function	Description
CYINIT	Initializes carry chain for a slice. Fixed selection of: · CIN carry input from the slice below · BX input
CY0F	Carry generation for bottom half of slice. Fixed selection of: · F1 or F2 inputs to the LUT (both equal 1 when a carry is to be generated) · FAND gate for multiplication · BX input for carry initialization · Fixed 1 or 0 input for use as a simple Boolean function

initialized distributed RAM contents are not disturbed during the configuration process.

The distributed RAM is useful for smaller amounts of memory. Larger memory requirements can use the dedicated 18Kbit RAM blocks (see Block RAM).

Shift Registers

For additional information, refer to the “Using Look-Up Tables as Shift Registers (SRL16)” chapter in UG331.

It is possible to program each SLICEM LUT as a 16-bit shift register (see Figure 28). Used in this way, each LUT can delay serial data anywhere from 1 to 16 clock cycles without using any of the dedicated flip-flops. The resulting programmable delays can be used to balance the timing of data pipelines.

The SLICEM LUTs cascade from the G-LUT to the F-LUT through the DIFMUX (see Figure 15). SHIFTIN and SHIFTOUT lines cascade a SLICEM to the SLICEM below to form larger shift registers. The four SLICEM LUTs of a single CLB can be combined to produce delays up to 64 clock cycles. It is also possible to combine shift registers across more than one CLB.

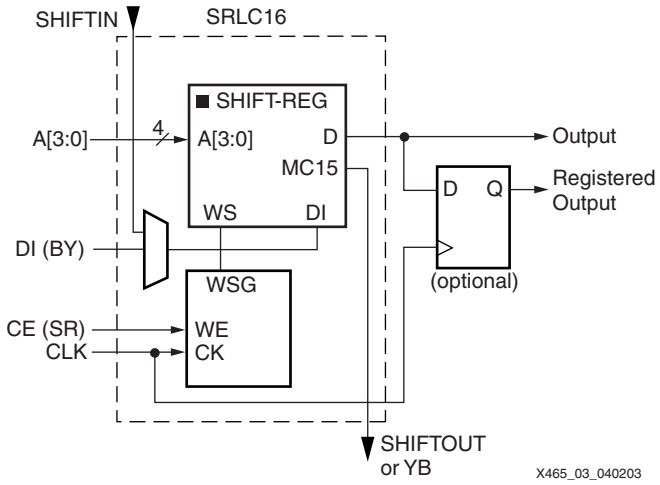

Figure 28: **Logic Cell SRL16 Structure**

Each shift register provides a shift output MC15 for the last bit in each LUT, in addition to providing addressable access to any bit in the shift register through the normal D output. The address inputs A[3:0] are the same as the distributed RAM address lines, which come from the LUT inputs F[4:1] or G[4:1]. At the end of the shift register, the CLB flip-flop can be used to provide one more shift delay for the addressable bit.

The shift register element is known as the SRL16 (Shift Register LUT 16-bit), with a ‘C’ added to signify a cascade ability (Q15 output) and ‘E’ to indicate a Clock Enable. See Figure 29 for an example of the SRLC16E component.

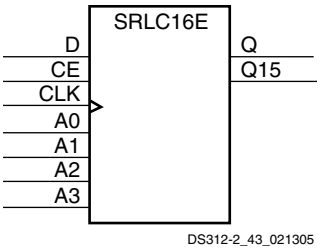

Figure 29: **SRL16 Shift Register Component with Cascade and Clock Enable**

The functionality of the shift register is shown in Table 20. The SRL16 shifts on the rising edge of the clock input when the Clock Enable control is High. This shift register cannot be initialized either during configuration or during operation except by shifting data into it. The clock enable and clock inputs are shared between the two LUTs in a SLICEM. The clock enable input is automatically kept active if unused.

Table 20: **SRL16 Shift Register Function**

Inputs				Outputs	
Am	**CLK**	**CE**	**D**	**Q**	**Q15**
Am	X	0	X	Q[Am]	Q[15]
Am	↑	1	D	Q[Am-1]	Q[15]

Notes:

1. m = 0, 1, 2, 3.

Block RAM Attribute Definitions

A block RAM has a number of attributes that control its behavior as shown in Table 24.

Table 24: **Block RAM Attributes**

Function	Attribute	Possible Values
Initial Content for Data Memory, Loaded during Configuration	INITxx (INIT_00 through INIT3F)	Each initialization string defines 32 hex values of the 16384-bit data memory of the block RAM.
Initial Content for Parity Memory, Loaded during Configuration	INITPxx (INITP_00 through INITP0F)	Each initialization string defines 32 hex values of the 2048-bit parity data memory of the block RAM.
Data Output Latch Initialization	INIT (single-port) INITA, INITB (dual-port)	Hex value the width of the chosen port.
Data Output Latch Synchronous Set/Reset Value	SRVAL (single-port) SRVAL_A, SRVAL_B (dual-port)	Hex value the width of the chosen port.
Data Output Latch Behavior during Write (see Block RAM Data Operations)	WRITE_MODE	WRITE_FIRST, READ_FIRST, NO_CHANGE

Block RAM Data Operations

Writing data to and accessing data from the block RAM are synchronous operations that take place independently on each of the two ports. Table 25 describes the data operations of each port as a result of the block RAM control signals in their default active-High edges.

The waveforms for the write operation are shown in the top half of Figure 33, Figure 34, and Figure 35. When the WE and EN signals enable the active edge of CLK, data at the DI input bus is written to the block RAM location addressed by the ADDR lines.

Table 25: **Block RAM Function Table**

Input Signals								Output Signals		RAM Data	
GSR	EN	SSR	WE	CLK	ADDR	DIP	DI	DOP	DO	Parity	Data
Immediately After Configuration											
Loaded During Configuration								X	X	INITP_xx	INIT_xx
Global Set/Reset Immediately After Configuration											
1	X	X	X	X	X	X	X	INIT	INIT	No Chg	No Chg
RAM Disabled											
0	0	X	X	X	X	X	X	No Chg	No Chg	No Chg	No Chg
Synchronous Set/Reset											
0	1	1	0	↑	X	X	X	SRVAL	SRVAL	No Chg	No Chg
Synchronous Set/Reset During Write RAM											
0	1	1	1	↑	addr	pdata	Data	SRVAL	SRVAL	RAM(addr) ← pdata	RAM(addr) ← data
Read RAM, no Write Operation											
0	1	0	0	↑	addr	X	X	RAM(pdata)	RAM(data)	No Chg	No Chg
Write RAM, Simultaneous Read Operation											
0	1	0	1	↑	addr	pdata	Data	WRITE_MODE = WRITE_FIRST			
								pdata	data	RAM(addr) ← pdata	RAM(addr) ← data
								WRITE_MODE = READ_FIRST			
								RAM(data)	RAM(data)	RAM(addr) ← pdata	RAM(addr) ← pdata
								WRITE_MODE = NO_CHANGE			
								No Chg	No Chg	RAM(addr) ← pdata	RAM(addr) ← pdata

By contrast, the clock switch matrixes on the top and bottom edges receive signals from any of the five following sources: two GCLK pins, two DCM outputs, or one Double-Line interconnect.

Table 41 indicates permissible connections between clock inputs and BUFGMUX elements. The I0-input provides the best input path to a clock buffer. The I1-input provides the secondary input for the clock multiplexer function.

The four BUFGMUX elements on the top edge are paired together and share inputs from the eight global clock inputs along the top edge. Each BUFGMUX pair connects to four of the eight global clock inputs, as shown in Figure 45. This optionally allows differential inputs to the global clock inputs without wasting a BUFGMUX element.

Table 41: **Connections from Clock Inputs to BUFGMUX Elements and Associated Quadrant Clock**

Quadrant Clock Line[1]	Left-Half BUFGMUX			Top or Bottom BUFGMUX			Right-Half BUFGMUX		
	Location[2]	I0 Input	I1 Input	Location[2]	I0 Input	I1 Input	Location[2]	I0 Input	I1 Input
H	*X0Y9*	LHCLK7	LHCLK6	*X1Y10*	GCLK7 or GCLK11	GCLK6 or GCLK10	*X3Y9*	RHCLK3	RHCLK2
G	*X0Y8*	LHCLK6	LHCLK7	*X1Y11*	GCLK6 or GCLK10	GCLK7 or GCLK11	*X3Y8*	RHCLK2	RHCLK3
F	*X0Y7*	LHCLK5	LHCLK4	*X2Y10*	GCLK5 or GCLK9	GCLK4 or GCLK8	*X3Y7*	RHCLK1	RHCLK0
E	*X0Y6*	LHCLK4	LHCLK5	*X2Y11*	GCLK4 or GCLK8	GCLK5 or GCLK9	*X3Y6*	RHCLK0	RHCLK1
D	*X0Y5*	LHCLK3	LHCLK2	*X1Y0*	GCLK3 or GCLK15	GCLK2 or GCLK14	*X3Y5*	RHCLK7	RHCLK6
C	*X0Y4*	LHCLK2	LHCLK3	*X1Y1*	GCLK2 or GCLK14	GCLK3 or GCLK15	*X3Y4*	RHCLK6	RHCLK7
B	*X0Y3*	LHCLK1	LHCLK0	*X2Y0*	GCLK1 or GCLK13	GCLK0 or GCLK12	*X3Y3*	RHCLK5	RHCLK4
A	*X0Y2*	LHCLK0	LHCLK1	*X2Y1*	GCLK0 or GCLK12	GCLK1 or GCLK13	*X3Y2*	RHCLK4	RHCLK5

Notes:

1. See Quadrant Clock Routing for connectivity details for the eight quadrant clocks.
2. See Figure 45 for specific BUFGMUX locations, and Figure 47 for information on how BUFGMUX elements drive onto a specific clock line within a quadrant.

Table 46: **Pin Behavior during Configuration *(Cont'd)***

Pin Name	Master Serial	SPI (Serial Flash)	BPI (Parallel NOR Flash)	JTAG	Slave Parallel	Slave Serial	I/O Bank[3]
D0/DIN	DIN	DIN	D0		D0	DIN	2
RDWR_B			RDWR_B		RDWR_B		2
A23			A23				2
A22			A22				2
A21			A21				2
A20			A20				2
A19/VS2		VS2	A19				2
A18/VS1		VS1	A18				2
A17/VS0		VS0	A17				2
A16			A16				1
A15			A15				1
A14			A14				1
A13			A13				1
A12			A12				1
A11			A11				1
A10			A10				1
A9			A9				1
A8			A8				1
A7			A7				1
A6			A6				1
A5			A5				1
A4			A4				1
A3			A3				1
A2			A2				1
A1			A1				1
A0			A0				1
LDC0			LDC0				1
LDC1			LDC1				1
LDC2			LDC2				1
HDC			HDC				1

Notes:
1. Gray shaded cells represent pins that are in a high-impedance state (Hi-Z, floating) during configuration. These pins have an optional internal pull-up resistor to their respective V_{CCO} supply pin that is active throughout configuration if the HSWAP input is Low.
2. Yellow shaded cells represent pins with an internal pull-up resistor to its respective voltage supply rail that is active during configuration, regardless of the HSWAP pin.
3. Note that dual-purpose outputs are supplied by V_{CCO}, and configuration inputs are supplied by V_{CCAUX}.

The HSWAP pin itself has a pull-up resistor enabled during configuration. However, the VCCO_0 supply voltage must be applied before the pull-up resistor becomes active. If the VCCO_0 supply ramps after the VCCO_2 power supply, do not let HSWAP float; tie HSWAP to the desired logic level externally.

Spartan-3E FPGAs have only six dedicated configuration pins, including the DONE and PROG_B pins, and the four JTAG boundary-scan pins: TDI, TDO, TMS, and TCK. All other configuration pins are dual-purpose I/O pins and are available to the FPGA application after the DONE pin goes High. See Start-Up for additional information.

Table 47 shows the default I/O standard setting for the various configuration pins during the configuration process. The configuration interface is designed primarily for 2.5V operation when the VCCO_2 (and VCCO_1 in BPI mode) connects to 2.5V.

Table 47: **Default I/O Standard Setting During Configuration (VCCO_2 = 2.5V)**

Pin(s)	I/O Standard	Output Drive	Slew Rate
All, including CCLK	LVCMOS25	8 mA	Slow

Master Serial Mode

For additional information, refer to the “Master Serial Mode” chapter in UG332.

In Master Serial mode (M[2:0] = <0:0:0>), the Spartan-3E FPGA configures itself from an attached Xilinx Platform Flash PROM, as illustrated in Figure 51. The FPGA supplies the CCLK output clock from its internal oscillator to the attached Platform Flash PROM. In response, the Platform Flash PROM supplies bit-serial data to the FPGA’s DIN input, and the FPGA accepts this data on each rising CCLK edge.

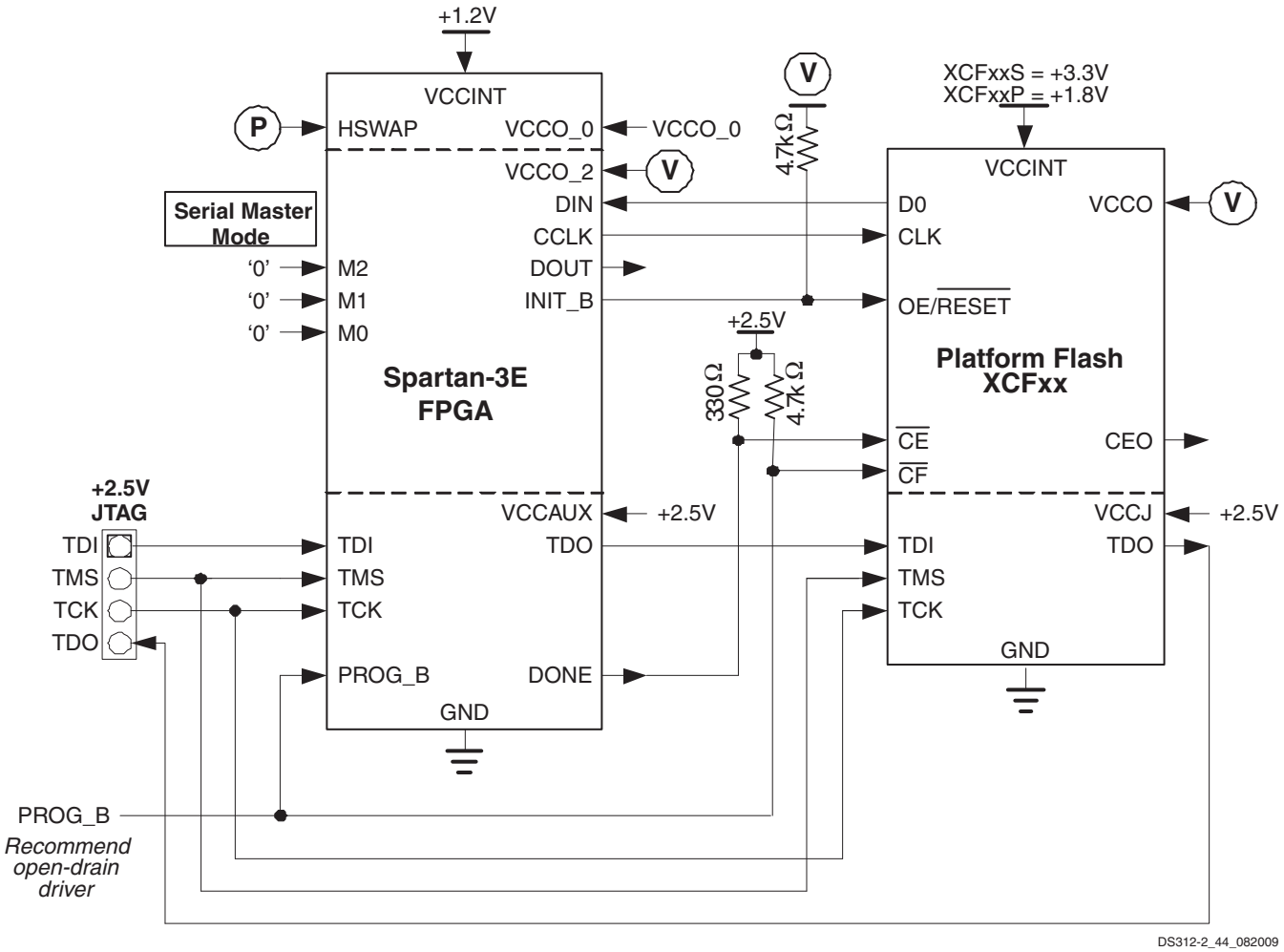

Figure 51: **Master Serial Mode using Platform Flash PROM**

All mode select pins, M[2:0], must be Low when sampled, when the FPGA’s INIT_B output goes High. After configuration, when the FPGA’s DONE output goes High, the mode select pins are available as full-featured user-I/O pins.

Table 55: **Serial Peripheral Interface (SPI) Connections *(Cont'd)***

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
VS[2:0] Ⓢ	Input	**Variant Select**. Instructs the FPGA how to communicate with the attached SPI Flash PROM. See Design Considerations for the HSWAP, M[2:0], and VS[2:0] Pins.	Must be at the logic levels shown in Table 53. Sampled when INIT_B goes High.	User I/O
MOSI	Output	**Serial Data Output**.	FPGA sends SPI Flash memory read commands and starting address to the PROM's serial data input.	User I/O
DIN	Input	**Serial Data Input**.	FPGA receives serial data from PROM's serial data output.	User I/O
CSO_B	Output	**Chip Select Output**. Active Low.	Connects to the SPI Flash PROM's chip-select input. If HSWAP = 1, connect this signal to a 4.7 kΩ pull-up resistor to 3.3V.	Drive CSO_B High after configuration to disable the SPI Flash and reclaim the MOSI, DIN, and CCLK pins. Optionally, re-use this pin and MOSI, DIN, and CCLK to continue communicating with SPI Flash.
CCLK	Output	**Configuration Clock**. Generated by FPGA internal oscillator. Frequency controlled by ***ConfigRate*** bitstream generator option. If CCLK PCB trace is long or has multiple connections, terminate this output to maintain signal integrity. See CCLK Design Considerations.	Drives PROM's clock input.	User I/O
DOUT	Output	**Serial Data Output**.	Actively drives. Not used in single-FPGA designs. In a daisy-chain configuration, this pin connects to DIN input of the next FPGA in the chain.	User I/O
INIT_B	Open-drain bidirectional I/O	**Initialization Indicator**. Active Low. Goes Low at start of configuration during Initialization memory clearing process. Released at end of memory clearing, when mode select pins are sampled. In daisy-chain applications, this signal requires an external 4.7 kΩ pull-up resistor to VCCO_2.	Active during configuration. If SPI Flash PROM requires > 2 ms to awake after powering on, hold INIT_B Low until PROM is ready. If CRC error detected during configuration, FPGA drives INIT_B Low.	User I/O. If unused in the application, drive INIT_B High.
DONE	Open-drain bidirectional I/O	**FPGA Configuration Done**. Low during configuration. Goes High when FPGA successfully completes configuration. Requires external 330 Ω pull-up resistor to 2.5V.	Low indicates that the FPGA is not yet configured.	Pulled High via external pull-up. When High, indicates that the FPGA successfully configured.
PROG_B	Input	**Program FPGA**. Active Low. When asserted Low for 500 ns or longer, forces the FPGA to restart its configuration process by clearing configuration memory and resetting the DONE and INIT_B pins once PROG_B returns High. Recommend external 4.7 kΩ pull-up resistor to 2.5V. Internal pull-up value may be weaker (see Table 78). If driving externally with a 3.3V output, use an open-drain or open-collector driver or use a current limiting series resistor.	Must be High to allow configuration to start.	Drive PROG_B Low and release to reprogram FPGA. Hold PROG_B to force FPGA I/O pins into Hi-Z, allowing direct programming access to SPI Flash PROM pins.

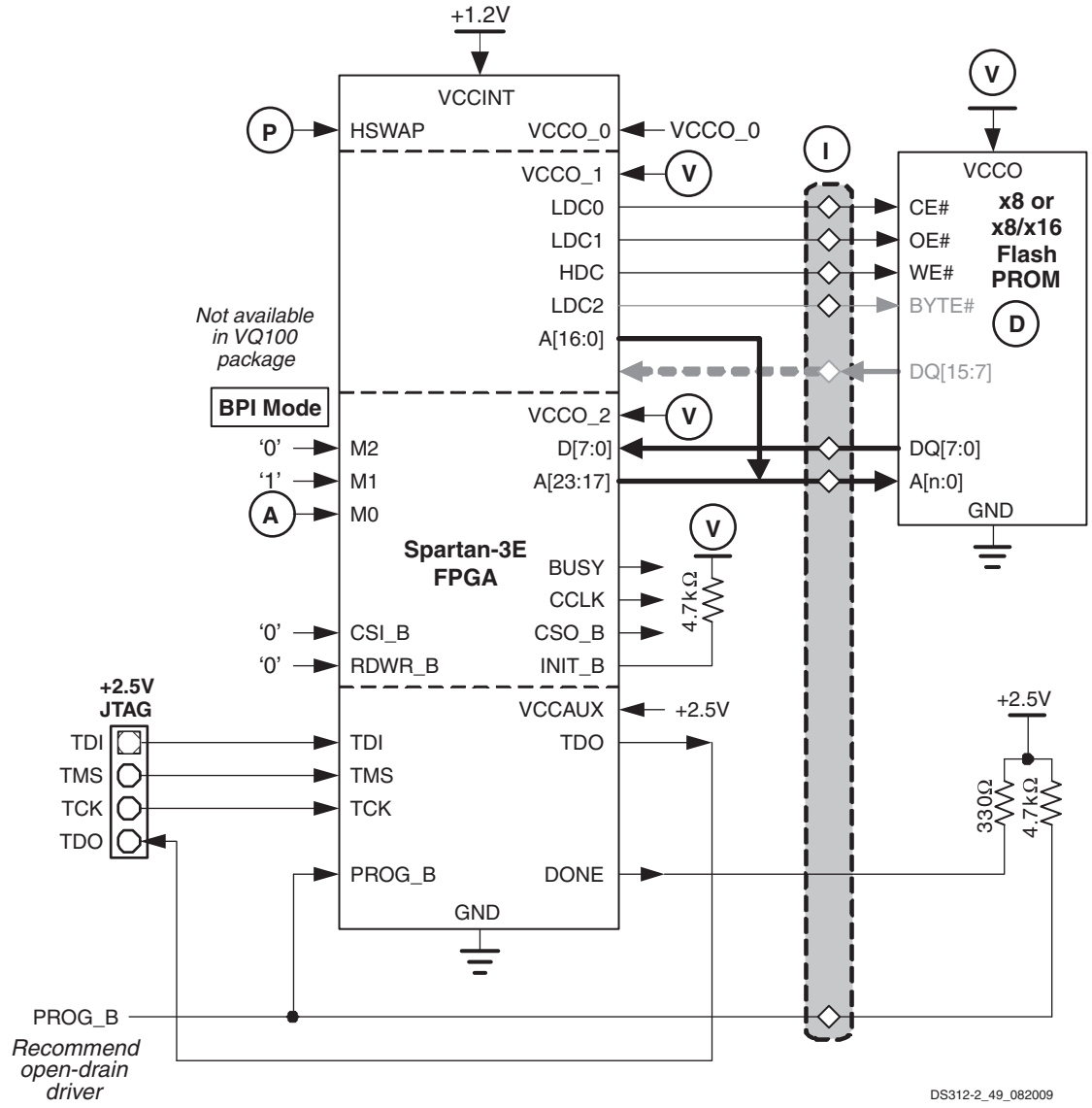

Figure 58: **Byte-wide Peripheral Interface (BPI) Mode Configured from Parallel NOR Flash PROMs**

(A) During configuration, the value of the M0 mode pin determines how the FPGA generates addresses, as shown Table 58. When M0 = 0, the FPGA generates addresses starting at 0 and increments the address on every falling CCLK edge. Conversely, when M0 = 1, the FPGA generates addresses starting at `0xFF_FFFF` (all ones) and decrements the address on every falling CCLK edge.

Table 58: **BPI Addressing Control**

M2	M1	M0	Start Address	Addressing
0	1	0	0	Incrementing
		1	`0xFF_FFFF`	Decrementing

support byte-wide data. However, after configuration, the FPGA supports either x8 or x16 modes. In x16 mode, up to eight additional user I/O pins are required for the upper data bits, D[15:8].

Connecting a Spartan-3E FPGA to a x8/x16 Flash PROM is simple, but does require a precaution. Various Flash PROM vendors use slightly different interfaces to support both x8 and x16 modes. Some vendors (Intel, Micron, some STMicroelectronics devices) use a straightforward interface with pin naming that matches the FPGA connections. However, the PROM's A0 pin is wasted in x16 applications and a separate FPGA user-I/O pin is required for the D15 data line. Fortunately, the FPGA A0 pin is still available as a user I/O after configuration, even though it connects to the Flash PROM.

Other vendors (AMD, Atmel, Silicon Storage Technology, some STMicroelectronics devices) use a pin-efficient interface but change the function of one pin, called IO15/A-1, depending if the PROM is in x8 or x16 mode. In x8 mode, BYTE# = 0, this pin is the least-significant address line. The A0 address line selects the halfword location. The A-1 address line selects the byte location. When in x16 mode, BYTE# = 1, the IO15/A-1 pin becomes the most-significant data bit, D15 because byte addressing is not required in this mode. Check to see if the Flash PROM has a pin named "IO15/A-1" or "DQ15/A-1". If so, be careful to connect x8/x16 Flash PROMs correctly, as shown in Table 63. Also, remember that the D[14:8] data connections require FPGA user I/O pins but that the D15 data is already connected for the FPGA's A0 pin.

Table 63: **FPGA Connections to Flash PROM with IO15/A-1 Pin**

FPGA Pin	Connection to Flash PROM with IO15/A-1 Pin	x8 Flash PROM Interface After FPGA Configuration	x16 Flash PROM Interface After FPGA Configuration
LDC2	BYTE#	Drive LDC2 Low or leave unconnected and tie PROM BYTE# input to GND	Drive LCD2 High
LDC1	OE#	Active-Low Flash PROM output-enable control	Active-Low Flash PROM output-enable control
LDC0	CS#	Active-Low Flash PROM chip-select control	Active-Low Flash PROM chip-select control
HDC	WE#	Flash PROM write-enable control	Flash PROM write-enable control
A[23:1]	A[n:0]	A[n:0]	A[n:0]
A0	IO15/A-1	IO15/A-1 is the least-significant address input	IO15/A-1 is the most-significant data line, IO15
D[7:0]	IO[7:0]	IO[7:0]	IO[7:0]
User I/O	Upper data lines IO[14:8] not required unless used as x16 Flash interface after configuration	Upper data lines IO[14:8] not required	IO[14:8]

Some x8/x16 Flash PROMs have a long setup time requirement on the BYTE# signal. For the FPGA to configure correctly, the PROM must be in x8 mode with BYTE# = 0 at power-on or when the FPGA's PROG_B pin is pulsed Low. If required, extend the BYTE# setup time for a 3.3V PROM using an external 680 Ω pull-down resistor on the FPGA's LDC2 pin or by delaying assertion of the CSI_B select input to the FPGA.

Daisy-Chaining

If the application requires multiple FPGAs with different configurations, then configure the FPGAs using a daisy chain, as shown in Figure 59. Use BPI mode (M[2:0] = <0:1:0> or <0:1:1>) for the FPGA connected to the parallel NOR Flash PROM and Slave Parallel mode (M[2:0] = <1:1:0>) for all downstream FPGAs in the daisy-chain. If there are more than two FPGAs in the chain, then last FPGA in the chain can be from any Xilinx FPGA family. However, all intermediate FPGAs located in the chain between the first and last FPGAs must from either the Spartan-3E or Virtex®-5 FPGA families.

After the master FPGA—the FPGA on the left in the diagram—finishes loading its configuration data from the parallel Flash PROM, the master device continues generating addresses to the Flash PROM and asserts its CSO_B output Low, enabling the next FPGA in the daisy-chain. The next FPGA then receives parallel configuration data from the Flash PROM. The master FPGA's CCLK output synchronizes data capture.

If HSWAP = 1, an external 4.7kΩ pull-up resistor must be added on the CSO_B pin. If HSWAP = 0, no external pull-up is necessary.

Design Note

BPI mode daisy chain software support is available starting in ISE 8.2i.

http://www.xilinx.com/support/answers/23061.htm

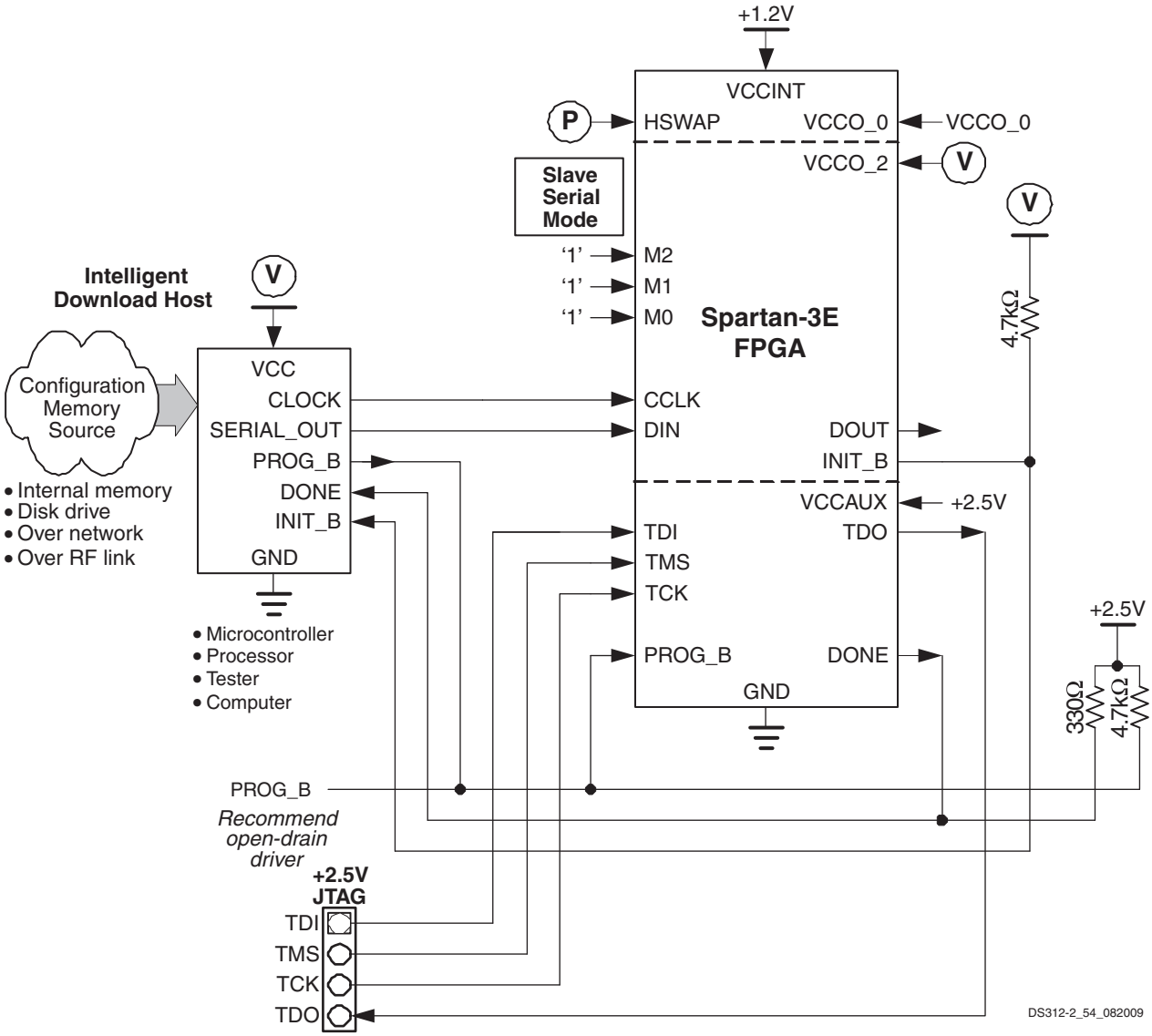

Figure 63: **Slave Serial Configuration**

The mode select pins, M[2:0], are sampled when the FPGA's INIT_B output goes High and must be at defined logic levels during this time. After configuration, when the FPGA's DONE output goes High, the mode pins are available as full-featured user-I/O pins.

(P) Similarly, the FPGA's HSWAP pin must be Low to enable pull-up resistors on all user-I/O pins or High to disable the pull-up resistors. The HSWAP control must remain at a constant logic level throughout FPGA configuration. After configuration, when the FPGA's DONE output goes High, the HSWAP pin is available as full-featured user-I/O pin and is powered by the VCCO_0 supply.

Voltage Compatibility

(V) Most Slave Serial interface signals are within the FPGA's I/O Bank 2, supplied by the VCCO_2 supply input. The VCCO_2 voltage can be 3.3V, 2.5V, or 1.8V to match the requirements of the external host, ideally 2.5V. Using 3.3V or 1.8V requires additional design considerations as the DONE and PROG_B pins are powered by the FPGA's 2.5V V_{CCAUX} supply. See XAPP453: *The 3.3V Configuration of Spartan-3 FPGAs* for additional information.

Daisy-Chaining

If the application requires multiple FPGAs with different configurations, then configure the FPGAs using a daisy chain, as shown in Figure 64. Use Slave Serial mode (M[2:0] = <1:1:1>) for all FPGAs in the daisy-chain. After the lead FPGA is filled with its configuration data, the lead

Powering Spartan-3E FPGAs

For additional information, refer to the “Powering Spartan-3 Generation FPGAs” chapter in UG331.

Voltage Supplies

Like Spartan-3 FPGAs, Spartan-3E FPGAs have multiple voltage supply inputs, as shown in Table 70. There are two supply inputs for internal logic functions, V_{CCINT} and V_{CCAUX}. Each of the four I/O banks has a separate V_{CCO} supply input that powers the output buffers within the associated I/O bank. All of the V_{CCO} connections to a specific I/O bank must be connected and must connect to the same voltage.

Table 70: **Spartan-3E Voltage Supplies**

Supply Input	Description	Nominal Supply Voltage
V_{CCINT}	Internal core supply voltage. Supplies all internal logic functions, such as CLBs, block RAM, and multipliers. Input to Power-On Reset (POR) circuit.	1.2V
V_{CCAUX}	Auxiliary supply voltage. Supplies Digital Clock Managers (DCMs), differential drivers, dedicated configuration pins, JTAG interface. Input to Power-On Reset (POR) circuit.	2.5V
VCCO_0	Supplies the output buffers in I/O Bank 0, the bank along the top edge of the FPGA.	Selectable, 3.3V, 2.5V, 1.8, 1.5V, or 1.2V
VCCO_1	Supplies the output buffers in I/O Bank 1, the bank along the right edge of the FPGA. In Byte-Wide Peripheral Interface (BPI) Parallel Flash Mode, connects to the same voltage as the Flash PROM.	Selectable, 3.3V, 2.5V, 1.8, 1.5V, or 1.2V
VCCO_2	Supplies the output buffers in I/O Bank 2, the bank along the bottom edge of the FPGA. Connects to the same voltage as the FPGA configuration source. Input to Power-On Reset (POR) circuit.	Selectable, 3.3V, 2.5V, 1.8, 1.5V, or 1.2V
VCCO_3	Supplies the output buffers in I/O Bank 3, the bank along the left edge of the FPGA.	Selectable, 3.3V, 2.5V, 1.8, 1.5V, or 1.2V

In a 3.3V-only application, all four V_{CCO} supplies connect to 3.3V. However, Spartan-3E FPGAs provide the ability to bridge between different I/O voltages and standards by applying different voltages to the V_{CCO} inputs of different banks. Refer to I/O Banking Rules for which I/O standards can be intermixed within a single I/O bank.

Each I/O bank also has an separate, optional input voltage reference supply, called V_{REF}. If the I/O bank includes an I/O standard that requires a voltage reference such as HSTL or SSTL, then all V_{REF} pins within the I/O bank must be connected to the same voltage.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/01/05	1.0	Initial Xilinx release.
03/21/05	1.1	Updated Figure 45. Modified title on Table 39 and Table 45.
11/23/05	2.0	Updated values of On-Chip Differential Termination resistors. Updated Table 7. Updated configuration bitstream sizes for XC3S250E through XC3S1600E in Table 45, Table 51, Table 57, and Table 60. Added DLL Performance Differences Between Steppings. Added Stepping 0 Limitations when Reprogramming via JTAG if FPGA Set for BPI Configuration. Added Stepping 0 limitations when Daisy-Chaining in SPI configuration mode. Added Multiplier/Block RAM Interaction section. Updated Digital Clock Managers (DCMs) section, especially Phase Shifter (PS) portion. Corrected and enhanced the clock infrastructure diagram in Figure 45 and Table 41. Added CCLK Design Considerations section. Added Design Considerations for the HSWAP, M[2:0], and VS[2:0] Pins section. Added Spansion, Winbond, and Macronix to list of SPI Flash vendors in Table 53 and Table 56. Clarified that SPI mode configuration supports Atmel 'C'- and 'D'-series DataFlash. Updated the Programming Support section for SPI Flash PROMs. Added Power-On Precautions if PROM Supply is Last in Sequence, Compatible Flash Families, and BPI Mode Interaction with Right and Bottom Edge Global Clock Inputs sections to BPI configuration mode topic. Updated and amplified Powering Spartan-3E FPGAs section. Added Production Stepping section.
03/22/06	3.0	Upgraded data sheet status to Preliminary. Updated Input Delay Functions and Figure 6. Added clarification that Input-only pins also have Pull-Up and Pull-Down Resistors. Added design note about address setup and hold requirements to Block RAM. Added warning message about software differences between ISE 8.1i, Service Pack 3 and earlier software to FIXED Phase Shift Mode and VARIABLE Phase Shift Mode. Added message about using GCLK1 in DLL Clock Input Connections and Clock Inputs. Updated Figure 45. Added additional information on HSWAP behavior to Pin Behavior During Configuration. Highlighted which pins have configuration pull-up resistors unaffected by HSWAP in Table 46. Updated bitstream image sizes for the XC3S1200E and XC3S1600E in Table 45, Table 51, Table 57, and Table 60. Clarified that 'B'-series Atmel DataFlash SPI PROMs can be used in Commercial temperature range applications in Table 53 and Figure 54. Updated Figure 56. Updated Dynamically Loading Multiple Configuration Images Using MultiBoot Option section. Added design note about BPI daisy-chaining software support to BPI Daisy-Chaining section. Updated JTAG revision codes in Table 67. Added No Internal Charge Pumps or Free-Running Oscillators. Updated information on production stepping differences in Table 71. Updated Software Version Requirements.
04/10/06	3.1	Updated JTAG User ID information. Clarified Note 1, Figure 5. Clarified that Figure 45 shows electrical connectivity and corrected left- and right-edge DCM coordinates. Updated Table 30, Table 31, and Table 32 to show the specific clock line driven by the associated BUFGMUX primitive. Corrected the coordinate locations for the associated BUFGMUX primitives in Table 31 and Table 32. Updated Table 41 to show that the I0-input is the preferred connection to a BUFGMUX.
05/19/06	3.2	Made further clarifying changes to Figure 46, showing both direct inputs to BUFGMUX primitives and to DCMs. Added Atmel AT45DBxxxD-series DataFlash serial PROMs to Table 53. Added details that intermediate FPGAs in a BPI-mode, multi-FPGA configuration daisy-chain must be from either the Spartan-3E or the Virtex-5 FPGA families (see BPI Daisy-Chaining). Added Using JTAG Interface to Communicate to a Configured FPGA Design. Minor updates to Figure 66 and Figure 67. Clarified which Spartan-3E FPGA product options support the Readback feature, shown in Table 68.
05/30/06	3.2.1	Corrected various typos and incorrect links.
10/02/06	3.3	Clarified that the block RAM Readback feature is available either on the -5 speed grade or the Industrial temperature range.
11/09/06	3.4	Updated the description of the Input Delay Functions. The ODDR2 flip-flop with C0 or C1 Alignment is no longer supported. Updated Figure 5. Updated Table 6 for improved PCI input voltage tolerance. Replaced missing text in Clock Buffers/Multiplexers. Updated SPI Flash devices in Table 53. Updated parallel NOR Flash devices in Table 61. Direct, SPI Flash in-system Programming Support was added beginning with ISE 8.1i iMPACT software for STMicro and Atmel SPI PROMs. Updated Table 71 and Table 72 as Stepping 1 is in full production. Freshened various hyper links. Promoted Module 2 to Production status.

Table 107: **Switching Characteristics for the DFS**

Symbol	Description		Device	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Output Frequency Ranges								
CLKOUT_FREQ_FX_LF	Frequency for the CLKFX and CLKFX180 outputs, low frequencies	Stepping 0	XC3S100E XC3S250E XC3S500E XC3S1600E	N/A	N/A	5	90	MHz
CLKOUT_FREQ_FX_HF	Frequency for the CLKFX and CLKFX180 outputs, high frequencies					220	307	MHz
CLKOUT_FREQ_FX	Frequency for the CLKFX and CLKFX180 outputs	Stepping 0	XC3S1200E			5	307	MHz
		Stepping 1	All	5	333		311	MHz
Output Clock Jitter(2,3)								
CLKOUT_PER_JITT_FX	Period jitter at the CLKFX and CLKFX180 outputs.		All	Typ	Max	Typ	Max	
		CLKIN ≤ 20 MHz		Note 6				ps
		CLKIN > 20 MHz		±[1% of CLKFX period + 100]	±[1% of CLKFX period + 200]	±[1% of CLKFX period + 100]	±[1% of CLKFX period + 200]	ps
Duty Cycle(4,5)								
CLKOUT_DUTY_CYCLE_FX	Duty cycle precision for the CLKFX and CLKFX180 outputs, including the BUFGMUX and clock tree duty-cycle distortion		All	-	±[1% of CLKFX period + 400]	-	±[1% of CLKFX period + 400]	ps
Phase Alignment(5)								
CLKOUT_PHASE_FX	Phase offset between the DFS CLKFX output and the DLL CLK0 output when both the DFS and DLL are used		All	-	±200	-	±200	ps
CLKOUT_PHASE_FX180	Phase offset between the DFS CLKFX180 output and the DLL CLK0 output when both the DFS and DLL are used		All	-	±[1% of CLKFX period + 300]	-	±[1% of CLKFX period + 300]	ps
Lock Time								
LOCK_FX(2)	The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX and CLKFX180 signals are valid. If using both the DLL and the DFS, use the longer locking time.	5 MHz ≤ F_{CLKIN} ≤ 15 MHz	All	-	5	-	5	ms
		F_{CLKIN} > 15 MHz		-	450	-	450	µs

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 77 and Table 106.
2. For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
3. Maximum output jitter is characterized within a reasonable noise environment (150 ps input period jitter, 40 SSOs and 25% CLB switching). Output jitter strongly depends on the environment, including the number of SSOs, the output drive strength, CLB utilization, CLB switching activities, switching frequency, power supply and PCB design. The actual maximum output jitter depends on the system application.
4. The CLKFX and CLKFX180 outputs always have an approximate 50% duty cycle.
5. Some duty-cycle and alignment specifications include 1% of the CLKFX output period or 0.01 UI.
   Example: The data sheet specifies a maximum jitter of ±[1% of CLKFX period + 300]. Assume the CLKFX output frequency is 100 MHz. The equivalent CLKFX period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 300 ps] = ±400 ps.
6. Use the Spartan-3A Jitter Calculator (www.xilinx.com/support/documentation/data_sheets/s3a_jitter_calc.zip) to estimate DFS output jitter. Use the Clocking Wizard to determine jitter for a specific design.

Serial Peripheral Interface (SPI) Configuration Timing

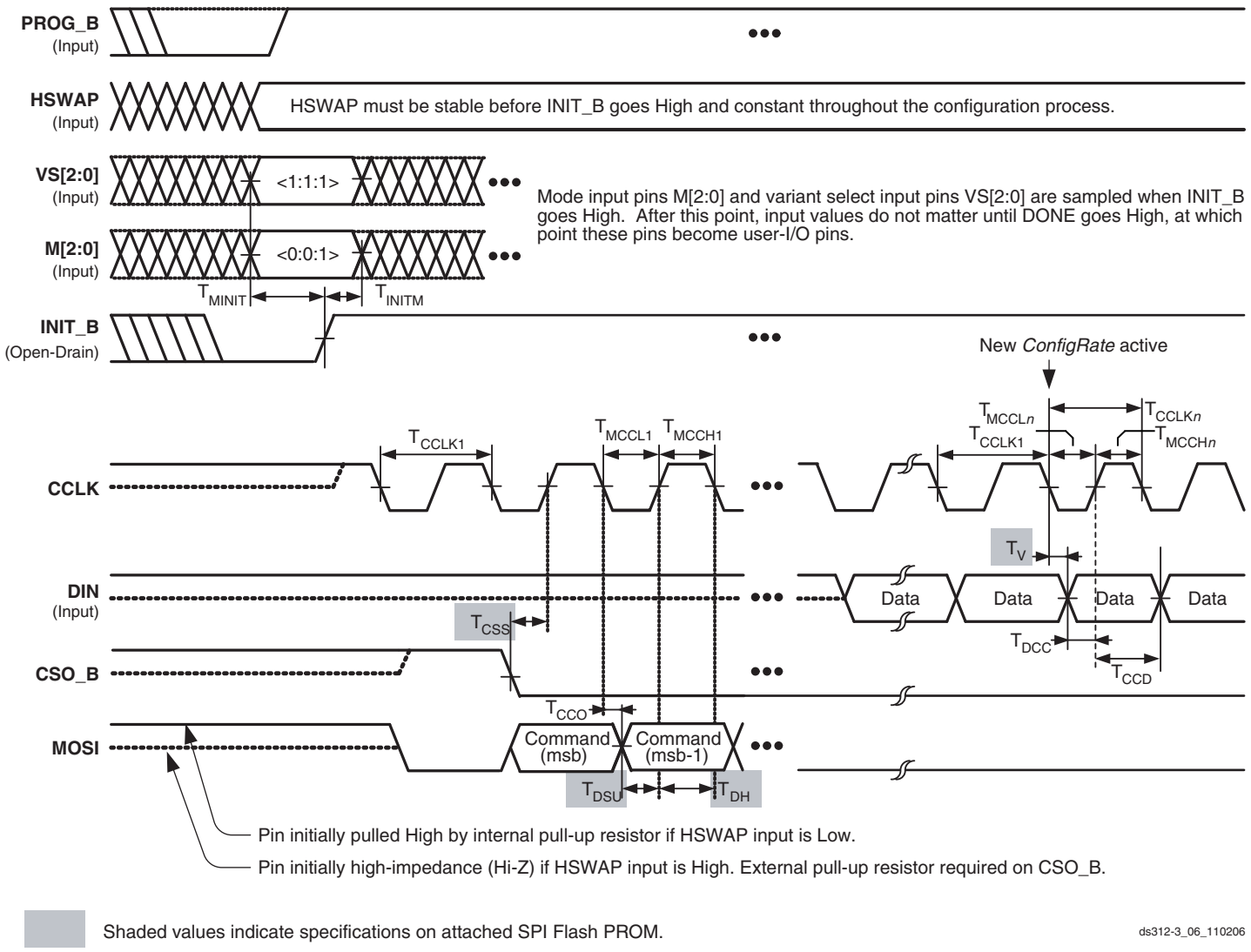

Figure 76: **Waveforms for Serial Peripheral Interface (SPI) Configuration**

Table 118: **Timing for Serial Peripheral Interface (SPI) Configuration Mode**

Symbol	Description	Minimum	Maximum	Units
T_{CCLK1}	Initial CCLK clock period	See Table 112		
T_{CCLKn}	CCLK clock period after FPGA loads ConfigRate setting	See Table 112		
T_{MINIT}	Setup time on VS[2:0] and M[2:0] mode pins before the rising edge of INIT_B	50	-	ns
T_{INITM}	Hold time on VS[2:0] and M[2:0]mode pins after the rising edge of INIT_B	0	-	ns
T_{CCO}	MOSI output valid after CCLK edge	See Table 116		
T_{DCC}	Setup time on DIN data input before CCLK edge	See Table 116		
T_{CCD}	Hold time on DIN data input after CCLK edge	See Table 116		

IEEE 1149.1/1532 JTAG Test Access Port Timing

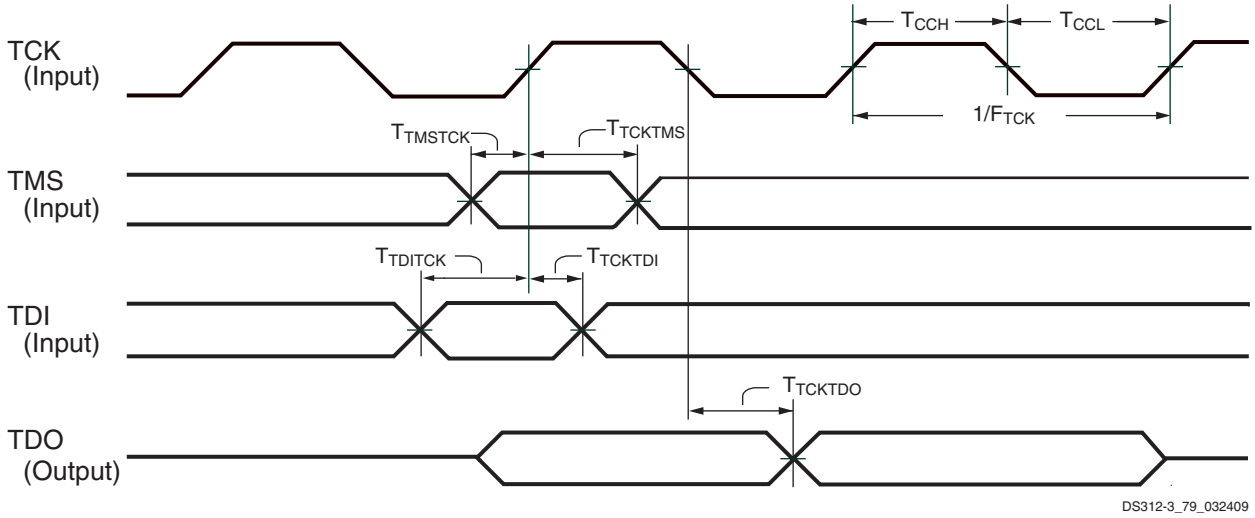

Figure 78: **JTAG Waveforms**

Table 123: **Timing for the JTAG Test Access Port**

Symbol	Description	All Speed Grades		Units
		Min	Max	
Clock-to-Output Times				
T_{TCKTDO}	The time from the falling transition on the TCK pin to data appearing at the TDO pin	1.0	11.0	ns
Setup Times				
T_{TDITCK}	The time from the setup of data at the TDI pin to the rising transition at the TCK pin	7.0	-	ns
T_{TMSTCK}	The time from the setup of a logic level at the TMS pin to the rising transition at the TCK pin	7.0	-	ns
Hold Times				
T_{TCKTDI}	The time from the rising transition at the TCK pin to the point when data is last held at the TDI pin	0	-	ns
T_{TCKTMS}	The time from the rising transition at the TCK pin to the point when a logic level is last held at the TMS pin	0	-	ns
Clock Timing				
T_{CCH}	The High pulse width at the TCK pin	5	-	ns
T_{CCL}	The Low pulse width at the TCK pin	5	-	ns
F_{TCK}	Frequency of the TCK signal	-	30	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 77.

TQ144: 144-lead Thin Quad Flat Package

The XC3S100E and the XC3S250E FPGAs are available in the 144-lead thin quad flat package, TQ144. Both devices share a common footprint for this package as shown in Table 137 and Figure 82.

Table 137 lists all the package pins. They are sorted by bank number and then by pin name of the largest device. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The TQ144 package only supports 20 address output pins in the Byte-wide Peripheral Interface (BPI) configuration mode. In larger packages, there are 24 BPI address outputs.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx web site at:

http://www.xilinx.com/support/documentation/data_sheets/s3e_pin.zip

Pinout Table

Table 137: **TQ144 Package Pinout**

Bank	XC3S100E Pin Name	XC3S250E Pin Name	TQ144 Pin	Type
0	IO	IO	P132	I/O
0	IO/VREF_0	IO/VREF_0	P124	VREF
0	IO_L01N_0	IO_L01N_0	P113	I/O
0	IO_L01P_0	IO_L01P_0	P112	I/O
0	IO_L02N_0	IO_L02N_0	P117	I/O
0	IO_L02P_0	IO_L02P_0	P116	I/O
0	IO_L04N_0/GCLK5	IO_L04N_0/GCLK5	P123	GCLK
0	IO_L04P_0/GCLK4	IO_L04P_0/GCLK4	P122	GCLK
0	IO_L05N_0/GCLK7	IO_L05N_0/GCLK7	P126	GCLK
0	IO_L05P_0/GCLK6	IO_L05P_0/GCLK6	P125	GCLK
0	IO_L07N_0/GCLK11	IO_L07N_0/GCLK11	P131	GCLK
0	IO_L07P_0/GCLK10	IO_L07P_0/GCLK10	P130	GCLK
0	IO_L08N_0/VREF_0	IO_L08N_0/VREF_0	P135	VREF
0	IO_L08P_0	IO_L08P_0	P134	I/O
0	IO_L09N_0	IO_L09N_0	P140	I/O
0	IO_L09P_0	IO_L09P_0	P139	I/O
0	IO_L10N_0/HSWAP	IO_L10N_0/HSWAP	P143	DUAL
0	IO_L10P_0	IO_L10P_0	P142	I/O
0	IP	IP	P111	INPUT
0	IP	IP	P114	INPUT
0	IP	IP	P136	INPUT
0	IP	IP	P141	INPUT
0	IP_L03N_0	IP_L03N_0	P120	INPUT
0	IP_L03P_0	IP_L03P_0	P119	INPUT
0	IP_L06N_0/GCLK9	IP_L06N_0/GCLK9	P129	GCLK
0	IP_L06P_0/GCLK8	IP_L06P_0/GCLK8	P128	GCLK
0	VCCO_0	VCCO_0	P121	VCCO
0	VCCO_0	VCCO_0	P138	VCCO
1	IO/A0	IO/A0	P98	DUAL
1	IO/VREF_1	IO/VREF_1	P83	VREF
1	IO_L01N_1/A15	IO_L01N_1/A15	P75	DUAL
1	IO_L01P_1/A16	IO_L01P_1/A16	P74	DUAL
1	IO_L02N_1/A13	IO_L02N_1/A13	P77	DUAL

Table 143: **FT256 Package Pinout *(Cont'd)***

Bank	XC3S250E Pin Name	XC3S500E Pin Name	XC3S1200E Pin Name	FT256 Ball	Type
3	IP	IP	IP	N3	INPUT
3	IP/VREF_3	IP/VREF_3	IP/VREF_3	G1	VREF
3	IO/VREF_3	IO/VREF_3	IP/VREF_3	N2	***250E:*** VREF(I/O) ***500E:*** VREF(I/O) ***1200E:*** VREF(INPUT)
3	VCCO_3	VCCO_3	VCCO_3	E2	VCCO
3	VCCO_3	VCCO_3	VCCO_3	G6	VCCO
3	VCCO_3	VCCO_3	VCCO_3	K6	VCCO
3	VCCO_3	VCCO_3	VCCO_3	M2	VCCO
GND	GND	GND	GND	A1	GND
GND	GND	GND	GND	A16	GND
GND	GND	GND	GND	B9	GND
GND	GND	GND	GND	F6	GND
GND	GND	GND	GND	F11	GND
GND	GND	GND	GND	G7	GND
GND	GND	GND	GND	G8	GND
GND	GND	GND	GND	G9	GND
GND	GND	GND	GND	G10	GND
GND	GND	GND	GND	H2	GND
GND	GND	GND	GND	H7	GND
GND	GND	GND	GND	H8	GND
GND	GND	GND	GND	H9	GND
GND	GND	GND	GND	H10	GND
GND	GND	GND	GND	J7	GND
GND	GND	GND	GND	J8	GND
GND	GND	GND	GND	J9	GND
GND	GND	GND	GND	J10	GND
GND	GND	GND	GND	J15	GND
GND	GND	GND	GND	K7	GND
GND	GND	GND	GND	K8	GND
GND	GND	GND	GND	K9	GND
GND	GND	GND	GND	K10	GND
GND	GND	GND	GND	L6	GND
GND	GND	GND	GND	L11	GND
GND	GND	GND	GND	R8	GND
GND	GND	GND	GND	T1	GND
GND	GND	GND	GND	T16	GND
VCCAUX	DONE	DONE	DONE	T15	CONFIG
VCCAUX	PROG_B	PROG_B	PROG_B	D3	CONFIG
VCCAUX	TCK	TCK	TCK	A15	JTAG
VCCAUX	TDI	TDI	TDI	A2	JTAG
VCCAUX	TDO	TDO	TDO	C14	JTAG
VCCAUX	TMS	TMS	TMS	B15	JTAG
VCCAUX	VCCAUX	VCCAUX	VCCAUX	A6	VCCAUX

Table 148: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S500E Pin Name	XC3S1200E Pin Name	XC3S1600E Pin Name	FG320 Ball	Type
GND	GND	GND	GND	K8	GND
GND	GND	GND	GND	K11	GND
GND	GND	GND	GND	K16	GND
GND	GND	GND	GND	L8	GND
GND	GND	GND	GND	L9	GND
GND	GND	GND	GND	L10	GND
GND	GND	GND	GND	L11	GND
GND	GND	GND	GND	M7	GND
GND	GND	GND	GND	M12	GND
GND	GND	GND	GND	T9	GND
GND	GND	GND	GND	U2	GND
GND	GND	GND	GND	U17	GND
GND	GND	GND	GND	V1	GND
GND	GND	GND	GND	V18	GND
VCCAUX	DONE	DONE	DONE	V17	CONFIG
VCCAUX	PROG_B	PROG_B	PROG_B	B1	CONFIG
VCCAUX	TCK	TCK	TCK	A17	JTAG
VCCAUX	TDI	TDI	TDI	A2	JTAG
VCCAUX	TDO	TDO	TDO	C16	JTAG
VCCAUX	TMS	TMS	TMS	D15	JTAG
VCCAUX	VCCAUX	VCCAUX	VCCAUX	B7	VCCAUX
VCCAUX	VCCAUX	VCCAUX	VCCAUX	B12	VCCAUX
VCCAUX	VCCAUX	VCCAUX	VCCAUX	G2	VCCAUX
VCCAUX	VCCAUX	VCCAUX	VCCAUX	G17	VCCAUX
VCCAUX	VCCAUX	VCCAUX	VCCAUX	M2	VCCAUX
VCCAUX	VCCAUX	VCCAUX	VCCAUX	M17	VCCAUX
VCCAUX	VCCAUX	VCCAUX	VCCAUX	U7	VCCAUX
VCCAUX	VCCAUX	VCCAUX	VCCAUX	U12	VCCAUX
VCCINT	VCCINT	VCCINT	VCCINT	E5	VCCINT
VCCINT	VCCINT	VCCINT	VCCINT	E14	VCCINT
VCCINT	VCCINT	VCCINT	VCCINT	F6	VCCINT
VCCINT	VCCINT	VCCINT	VCCINT	F13	VCCINT
VCCINT	VCCINT	VCCINT	VCCINT	N6	VCCINT
VCCINT	VCCINT	VCCINT	VCCINT	N13	VCCINT
VCCINT	VCCINT	VCCINT	VCCINT	P5	VCCINT
VCCINT	VCCINT	VCCINT	VCCINT	P14	VCCINT