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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	612
Number of Logic Elements/Cells	5508
Total RAM Bits	221184
Number of I/O	66
Number of Gates	250000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s250e-4vqg100c

Spartan-3E FPGAs provide additional input flexibility by allowing I/O standards to be mixed in different banks. For a particular V_{CCO} voltage, Table 6 and Table 7 list all of the IOSTANDARDs that can be combined and if the IOSTANDARD is supported as an input only or can be used for both inputs and outputs.

Table 6: **Single-Ended IOSTANDARD Bank Compatibility**

Single-Ended IOSTANDARD	V_{CCO} Supply/Compatibility					Input Requirements	
	1.2V	1.5V	1.8V	2.5V	3.3V	V_{REF}	Board Termination Voltage (V_{TT})
LVTTL	-	-	-	-	Input/ Output	N/R(1)	N/R
LVCMOS33	-	-	-	-	Input/ Output	N/R	N/R
LVCMOS25	-	-	-	Input/ Output	Input	N/R	N/R
LVCMOS18	-	-	Input/ Output	Input	Input	N/R	N/R
LVCMOS15	-	Input/ Output	Input	Input	Input	N/R	N/R
LVCMOS12	Input/ Output	Input	Input	Input	Input	N/R	N/R
PCI33_3	-	-	-	-	Input/ Output	N/R	N/R
PCI66_3	-	-	-	-	Input/ Output	N/R	N/R
HSTL_I_18	-	-	Input/ Output	Input	Input	0.9	0.9
HSTL_III_18	-	-	Input/ Output	Input	Input	1.1	1.8
SSTL18_I	-	-	Input/ Output	Input	Input	0.9	0.9
SSTL2_I	-	-	-	Input/ Output	Input	1.25	1.25

Notes:

1. N/R - Not required for input operation.

Block RAM Attribute Definitions

A block RAM has a number of attributes that control its behavior as shown in Table 24.

Table 24: **Block RAM Attributes**

Function	Attribute	Possible Values
Initial Content for Data Memory, Loaded during Configuration	INITxx (INIT_00 through INIT3F)	Each initialization string defines 32 hex values of the 16384-bit data memory of the block RAM.
Initial Content for Parity Memory, Loaded during Configuration	INITPxx (INITP_00 through INITP0F)	Each initialization string defines 32 hex values of the 2048-bit parity data memory of the block RAM.
Data Output Latch Initialization	INIT (single-port) INITA, INITB (dual-port)	Hex value the width of the chosen port.
Data Output Latch Synchronous Set/Reset Value	SRVAL (single-port) SRVAL_A, SRVAL_B (dual-port)	Hex value the width of the chosen port.
Data Output Latch Behavior during Write (see Block RAM Data Operations)	WRITE_MODE	WRITE_FIRST, READ_FIRST, NO_CHANGE

Block RAM Data Operations

Writing data to and accessing data from the block RAM are synchronous operations that take place independently on each of the two ports. Table 25 describes the data operations of each port as a result of the block RAM control signals in their default active-High edges.

The waveforms for the write operation are shown in the top half of Figure 33, Figure 34, and Figure 35. When the WE and EN signals enable the active edge of CLK, data at the DI input bus is written to the block RAM location addressed by the ADDR lines.

Table 25: **Block RAM Function Table**

Input Signals								Output Signals		RAM Data	
GSR	EN	SSR	WE	CLK	ADDR	DIP	DI	DOP	DO	Parity	Data
Immediately After Configuration											
Loaded During Configuration								X	X	INITP_xx	INIT_xx
Global Set/Reset Immediately After Configuration											
1	X	X	X	X	X	X	X	INIT	INIT	No Chg	No Chg
RAM Disabled											
0	0	X	X	X	X	X	X	No Chg	No Chg	No Chg	No Chg
Synchronous Set/Reset											
0	1	1	0	↑	X	X	X	SRVAL	SRVAL	No Chg	No Chg
Synchronous Set/Reset During Write RAM											
0	1	1	1	↑	addr	pdata	Data	SRVAL	SRVAL	RAM(addr) ← pdata	RAM(addr) ← data
Read RAM, no Write Operation											
0	1	0	0	↑	addr	X	X	RAM(pdata)	RAM(data)	No Chg	No Chg
Write RAM, Simultaneous Read Operation											
0	1	0	1	↑	addr	pdata	Data	WRITE_MODE = WRITE_FIRST			
								pdata	data	RAM(addr) ← pdata	RAM(addr) ← data
								WRITE_MODE = READ_FIRST			
								RAM(data)	RAM(data)	RAM(addr) ← pdata	RAM(addr) ← pdata
								WRITE_MODE = NO_CHANGE			
								No Chg	No Chg	RAM(addr) ← pdata	RAM(addr) ← pdata

cancel out the clock skew. When the DLL phase-aligns the CLK0 signal with the CLKIN signal, it asserts the LOCKED output, indicating a lock on to the CLKIN signal.

DLL Attributes and Related Functions

The DLL unit has a variety of associated attributes as described in Table 29. Each attribute is described in detail in the sections that follow.

Table 29: **DLL Attributes**

Attribute	Description	Values
CLK_FEEDBACK	Chooses either the CLK0 or CLK2X output to drive the CLKFB input	NONE, ***1X***, 2X
CLKIN_DIVIDE_BY_2	Halves the frequency of the CLKIN signal just as it enters the DCM	***FALSE***, TRUE
CLKDV_DIVIDE	Selects the constant used to divide the CLKIN input frequency to generate the CLKDV output frequency	1.5, ***2***, 2.5, 3, 3.5, 4, 4.5, 5, 5.5, 6.0, 6.5, 7.0, 7.5, 8, 9, 10, 11, 12, 13, 14, 15, and 16
CLKIN_PERIOD	Additional information that allows the DLL to operate with the most efficient lock time and the best jitter tolerance	Floating-point value representing the CLKIN period in nanoseconds

DLL Clock Input Connections

For best results, an external clock source enters the FPGA via a Global Clock Input (GCLK). Each specific DCM has four possible direct, optimal GCLK inputs that feed the DCM's CLKIN input, as shown in Table 30. Table 30 also provides the specific pin numbers by package for each GCLK input. The two additional DCM's on the XC3S1200E and XC3S1600E have similar optimal connections from the left-edge LHCLK and the right-edge RHCLK inputs, as described in Table 31 and Table 32.

- The DCM supports differential clock inputs (for example, LVDS, LVPECL_25) via a pair of GCLK inputs that feed an internal single-ended signal to the DCM's CLKIN input.

Design Note

Avoid using global clock input GCLK1 as it is always shared with the M2 mode select pin. Global clock inputs GCLK0, GCLK2, GCLK3, GCLK12, GCLK13, GCLK14, and GCLK15 have shared functionality in some configuration modes.

(P) Similarly, the FPGA's HSWAP pin must be Low to enable pull-up resistors on all user-I/O pins during configuration or High to disable the pull-up resistors. The HSWAP control must remain at a constant logic level throughout FPGA configuration. After configuration, when the FPGA's DONE output goes High, the HSWAP pin is available as full-featured user-I/O pin and is powered by the VCCO_0 supply.

The FPGA's DOUT pin is used in daisy-chain applications, described later. In a single-FPGA application, the FPGA's DOUT pin is not used but is actively driving during the configuration process.

Table 50: **Serial Master Mode Connections**

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
HSWAP (P)	Input	**User I/O Pull-Up Control**. When Low during configuration, enables pull-up resistors in all I/O pins to respective I/O bank V_{CCO} input. 0: Pull-ups during configuration 1: No pull-ups	Drive at valid logic level throughout configuration.	User I/O
M[2:0]	Input	**Mode Select**. Selects the FPGA configuration mode. See Design Considerations for the HSWAP, M[2:0], and VS[2:0] Pins.	M2 = 0, M1 = 0, M0 = 0. Sampled when INIT_B goes High.	User I/O
DIN	Input	**Serial Data Input**.	Receives serial data from PROM's D0 output.	User I/O
CCLK	Output	**Configuration Clock**. Generated by FPGA internal oscillator. Frequency controlled by ***ConfigRate*** bitstream generator option. If CCLK PCB trace is long or has multiple connections, terminate this output to maintain signal integrity. See CCLK Design Considerations.	Drives PROM's CLK clock input.	User I/O
DOUT	Output	**Serial Data Output**.	Actively drives. Not used in single-FPGA designs. In a daisy-chain configuration, this pin connects to DIN input of the next FPGA in the chain.	User I/O
INIT_B	Open-drain bidirectional I/O	**Initialization Indicator**. Active Low. Goes Low at start of configuration during Initialization memory clearing process. Released at end of memory clearing, when mode select pins are sampled. Requires external 4.7 kΩ pull-up resistor to VCCO_2.	Connects to PROM's OE/RESET input. FPGA clears PROM's address counter at start of configuration, enables outputs during configuration. PROM also holds FPGA in Initialization state until PROM reaches Power-On Reset (POR) state. If CRC error detected during configuration, FPGA drives INIT_B Low.	User I/O. If unused in the application, drive INIT_B High.
DONE	Open-drain bidirectional I/O	**FPGA Configuration Done**. Low during configuration. Goes High when FPGA successfully completes configuration. Requires external 330 Ω pull-up resistor to 2.5V.	Connects to PROM's chip-enable (CE) input. Enables PROM during configuration. Disables PROM after configuration.	Pulled High via external pull-up. When High, indicates that the FPGA successfully configured.
PROG_B	Input	**Program FPGA**. Active Low. When asserted Low for 500 ns or longer, forces the FPGA to restart its configuration process by clearing configuration memory and resetting the DONE and INIT_B pins once PROG_B returns High. Recommend external 4.7 kΩ pull-up resistor to 2.5V. Internal pull-up value may be weaker (see Table 78). If driving externally with a 3.3V output, use an open-drain or open-collector driver or use a current limiting series resistor.	Must be High during configuration to allow configuration to start. Connects to PROM's CF pin, allowing JTAG PROM programming algorithm to reprogram the FPGA.	Drive PROG_B Low and release to reprogram FPGA.

SPI serial Flash PROMs and the Atmel AT45DB-series Data Flash PROMs using the Platform Cable USB, Xilinx Parallel IV, or other compatible programming cable.

Byte-Wide Peripheral Interface (BPI) Parallel Flash Mode

For additional information, refer to the “Master BPI Mode” chapter in UG332.

In Byte-wide Peripheral Interface (BPI) mode (M[2:0] = <0:1:0> or <0:1:1>), a Spartan-3E FPGA configures itself from an industry-standard parallel NOR Flash PROM, as illustrated in Figure 58. The FPGA generates up to a 24-bit address lines to access an attached parallel Flash. Only 20 address lines are generated for Spartan-3E FPGAs in the TQ144 package. Similarly, the XC3S100E FPGA in the CP132 package only has 20 address lines while the XC3S250E and XC3S500E FPGAs in the same package have 24 address lines. When using the VQ100 package, the BPI mode is not available when using parallel NOR Flash, but is supported using parallel Platform Flash (XCFxxP).

The BPI configuration interface is primarily designed for standard parallel NOR Flash PROMs and supports both byte-wide (x8) and byte-wide/halfword (x8/x16) PROMs. The interface functions with halfword-only (x16) PROMs, but the upper byte in a portion of the PROM remains unused. For configuration, the BPI interface does not require any specific Flash PROM features, such as boot block or a specific sector size.

The BPI interface also functions with Xilinx parallel Platform Flash PROMs (XCFxxP), although the FPGA’s address lines are left unconnected.

The BPI interface also works equally wells with other asynchronous memories that use a similar SRAM-style interface such as SRAM, NVRAM, EEPROM, EPROM, or masked ROM.

NAND Flash memory is commonly used in memory cards for digital cameras. Spartan-3E FPGAs do not configure directly from NAND Flash memories.

The FPGA’s internal oscillator controls the interface timing and the FPGA supplies the clock on the CCLK output pin. However, the CCLK signal is not used in single FPGA applications. Similarly, the FPGA drives three pins Low during configuration (LDC[2:0]) and one pin High during configuration (HDC) to the PROM’s control inputs.

Table 59: **Byte-Wide Peripheral Interface (BPI) Connections *(Cont'd)***

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
DONE	Open-drain bidirectional I/O	**FPGA Configuration Done**. Low during configuration. Goes High when FPGA successfully completes configuration. Requires external 330 Ω pull-up resistor to 2.5V.	Low indicates that the FPGA is not yet configured.	Pulled High via external pull-up. When High, indicates that the FPGA is successfully configured.
PROG_B	Input	**Program FPGA**. Active Low. When asserted Low for 500 ns or longer, forces the FPGA to restart its configuration process by clearing configuration memory and resetting the DONE and INIT_B pins once PROG_B returns High. Recommend external 4.7 kΩ pull-up resistor to 2.5V. Internal pull-up value may be weaker (see Table 78). If driving externally with a 3.3V output, use an open-drain or open-collector driver or use a current limiting series resistor.	Must be High to allow configuration to start.	Drive PROG_B Low and release to reprogram FPGA. Hold PROG_B to force FPGA I/O pins into Hi-Z, allowing direct programming access to Flash PROM pins.

Voltage Compatibility

The FPGA's parallel Flash interface signals are within I/O Banks 1 and 2. The majority of parallel Flash PROMs use a single 3.3V supply voltage. Consequently, in most cases, the FPGA's VCCO_1 and VCCO_2 supply voltages must also be 3.3V to match the parallel Flash PROM. There are some 1.8V parallel Flash PROMs available and the FPGA interfaces with these devices if the VCCO_1 and VCCO_2 supplies are also 1.8V.

Power-On Precautions if PROM Supply is Last in Sequence

Like SPI Flash PROMs, parallel Flash PROMs typically require some amount of internal initialization time when the supply voltage reaches its minimum value.

The PROM supply voltage also connects to the FPGA's VCCO_2 supply input. In many systems, the PROM supply feeding the FPGA's VCCO_2 input is valid before the FPGA's other V_{CCINT} and V_{CCAUX} supplies, and consequently, there is no issue. However, if the PROM supply is last in the sequence, a potential race occurs between the FPGA and the parallel Flash PROM. See Power-On Precautions if 3.3V Supply is Last in Sequence for a similar description of the issue for SPI Flash PROMs.

Supported Parallel NOR Flash PROM Densities

Table 60 indicates the smallest usable parallel Flash PROM to program a single Spartan-3E FPGA. Parallel Flash density is specified in bits but addressed as bytes. The FPGA presents up to 24 address lines during configuration but not all are required for single FPGA applications. Table 60 shows the minimum required number of address lines between the FPGA and parallel Flash PROM. The actual number of address line required depends on the density of the attached parallel Flash PROM.

A multiple-FPGA daisy-chained application requires a parallel Flash PROM large enough to contain the sum of the FPGA file sizes. An application can also use a larger-density parallel Flash PROM to hold additional data beyond just FPGA configuration data. For example, the parallel Flash PROM can also contain the application code for a MicroBlaze RISC processor core implemented within the Spartan-3E FPGA. After configuration, the MicroBlaze processor can execute directly from external Flash or can copy the code to other, faster system memory before executing the code.

Table 60: **Number of Bits to Program a Spartan-3E FPGA and Smallest Parallel Flash PROM**

Spartan-3E FPGA	Uncompressed File Sizes (bits)	Smallest Usable Parallel Flash PROM	Minimum Required Address Lines
XC3S100E	581,344	1 Mbit	A[16:0]
XC3S250E	1,353,728	2 Mbit	A[17:0]
XC3S500E	2,270,208	4 Mbit	A[18:0]
XC3S1200E	3,841,184	4 Mbit	A[18:0]
XC3S1600E	5,969,696	8 Mbit	A[19:0]

can also be eliminated from the interface. However, RDWR_B must remain Low during configuration.

After configuration, all of the interface pins except DONE and PROG_B are available as user I/Os. Alternatively, the bidirectional SelectMAP configuration interface is available after configuration. To continue using SelectMAP mode, set the ***Persist*** bitstream generator option to ***Yes***. The external host can then read and verify configuration data.

The Persist option will maintain A20-A23 as configuration pins although they are not used in SelectMAP mode.

The Slave Parallel mode is also used with BPI mode to create multi-FPGA daisy-chains. The lead FPGA is set for BPI mode configuration; all the downstream daisy-chain FPGAs are set for Slave Parallel configuration, as highlighted in Figure 59.

Table 65: **Slave Parallel Mode Connections**

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
HSWAP	Input	**User I/O Pull-Up Control**. When Low during configuration, enables pull-up resistors in all I/O pins to respective I/O bank V_{CCO} input. 0: Pull-ups during configuration 1: No pull-ups	Drive at valid logic level throughout configuration.	User I/O
M[2:0]	Input	**Mode Select**. Selects the FPGA configuration mode. See Design Considerations for the HSWAP, M[2:0], and VS[2:0] Pins.	M2 = 1, M1 = 1, M0 = 0 Sampled when INIT_B goes High.	User I/O
D[7:0]	Input	**Data Input**.	Byte-wide data provided by host. FPGA captures data on rising CCLK edge.	User I/O. If bitstream option ***Persist=Yes***, becomes part of SelectMap parallel peripheral interface.
BUSY	Output	**Busy Indicator**.	If CCLK frequency is < 50 MHz, this pin may be ignored. When High, indicates that the FPGA is not ready to receive additional configuration data. Host must hold data an additional clock cycle.	User I/O. If bitstream option ***Persist=Yes***, becomes part of SelectMap parallel peripheral interface.
CSI_B	Input	**Chip Select Input**. Active Low.	Must be Low throughout configuration.	User I/O. If bitstream option ***Persist=Yes***, becomes part of SelectMap parallel peripheral interface.
RDWR_B	Input	**Read/Write Control**. Active Low write enable.	Must be Low throughout configuration.	User I/O. If bitstream option ***Persist=Yes***, becomes part of SelectMap parallel peripheral interface.
CCLK	Input	**Configuration Clock**. If CCLK PCB trace is long or has multiple connections, terminate this output to maintain signal integrity. See CCLK Design Considerations.	External clock.	User I/O If bitstream option ***Persist=Yes***, becomes part of SelectMap parallel peripheral interface.
CSO_B	Output	**Chip Select Output**. Active Low.	Not used in single FPGA applications. In a daisy-chain configuration, this pin connects to the CSI_B pin of the next FPGA in the chain. Actively drives.	User I/O

Table 65: **Slave Parallel Mode Connections *(Cont'd)***

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
INIT_B	Open-drain bidirectional I/O	**Initialization Indicator**. Active Low. Goes Low at the start of configuration during the Initialization memory clearing process. Released at the end of memory clearing, when mode select pins are sampled. In daisy-chain applications, this signal requires an external 4.7 kΩ pull-up resistor to VCCO_2.	Active during configuration. If CRC error detected during configuration, FPGA drives INIT_B Low.	User I/O. If unused in the application, drive INIT_B High.
DONE	Open-drain bidirectional I/O	**FPGA Configuration Done**. Low during configuration. Goes High when FPGA successfully completes configuration. Requires external 330 Ω pull-up resistor to 2.5V.	Low indicates that the FPGA is not yet configured.	Pulled High via external pull-up. When High, indicates that the FPGA successfully configured.
PROG_B	Input	**Program FPGA**. Active Low. When asserted Low for 500 ns or longer, forces the FPGA to restart its configuration process by clearing configuration memory and resetting the DONE and INIT_B pins once PROG_B returns High. Recommend external 4.7 kΩ pull-up resistor to 2.5V. Internal pull-up value may be weaker (see Table 78). If driving externally with a 3.3V output, use an open-drain or open-collector driver or use a current limiting series resistor.	Must be High to allow configuration to start.	Drive PROG_B Low and release to reprogram FPGA.

Voltage Compatibility

Ⓥ Most Slave Parallel interface signals are within the FPGA's I/O Bank 2, supplied by the VCCO_2 supply input. The VCCO_2 voltage can be 1.8V, 2.5V, or 3.3V to match the requirements of the external host, ideally 2.5V. Using 1.8V or 3.3V requires additional design considerations as the DONE and PROG_B pins are powered by the FPGA's 2.5V V_{CCAUX} supply. See XAPP453: *The 3.3V Configuration of Spartan-3 FPGAs* for additional information.

Daisy-Chaining

If the application requires multiple FPGAs with different configurations, then configure the FPGAs using a daisy chain. Use Slave Parallel mode (M[2:0] = <1:1:0>) for all FPGAs in the daisy-chain. The schematic in Figure 62 is optimized for FPGA downloading and does not support the SelectMAP read interface. The FPGA's RDWR_B pin must be Low during configuration.

After the lead FPGA is filled with its configuration data, the lead FPGA enables the next FPGA in the daisy-chain by asserting is chip-select output, CSO_B.

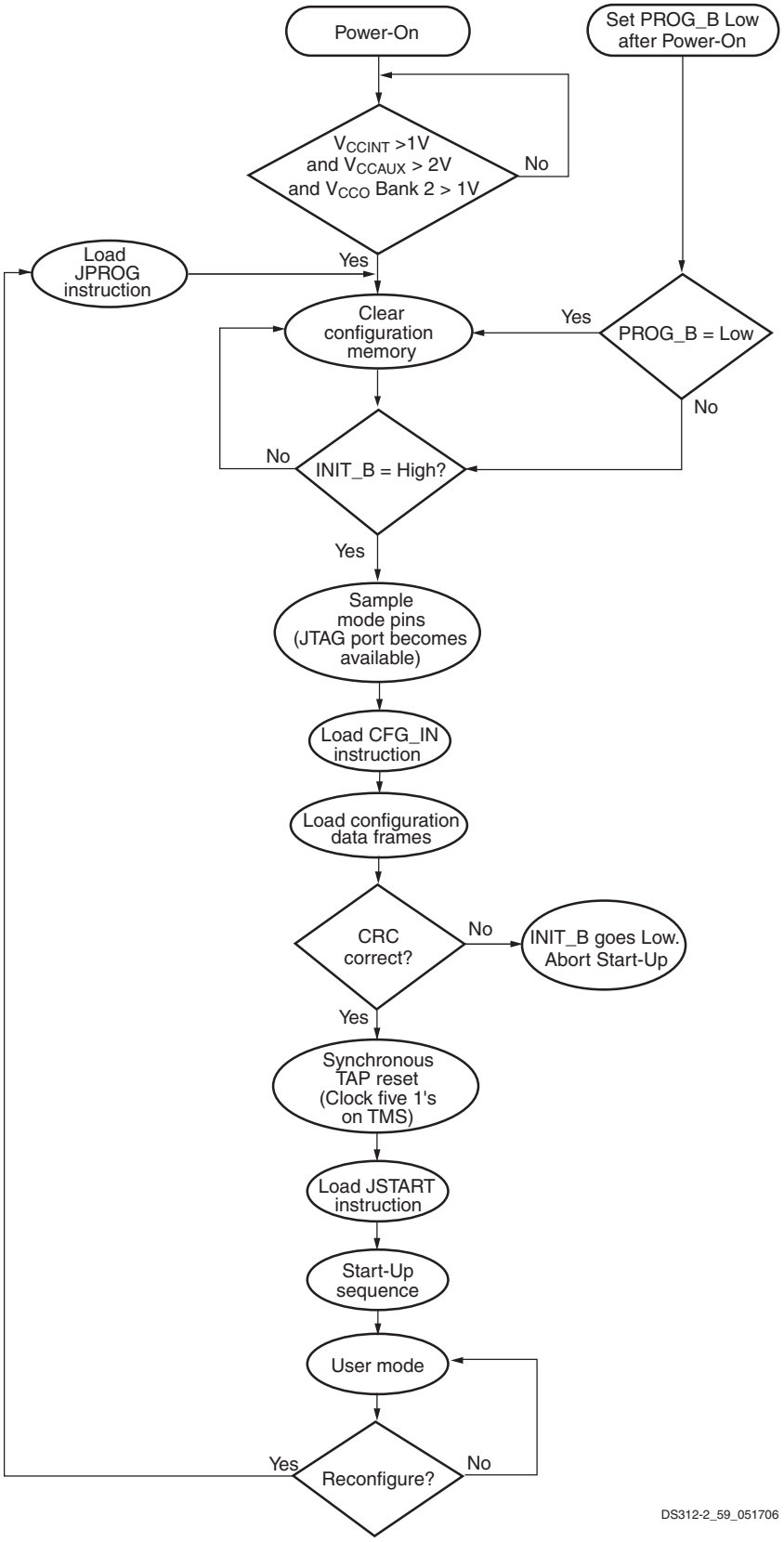

Figure 67: **Boundary-Scan Configuration Flow Diagram**

Date	Version	Revision
03/16/07	3.5	Added information about new Spartan-3 Generation user guides (Design Documentation Available). Added cross-references to UG331: *Spartan-3 Generation FPGA User Guide* and to UG332: *Spartan-3 Generation Configuration User Guide*. Added note about possible JTAG configuration issues when the FPGA mode pins are set for Master mode and using software prior to ISE 9.1.01i (JTAG Mode). Removed a few lingering references to "weak" pull-up resistors, including in Figure 12. Removed vestigial references regarding the LDC[2:0] and HDC pins during Slave Parallel Mode configuration. These pins are not used in this configuration mode.
05/29/07	3.6	Added information about HSWAP and PCI differences between steppings to Table 71. Removed "Performance Differences between Global Buffers" to match improved specs in Module 3. Updated PROG_B pulse width descriptions to match specification in Module 3.
04/18/08	3.7	Corrected Figure 6 to show six taps and updated associated text. Added note for recommended pull-up on DONE in Table 55 and elsewhere. Added a caution regarding Persist of pins A20-A23. Updated Stepping description in Table 71 to note that only Stepping 1 is in production today. Updated links.
08/26/09	3.8	Added a frequency limitation to Equation 6. Added a new Equation 7 with a frequency limitation. Added a Spread Spectrum, page 56 paragraph. Added Table 42, page 60. Updated a Flash vendor name in Table 61, page 88. Removed the $\leq$ symbol from the flash read access times in Table 62, page 88. Revised the first paragraph in Configuration Sequence, page 101. Revised the first paragraph in Power-On Behavior, page 110. Revised the second paragraph in Production Stepping, page 111. Revised the first paragraph in Ordering a Later Stepping, page 111.
10/29/12	4.0	Added Notice of Disclaimer. This product is not recommended for new designs. Updated the design note section in VARIABLE Phase Shift Mode. Added the VQ100 to the Quadrant Clock Routing section.

Notice of Disclaimer

Power Supply Specifications

Table 74: **Supply Voltage Thresholds for Power-On Reset**

Symbol	Description	Min	Max	Units
V_{CCINTT}	Threshold for the V_{CCINT} supply	0.4	1.0	V
V_{CCAUXT}	Threshold for the V_{CCAUX} supply	0.8	2.0	V
V_{CCO2T}	Threshold for the V_{CCO} Bank 2 supply	0.4	1.0	V

Notes:

1. V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies to the FPGA can be applied in any order. However, the FPGA's configuration source (Platform Flash, SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source. In Step 0 devices using the HSWAP internal pull-up, V_{CCINT} must be applied before V_{CCAUX}.
2. To ensure successful power-on, V_{CCINT}, V_{CCO} Bank 2, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 75: **Supply Voltage Ramp Rate**

Symbol	Description	Min	Max	Units
V_{CCINTR}	Ramp rate from GND to valid V_{CCINT} supply level	0.2	50	ms
V_{CCAUXR}	Ramp rate from GND to valid V_{CCAUX} supply level	0.2	50	ms
V_{CCO2R}	Ramp rate from GND to valid V_{CCO} Bank 2 supply level	0.2	50	ms

Notes:

1. V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies to the FPGA can be applied in any order. However, the FPGA's configuration source (Platform Flash, SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source. In Step 0 devices using the HSWAP internal pull-up, V_{CCINT} must be applied before V_{CCAUX}.
2. To ensure successful power-on, V_{CCINT}, V_{CCO} Bank 2, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 76: **Supply Voltage Levels Necessary for Preserving RAM Contents**

Symbol	Description	Min	Units
V_{DRINT}	V_{CCINT} level required to retain RAM data	1.0	V
V_{DRAUX}	V_{CCAUX} level required to retain RAM data	2.0	V

Notes:

1. RAM contents include configuration data.

Block RAM Timing

Table 103: **Block RAM Timing**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{BCKO}	When reading from block RAM, the delay from the active transition at the CLK input to data appearing at the DOUT output	-	2.45	-	2.82	ns
Setup Times						
T_{BACK}	Setup time for the ADDR inputs before the active transition at the CLK input of the block RAM	0.33	-	0.38	-	ns
T_{BDCK}	Setup time for data at the DIN inputs before the active transition at the CLK input of the block RAM	0.23	-	0.23	-	ns
T_{BECK}	Setup time for the EN input before the active transition at the CLK input of the block RAM	0.67	-	0.77	-	ns
T_{BWCK}	Setup time for the WE input before the active transition at the CLK input of the block RAM	1.09	-	1.26	-	ns
Hold Times						
T_{BCKA}	Hold time on the ADDR inputs after the active transition at the CLK input	0.12	-	0.14	-	ns
T_{BCKD}	Hold time on the DIN inputs after the active transition at the CLK input	0.12	-	0.13	-	ns
T_{BCKE}	Hold time on the EN input after the active transition at the CLK input	0	-	0	-	ns
T_{BCKW}	Hold time on the WE input after the active transition at the CLK input	0	-	0	-	ns
Clock Timing						
T_{BPWH}	High pulse width of the CLK signal	1.39	-	1.59	-	ns
T_{BPWL}	Low pulse width of the CLK signal	1.39	-	1.59	-	ns
Clock Frequency						
F_{BRAM}	Block RAM clock frequency. RAM read output value written back into RAM, for shift-registers and circular buffers. Write-only or read-only performance is faster.	0	270	0	230	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 77.

Date	Version	Revision
08/26/09	3.8	Added reference to XAPP459 in Table 73 note 2. Updated BPI timing in Figure 77, Table 119, and Table 120. Removed V_{REF} requirements for differential HSTL and differential SSTL in Table 95. Added Spread Spectrum paragraph. Revised hold times for $T_{IOICKPD}$ in Table 88 and setup times for T_{DICK} in Table 98. Added note 4 to Table 106 and note 3 to Table 107, and updated note 6 for Table 107 to add input jitter.
10/29/12	4.0	Added Notice of Disclaimer. This product is not recommended for new designs. Revised note 2 in Table 73. Revised note 2 and V_{IN} description in Table 77, and added note 5. Added note 3 to Table 78.

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Spartan-3 FPGA Family: Pinout Descriptions

DS312 (4.0) October 29, 2012 **Product Specification**

Introduction

This section describes the various pins on a Spartan®-3E FPGA and how they connect within the supported component packages.

Pin Types

Most pins on a Spartan-3E FPGA are general-purpose, user-defined I/O pins. There are, however, up to 11 different functional types of pins on Spartan-3E packages, as outlined in Table 124. In the package footprint drawings that follow, the individual pins are color-coded according to pin type as in the table.

Table 124: **Types of Pins on Spartan-3E FPGAs**

Type / Color Code	Description	Pin Name(s) in Type[1]
I/O	Unrestricted, general-purpose user-I/O pin. Most pins can be paired together to form differential I/Os.	IO IO_Lxxy_#
INPUT	Unrestricted, general-purpose input-only pin. This pin does not have an output structure, differential termination resistor, or PCI clamp diode.	IP IP_Lxxy_#
DUAL	Dual-purpose pin used in some configuration modes during the configuration process and then usually available as a user I/O after configuration. If the pin is not used during configuration, this pin behaves as an I/O-type pin. Some of the dual-purpose pins are also shared with bottom-edge global (GCLK) or right-half (RHCLK) clock inputs. See the Configuration section in Module 2 for additional information on these signals.	M[2:0] HSWAP CCLK MOSI/CSI_B D[7:1] D0/DIN CSO_B RDWR_B BUSY/DOUT INIT_B A[23:20] A19/VS2 A18/VS1 A17/VS0 A[16:0] LDC[2:0] HDC
VREF	Dual-purpose pin that is either a user-I/O pin or Input-only pin, or, along with all other VREF pins in the same bank, provides a reference voltage input for certain I/O standards. If used for a reference voltage within a bank, all VREF pins within the bank must be connected.	IP/VREF_# IP_Lxxy_#/VREF_# IO/VREF_# IO_Lxxy_#/VREF_#
CLK	Either a user-I/O pin or Input-only pin, or an input to a specific clock buffer driver. Every package has 16 global clock inputs that optionally clock the entire device. The RHCLK inputs optionally clock the right-half of the device. The LHCLK inputs optionally clock the left-half of the device. Some of the clock pins are shared with the dual-purpose configuration pins and are considered DUAL-type. See the Clocking Infrastructure section in Module 2 for additional information on these signals.	IO_Lxxy_#/GCLK[15:10, 7:2] IP_Lxxy_#/GCLK[9:8, 1:0] IO_Lxxy_#/LHCLK[7:0] IO_Lxxy_#/RHCLK[7:0]
CONFIG	Dedicated configuration pin. Not available as a user-I/O pin. Every package has two dedicated configuration pins. These pins are powered by VCCAUX. See the Configuration section in Module 2 for details.	DONE, PROG_B
JTAG	Dedicated JTAG pin. Not available as a user-I/O pin. Every package has four dedicated JTAG pins. These pins are powered by VCCAUX.	TDI, TMS, TCK, TDO
GND	Dedicated ground pin. The number of GND pins depends on the package used. All must be connected.	GND

PQ208 Footprint (Right)

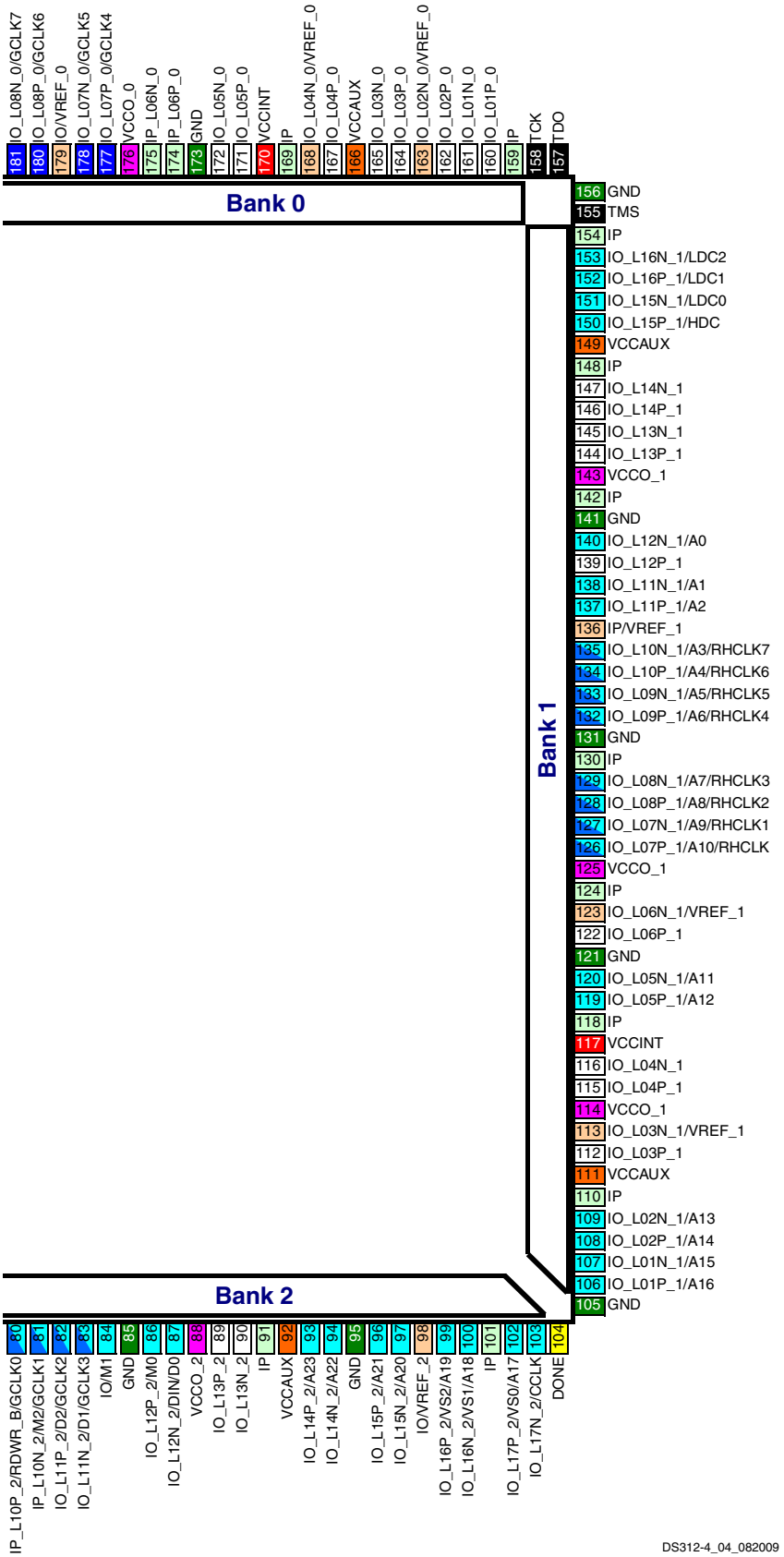


Figure 84: **PQ208 Footprint (Right)**

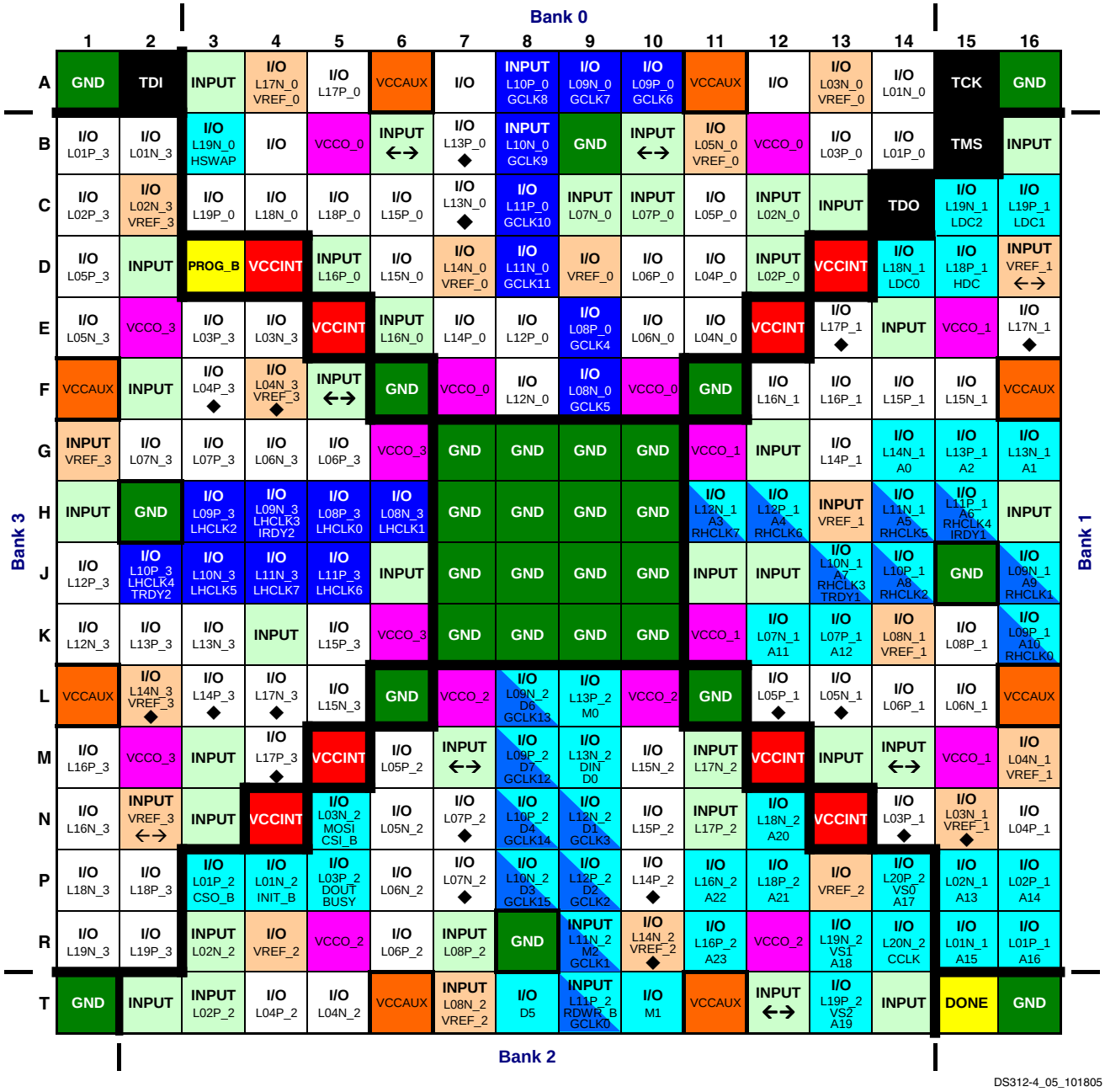
Table 143: **FT256 Package Pinout *(Cont'd)***

Bank	XC3S250E Pin Name	XC3S500E Pin Name	XC3S1200E Pin Name	FT256 Ball	Type
1	N.C. (◆)	IO_L05P_1	IO_L05P_1	L12	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O
1	IO_L06N_1	IO_L06N_1	IO_L06N_1	L15	I/O
1	IO_L06P_1	IO_L06P_1	IO_L06P_1	L14	I/O
1	IO_L07N_1/A11	IO_L07N_1/A11	IO_L07N_1/A11	K12	DUAL
1	IO_L07P_1/A12	IO_L07P_1/A12	IO_L07P_1/A12	K13	DUAL
1	IO_L08N_1/VREF_1	IO_L08N_1/VREF_1	IO_L08N_1/VREF_1	K14	VREF
1	IO_L08P_1	IO_L08P_1	IO_L08P_1	K15	I/O
1	IO_L09N_1/A9/RHCLK1	IO_L09N_1/A9/RHCLK1	IO_L09N_1/A9/RHCLK1	J16	RHCLK/DUAL
1	IO_L09P_1/A10/RHCLK0	IO_L09P_1/A10/RHCLK0	IO_L09P_1/A10/RHCLK0	K16	RHCLK/DUAL
1	IO_L10N_1/A7/RHCLK3/ TRDY1	IO_L10N_1/A7/RHCLK3/ TRDY1	IO_L10N_1/A7/RHCLK3/ TRDY1	J13	RHCLK/DUAL
1	IO_L10P_1/A8/RHCLK2	IO_L10P_1/A8/RHCLK2	IO_L10P_1/A8/RHCLK2	J14	RHCLK/DUAL
1	IO_L11N_1/A5/RHCLK5	IO_L11N_1/A5/RHCLK5	IO_L11N_1/A5/RHCLK5	H14	RHCLK/DUAL
1	IO_L11P_1/A6/RHCLK4/ IRDY1	IO_L11P_1/A6/RHCLK4/ IRDY1	IO_L11P_1/A6/RHCLK4/ IRDY1	H15	RHCLK/DUAL
1	IO_L12N_1/A3/RHCLK7	IO_L12N_1/A3/RHCLK7	IO_L12N_1/A3/RHCLK7	H11	RHCLK/DUAL
1	IO_L12P_1/A4/RHCLK6	IO_L12P_1/A4/RHCLK6	IO_L12P_1/A4/RHCLK6	H12	RHCLK/DUAL
1	IO_L13N_1/A1	IO_L13N_1/A1	IO_L13N_1/A1	G16	DUAL
1	IO_L13P_1/A2	IO_L13P_1/A2	IO_L13P_1/A2	G15	DUAL
1	IO_L14N_1/A0	IO_L14N_1/A0	IO_L14N_1/A0	G14	DUAL
1	IO_L14P_1	IO_L14P_1	IO_L14P_1	G13	I/O
1	IO_L15N_1	IO_L15N_1	IO_L15N_1	F15	I/O
1	IO_L15P_1	IO_L15P_1	IO_L15P_1	F14	I/O
1	IO_L16N_1	IO_L16N_1	IO_L16N_1	F12	I/O
1	IO_L16P_1	IO_L16P_1	IO_L16P_1	F13	I/O
1	N.C. (◆)	IO_L17N_1	IO_L17N_1	E16	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O
1	N.C. (◆).	IO_L17P_1	IO_L17P_1	E13	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O
1	IO_L18N_1/LDC0	IO_L18N_1/LDC0	IO_L18N_1/LDC0	D14	DUAL
1	IO_L18P_1/HDC	IO_L18P_1/HDC	IO_L18P_1/HDC	D15	DUAL
1	IO_L19N_1/LDC2	IO_L19N_1/LDC2	IO_L19N_1/LDC2	C15	DUAL
1	IO_L19P_1/LDC1	IO_L19P_1/LDC1	IO_L19P_1/LDC1	C16	DUAL
1	IP	IP	IP	B16	INPUT
1	IP	IP	IP	E14	INPUT
1	IP	IP	IP	G12	INPUT
1	IP	IP	IP	H16	INPUT
1	IP	IP	IP	J11	INPUT
1	IP	IP	IP	J12	INPUT
1	IP	IP	IP	M13	INPUT

Table 143: **FT256 Package Pinout *(Cont'd)***

Bank	XC3S250E Pin Name	XC3S500E Pin Name	XC3S1200E Pin Name	FT256 Ball	Type
1	IO	IO	IP	M14	***250E:*** I/O ***500E:*** I/O ***1200E:*** INPUT
1	IO/VREF_1	IP/VREF_1	IP/VREF_1	D16	***250E:*** VREF(I/O) ***500E:*** VREF(INPUT) ***1200E:*** VREF(INPUT)
1	IP/VREF_1	IP/VREF_1	IP/VREF_1	H13	VREF
1	VCCO_1	VCCO_1	VCCO_1	E15	VCCO
1	VCCO_1	VCCO_1	VCCO_1	G11	VCCO
1	VCCO_1	VCCO_1	VCCO_1	K11	VCCO
1	VCCO_1	VCCO_1	VCCO_1	M15	VCCO
2	IP	IP	IO	M7	***250E:*** INPUT ***500E:*** INPUT ***1200E:*** I/O
2	IP	IP	IO	T12	***250E:*** INPUT ***500E:*** INPUT ***1200E:*** I/O
2	IO/D5	IO/D5	IO/D5	T8	DUAL
2	IO/M1	IO/M1	IO/M1	T10	DUAL
2	IO/VREF_2	IO/VREF_2	IO/VREF_2	P13	VREF
2	IO/VREF_2	IO/VREF_2	IO/VREF_2	R4	VREF
2	IO_L01N_2/INIT_B	IO_L01N_2/INIT_B	IO_L01N_2/INIT_B	P4	DUAL
2	IO_L01P_2/CSO_B	IO_L01P_2/CSO_B	IO_L01P_2/CSO_B	P3	DUAL
2	IO_L03N_2/MOSI/CSI_B	IO_L03N_2/MOSI/CSI_B	IO_L03N_2/MOSI/CSI_B	N5	DUAL
2	IO_L03P_2/DOUT/BUSY	IO_L03P_2/DOUT/BUSY	IO_L03P_2/DOUT/BUSY	P5	DUAL
2	IO_L04N_2	IO_L04N_2	IO_L04N_2	T5	I/O
2	IO_L04P_2	IO_L04P_2	IO_L04P_2	T4	I/O
2	IO_L05N_2	IO_L05N_2	IO_L05N_2	N6	I/O
2	IO_L05P_2	IO_L05P_2	IO_L05P_2	M6	I/O
2	IO_L06N_2	IO_L06N_2	IO_L06N_2	P6	I/O
2	IO_L06P_2	IO_L06P_2	IO_L06P_2	R6	I/O
2	N.C. (◆)	IO_L07N_2	IO_L07N_2	P7	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O
2	N.C. (◆)	IO_L07P_2	IO_L07P_2	N7	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O
2	IO_L09N_2/D6/GCLK13	IO_L09N_2/D6/GCLK13	IO_L09N_2/D6/GCLK13	L8	DUAL/GCLK
2	IO_L09P_2/D7/GCLK12	IO_L09P_2/D7/GCLK12	IO_L09P_2/D7/GCLK12	M8	DUAL/GCLK
2	IO_L10N_2/D3/GCLK15	IO_L10N_2/D3/GCLK15	IO_L10N_2/D3/GCLK15	P8	DUAL/GCLK
2	IO_L10P_2/D4/GCLK14	IO_L10P_2/D4/GCLK14	IO_L10P_2/D4/GCLK14	N8	DUAL/GCLK
2	IO_L12N_2/D1/GCLK3	IO_L12N_2/D1/GCLK3	IO_L12N_2/D1/GCLK3	N9	DUAL/GCLK
2	IO_L12P_2/D2/GCLK2	IO_L12P_2/D2/GCLK2	IO_L12P_2/D2/GCLK2	P9	DUAL/GCLK
2	IO_L13N_2/DIN/D0	IO_L13N_2/DIN/D0	IO_L13N_2/DIN/D0	M9	DUAL
2	IO_L13P_2/M0	IO_L13P_2/M0	IO_L13P_2/M0	L9	DUAL

FT256 Footprint



DS312-4_05_101805

Figure 85: **FT256 Package Footprint (top view)**

2	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	8	**VCCINT:** Internal core supply voltage (+1.2V)
28	**GND:** Ground	16	**VCCO:** Output voltage supply for bank	8	**VCCAUX:** Auxiliary supply voltage (+2.5V)
6 ↔	**Migration Difference:** For flexible package migration, use these pins as inputs.	18 (◆)	Unconnected pins on XC3S250E		

FG484: 484-ball Fine-pitch Ball Grid Array

The 484-ball fine-pitch ball grid array, FG484, supports the XC3S1600E FPGA.

Table 154 lists all the FG484 package pins. They are sorted by bank number and then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at:

http://www.xilinx.com/support/documentation/data_sheets/s3e_pin.zip

Pinout Table

Table 154: **FG484 Package Pinout**

Bank	XC3S1600E Pin Name	FG484 Ball	Type
0	IO	B6	I/O
0	IO	B13	I/O
0	IO	C5	I/O
0	IO	C14	I/O
0	IO	E16	I/O
0	IO	F9	I/O
0	IO	F16	I/O
0	IO	G8	I/O
0	IO	H10	I/O
0	IO	H15	I/O
0	IO	J11	I/O
0	IO/VREF_0	G12	VREF
0	IO_L01N_0	C18	I/O
0	IO_L01P_0	C19	I/O
0	IO_L03N_0/VREF_0	A20	VREF
0	IO_L03P_0	A21	I/O
0	IO_L04N_0	A19	I/O
0	IO_L04P_0	A18	I/O
0	IO_L06N_0	C16	I/O
0	IO_L06P_0	D16	I/O
0	IO_L07N_0	A16	I/O
0	IO_L07P_0	A17	I/O
0	IO_L09N_0/VREF_0	B15	VREF
0	IO_L09P_0	C15	I/O
0	IO_L10N_0	G15	I/O
0	IO_L10P_0	F15	I/O
0	IO_L11N_0	D14	I/O
0	IO_L11P_0	E14	I/O
0	IO_L12N_0/VREF_0	A14	VREF
0	IO_L12P_0	A15	I/O
0	IO_L13N_0	H14	I/O
0	IO_L13P_0	G14	I/O
0	IO_L15N_0	G13	I/O
0	IO_L15P_0	F13	I/O
0	IO_L16N_0	J13	I/O
0	IO_L16P_0	H13	I/O
0	IO_L18N_0/GCLK5	E12	GCLK
0	IO_L18P_0/GCLK4	F12	GCLK
0	IO_L19N_0/GCLK7	C12	GCLK
0	IO_L19P_0/GCLK6	B12	GCLK
0	IO_L21N_0/GCLK11	B11	GCLK
0	IO_L21P_0/GCLK10	C11	GCLK
0	IO_L22N_0	D11	I/O
0	IO_L22P_0	E11	I/O
0	IO_L24N_0	A9	I/O
0	IO_L24P_0	A10	I/O
0	IO_L25N_0/VREF_0	D10	VREF
0	IO_L25P_0	C10	I/O
0	IO_L27N_0	H8	I/O
0	IO_L27P_0	H9	I/O
0	IO_L28N_0	C9	I/O
0	IO_L28P_0	B9	I/O
0	IO_L29N_0	E9	I/O
0	IO_L29P_0	D9	I/O
0	IO_L30N_0	B8	I/O
0	IO_L30P_0	A8	I/O
0	IO_L32N_0/VREF_0	F7	VREF
0	IO_L32P_0	F8	I/O
0	IO_L33N_0	A6	I/O
0	IO_L33P_0	A7	I/O
0	IO_L35N_0	A4	I/O
0	IO_L35P_0	A5	I/O
0	IO_L36N_0	E7	I/O
0	IO_L36P_0	D7	I/O
0	IO_L38N_0/VREF_0	D6	VREF
0	IO_L38P_0	D5	I/O
0	IO_L39N_0	B4	I/O
0	IO_L39P_0	B3	I/O
0	IO_L40N_0/HSWAP	D4	DUAL
0	IO_L40P_0	C4	I/O
0	IP	B19	INPUT

Table 154: **FG484 Package Pinout *(Cont'd)***

Bank	XC3S1600E Pin Name	FG484 Ball	Type
3	IO_L11N_3	H1	I/O
3	IO_L11P_3	J1	I/O
3	IO_L12N_3	J6	I/O
3	IO_L12P_3	J5	I/O
3	IO_L13N_3/VREF_3	J3	VREF
3	IO_L13P_3	K3	I/O
3	IO_L14N_3	J8	I/O
3	IO_L14P_3	K8	I/O
3	IO_L15N_3	K4	I/O
3	IO_L15P_3	K5	I/O
3	IO_L16N_3	K1	I/O
3	IO_L16P_3	L1	I/O
3	IO_L17N_3	L7	I/O
3	IO_L17P_3	K7	I/O
3	IO_L18N_3/LHCLK1	L5	LHCLK
3	IO_L18P_3/LHCLK0	M5	LHCLK
3	IO_L19N_3/LHCLK3/IRDY2	M8	LHCLK
3	IO_L19P_3/LHCLK2	L8	LHCLK
3	IO_L20N_3/LHCLK5	N1	LHCLK
3	IO_L20P_3/LHCLK4/TRDY2	M1	LHCLK
3	IO_L21N_3/LHCLK7	M4	LHCLK
3	IO_L21P_3/LHCLK6	M3	LHCLK
3	IO_L22N_3	N6	I/O
3	IO_L22P_3	N7	I/O
3	IO_L23N_3	P8	I/O
3	IO_L23P_3	N8	I/O
3	IO_L24N_3/VREF_3	N4	VREF
3	IO_L24P_3	N5	I/O
3	IO_L25N_3	P2	I/O
3	IO_L25P_3	P1	I/O
3	IO_L26N_3	R7	I/O
3	IO_L26P_3	P7	I/O
3	IO_L27N_3	P6	I/O
3	IO_L27P_3	P5	I/O
3	IO_L28N_3	R2	I/O
3	IO_L28P_3	R1	I/O
3	IO_L29N_3	R3	I/O
3	IO_L29P_3	R4	I/O
3	IO_L30N_3	T6	I/O
3	IO_L30P_3	R6	I/O
3	IO_L31N_3	U2	I/O
3	IO_L31P_3	U1	I/O
3	IO_L32N_3	T4	I/O
3	IO_L32P_3	T5	I/O

Table 154: **FG484 Package Pinout *(Cont'd)***

Bank	XC3S1600E Pin Name	FG484 Ball	Type
3	IO_L33N_3	W1	I/O
3	IO_L33P_3	V1	I/O
3	IO_L34N_3	U4	I/O
3	IO_L34P_3	U3	I/O
3	IO_L35N_3	V4	I/O
3	IO_L35P_3	V3	I/O
3	IO_L36N_3/VREF_3	W3	VREF
3	IO_L36P_3	W2	I/O
3	IO_L37N_3	Y2	I/O
3	IO_L37P_3	Y1	I/O
3	IO_L38N_3	AA1	I/O
3	IO_L38P_3	AA2	I/O
3	IP	F2	INPUT
3	IP	F5	INPUT
3	IP	G3	INPUT
3	IP	H7	INPUT
3	IP	J7	INPUT
3	IP	K2	INPUT
3	IP	K6	INPUT
3	IP	M2	INPUT
3	IP	M6	INPUT
3	IP	N3	INPUT
3	IP	P3	INPUT
3	IP	R8	INPUT
3	IP	T1	INPUT
3	IP	T7	INPUT
3	IP	U5	INPUT
3	IP	W4	INPUT
3	IP/VREF_3	L3	VREF
3	IP/VREF_3	T3	VREF
3	VCCO_3	E2	VCCO
3	VCCO_3	H6	VCCO
3	VCCO_3	J2	VCCO
3	VCCO_3	M7	VCCO
3	VCCO_3	N2	VCCO
3	VCCO_3	R5	VCCO
3	VCCO_3	V2	VCCO
GND	GND	A1	GND
GND	GND	A11	GND
GND	GND	A22	GND
GND	GND	B7	GND
GND	GND	B16	GND
GND	GND	C3	GND
GND	GND	C20	GND