AMD Xilinx - XC3S250E-5FTG256C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	612
Number of Logic Elements/Cells	5508
Total RAM Bits	221184
Number of I/O	172
Number of Gates	250000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s250e-5ftg256c

Configuration

Spartan-3E FPGAs are programmed by loading configuration data into robust, reprogrammable, static CMOS configuration latches (CCLs) that collectively control all functional elements and routing resources. The FPGA's configuration data is stored externally in a PROM or some other non-volatile medium, either on or off the board. After applying power, the configuration data is written to the FPGA using any of seven different modes:

- Master Serial from a Xilinx Platform Flash PROM
- Serial Peripheral Interface (SPI) from an industry-standard SPI serial Flash
- Byte Peripheral Interface (BPI) Up or Down from an industry-standard x8 or x8/x16 parallel NOR Flash
- Slave Serial, typically downloaded from a processor
- Slave Parallel, typically downloaded from a processor
- Boundary Scan (JTAG), typically downloaded from a processor or system tester.

Furthermore, Spartan-3E FPGAs support MultiBoot configuration, allowing two or more FPGA configuration bitstreams to be stored in a single parallel NOR Flash. The FPGA application controls which configuration to load next and when to load it.

I/O Capabilities

The Spartan-3E FPGA SelectIO interface supports many popular single-ended and differential standards. Table 2 shows the number of user I/Os as well as the number of differential I/O pairs available for each device/package combination.

Spartan-3E FPGAs support the following single-ended standards:

- 3.3V low-voltage TTL (LVTTL)
- Low-voltage CMOS (LVCMOS) at 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V
- 3V PCI at 33 MHz, and in some devices, 66 MHz
- HSTL I and III at 1.8V, commonly used in memory applications
- SSTL I at 1.8V and 2.5V, commonly used for memory applications

Spartan-3E FPGAs support the following differential standards:

- LVDS
- Bus LVDS
- mini-LVDS
- RSDS
- Differential HSTL (1.8V, Types I and III)
- Differential SSTL (2.5V and 1.8V, Type I)
- 2.5V LVPECL inputs

Table 2: **Available User I/Os and Differential (Diff) I/O Pairs**

Package	VQ100 VQG100		CP132 CPG132		TQ144 TQG144		PQ208 PQG208		FT256 FTG256		FG320 FGG320		FG400 FGG400		FG484 FGG484	
Footprint Size (mm)	**16 x 16**		**8 x 8**		**22 x 22**		**30.5 x 30.5**		**17 x 17**		**19 x 19**		**21 x 21**		**23 x 23**	
Device	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**
XC3S100E	**66**(2) *9(7)*	**30** *(2)*	**83** *(11)*	**35** *(2)*	**108** *(28)*	**40** *(4)*	-	-	-	-	-	-	-	-	-	-
XC3S250E	**66** *(7)*	**30** *(2)*	**92** *(7)*	**41** *(2)*	**108** *(28)*	**40** *(4)*	**158** *(32)*	**65** *(5)*	**172** *(40)*	**68** *(8)*	-	-	-	-	-	-
XC3S500E	**66**(3) *(7)*	**30** *(2)*	**92** *(7)*	**41** *(2)*	-	-	**158** *(32)*	**65** *(5)*	**190** *(41)*	**77** *(8)*	**232** *(56)*	**92** *(12)*	-	-	-	-
XC3S1200E	-	-	-	-	-	-	-	-	**190** *(40)*	**77** *(8)*	**250** *(56)*	**99** *(12)*	**304** *(72)*	**124** *(20)*	-	-
XC3S1600E	-	-	-	-	-	-	-	-	-	-	**250** *(56)*	**99** *(12)*	**304** *(72)*	**124** *(20)*	**376** *(82)*	**156** *(21)*

Notes:

1. All Spartan-3E devices provided in the same package are pin-compatible as further described in Module 4, Pinout Descriptions.
2. The number shown in **bold** indicates the maximum number of I/O and input-only pins. The number shown in (*italics*) indicates the number of input-only pins.
3. The XC3S500E is available in the VQG100 Pb-free package and not the standard VQ100. The VQG100 and VQ100 pin-outs are identical and general references to the VQ100 will apply to the XC3S500E.

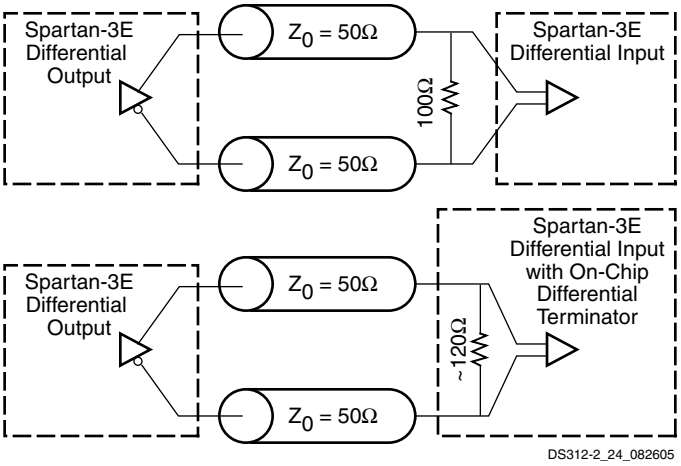

Figure 11: **Differential Inputs and Outputs**

Pull-Up and Pull-Down Resistors

Pull-up and pull-down resistors inside each IOB optionally force a floating I/O or Input-only pin to a determined state. Pull-up and pull-down resistors are commonly applied to unused I/Os, inputs, and three-state outputs, but can be used on any I/O or Input-only pin. The pull-up resistor connects an IOB to V_{CCO} through a resistor. The resistance value depends on the V_{CCO} voltage (see Module 3, DC and Switching Characteristics for the specifications). The pull-down resistor similarly connects an IOB to ground with a resistor. The PULLUP and PULLDOWN attributes and library primitives turn on these optional resistors.

By default, PULLDOWN resistors terminate all unused I/O and Input-only pins. Unused I/O and Input-only pins can alternatively be set to PULLUP or FLOAT. To change the unused I/O Pad setting, set the Bitstream Generator (BitGen) option ***UnusedPin*** to PULLUP, PULLDOWN, or FLOAT. The ***UnusedPin*** option is accessed through the Properties for Generate Programming File in ISE. See Bitstream Generator (BitGen) Options.

During configuration a Low logic level on the HSWAP pin activates pull-up resistors on all I/O and Input-only pins not actively used in the selected configuration mode.

Keeper Circuit

Each I/O has an optional keeper circuit (see Figure 12) that keeps bus lines from floating when not being actively driven. The KEEPER circuit retains the last logic level on a line after all drivers have been turned off. Apply the KEEPER attribute or use the KEEPER library primitive to use the KEEPER circuitry. Pull-up and pull-down resistors override the KEEPER settings.

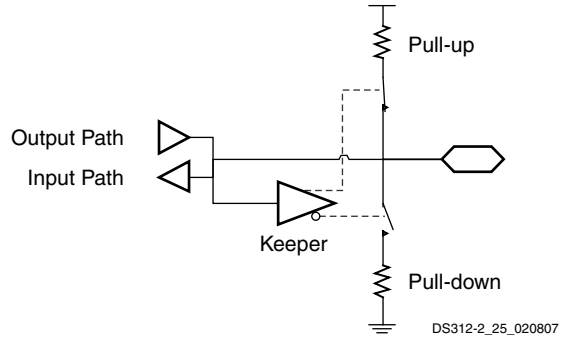

Figure 12: **Keeper Circuit**

Slew Rate Control and Drive Strength

Each IOB has a slew-rate control that sets the output switching edge-rate for LVCMOS and LVTTL outputs. The SLEW attribute controls the slew rate and can either be set to SLOW (default) or FAST.

Each LVCMOS and LVTTL output additionally supports up to six different drive current strengths as shown in Table 8. To adjust the drive strength for each output, the DRIVE attribute is set to the desired drive strength: 2, 4, 6, 8, 12, and 16. Unless otherwise specified in the FPGA application, the software default IOSTANDARD is LVCMOS25, SLOW slew rate, and 12 mA output drive.

Table 8: **Programmable Output Drive Current**

IOSTANDARD	Output Drive Current (mA)					
	2	4	6	8	12	16
LVTTL	✔	✔	✔	✔	✔	✔
LVCMOS33	✔	✔	✔	✔	✔	✔
LVCMOS25	✔	✔	✔	✔	✔	-
LVCMOS18	✔	✔	✔	✔	-	-
LVCMOS15	✔	✔	✔	-	-	-
LVCMOS12	✔	-	-	-	-	-

High output current drive strength and FAST output slew rates generally result in fastest I/O performance. However, these same settings generally also result in transmission line effects on the printed circuit board (PCB) for all but the shortest board traces. Each IOB has independent slew rate and drive strength controls. Use the slowest slew rate and lowest output drive current that meets the performance requirements for the end application.

Likewise, due to lead inductance, a given package supports a limited number of simultaneous switching outputs (SSOs) when using fast, high-drive outputs. Only use fast, high-drive outputs when required by the application.

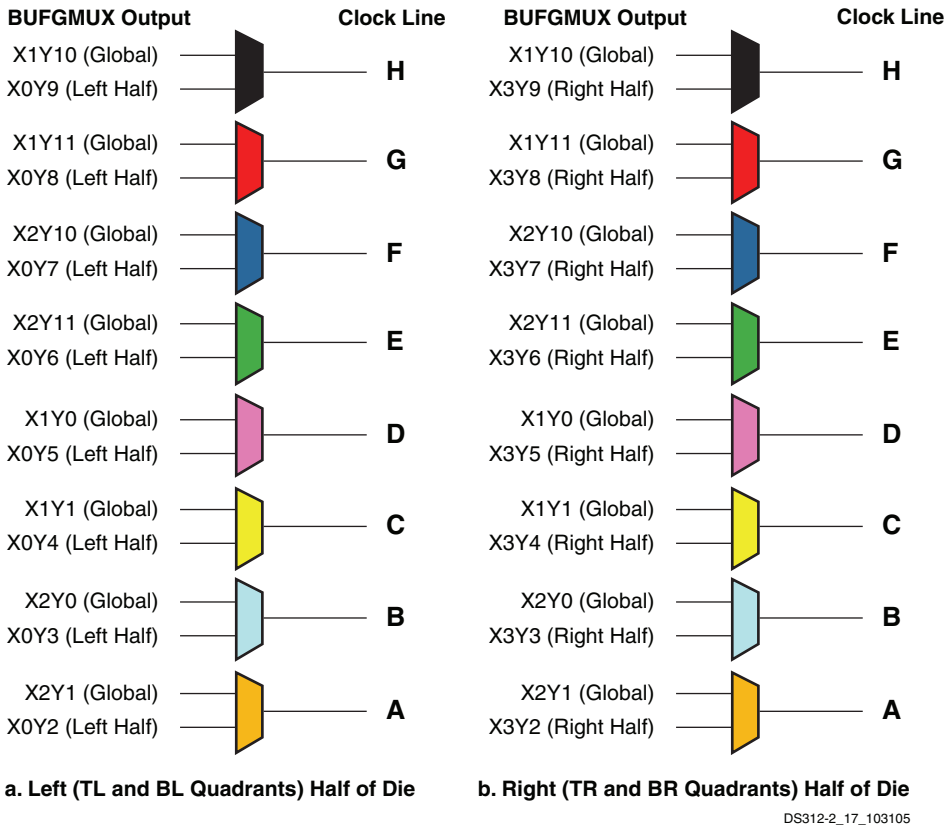

Figure 47: **Clock Sources for the Eight Clock Lines within a Clock Quadrant**

The outputs of the top or bottom BUFGMUX elements connect to two vertical spines, each comprising four vertical clock lines as shown in Figure 45. At the center of the die, these clock signals connect to the eight-line horizontal clock spine.

Outputs of the left and right BUFGMUX elements are routed onto the left or right horizontal spines, each comprising eight horizontal clock lines.

Each of the eight clock signals in a clock quadrant derives either from a global clock signal or a half clock signal. In other words, there are up to 24 total potential clock inputs to the FPGA, eight of which can connect to clocked elements in a single clock quadrant. Figure 47 shows how the clock lines in each quadrant are selected from associated BUFGMUX sources. For example, if quadrant clock ‘A’ in the bottom left (BL) quadrant originates from BUFGMUX_X2Y1, then the clock signal from BUFGMUX_X0Y2 is unavailable in the bottom left quadrant. However, the top left (TL) quadrant clock ‘A’ can still solely use the output from either BUFGMUX_X2Y1 or BUFGMUX_X0Y2 as the source.

To minimize the dynamic power dissipation of the clock network, the Xilinx development software automatically disables all clock segments not in use.

Compatible Flash Families

The Spartan-3E BPI configuration interface operates with a wide variety of x8 or x8/x16 parallel NOR Flash devices. Table 61 provides a few Flash memory families that operate with the Spartan-3E BPI interface. Consult the data sheet for the desired parallel NOR Flash to determine its suitability The basic timing requirements and waveforms are provided in Byte Peripheral Interface (BPI) Configuration Timing (Module 3).

Table 61: **Compatible Parallel NOR Flash Families**

Flash Vendor	Flash Memory Family
Numonyx	M29W, J3D StrataFlash
Atmel	AT29 / AT49
Spansion	S29
Macronix	MX29

CCLK Frequency

In BPI mode, the FPGA's internal oscillator generates the configuration clock frequency that controls all the interface timing. The FPGA starts configuration at its lowest frequency and increases its frequency for the remainder of the configuration process if so specified in the configuration bitstream. The maximum frequency is specified using the ***ConfigRate*** bitstream generator option.

Table 62: **Maximum ConfigRate Settings for Parallel Flash PROMs (Commercial Temperature Range)**

Flash Read Access Time	Maximum *ConfigRate* Setting
250 ns	3
115 ns	6
45 ns	12

Table 62 shows the maximum ***ConfigRate*** settings for various typical PROM read access times over the Commercial temperature operating range. See Byte Peripheral Interface (BPI) Configuration Timing (Module 3) and UG332 for more detailed information. Despite using slower ***ConfigRate*** settings, BPI mode is equally fast as the other configuration modes. In BPI mode, data is accessed at the ***ConfigRate*** frequency and internally serialized with an 8X clock frequency.

Using the BPI Interface after Configuration

After the FPGA successfully completes configuration, all pins connected to the parallel Flash PROM are available as user I/Os.

If not using the parallel Flash PROM after configuration, drive LDC0 High to disable the PROM's chip-select input. The remainder of the BPI pins then become available to the FPGA application, including all 24 address lines, the eight data lines, and the LDC2, LDC1, and HDC control pins.

Because all the interface pins are user I/Os after configuration, the FPGA application can continue to use the interface pins to communicate with the parallel Flash PROM. Parallel Flash PROMs are available in densities ranging from 1 Mbit up to 128 Mbits and beyond. However, a single Spartan-3E FPGA requires less than 6 Mbits for configuration. If desired, use a larger parallel Flash PROM to contain additional non-volatile application data, such as MicroBlaze processor code, or other user data, such as serial numbers and Ethernet MAC IDs. In such an example, the FPGA configures from parallel Flash PROM. Then using FPGA logic after configuration, a MicroBlaze processor embedded within the FPGA can either execute code directly from parallel Flash PROM or copy the code to external DDR SDRAM and execute from DDR SDRAM. Similarly, the FPGA application can store non-volatile application data within the parallel Flash PROM.

The FPGA configuration data is stored starting at either at location 0 or the top of memory (addresses all ones) or at both locations for MultiBoot mode. Store any additional data beginning in other available parallel Flash PROM sectors. Do not mix configuration data and user data in the same sector.

Similarly, the parallel Flash PROM interface can be expanded to additional parallel peripherals.

The address, data, and LDC1 (OE#) and HDC (WE#) control signals are common to all parallel peripherals. Connect the chip-select input on each additional peripheral to one of the FPGA user I/O pins. If HSWAP = 0 during configuration, the FPGA holds the chip-select line High via an internal pull-up resistor. If HSWAP = 1, connect the select line to +3.3V via an external 4.7 kΩ pull-up resistor to avoid spurious read or write operations. After configuration, drive the select line Low to select the desired peripheral. Refer to the individual peripheral data sheet for specific interface and communication protocol requirements.

The FPGA optionally supports a 16-bit peripheral interface by driving the LDC2 (BYTE#) control pin High after configuration. See Precautions Using x8/x16 Flash PROMs for additional information.

The FPGA provides up to 24 address lines during configuration, addressing up to 128 Mbits (16 Mbytes). If using a larger parallel PROM, connect the upper address lines to FPGA user I/O. During configuration, the upper address lines will be pulled High if HSWAP = 0. Otherwise, use external pull-up or pull-down resistors on these address lines to define their values during configuration.

Precautions Using x8/x16 Flash PROMs

(D) Most low- to mid-density PROMs are byte-wide (x8) only. Many higher-density Flash PROMs support both byte-wide (x8) and halfword-wide (x16) data paths and include a mode input called BYTE# that switches between x8 or x16. During configuration, Spartan-3E FPGAs only

Stepping 0 Limitations when Reprogramming via JTAG if FPGA Set for BPI Configuration

The FPGA can always be reprogrammed via the JTAG port, regardless of the mode pin (M[2:0]) settings. However, Stepping 0 devices have a minor limitation. If a Stepping 0 FPGA is set to configure in BPI mode and the FPGA is attached to a parallel memory containing a valid FPGA configuration file, then subsequent reconfigurations using the JTAG port will fail. Potential workarounds include setting the mode pins for JTAG configuration (M[2:0] = <1:0:1>) or offsetting the initial memory location in Flash by 0x2000.

Stepping 1 devices fully support JTAG configuration even when the FPGA mode pins are set for BPI mode.

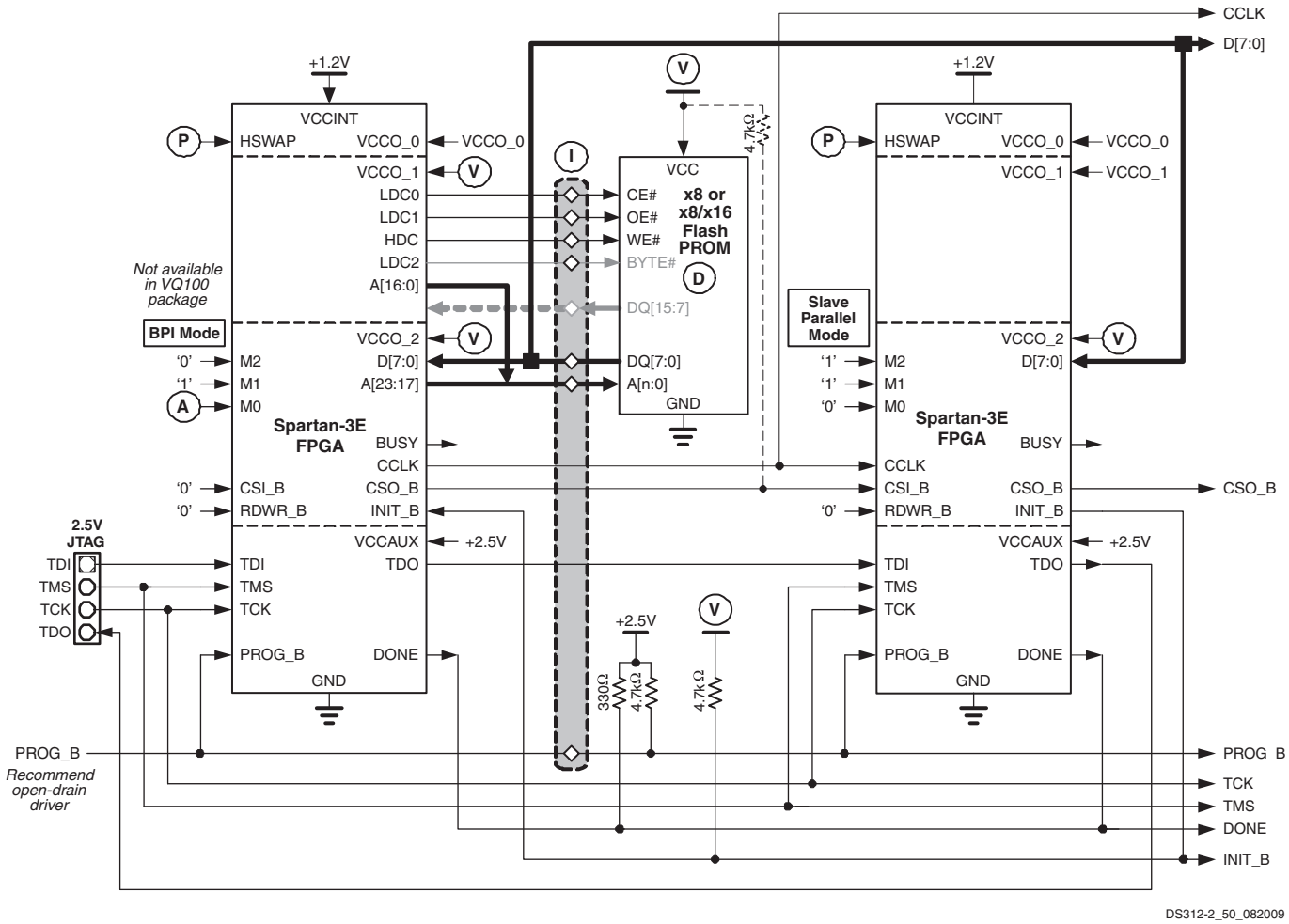

Figure 59: **Daisy-Chaining from BPI Flash Mode**

In-System Programming Support

(I) In a production application, the parallel Flash PROM is usually preprogrammed before it is mounted on the printed circuit board. In-system programming support is available from third-party boundary-scan tool vendors and from some third-party PROM programmers using a socket adapter with attached wires. To gain access to the parallel Flash signals, drive the FPGA's PROG_B input Low with an open-drain driver. This action places all FPGA I/O pins, including those attached to the parallel Flash, in high-impedance (Hi-Z). If the HSWAP input is Low, the I/Os have pull-up resistors to the V_{CCO} input on their respective I/O bank. The external programming hardware then has direct access to the parallel Flash pins. The programming access points are highlighted in the gray boxes in Figure 58 and Figure 59.

The FPGA itself can also be used as a parallel Flash PROM programmer during development and test phases. Initially, an FPGA-based programmer is downloaded into the FPGA via JTAG. Then the FPGA performs the Flash PROM programming algorithms and receives programming data from the host via the FPGA's JTAG interface. See the Embedded System Tools Reference Manual.

Dynamically Loading Multiple Configuration Images Using MultiBoot Option

For additional information, refer to the "Reconfiguration and MultiBoot" chapter in UG332.

Table 69: **Spartan-3E FPGA Bitstream Generator (BitGen) Options *(Cont'd)***

Option Name	Pins/Function Affected	Values (***default***)	Description
DriveDone	DONE pin	***No***	When configuration completes, the DONE pin stops driving Low and relies on an external 330 Ω pull-up resistor to V_{CCAUX} for a valid logic High.
		Yes	When configuration completes, the DONE pin actively drives High. When using this option, an external pull-up resistor is no longer required. Only one device in an FPGA daisy-chain should use this setting.
DonePipe	DONE pin	***No***	The input path from DONE pin input back to the Startup sequencer is not pipelined.
		Yes	This option adds a pipeline register stage between the DONE pin input and the Startup sequencer. Used for high-speed daisy-chain configurations when DONE cannot rise in a single CCLK cycle. Releases GWE and GTS signals on the first rising edge of StartupClk after the DONE pin input goes High.
ProgPin	PROG_B pin	***Pullup***	Internally connects a pull-up resistor or between PROG_B pin and V_{CCAUX}. An external 4.7 kΩ pull-up resistor to V_{CCAUX} is still recommended since the internal pull-up value may be weaker (see Table 78).
		Pullnone	No internal pull-up resistor on PROG_B pin. An external 4.7 kΩ pull-up resistor to V_{CCAUX} is required.
TckPin	JTAG TCK pin	***Pullup***	Internally connects a pull-up resistor between JTAG TCK pin and V_{CCAUX}.
		Pulldown	Internally connects a pull-down resistor between JTAG TCK pin and GND.
		Pullnone	No internal pull-up resistor on JTAG TCK pin.
TdiPin	JTAG TDI pin	***Pullup***	Internally connects a pull-up resistor between JTAG TDI pin and V_{CCAUX}.
		Pulldown	Internally connects a pull-down resistor between JTAG TDI pin and GND.
		Pullnone	No internal pull-up resistor on JTAG TDI pin.
TdoPin	JTAG TDO pin	***Pullup***	Internally connects a pull-up resistor between JTAG TDO pin and V_{CCAUX}.
		Pulldown	Internally connects a pull-down resistor between JTAG TDO pin and GND.
		Pullnone	No internal pull-up resistor on JTAG TDO pin.
TmsPin	JTAG TMS pin	***Pullup***	Internally connects a pull-up resistor between JTAG TMS pin and V_{CCAUX}.
		Pulldown	Internally connects a pull-down resistor between JTAG TMS pin and GND.
		Pullnone	No internal pull-up resistor on JTAG TMS pin.
UserID	JTAG User ID register	User string	The 32-bit JTAG User ID register value is loaded during configuration. The default value is all ones, `0xFFFF_FFFF` hexadecimal. To specify another value, enter an 8-character hexadecimal value.
Security	JTAG, SelectMAP, Readback, Partial reconfiguration	***None***	Readback and limited partial reconfiguration are available via the JTAG port or via the SelectMAP interface, if the ***Persist*** option is set to ***Yes***.
		Level1	Readback function is disabled. Limited partial reconfiguration is still available via the JTAG port or via the SelectMAP interface, if the ***Persist*** option is set to ***Yes***.
		Level2	Readback function is disabled. Limited partial reconfiguration is disabled.
CRC	Configuration	**Enable**	***Default.*** Enable CRC checking on the FPGA bitstream. If error detected, FPGA asserts INIT_B Low and DONE pin stays Low.
		Disable	Turn off CRC checking.
Persist	SelectMAP interface pins, BPI mode, Slave mode, Configuration	***No***	All BPI and Slave mode configuration pins are available as user-I/O after configuration.
		Yes	This option is required for Readback and partial reconfiguration using the SelectMAP interface. The SelectMAP interface pins (see Slave Parallel Mode) are reserved after configuration and are not available as user-I/O.

DC Electrical Characteristics

In this section, specifications may be designated as Advance, Preliminary, or Production. These terms are defined as follows:

Advance: Initial estimates are based on simulation, early characterization, and/or extrapolation from the characteristics of other families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on characterization. Further changes are not expected.

Production: These specifications are approved once the silicon has been characterized over numerous production lots. Parameter values are considered stable with no future changes expected.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all Spartan®-3E devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.**

Absolute Maximum Ratings

Stresses beyond those listed under Table 73, Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to absolute maximum conditions for extended periods of time adversely affects device reliability.

Table 73: **Absolute Maximum Ratings**

Symbol	Description	Conditions		Min	Max	Units
V_{CCINT}	Internal supply voltage			–0.5	1.32	V
V_{CCAUX}	Auxiliary supply voltage			–0.5	3.00	V
V_{CCO}	Output driver supply voltage			–0.5	3.75	V
V_{REF}	Input reference voltage			–0.5	V_{CCO} + 0.5 (1)	V
V_{IN} (1,2,3,4)	Voltage applied to all User I/O pins and Dual-Purpose pins	Driver in a high-impedance state	Commercial	–0.95	4.4	V
			Industrial	–0.85	4.3	V
	Voltage applied to all Dedicated pins		All temp. ranges	–0.5	V_{CCAUX} + 0.5 (3)	V
I_{IK}	Input clamp current per I/O pin	–0.5 V < V_{IN} < (V_{CCO} + 0.5 V)		–	±100	mA
V_{ESD}	Electrostatic Discharge Voltage	Human body model		–	±2000	V
		Charged device model		–	±500	V
		Machine model		–	±200	V
T_J	Junction temperature			–	125	°C
T_{STG}	Storage temperature			–65	150	°C

Notes:

1. Each of the User I/O and Dual-Purpose pins is associated with one of the four banks' V_{CCO} rails. Keeping V_{IN} within 500 mV of the associated V_{CCO} rails or ground rail ensures that the internal diode junctions do not turn on. Table 77 specifies the V_{CCO} range used to evaluate the maximum V_{IN} voltage.
2. Input voltages outside the -0.5V to V_{CCO} + 0.5V (or V_{CCAUX} + 0.5V) voltage range are require the I_{IK} input diode clamp diode rating is met and no more than 100 pins exceed the range simultaneously. Prolonged exposure to such current may compromise device reliability. A sustained current of 10 mA will not compromise device reliability. See XAPP459: *Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins on Spartan-3 Families* for more details.
3. All Dedicated pins (PROG_B, DONE, TCK, TDI, TDO, and TMS) draw power from the V_{CCAUX} rail (2.5V). Meeting the V_{IN} max limit ensures that the internal diode junctions that exist between each of these pins and the V_{CCAUX} rail do not turn on. Table 77 specifies the V_{CCAUX} range used to evaluate the maximum V_{IN} voltage. As long as the V_{IN} max specification is met, oxide stress is not possible.
4. See XAPP459: *Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins on Spartan-3 Families*.
5. For soldering guidelines, see UG112: *Device Packaging and Thermal Characteristics* and XAPP427: *Implementation and Solder Reflow Guidelines for Pb-Free Packages*.

Power Supply Specifications

Table 74: **Supply Voltage Thresholds for Power-On Reset**

Symbol	Description	Min	Max	Units
V_{CCINTT}	Threshold for the V_{CCINT} supply	0.4	1.0	V
V_{CCAUXT}	Threshold for the V_{CCAUX} supply	0.8	2.0	V
V_{CCO2T}	Threshold for the V_{CCO} Bank 2 supply	0.4	1.0	V

Notes:

1. V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies to the FPGA can be applied in any order. However, the FPGA's configuration source (Platform Flash, SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source. In Step 0 devices using the HSWAP internal pull-up, V_{CCINT} must be applied before V_{CCAUX}.
2. To ensure successful power-on, V_{CCINT}, V_{CCO} Bank 2, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 75: **Supply Voltage Ramp Rate**

Symbol	Description	Min	Max	Units
V_{CCINTR}	Ramp rate from GND to valid V_{CCINT} supply level	0.2	50	ms
V_{CCAUXR}	Ramp rate from GND to valid V_{CCAUX} supply level	0.2	50	ms
V_{CCO2R}	Ramp rate from GND to valid V_{CCO} Bank 2 supply level	0.2	50	ms

Notes:

1. V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies to the FPGA can be applied in any order. However, the FPGA's configuration source (Platform Flash, SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source. In Step 0 devices using the HSWAP internal pull-up, V_{CCINT} must be applied before V_{CCAUX}.
2. To ensure successful power-on, V_{CCINT}, V_{CCO} Bank 2, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 76: **Supply Voltage Levels Necessary for Preserving RAM Contents**

Symbol	Description	Min	Units
V_{DRINT}	V_{CCINT} level required to retain RAM data	1.0	V
V_{DRAUX}	V_{CCAUX} level required to retain RAM data	2.0	V

Notes:

1. RAM contents include configuration data.

Switching Characteristics

All Spartan-3E FPGAs ship in two speed grades: -4 and the higher performance -5. Switching characteristics in this document may be designated as Advance, Preliminary, or Production, as shown in Table 84. Each category is defined as follows:

Advance: These specifications are based on simulations only and are typically available soon after establishing FPGA specifications. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These specifications are based on complete early silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting preliminary delays is greatly reduced compared to Advance data.

Production: These specifications are approved once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Software Version Requirements

Production-quality systems must use FPGA designs compiled using a speed file designated as PRODUCTION status. FPGAs designs using a less mature speed file designation should only be used during system prototyping or pre-production qualification. FPGA designs with speed files designated as Advance or Preliminary should not be used in a production-quality system.

Whenever a speed file designation changes, as a device matures toward Production status, rerun the latest Xilinx ISE software on the FPGA design to ensure that the FPGA design incorporates the latest timing information and software updates.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all Spartan-3E devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.**

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Timing parameters and their representative values are selected for inclusion below either because they are important as general design requirements or they indicate fundamental device performance characteristics. The Spartan-3E speed files (v1.27), part of the Xilinx Development Software, are the original source for many but not all of the values. The speed grade designations for these files are shown in Table 84. For more complete, more precise, and worst-case data, use the values reported by the Xilinx static timing analyzer (TRACE in the Xilinx development software) and back-annotated to the simulation netlist.

Table 84: **Spartan-3E v1.27 Speed Grade Designations**

Device	Advance	Preliminary	Production
XC3S100E			-MIN, -4, -5
XC3S250E			-MIN, -4, -5
XC3S500E			-MIN, -4, -5
XC3S1200E			-MIN, -4, -5
XC3S1600E			-MIN, -4, -5

Table 85 provides the history of the Spartan-3E speed files since all devices reached Production status.

Table 85: **Spartan-3E Speed File Version History**

Version	ISE Release	Description
1.27	9.2.03i	Added XA Automotive.
1.26	8.2.02i	Added -0/-MIN speed grade, which includes minimum values.
1.25	8.2.01i	Added XA Automotive devices to speed file. Improved model for left and right DCMs.
1.23	8.2i	Updated input setup/hold values based on default IFD_DELAY_VALUE settings.
1.21	8.1.03i	All Spartan-3E FPGAs and all speed grades elevated to Production status.

Table 92: **Timing for the IOB Output Path**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Min	Min	
Clock-to-Output Times						
T_{IOCKP}	When reading from the Output Flip-Flop (OFF), the time from the active transition at the OCLK input to data appearing at the Output pin	LVCMOS25(2), 12 mA output drive, Fast slew rate	All	2.18	2.50	ns
Propagation Times						
T_{IOOP}	The time it takes for data to travel from the IOB's O input to the Output pin	LVCMOS25(2), 12 mA output drive, Fast slew rate	All	2.24	2.58	ns
T_{IOOLP}	The time it takes for data to travel from the O input through the OFF latch to the Output pin			2.32	2.67	ns
Set/Reset Times						
T_{IOSRP}	Time from asserting the OFF's SR input to setting/resetting data at the Output pin	LVCMOS25(2), 12 mA output drive, Fast slew rate	All	3.27	3.76	ns
T_{IOGSRQ}	Time from asserting the Global Set Reset (GSR) input on the STARTUP_SPARTAN3E primitive to setting/resetting data at the Output pin			8.40	9.65	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 95 and are based on the operating conditions set forth in Table 77 and Table 80.
2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from Table 94.
3. For minimum delays use the values reported by the Timing Analyzer.

Table 99: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	-5		-4		Units
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{SHCKO}	Time from the active edge at the CLK input to data appearing on the distributed RAM output	-	2.05	-	2.35	ns
Setup Times						
T_{DS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the distributed RAM	0.40	-	0.46	-	ns
T_{AS}	Setup time of the F/G address inputs before the active transition at the CLK input of the distributed RAM	0.46	-	0.52	-	ns
T_{WS}	Setup time of the write enable input before the active transition at the CLK input of the distributed RAM	0.34	-	0.40	-	ns
Hold Times						
T_{DH}	Hold time of the BX, BY data inputs after the active transition at the CLK input of the distributed RAM	0.13	-	0.15	-	ns
T_{AH}, T_{WH}	Hold time of the F/G address inputs or the write enable input after the active transition at the CLK input of the distributed RAM	0	-	0	-	ns
Clock Pulse Width						
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	0.88	-	1.01	-	ns

Table 100: **CLB Shift Register Switching Characteristics**

Symbol	Description	-5		-4		Units
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{REG}	Time from the active edge at the CLK input to data appearing on the shift register output	-	3.62	-	4.16	ns
Setup Times						
T_{SRLDS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the shift register	0.41	-	0.46	-	ns
Hold Times						
T_{SRLDH}	Hold time of the BX or BY data input after the active transition at the CLK input of the shift register	0.14	-	0.16	-	ns
Clock Pulse Width						
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	0.88	-	1.01	-	ns

Clock Buffer/Multiplexer Switching Characteristics

Table 101: **Clock Distribution Switching Characteristics**

Description	Symbol	Maximum		Units
		Speed Grade		
		-5	-4	
Global clock buffer (BUFG, BUFGMUX, BUFGCE) I input to O-output delay	T_{GIO}	1.46	1.46	ns
Global clock multiplexer (BUFGMUX) select S-input setup to I0 and I1 inputs. Same as BUFGCE enable CE-input	T_{GSI}	0.55	0.63	ns
Frequency of signals distributed on global buffers (all sides)	F_{BUFG}	333	311	MHz

Configuration Clock (CCLK) Characteristics

Table 112: **Master Mode CCLK Output Period by *ConfigRate* Option Setting**

Symbol	Description	*ConfigRate* Setting	Temperature Range	Minimum	Maximum	Units
T_{CCLK1}	CCLK clock period by ***ConfigRate*** setting	1 *(power-on value and default value)*	Commercial	570	1,250	ns
			Industrial	485		ns
T_{CCLK3}		3	Commercial	285	625	ns
			Industrial	242		ns
T_{CCLK6}		6	Commercial	142	313	ns
			Industrial	121		ns
T_{CCLK12}		12	Commercial	71.2	157	ns
			Industrial	60.6		ns
T_{CCLK25}		25	Commercial	35.5	78.2	ns
			Industrial	30.3		ns
T_{CCLK50}		50	Commercial	17.8	39.1	ns
			Industrial	15.1		ns

Notes:

1. Set the ***ConfigRate*** option value when generating a configuration bitstream. See Bitstream Generator (BitGen) Options in Module 2.

Table 113: **Master Mode CCLK Output Frequency by *ConfigRate* Option Setting**

Symbol	Description	*ConfigRate* Setting	Temperature Range	Minimum	Maximum	Units
F_{CCLK1}	Equivalent CCLK clock frequency by ***ConfigRate*** setting	1 *(power-on value and default value)*	Commercial	0.8	1.8	MHz
			Industrial		2.1	MHz
F_{CCLK3}		3	Commercial	1.6	3.6	MHz
			Industrial		4.2	MHz
F_{CCLK6}		6	Commercial	3.2	7.1	MHz
			Industrial		8.3	MHz
F_{CCLK12}		12	Commercial	6.4	14.1	MHz
			Industrial		16.5	MHz
F_{CCLK25}		25	Commercial	12.8	28.1	MHz
			Industrial		33.0	MHz
F_{CCLK50}		50	Commercial	25.6	56.2	MHz
			Industrial		66.0	MHz

Table 114: **Master Mode CCLK Output Minimum Low and High Time**

Symbol	Description		*ConfigRate* Setting						Units
			1	3	6	12	25	50	
T_{MCCL}, T_{MCCH}	Master mode CCLK minimum Low and High time	Commercial	276	138	69	34.5	17.1	8.5	ns
		Industrial	235	117	58	29.3	14.5	7.3	ns

Table 115: **Slave Mode CCLK Input Low and High Time**

Symbol	Description	Min	Max	Units
T_{SCCL}, T_{SCCH}	CCLK Low and High time	5	∞	ns

CP132: 132-ball Chip-scale Package

The XC3S100E, XC3S250E and the XC3S500E FPGAs are available in the 132-ball chip-scale package, CP132. The devices share a common footprint for this package as shown in Table 133 and Figure 81.

Table 133 lists all the CP132 package pins. They are sorted by bank number and then by pin name. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

Physically, the D14 and K2 balls on the XC3S100E and XC3S250E FPGAs are not connected but should be connected to VCCINT to maintain density migration compatibility.

Similarly, the A4, C1, and P10 balls on the XC3S100E FPGA are not connected but should be connected to GND to maintain density migration compatibility.

The XC3S100E FPGA has four fewer BPI address pins, A[19:0], whereas the XC3S250E and XC3S500E support A[23:0].

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx web site at:

http://www.xilinx.com/support/documentation/data_sheets/s3e_pin.zip

Pinout Table

Table 133: **CP132 Package Pinout**

Bank	XC3S100E Pin Name	XC3S250E XC3S500E Pin Name	CP132 Ball	Type
0	IO_L01N_0	IO_L01N_0	C12	I/O
0	IO_L01P_0	IO_L01P_0	A13	I/O
0	N.C. (◆)	IO_L02N_0	A12	***100E:*** N.C. ***Others:*** I/O
0	N.C. (◆)	IO_L02P_0	B12	***100E:*** N.C. ***Others:*** I/O
0	N.C. (◆)	IO_L03N_0/VREF_0	B11	***100E:*** N.C. ***Others:*** VREF (I/O)
0	IP	IO_L03P_0	C11	***100E:*** INPUT ***Others:*** I/O
0	IO_L04N_0/GCLK5	IO_L04N_0/GCLK5	C9	GCLK
0	IO_L04P_0/GCLK4	IO_L04P_0/GCLK4	A10	GCLK
0	IO_L05N_0/GCLK7	IO_L05N_0/GCLK7	A9	GCLK
0	IO_L05P_0/GCLK6	IO_L05P_0/GCLK6	B9	GCLK
0	IO_L07N_0/GCLK11	IO_L07N_0/GCLK11	B7	GCLK
0	IO_L07P_0/GCLK10	IO_L07P_0/GCLK10	A7	GCLK
0	IO_L08N_0/VREF_0	IO_L08N_0/VREF_0	C6	VREF
0	IO_L08P_0	IO_L08P_0	B6	I/O
0	IO_L09N_0	IO_L09N_0	C5	I/O
0	IO_L09P_0	IO_L09P_0	B5	I/O
0	N.C. (◆)	IO_L10N_0	C4	***100E:*** N.C. ***Others:*** I/O
0	IP	IO_L10P_0	B4	***100E:*** INPUT ***Others:*** I/O
0	IO_L11N_0/HSWAP	IO_L11N_0/HSWAP	B3	DUAL
0	IO_L11P_0	IO_L11P_0	A3	I/O
0	IP_L06N_0/GCLK9	IP_L06N_0/GCLK9	C8	GCLK
0	IP_L06P_0/GCLK8	IP_L06P_0/GCLK8	B8	GCLK
0	VCCO_0	VCCO_0	A6	VCCO

Table 137: **TQ144 Package Pinout *(Cont'd)***

Bank	XC3S100E Pin Name	XC3S250E Pin Name	TQ144 Pin	Type
2	IP	IP	P38	INPUT
2	IP	IP	P41	INPUT
2	IP	IP	P69	INPUT
2	IP_L03N_2/VREF_2	IP_L03N_2/VREF_2	P48	VREF
2	IP_L03P_2	IP_L03P_2	P47	INPUT
2	IP_L06N_2/M2/GCLK1	IP_L06N_2/M2/GCLK1	P57	DUAL/GCLK
2	IP_L06P_2/RDWR_B/GCLK0	IP_L06P_2/RDWR_B/GCLK0	P56	DUAL/GCLK
2	VCCO_2	VCCO_2	P42	VCCO
2	VCCO_2	VCCO_2	P49	VCCO
2	VCCO_2	VCCO_2	P64	VCCO
3	IP/VREF_3	IO/VREF_3	P31	***100E:*** VREF(INPUT) ***250E:*** VREF(I/O)
3	IO_L01N_3	IO_L01N_3	P3	I/O
3	IO_L01P_3	IO_L01P_3	P2	I/O
3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	P5	VREF
3	IO_L02P_3	IO_L02P_3	P4	I/O
3	IO_L03N_3	IO_L03N_3	P8	I/O
3	IO_L03P_3	IO_L03P_3	P7	I/O
3	IO_L04N_3/LHCLK1	IO_L04N_3/LHCLK1	P15	LHCLK
3	IO_L04P_3/LHCLK0	IO_L04P_3/LHCLK0	P14	LHCLK
3	IO_L05N_3/LHCLK3/IRDY2	IO_L05N_3/LHCLK3	P17	LHCLK
3	IO_L05P_3/LHCLK2	IO_L05P_3/LHCLK2	P16	LHCLK
3	IO_L06N_3/LHCLK5	IO_L06N_3/LHCLK5	P21	LHCLK
3	IO_L06P_3/LHCLK4/TRDY2	IO_L06P_3/LHCLK4	P20	LHCLK
3	IO_L07N_3/LHCLK7	IO_L07N_3/LHCLK7	P23	LHCLK
3	IO_L07P_3/LHCLK6	IO_L07P_3/LHCLK6	P22	LHCLK
3	IO_L08N_3	IO_L08N_3	P26	I/O
3	IO_L08P_3	IO_L08P_3	P25	I/O
3	IO_L09N_3	IO_L09N_3	P33	I/O
3	IO_L09P_3	IO_L09P_3	P32	I/O
3	IO_L10N_3	IO_L10N_3	P35	I/O
3	IO_L10P_3	IO_L10P_3	P34	I/O
3	IP	IP	P6	INPUT
3	IO	IP	P10	***100E:*** I/O ***250E:*** INPUT
3	IP	IP	P18	INPUT
3	IP	IP	P24	INPUT
3	IO	IP	P29	***100E:*** I/O ***250E:*** INPUT
3	IP	IP	P36	INPUT
3	IP/VREF_3	IP/VREF_3	P12	VREF
3	VCCO_3	VCCO_3	P13	VCCO
3	VCCO_3	VCCO_3	P28	VCCO
GND	GND	GND	P11	GND
GND	GND	GND	P19	GND

Table 141: **PQ208 Package Pinout *(Cont'd)***

Bank	XC3S250E XC3S500E Pin Name	PQ208 Pin	Type
3	IO_L14P_3	P41	I/O
3	IO_L15N_3	P48	I/O
3	IO_L15P_3	P47	I/O
3	IO_L16N_3	P50	I/O
3	IO_L16P_3	P49	I/O
3	IP	P6	INPUT
3	IP	P14	INPUT
3	IP	P26	INPUT
3	IP	P32	INPUT
3	IP	P43	INPUT
3	IP	P51	INPUT
3	IP/VREF_3	P20	VREF
3	VCCO_3	P21	VCCO
3	VCCO_3	P38	VCCO
3	VCCO_3	P46	VCCO
GND	GND	P10	GND
GND	GND	P17	GND
GND	GND	P27	GND
GND	GND	P37	GND
GND	GND	P52	GND
GND	GND	P53	GND
GND	GND	P70	GND
GND	GND	P79	GND
GND	GND	P85	GND
GND	GND	P95	GND
GND	GND	P105	GND
GND	GND	P121	GND
GND	GND	P131	GND
GND	GND	P141	GND
GND	GND	P156	GND
GND	GND	P173	GND
GND	GND	P182	GND
GND	GND	P188	GND
GND	GND	P198	GND
GND	GND	P208	GND
VCCAUX	DONE	P104	CONFIG
VCCAUX	PROG_B	P1	CONFIG
VCCAUX	TCK	P158	JTAG
VCCAUX	TDI	P207	JTAG
VCCAUX	TDO	P157	JTAG
VCCAUX	TMS	P155	JTAG
VCCAUX	VCCAUX	P7	VCCAUX
VCCAUX	VCCAUX	P44	VCCAUX

Table 141: **PQ208 Package Pinout *(Cont'd)***

Bank	XC3S250E XC3S500E Pin Name	PQ208 Pin	Type
VCCAUX	VCCAUX	P66	VCCAUX
VCCAUX	VCCAUX	P92	VCCAUX
VCCAUX	VCCAUX	P111	VCCAUX
VCCAUX	VCCAUX	P149	VCCAUX
VCCAUX	VCCAUX	P166	VCCAUX
VCCAUX	VCCAUX	P195	VCCAUX
VCCINT	VCCINT	P13	VCCINT
VCCINT	VCCINT	P67	VCCINT
VCCINT	VCCINT	P117	VCCINT
VCCINT	VCCINT	P170	VCCINT

Table 148: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S500E Pin Name	XC3S1200E Pin Name	XC3S1600E Pin Name	FG320 Ball	Type
1	IO_L17N_1	IO_L17N_1	IO_L17N_1	H15	I/O
1	IO_L17P_1	IO_L17P_1	IO_L17P_1	H14	I/O
1	IO_L18N_1	IO_L18N_1	IO_L18N_1	G16	I/O
1	IO_L18P_1	IO_L18P_1	IO_L18P_1	G15	I/O
1	IO_L19N_1	IO_L19N_1	IO_L19N_1	F17	I/O
1	IO_L19P_1	IO_L19P_1	IO_L19P_1	F18	I/O
1	IO_L20N_1	IO_L20N_1	IO_L20N_1	G13	I/O
1	IO_L20P_1	IO_L20P_1	IO_L20P_1	G14	I/O
1	IO_L21N_1	IO_L21N_1	IO_L21N_1	F14	I/O
1	IO_L21P_1	IO_L21P_1	IO_L21P_1	F15	I/O
1	N.C. (◆)	IO_L22N_1	IO_L22N_1	E16	**500E:** N.C. **1200E:** I/O **1600E:** I/O
1	N.C. (◆)	IO_L22P_1	IO_L22P_1	E15	**500E:** N.C. **1200E:** I/O **1600E:** I/O
1	IO_L23N_1/LDC0	IO_L23N_1/LDC0	IO_L23N_1/LDC0	D16	DUAL
1	IO_L23P_1/HDC	IO_L23P_1/HDC	IO_L23P_1/HDC	D17	DUAL
1	IO_L24N_1/LDC2	IO_L24N_1/LDC2	IO_L24N_1/LDC2	C17	DUAL
1	IO_L24P_1/LDC1	IO_L24P_1/LDC1	IO_L24P_1/LDC1	C18	DUAL
1	IP	IP	IP	B18	INPUT
1	IO	IP	IP	E17	**500E:** I/O **1200E:** INPUT **1600E:** INPUT
1	IP	IP	IP	E18	INPUT
1	IP	IP	IP	G18	INPUT
1	IP	IP	IP	H13	INPUT
1	IP	IP	IP	K17	INPUT
1	IP	IP	IP	K18	INPUT
1	IP	IP	IP	L13	INPUT
1	IP	IP	IP	L14	INPUT
1	IP	IP	IP	N17	INPUT
1	IO	IP	IP	P15	**500E:** I/O **1200E:** INPUT **1600E:** INPUT
1	IP	IP	IP	R17	INPUT
1	IP/VREF_1	IP/VREF_1	IP/VREF_1	D18	VREF
1	IP/VREF_1	IP/VREF_1	IP/VREF_1	H18	VREF
1	VCCO_1	VCCO_1	VCCO_1	F16	VCCO
1	VCCO_1	VCCO_1	VCCO_1	H12	VCCO
1	VCCO_1	VCCO_1	VCCO_1	J18	VCCO
1	VCCO_1	VCCO_1	VCCO_1	L12	VCCO
1	VCCO_1	VCCO_1	VCCO_1	N16	VCCO
2	IO	IO	IO	P9	I/O
2	IO	IO	IO	R11	I/O

Table 148: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S500E Pin Name	XC3S1200E Pin Name	XC3S1600E Pin Name	FG320 Ball	Type
2	IP	IO	IO	U6	**500E:** INPUT **1200E:** I/O **1600E:** I/O
2	IP	IO	IO	U13	**500E:** INPUT **1200E:** I/O **1600E:** I/O
2	N.C. (◆)	IO	IO	V7	**500E:** N.C. **1200E:** I/O **1600E:** I/O
2	IO/D5	IO/D5	IO/D5	R9	DUAL
2	IO/M1	IO/M1	IO/M1	V11	DUAL
2	IO/VREF_2	IO/VREF_2	IO/VREF_2	T15	VREF
2	IO/VREF_2	IO/VREF_2	IO/VREF_2	U5	VREF
2	IO_L01N_2/INIT_B	IO_L01N_2/INIT_B	IO_L01N_2/INIT_B	T3	DUAL
2	IO_L01P_2/CSO_B	IO_L01P_2/CSO_B	IO_L01P_2/CSO_B	U3	DUAL
2	IO_L03N_2/MOSI/CSI_B	IO_L03N_2/MOSI/CSI_B	IO_L03N_2/MOSI/CSI_B	T4	DUAL
2	IO_L03P_2/DOUT/BUSY	IO_L03P_2/DOUT/BUSY	IO_L03P_2/DOUT/BUSY	U4	DUAL
2	IO_L04N_2	IO_L04N_2	IO_L04N_2	T5	I/O
2	IO_L04P_2	IO_L04P_2	IO_L04P_2	R5	I/O
2	IO_L05N_2	IO_L05N_2	IO_L05N_2	P6	I/O
2	IO_L05P_2	IO_L05P_2	IO_L05P_2	R6	I/O
2	N.C. (◆)	IO_L06N_2/VREF_2	IO_L06N_2/VREF_2	V6	**500E:** N.C. **1200E:** VREF **1600E:** VREF
2	N.C. (◆)	IO_L06P_2	IO_L06P_2	V5	**500E:** N.C. **1200E:** I/O **1600E:** I/O
2	IO_L07N_2	IO_L07N_2	IO_L07N_2	P7	I/O
2	IO_L07P_2	IO_L07P_2	IO_L07P_2	N7	I/O
2	IO_L09N_2	IO_L09N_2	IO_L09N_2	N8	I/O
2	IO_L09P_2	IO_L09P_2	IO_L09P_2	P8	I/O
2	IO_L10N_2	IO_L10N_2	IO_L10N_2	T8	I/O
2	IO_L10P_2	IO_L10P_2	IO_L10P_2	R8	I/O
2	IO_L12N_2/D6/GCLK13	IO_L12N_2/D6/GCLK13	IO_L12N_2/D6/GCLK13	M9	DUAL/GCLK
2	IO_L12P_2/D7/GCLK12	IO_L12P_2/D7/GCLK12	IO_L12P_2/D7/GCLK12	N9	DUAL/GCLK
2	IO_L13N_2/D3/GCLK15	IO_L13N_2/D3/GCLK15	IO_L13N_2/D3/GCLK15	V9	DUAL/GCLK
2	IO_L13P_2/D4/GCLK14	IO_L13P_2/D4/GCLK14	IO_L13P_2/D4/GCLK14	U9	DUAL/GCLK
2	IO_L15N_2/D1/GCLK3	IO_L15N_2/D1/GCLK3	IO_L15N_2/D1/GCLK3	P10	DUAL/GCLK
2	IO_L15P_2/D2/GCLK2	IO_L15P_2/D2/GCLK2	IO_L15P_2/D2/GCLK2	R10	DUAL/GCLK
2	IO_L16N_2/DIN/D0	IO_L16N_2/DIN/D0	IO_L16N_2/DIN/D0	N10	DUAL
2	IO_L16P_2/M0	IO_L16P_2/M0	IO_L16P_2/M0	M10	DUAL
2	IO_L18N_2	IO_L18N_2	IO_L18N_2	N11	I/O
2	IO_L18P_2	IO_L18P_2	IO_L18P_2	P11	I/O
2	IO_L19N_2/VREF_2	IO_L19N_2/VREF_2	IO_L19N_2/VREF_2	V13	VREF
2	IO_L19P_2	IO_L19P_2	IO_L19P_2	V12	I/O
2	IO_L20N_2	IO_L20N_2	IO_L20N_2	R12	I/O

Table 152: **FG400 Package Pinout *(Cont'd)***

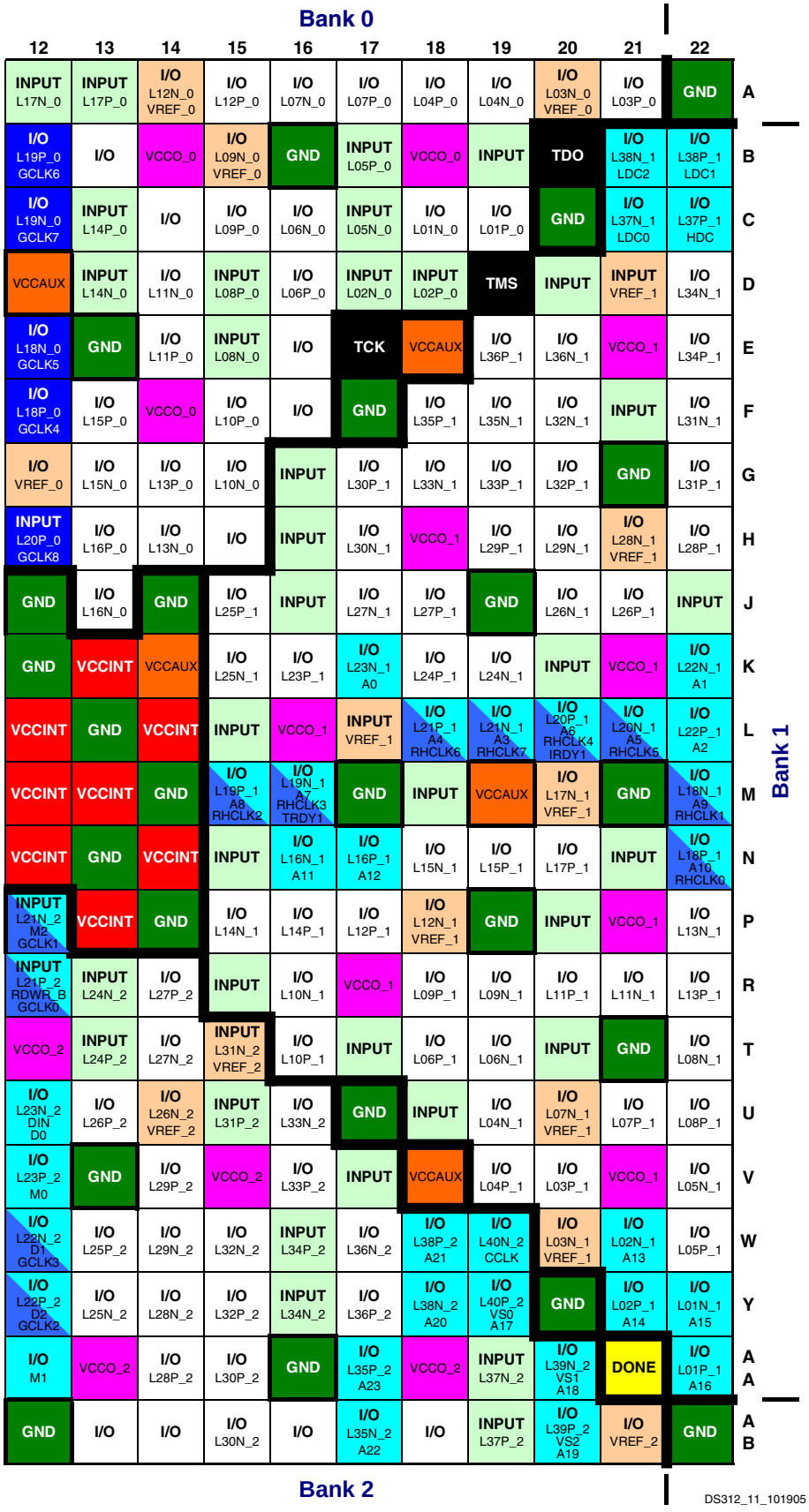
Bank	XC3S1200E XC3S1600E Pin Name	FG400 Ball	Type
3	IP	N5	INPUT
3	IP	P3	INPUT
3	IP	T4	INPUT
3	IP	W1	INPUT
3	IP/VREF_3	K5	VREF
3	IP/VREF_3	P6	VREF
3	VCCO_3	E2	VCCO
3	VCCO_3	H4	VCCO
3	VCCO_3	L2	VCCO
3	VCCO_3	L6	VCCO
3	VCCO_3	P4	VCCO
3	VCCO_3	U2	VCCO
GND	GND	A1	GND
GND	GND	A11	GND
GND	GND	A20	GND
GND	GND	B7	GND
GND	GND	B14	GND
GND	GND	C3	GND
GND	GND	C18	GND
GND	GND	D10	GND
GND	GND	F6	GND
GND	GND	F15	GND
GND	GND	G2	GND
GND	GND	G12	GND
GND	GND	G19	GND
GND	GND	H8	GND
GND	GND	J9	GND
GND	GND	J11	GND
GND	GND	K1	GND
GND	GND	K8	GND
GND	GND	K10	GND
GND	GND	K12	GND
GND	GND	K17	GND
GND	GND	L4	GND
GND	GND	L9	GND
GND	GND	L11	GND
GND	GND	L13	GND
GND	GND	L20	GND
GND	GND	M10	GND
GND	GND	M12	GND
GND	GND	N13	GND
GND	GND	P2	GND
GND	GND	P9	GND

Table 152: **FG400 Package Pinout *(Cont'd)***

Bank	XC3S1200E XC3S1600E Pin Name	FG400 Ball	Type
GND	GND	P19	GND
GND	GND	R6	GND
GND	GND	R15	GND
GND	GND	U11	GND
GND	GND	V3	GND
GND	GND	V18	GND
GND	GND	W7	GND
GND	GND	W14	GND
GND	GND	Y1	GND
GND	GND	Y10	GND
GND	GND	Y20	GND
VCCAUX	DONE	V17	CONFIG
VCCAUX	PROG_B	C2	CONFIG
VCCAUX	TCK	D17	JTAG
VCCAUX	TDI	B3	JTAG
VCCAUX	TDO	B19	JTAG
VCCAUX	TMS	E17	JTAG
VCCAUX	VCCAUX	D11	VCCAUX
VCCAUX	VCCAUX	H12	VCCAUX
VCCAUX	VCCAUX	J7	VCCAUX
VCCAUX	VCCAUX	K4	VCCAUX
VCCAUX	VCCAUX	L17	VCCAUX
VCCAUX	VCCAUX	M14	VCCAUX
VCCAUX	VCCAUX	N9	VCCAUX
VCCAUX	VCCAUX	U10	VCCAUX
VCCINT	VCCINT	H9	VCCINT
VCCINT	VCCINT	H11	VCCINT
VCCINT	VCCINT	H13	VCCINT
VCCINT	VCCINT	J8	VCCINT
VCCINT	VCCINT	J10	VCCINT
VCCINT	VCCINT	J12	VCCINT
VCCINT	VCCINT	K9	VCCINT
VCCINT	VCCINT	K11	VCCINT
VCCINT	VCCINT	L10	VCCINT
VCCINT	VCCINT	L12	VCCINT
VCCINT	VCCINT	M9	VCCINT
VCCINT	VCCINT	M11	VCCINT
VCCINT	VCCINT	M13	VCCINT
VCCINT	VCCINT	N8	VCCINT
VCCINT	VCCINT	N10	VCCINT
VCCINT	VCCINT	N12	VCCINT

FG484 Footprint

Right Half of Package (top view)



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