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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	612
Number of Logic Elements/Cells	5508
Total RAM Bits	221184
Number of I/O	158
Number of Gates	250000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s250e-5pq208c

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/01/05	1.0	Initial Xilinx release.
03/21/05	1.1	Added XC3S250E in CP132 package to Table 2. Corrected number of differential I/O pairs for CP132 package. Added package markings for QFP packages (Figure 2) and CP132/CPG132 packages (Figure 4).
11/23/05	2.0	Added differential HSTL and SSTL I/O standards. Updated Table 2 to indicate number of input-only pins. Added Production Stepping information, including example top marking diagrams.
03/22/06	3.0	Upgraded data sheet status to Preliminary. Added XC3S100E in CP132 package and updated I/O counts for the XC3S1600E in FG320 package (Table 2). Added information about dual markings for –5C and –4I product combinations to Package Marking.
11/09/06	3.4	Added 66 MHz PCI support and links to the Xilinx PCI LogiCORE data sheet. Indicated that Stepping 1 parts are Production status. Promoted Module 1 to Production status. Synchronized all modules to v3.4.
04/18/08	3.7	Added XC3S500E VQG100 package. Added reference to XA Automotive version. Updated links.
08/26/09	3.8	Added paragraph to Configuration indicating the device supports MultiBoot configuration. Added package sizes to Table 2. Described the speed grade and temperature range guarantee for devices having a single mark in paragraph 3 under Package Marking. Deleted Pb-Free Packaging example under Ordering Information. Revised information under Production Stepping. Revised description of Table 3.
10/29/12	4.0	Added Notice of Disclaimer. This product is not recommended for new designs. Updated Table 2 footprint size of PQ208.

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Introduction

As described in Architectural Overview, the Spartan-3E FPGA architecture consists of five fundamental functional elements:

- Input/Output Blocks (IOBs)
- Configurable Logic Block (CLB) and Slice Resources
- Block RAM
- Dedicated Multipliers
- Digital Clock Managers (DCMs)

The following sections provide detailed information on each of these functions. In addition, this section also describes the following functions:

- Clocking Infrastructure
- Interconnect
- Configuration
- Powering Spartan-3E FPGAs

Input/Output Blocks (IOBs)

For additional information, refer to the “Using I/O Resources” chapter in UG331.

IOB Overview

The Input/Output Block (IOB) provides a programmable, unidirectional or bidirectional interface between a package pin and the FPGA’s internal logic. The IOB is similar to that of the Spartan-3 family with the following differences:

- Input-only blocks are added
- Programmable input delays are added to all blocks
- DDR flip-flops can be shared between adjacent IOBs

The unidirectional input-only block has a subset of the full IOB capabilities. Thus there are no connections or logic for an output path. The following paragraphs assume that any reference to output functionality does not apply to the input-only blocks. The number of input-only blocks varies with device size, but is never more than 25% of the total IOB count.

Figure 5 is a simplified diagram of the IOB’s internal structure. There are three main signal paths within the IOB: the output path, input path, and 3-state path. Each path has its own pair of storage elements that can act as either registers or latches. For more information, see Storage Element Functions. The three main signal paths are as follows:

- The input path carries data from the pad, which is bonded to a package pin, through an optional programmable delay element directly to the I line. After the delay element, there are alternate routes through a pair of storage elements to the IQ1 and IQ2 lines. The IOB outputs I, IQ1, and IQ2 lead to the FPGA’s internal logic. The delay element can be set to ensure a hold time of zero (see Input Delay Functions).
- The output path, starting with the O1 and O2 lines, carries data from the FPGA’s internal logic through a multiplexer and then a three-state driver to the IOB pad. In addition to this direct path, the multiplexer provides the option to insert a pair of storage elements.
- The 3-state path determines when the output driver is high impedance. The T1 and T2 lines carry data from the FPGA’s internal logic through a multiplexer to the output driver. In addition to this direct path, the multiplexer provides the option to insert a pair of storage elements.
- All signal paths entering the IOB, including those associated with the storage elements, have an inverter option. Any inverter placed on these paths is automatically absorbed into the IOB.

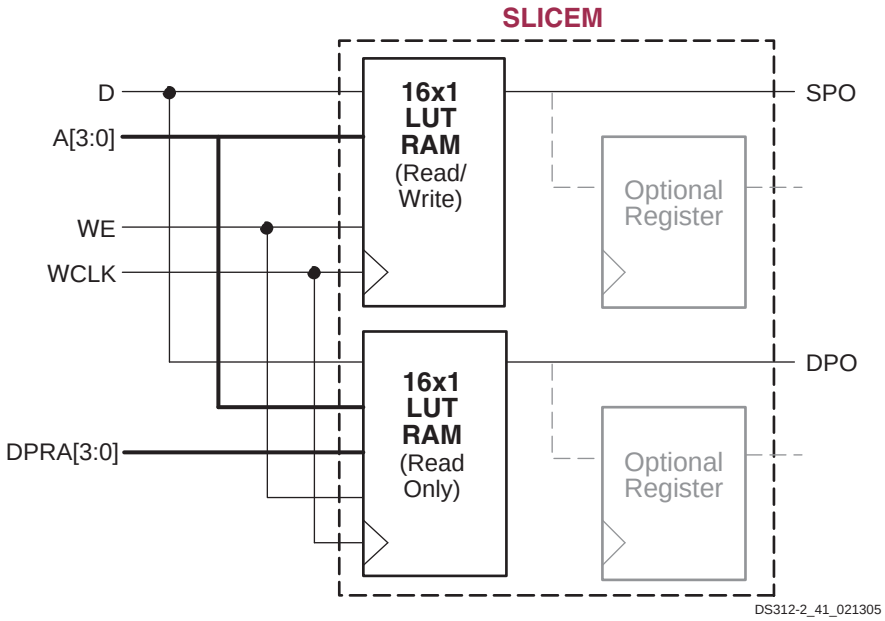


Figure 26: RAM16X1D Dual-Port Usage

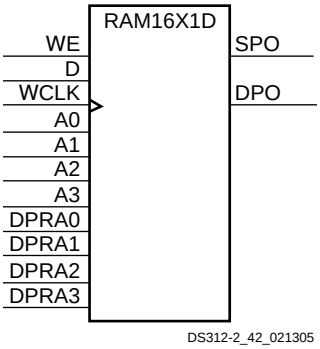


Figure 27: Dual-Port RAM Component

Table 18: Dual-Port RAM Function

Inputs			Outputs	
WE (mode)	WCLK	D	SPO	DPO
0 (read)	X	X	data_a	data_d
1 (read)	0	X	data_a	data_d
1 (read)	1	X	data_a	data_d
1 (write)	↑	D	D	data_d
1 (read)	↓	X	data_a	data_d

Notes:

1. data_a = word addressed by bits A3-A0.
2. data_d = word addressed by bits DPRA3-DPRA0.

Table 19: Distributed RAM Signals

Signal	Description
WCLK	The clock is used for synchronous writes. The data and the address input pins have setup times referenced to the WCLK pin. Active on the positive edge by default with built-in programmable polarity.
WE	The enable pin affects the write functionality of the port. An inactive Write Enable prevents any writing to memory cells. An active Write Enable causes the clock edge to write the data input signal to the memory location pointed to by the address inputs. Active High by default with built-in programmable polarity.
A0, A1, A2, A3 (A4, A5)	The address inputs select the memory cells for read or write. The width of the port determines the required address inputs.
D	The data input provides the new data value to be written into the RAM.
O, SPO, and DPO	The data output O on single-port RAM or the SPO and DPO outputs on dual-port RAM reflects the contents of the memory cells referenced by the address inputs. Following an active write clock edge, the data out (O or SPO) reflects the newly written data.

The INIT attribute can be used to preload the memory with data during FPGA configuration. The default initial contents for RAM is all zeros. If the WE is held Low, the element can be considered a ROM. The ROM function is possible even in the SLICEL.

The global write enable signal, GWE, is asserted automatically at the end of device configuration to enable all writable elements. The GWE signal guarantees that the

Table 22: Port Aspect Ratios

Total Data Path Width (w bits)	DI/DO Data Bus Width (w-p bits) (1)	DIP/DOP Parity Bus Width (p bits)	ADDR Bus Width (r bits) (2)	DI/DO [w-p-1:0]	DIP/DOP [p-1:0]	ADDR [r-1:0]	No. of Addressable Locations (n) (3)	Block RAM Capacity (w*n bits) (4)
1	1	0	14	[0:0]	-	[13:0]	16,384	16,384
2	2	0	13	[1:0]	-	[12:0]	8,192	16,384
4	4	0	12	[3:0]	-	[11:0]	4,096	16,384
9	8	1	11	[7:0]	[0:0]	[10:0]	2,048	18,432
18	16	2	10	[15:0]	[1:0]	[9:0]	1,024	18,432
36	32	4	9	[31:0]	[3:0]	[8:0]	512	18,432

Notes:

1. The width of the total data path (w) is the sum of the DI/DO bus width (w-p) and any parity bits (p).
2. The width selection made for the DI/DO bus determines the number of address lines (r) according to the relationship expressed as: r = 14 – [log(w–p)/log9(2)].
3. The number of address lines delimits the total number (n) of addressable locations or depth according to the following equation: $n = 2^r$.
4. The product of w and n yields the total block RAM capacity.

If the data bus width of Port A differs from that of Port B, the block RAM automatically performs a bus-matching function as described in Figure 31. When data is written to a port with a narrow bus and then read from a port with a wide bus, the latter port effectively combines “narrow” words to form “wide” words. Similarly, when data is written into a port with a wide bus and then read from a port with a narrow bus, the latter port divides “wide” words to form “narrow” words. Parity bits are not available if the data port width is configured as x4, x2, or x1. For example, if a x36 data word (32 data, 4 parity) is addressed as two x18 halfwords (16 data, 2 parity), the parity bits associated with each data byte are mapped within the block RAM to the appropriate parity bits. The same effect happens when the x36 data word is mapped as four x9 words.

Table 55: Serial Peripheral Interface (SPI) Connections ***(Cont'd)***

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
VS[2:0] (S)	Input	Variant Select . Instructs the FPGA how to communicate with the attached SPI Flash PROM. See Design Considerations for the HSWAP, M[2:0], and VS[2:0] Pins.	Must be at the logic levels shown in Table 53. Sampled when INIT_B goes High.	User I/O
MOSI	Output	Serial Data Output .	FPGA sends SPI Flash memory read commands and starting address to the PROM's serial data input.	User I/O
DIN	Input	Serial Data Input .	FPGA receives serial data from PROM's serial data output.	User I/O
CSO_B	Output	Chip Select Output . Active Low.	Connects to the SPI Flash PROM's chip-select input. If HSWAP = 1, connect this signal to a 4.7 kΩ pull-up resistor to 3.3V.	Drive CSO_B High after configuration to disable the SPI Flash and reclaim the MOSI, DIN, and CCLK pins. Optionally, re-use this pin and MOSI, DIN, and CCLK to continue communicating with SPI Flash.
CCLK	Output	Configuration Clock . Generated by FPGA internal oscillator. Frequency controlled by ***ConfigRate*** bitstream generator option. If CCLK PCB trace is long or has multiple connections, terminate this output to maintain signal integrity. See CCLK Design Considerations.	Drives PROM's clock input.	User I/O
DOUT	Output	Serial Data Output .	Actively drives. Not used in single-FPGA designs. In a daisy-chain configuration, this pin connects to DIN input of the next FPGA in the chain.	User I/O
INIT_B	Open-drain bidirectional I/O	Initialization Indicator . Active Low. Goes Low at start of configuration during Initialization memory clearing process. Released at end of memory clearing, when mode select pins are sampled. In daisy-chain applications, this signal requires an external 4.7 kΩ pull-up resistor to VCCO_2.	Active during configuration. If SPI Flash PROM requires > 2 ms to awake after powering on, hold INIT_B Low until PROM is ready. If CRC error detected during configuration, FPGA drives INIT_B Low.	User I/O. If unused in the application, drive INIT_B High.
DONE	Open-drain bidirectional I/O	FPGA Configuration Done . Low during configuration. Goes High when FPGA successfully completes configuration. Requires external 330 Ω pull-up resistor to 2.5V.	Low indicates that the FPGA is not yet configured.	Pulled High via external pull-up. When High, indicates that the FPGA successfully configured.
PROG_B	Input	Program FPGA . Active Low. When asserted Low for 500 ns or longer, forces the FPGA to restart its configuration process by clearing configuration memory and resetting the DONE and INIT_B pins once PROG_B returns High. Recommend external 4.7 kΩ pull-up resistor to 2.5V. Internal pull-up value may be weaker (see Table 78). If driving externally with a 3.3V output, use an open-drain or open-collector driver or use a current limiting series resistor.	Must be High to allow configuration to start.	Drive PROG_B Low and release to reprogram FPGA. Hold PROG_B to force FPGA I/O pins into Hi-Z, allowing direct programming access to SPI Flash PROM pins.

After the FPGA configures itself using BPI mode from one end of the parallel Flash PROM, then the FPGA can trigger a MultiBoot event and reconfigure itself from the opposite end of the parallel Flash PROM. MultiBoot is only available when using BPI mode and only for applications with a single Spartan-3E FPGA.

By default, MultiBoot mode is disabled. To trigger a MultiBoot event, assert a Low pulse lasting at least 300 ns on the MultiBoot Trigger (MBT) input to the STARTUP_SPARTAN3E library primitive. When the MBT signal returns High after the 300 ns or longer pulse, the FPGA automatically reconfigures from the opposite end of the parallel Flash memory.

Figure 60 shows an example usage. At power up, the FPGA loads itself from the attached parallel Flash PROM. In this example, the M0 mode pin is Low so the FPGA starts at address 0 and increments through the Flash PROM memory locations. After the FPGA completes configuration, the application initially loaded into the FPGA performs a board-level or system test using FPGA logic. If the test is successful, the FPGA then triggers a MultiBoot event, causing the FPGA to reconfigure from the opposite end of the Flash PROM memory. This second configuration contains the FPGA application for normal operation.

Similarly, the general FPGA application could trigger another MultiBoot event at any time to reload the diagnostics design, and so on.

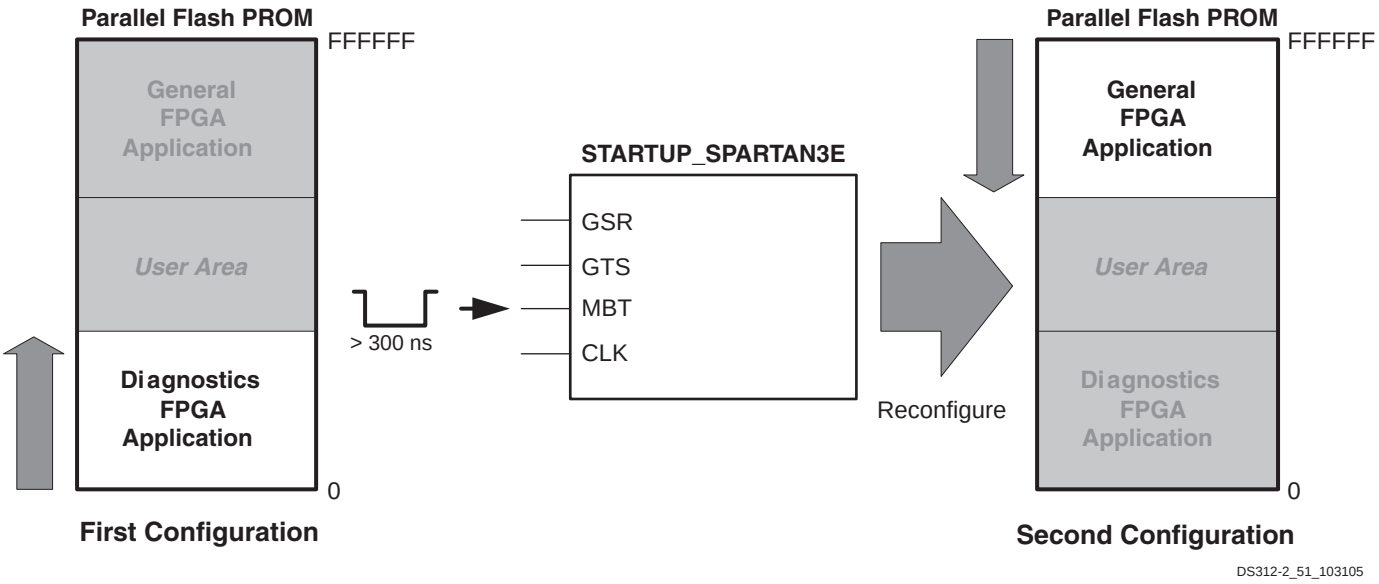


Figure 60: Use MultiBoot to Load Alternate Configuration Images

In another potential application, the initial design loaded into the FPGA image contains a “golden” or “fail-safe” configuration image, which then communicates with the outside world and checks for a newer image. If there is a new configuration revision and the new image verifies as good, the “golden” configuration triggers a MultiBoot event to load the new image.

When a MultiBoot event is triggered, the FPGA then again drives its configuration pins as described in Table 59. However, the FPGA does not assert the PROG_B pin. The system design must ensure that no other device drives on these same pins during the reconfiguration process. The FPGA’s DONE, LDC[2:0], or HDC pins can temporarily disable any conflicting drivers during reconfiguration.

Asserting the PROG_B pin Low overrides the MultiBoot feature and forces the FPGA to reconfigure starting from the end of memory defined by the mode pins, shown in Table 58.

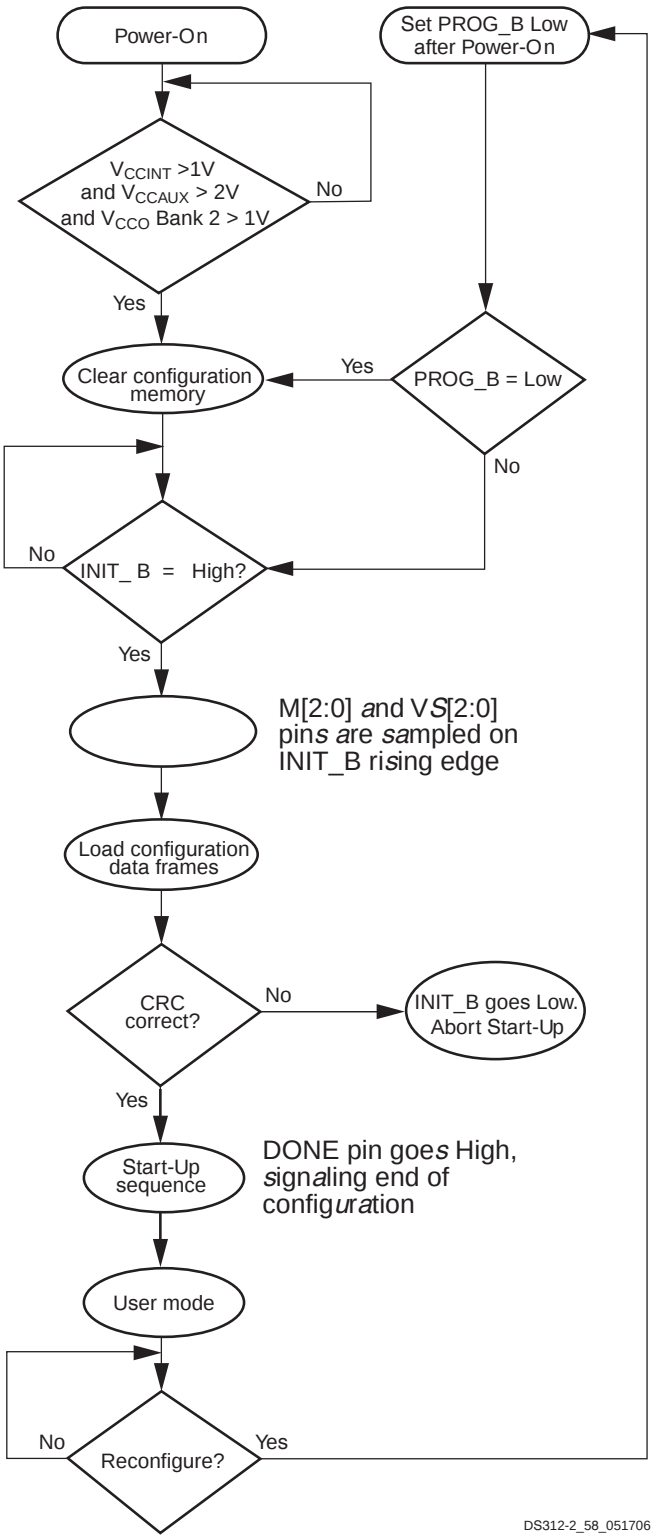


Figure 66: General Configuration Process

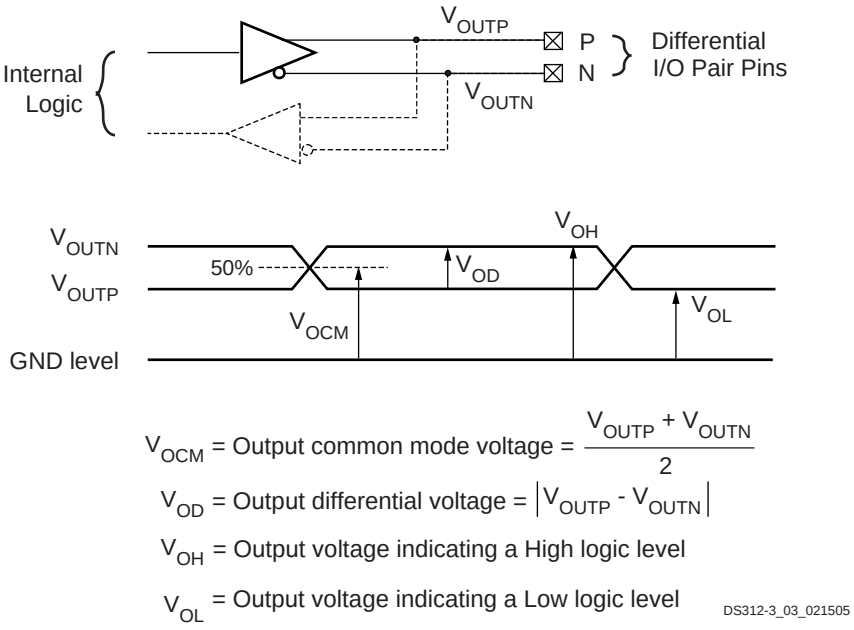


Figure 70: Differential Output Voltages

Table 83: DC Characteristics of User I/Os Using Differential Signal Standards

IOSTANDARD Attribute	V_{OD}			ΔV_{OD}		V_{OCM}			ΔV_{OCM}		V_{OH}	V_{OL}
	Min (mV)	Typ (mV)	Max (mV)	Min (mV)	Max (mV)	Min (V)	Typ (V)	Max (V)	Min (mV)	Max (mV)	Min (V)	Max (V)
LVDS_25	250	350	450	–	–	1.125	–	1.375	–	–	–	–
BLVDS_25	250	350	450	–	–	–	1.20	–	–	–	–	–
MINI_LVDS_25	300	–	600	–	50	1.0	–	1.4	–	50	–	–
RSDS_25	100	–	400	–	–	1.1	–	1.4	–	–	–	–
DIFF_HSTL_I_18	–	–	–	–	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_III_18	–	–	–	–	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_SSTL18_I	–	–	–	–	–	–	–	–	–	–	V_{TT} + 0.475	V_{TT} – 0.475
DIFF_SSTL2_I	–	–	–	–	–	–	–	–	–	–	V_{TT} + 0.61	V_{TT} – 0.61

Notes:

1. The numbers in this table are based on the conditions set forth in Table 77 and Table 82.
2. Output voltage measurements for all differential standards are made with a termination resistor (R_T) of 100Ω across the N and P pins of the differential signal pair. The exception is for BLVDS, shown in Figure 71.
3. At any given time, no more than two of the following differential output standards may be assigned to an I/O bank: LVDS_25, RSDS_25, MINI_LVDS_25

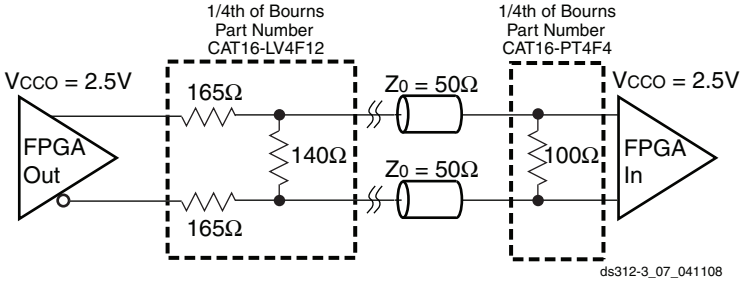


Figure 71: External Termination Resistors for BLVDS Transmitter and BLVDS Receiver

Table 88: Setup and Hold Times for the IOB Input Path

Symbol	Description	Conditions	IFD_DELAY_VALUE=	Device	Speed Grade		Units
					-5	-4	
					Min	Min	
Setup Times							
T_{IOPICK}	Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). No Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = 0	0	All	1.84	2.12	ns
$T_{IOPICKD}$	Time from the setup of data at the Input pin to the active transition at the IFF's ICLK input. The Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = default software setting	2	XC3S100E	6.12	7.01	ns
			3	All Others	6.76	7.72	
Hold Times							
T_{IOICKP}	Time from the active transition at the IFF's ICLK input to the point where data must be held at the Input pin. No Input Delay is programmed.	LVCMOS25(3), IFD_DELAY_VALUE = 0	0	All	–0.76	–0.76	ns
$T_{IOICKPD}$	Time from the active transition at the IFF's ICLK input to the point where data must be held at the Input pin. The Input Delay is programmed.	LVCMOS25(3), IFD_DELAY_VALUE = default software setting	2	XC3S100E	–3.93	–3.93	ns
			3	All Others	–3.50	–3.50	
Set/Reset Pulse Width							
T_{RPW_IOB}	Minimum pulse width to SR control input on IOB			All	1.57	1.80	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 95 and are based on the operating conditions set forth in Table 77 and Table 80.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, add the appropriate Input adjustment from Table 91.
3. These hold times require adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, subtract the appropriate Input adjustment from Table 91. When the hold time is negative, it is possible to change the data before the clock's active edge.

Table 89: Sample Window (Source Synchronous)

Symbol	Description	Max	Units
T_{SAMP}	Setup and hold capture window of an IOB input flip-flop	The input capture sample window value is highly specific to a particular application, device, package, I/O standard, I/O placement, DCM usage, and clock buffer. Please consult the appropriate Xilinx application note for application-specific values. • XAPP485: 1:7 Deserialization in Spartan-3E FPGAs at Speeds Up to 666 Mbps	ps

Table 92: Timing for the IOB Output Path

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Min	Min	
Clock-to-Output Times						
T_{IOCKP}	When reading from the Output Flip-Flop (OFF), the time from the active transition at the OCLK input to data appearing at the Output pin	LVCMOS25(2), 12 mA output drive, Fast slew rate	All	2.18	2.50	ns
Propagation Times						
T_{IOOP}	The time it takes for data to travel from the IOB's O input to the Output pin	LVCMOS25(2), 12 mA output drive, Fast slew rate	All	2.24	2.58	ns
T_{IOOLP}	The time it takes for data to travel from the O input through the OFF latch to the Output pin			2.32	2.67	ns
Set/Reset Times						
T_{IOSRP}	Time from asserting the OFF's SR input to setting/resetting data at the Output pin	LVCMOS25(2), 12 mA output drive, Fast slew rate	All	3.27	3.76	ns
T_{IOGSRQ}	Time from asserting the Global Set Reset (GSR) input on the STARTUP_SPARTAN3E primitive to setting/resetting data at the Output pin			8.40	9.65	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 95 and are based on the operating conditions set forth in Table 77 and Table 80.
2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, add the appropriate Output adjustment from Table 94.
3. For minimum delays use the values reported by the Timing Analyzer.

Phase Shifter (PS)

Table 108: Recommended Operating Conditions for the PS in Variable Phase Mode

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Operating Frequency Ranges						
PSCLK_FREQ (F_{PSCLK})	Frequency for the PSCLK input	1	167	1	167	MHz
Input Pulse Requirements						
PSCLK_PULSE	PSCLK pulse width as a percentage of the PSCLK period	40%	60%	40%	60%	-

Table 109: Switching Characteristics for the PS in Variable Phase Mode

Symbol	Description	Equation		Units
Phase Shifting Range				
MAX_STEPS(2)	Maximum allowed number of DCM_DELAY_STEP steps for a given CLKIN clock period, where T = CLKIN clock period in ns. If using CLKIN_DIVIDE_BY_2 = TRUE, double the effective clock period.(3)	CLKIN < 60 MHz	±[INTEGER(10 • (T_{CLKIN} – 3 ns))]	steps
		CLKIN ≥ 60 MHz	±[INTEGER(15 • (T_{CLKIN} – 3 ns))]	steps
FINE_SHIFT_RANGE_MIN	Minimum guaranteed delay for variable phase shifting	±[MAX_STEPS • DCM_DELAY_STEP_MIN]		ns
FINE_SHIFT_RANGE_MAX	Maximum guaranteed delay for variable phase shifting	±[MAX_STEPS • DCM_DELAY_STEP_MAX]		ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 77 and Table 108.
2. The maximum variable phase shift range, MAX_STEPS, is only valid when the DCM is has no initial fixed phase shifting, i.e., the PHASE_SHIFT attribute is set to 0.
3. The DCM_DELAY_STEP values are provided at the bottom of Table 105.

Miscellaneous DCM Timing

Table 110: Miscellaneous DCM Timing

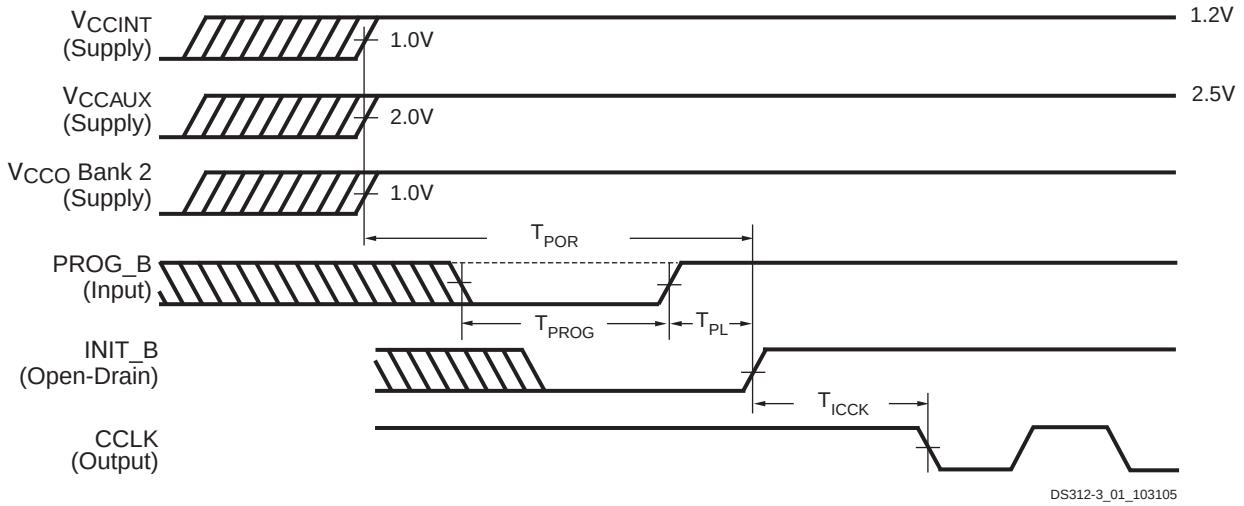
Symbol	Description	Min	Max	Units
DCM_RST_PW_MIN(1)	Minimum duration of a RST pulse width	3	-	CLKIN cycles
DCM_RST_PW_MAX(2)	Maximum duration of a RST pulse width	N/A	N/A	seconds
DCM_CONFIG_LAG_TIME(3)	Maximum duration from V_{CCINT} applied to FPGA configuration successfully completed (DONE pin goes High) and clocks applied to DCM DLL	N/A	N/A	minutes

Notes:

1. This limit only applies to applications that use the DCM DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV). The DCM DFS outputs (CLKFX, CLKFX180) are unaffected.
2. This specification is equivalent to the Virtex-4 DCM_RESET specfication.This specification does not apply for Spartan-3E FPGAs.
3. This specification is equivalent to the Virtex-4 TCONFIG specification. This specification does not apply for Spartan-3E FPGAs.

Configuration and JTAG Timing

General Configuration Power-On/Reconfigure Timing



Notes:

1. The V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies may be applied in any order.
2. The Low-going pulse on PROG_B is optional after power-on but necessary for reconfiguration without a power cycle.
3. The rising edge of INIT_B samples the voltage levels applied to the mode pins (M0 - M2).

Figure 73: Waveforms for Power-On and the Beginning of Configuration

Table 111: Power-On Timing and the Beginning of Configuration

Symbol	Description	Device	All Speed Grades		Units
			Min	Max	
T_{POR}(2)	The time from the application of V_{CCINT}, V_{CCAUX}, and V_{CCO} Bank 2 supply voltage ramps (whichever occurs last) to the rising transition of the INIT_B pin	XC3S100E	-	5	ms
		XC3S250E	-	5	ms
		XC3S500E	-	5	ms
		XC3S1200E	-	5	ms
		XC3S1600E	-	7	ms
T_{PROG}	The width of the low-going pulse on the PROG_B pin	All	0.5	-	µs
T_{PL}(2)	The time from the rising edge of the PROG_B pin to the rising transition on the INIT_B pin	XC3S100E	-	0.5	ms
		XC3S250E	-	0.5	ms
		XC3S500E	-	1	ms
		XC3S1200E	-	2	ms
		XC3S1600E	-	2	ms
T_{INIT}	Minimum Low pulse width on INIT_B output	All	250	-	ns
T_{ICCK}(3)	The time from the rising edge of the INIT_B pin to the generation of the configuration clock signal at the CCLK output pin	All	0.5	4.0	µs

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 77. This means power must be applied to all V_{CCINT}, V_{CCO}, and V_{CCAUX} lines.
2. Power-on reset and the clearing of configuration memory occurs during this period.
3. This specification applies only to the Master Serial, SPI, BPI-Up, and BPI-Down modes.

Configuration Clock (CCLK) Characteristics

Table 112: Master Mode CCLK Output Period by ***ConfigRate*** Option Setting

Symbol	Description	***ConfigRate*** Setting	Temperature Range	Minimum	Maximum	Units
T_{CCLK1}	CCLK clock period by ***ConfigRate*** setting	1 (power-on value and default value)	Commercial	570	1,250	ns
			Industrial	485		ns
T_{CCLK3}		3	Commercial	285	625	ns
			Industrial	242		ns
T_{CCLK6}		6	Commercial	142	313	ns
			Industrial	121		ns
T_{CCLK12}		12	Commercial	71.2	157	ns
			Industrial	60.6		ns
T_{CCLK25}		25	Commercial	35.5	78.2	ns
			Industrial	30.3		ns
T_{CCLK50}		50	Commercial	17.8	39.1	ns
			Industrial	15.1		ns

Notes:

1. Set the ***ConfigRate*** option value when generating a configuration bitstream. See Bitstream Generator (BitGen) Options in Module 2.

Table 113: Master Mode CCLK Output Frequency by ***ConfigRate*** Option Setting

Symbol	Description	***ConfigRate*** Setting	Temperature Range	Minimum	Maximum	Units
F_{CCLK1}	Equivalent CCLK clock frequency by ***ConfigRate*** setting	1 (power-on value and default value)	Commercial	0.8	1.8	MHz
			Industrial		2.1	MHz
F_{CCLK3}		3	Commercial	1.6	3.6	MHz
			Industrial		4.2	MHz
F_{CCLK6}		6	Commercial	3.2	7.1	MHz
			Industrial		8.3	MHz
F_{CCLK12}		12	Commercial	6.4	14.1	MHz
			Industrial		16.5	MHz
F_{CCLK25}		25	Commercial	12.8	28.1	MHz
			Industrial		33.0	MHz
F_{CCLK50}		50	Commercial	25.6	56.2	MHz
			Industrial		66.0	MHz

Table 114: Master Mode CCLK Output Minimum Low and High Time

Symbol	Description		***ConfigRate*** Setting						Units
			1	3	6	12	25	50	
T_{MCCL}, T_{MCCH}	Master mode CCLK minimum Low and High time	Commercial	276	138	69	34.5	17.1	8.5	ns
		Industrial	235	117	58	29.3	14.5	7.3	ns

Table 115: Slave Mode CCLK Input Low and High Time

Symbol	Description	Min	Max	Units
T_{SCCL}, T_{SCCH}	CCLK Low and High time	5	∞	ns

Byte Peripheral Interface (BPI) Configuration Timing

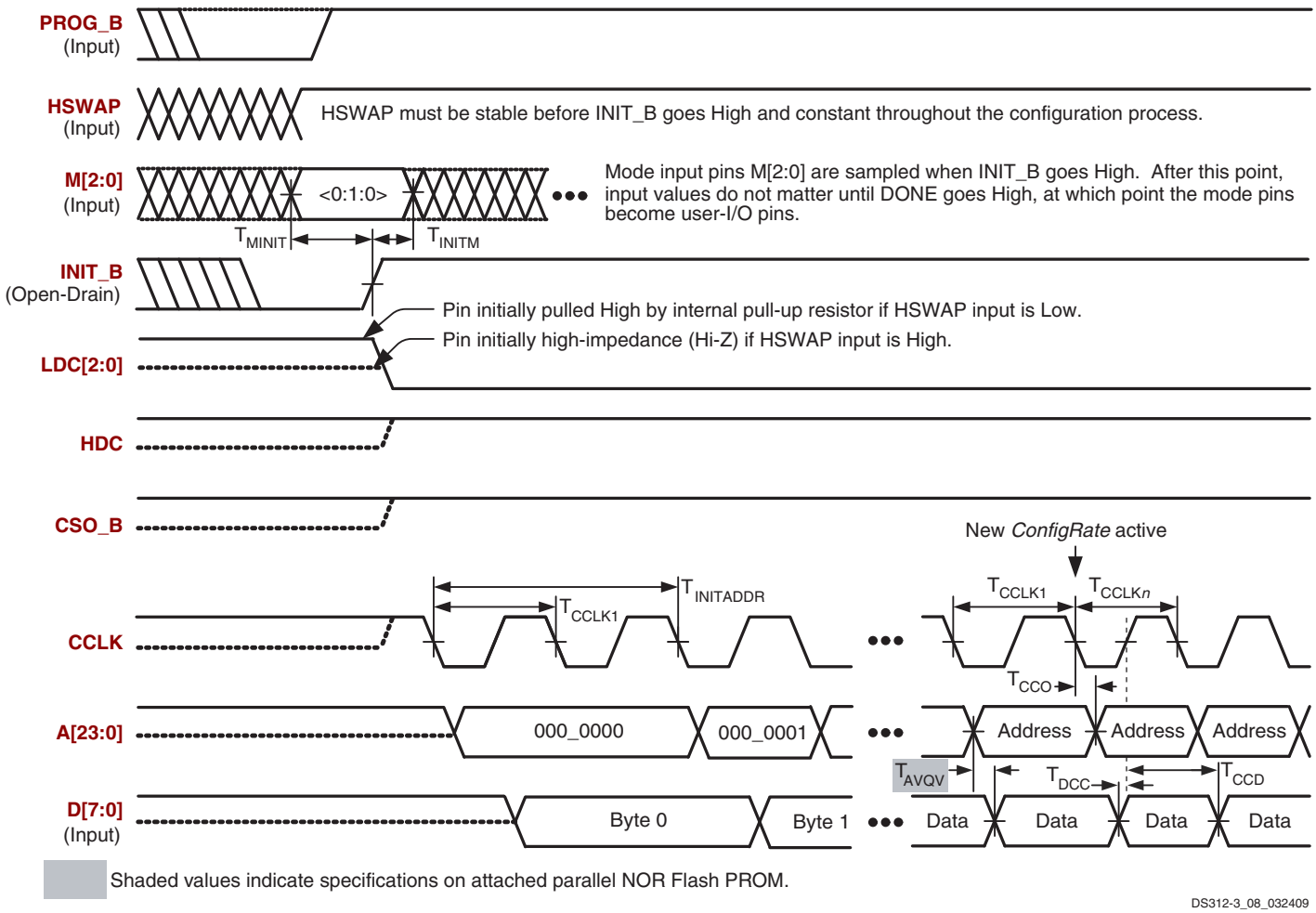


Figure 77: Waveforms for Byte-wide Peripheral Interface (BPI) Configuration (BPI-DN mode shown)

Table 120: Timing for Byte-wide Peripheral Interface (BPI) Configuration Mode

Symbol	Description		Minimum	Maximum	Units
T_{CCLK1}	Initial CCLK clock period		See Table 112		
T_{CCLKn}	CCLK clock period after FPGA loads ConfigRate setting		See Table 112		
T_{MINIT}	Setup time on CSI_B, RDWR_B, and M[2:0] mode pins before the rising edge of INIT_B		50	-	ns
T_{INITM}	Hold time on CSI_B, RDWR_B, and M[2:0] mode pins after the rising edge of INIT_B		0	-	ns
$T_{INITADDR}$	Minimum period of initial A[23:0] address cycle; LDC[2:0] and HDC are asserted and valid	BPI-UP: (M[2:0] = <0:1:0>)	5	5	T_{CCLK1} cycles
		BPI-DN: (M[2:0] = <0:1:1>)	2	2	
T_{CCO}	Address A[23:0] outputs valid after CCLK falling edge		See Table 116		
T_{DCC}	Setup time on D[7:0] data inputs before CCLK rising edge		See Table 116		
T_{CCD}	Hold time on D[7:0] data inputs after CCLK rising edge		See Table 116		

TQ144 Footprint

Note pin 1 indicator in top-left corner and logo orientation.
Double arrows (↔) indicates a pinout migration difference between the XC3S100E and XC3S250E.

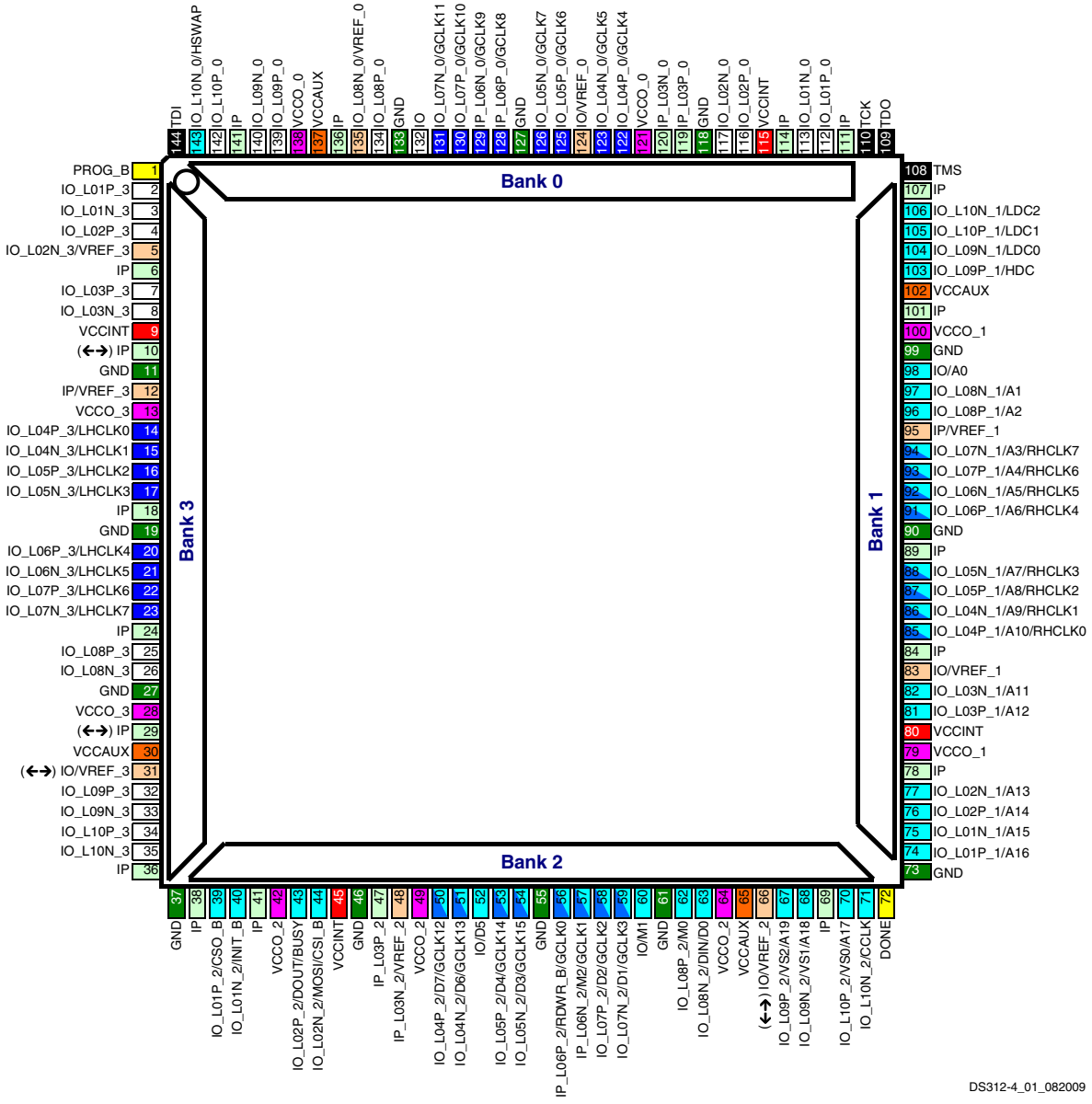


Figure 82: TQ144 Package Footprint (top view)

20	I/O: Unrestricted, general-purpose user I/O	42	DUAL: Configuration pin, then possible user I/O	9	VREF: User I/O or input voltage reference for bank
21	INPUT: Unrestricted, general-purpose input pin	16	CLK: User I/O, input, or global buffer input	9	VCCO: Output voltage supply for bank
2	CONFIG: Dedicated configuration pins	4	JTAG: Dedicated JTAG port pins	4	VCCINT: Internal core supply voltage (+1.2V)
0	N.C.: Not connected	13	GND: Ground	4	VCCAUX: Auxiliary supply voltage (+2.5V)

Footprint Migration Differences

Table 151 summarizes any footprint and functionality differences between the XC3S500E, the XC3S1200E, and the XC3S1600E FPGAs that may affect easy migration between devices available in the FG320 package. There are 26 such balls. All other pins not listed in Table 151 unconditionally migrate between Spartan-3E devices available in the FG320 package.

The XC3S500E is duplicated on both the left and right sides of the table to show migrations to and from the XC3S1200E and the XC3S1600E. The arrows indicate the direction for easy migration. A double-ended arrow (↔) indicates that the two pins have identical functionality. A left-facing arrow (←) indicates that the pin on the device on the right unconditionally migrates to the pin on the device on the left. It may be possible to migrate the opposite direction depending on the I/O configuration. For example, an I/O pin (Type = I/O) can migrate to an input-only pin (Type = INPUT) if the I/O pin is configured as an input.

Table 151: FG320 Footprint Migration Differences

Pin	Bank	XC3S500E	Migration	XC3S1200E	Migration	XC3S1600E	Migration	XC3S500E
A7	0	INPUT	→	I/O	↔	I/O	←	INPUT
A12	0	N.C.	→	I/O	↔	I/O	←	N.C.
D4	3	N.C.	→	I/O	↔	I/O	←	N.C.
D6	0	N.C.	→	I/O	↔	I/O	←	N.C.
D13	0	INPUT	→	I/O	↔	I/O	←	INPUT
E3	3	N.C.	→	I/O	↔	I/O	←	N.C.
E4	3	N.C.	→	I/O	↔	I/O	←	N.C.
E6	0	N.C.	→	I/O	↔	I/O	←	N.C.
E15	1	N.C.	→	I/O	↔	I/O	←	N.C.
E16	1	N.C.	→	I/O	↔	I/O	←	N.C.
E17	1	I/O	←	INPUT	↔	INPUT	→	I/O
F4	3	I/O	←	INPUT	↔	INPUT	→	I/O
N12	2	N.C.	→	I/O	↔	I/O	←	N.C.
N14	1	N.C.	→	I/O	↔	I/O	←	N.C.
N15	1	N.C.	→	I/O	↔	I/O	←	N.C.
P3	3	N.C.	→	I/O	↔	I/O	←	N.C.
P4	3	N.C.	→	I/O	↔	I/O	←	N.C.
P12	2	N.C.	→	I/O	↔	I/O	←	N.C.
P15	1	I/O	←	INPUT	↔	INPUT	→	I/O
P16	1	N.C.	→	I/O	↔	I/O	←	N.C.
R4	3	VREF(I/O)	←	VREF(INPUT)	↔	VREF(INPUT)	→	VREF(I/O)
U6	2	INPUT	→	I/O	↔	I/O	←	INPUT
U13	2	INPUT	→	I/O	↔	I/O	←	INPUT
V5	2	N.C.	→	I/O	↔	I/O	←	N.C.
V6	2	N.C.	→	VREF	↔	VREF	←	N.C.
V7	2	N.C.	→	I/O	↔	I/O	←	N.C.
DIFFERENCES			26		0		26	

Legend:

- ↔ This pin is identical on the device on the left and the right.
- → This pin can unconditionally migrate from the device on the left to the device on the right. Migration in the other direction may be possible depending on how the pin is configured for the device on the right.
- ← This pin can unconditionally migrate from the device on the right to the device on the left. Migration in the other direction may be possible depending on how the pin is configured for the device on the left.

FG320 Footprint

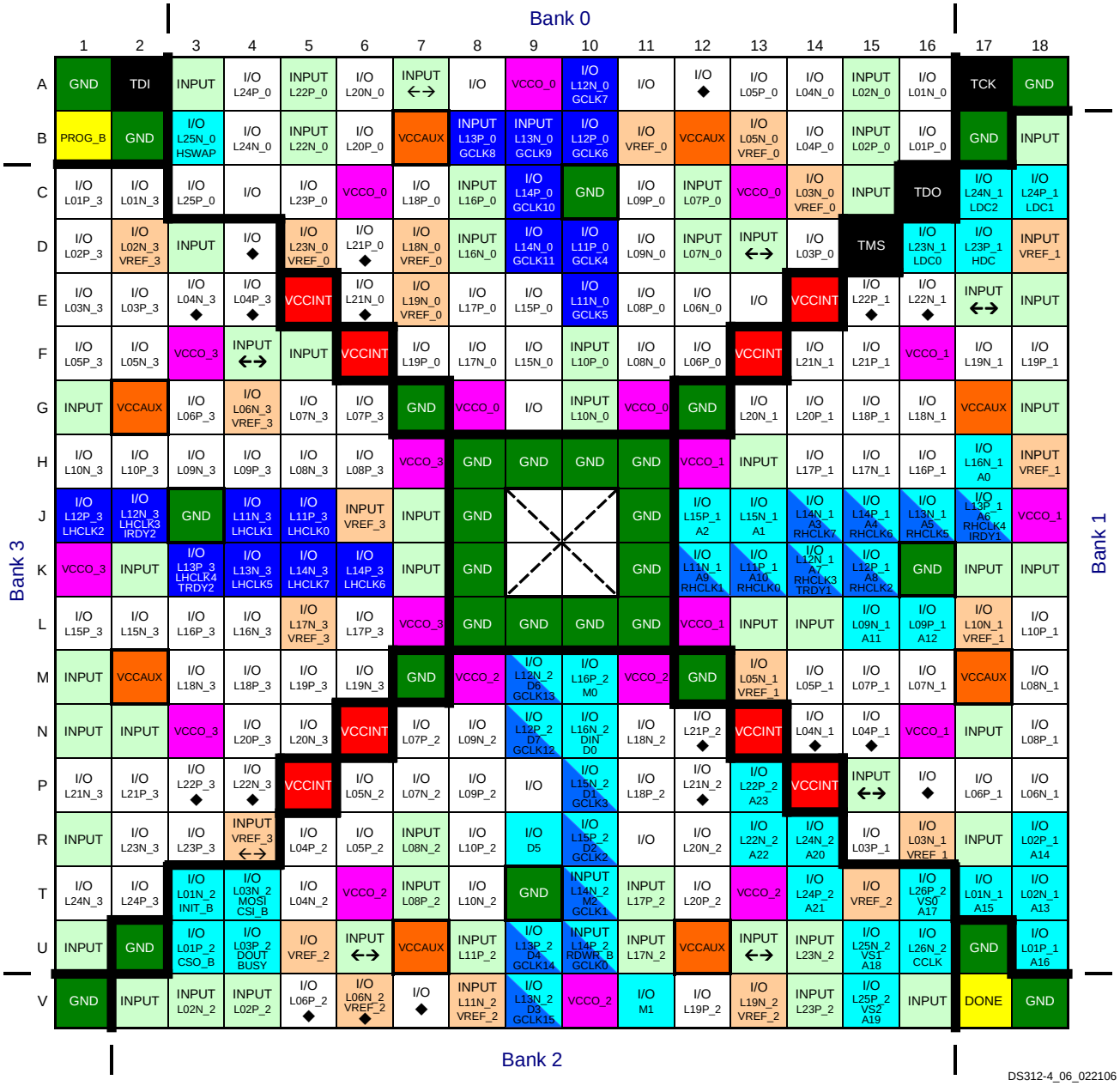


Figure 86: FG320 Package Footprint (top view)

102-120	I/O: Unrestricted, general-purpose user I/O	46	DUAL: Configuration pin, then possible user-I/O	20-21	VREF: User I/O or input voltage reference for bank
47-48	INPUT: Unrestricted, general-purpose input pin	16	CLK: User I/O, input, or global buffer input	20	VCCO: Output voltage supply for bank
2	CONFIG: Dedicated configuration pins	4	JTAG: Dedicated JTAG port pins	8	VCCINT: Internal core supply voltage (+1.2V)
18	N.C.: Not connected. Only the XC3S500E has these pins (◆).	28	GND: Ground	8	VCCAUX: Auxiliary supply voltage (+2.5V)

FG400: 400-ball Fine-p itch Ball Grid Array

The 400-ball fine-pitch ball grid array, FG400, supports two different Spartan-3E FPGAs, including the XC3S1200E and the XC3S1600E. Both devices share a common footprint for this package as shown in Table 152 and Figure 87.

Table 152 lists all the FG400 package pins. They are sorted by bank number and then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at:

http://www.xilinx.com/support/documentation/data_sheets/s3e_pin.zip

Pinout Table

Table 152: FG400 Package Pinout

Bank	XC3S1200E XC3S1600E Pin Name	FG400 Ball	Type
0	IO	A3	I/O
0	IO	A8	I/O
0	IO	A12	I/O
0	IO	C7	I/O
0	IO	C10	I/O
0	IO	E8	I/O
0	IO	E13	I/O
0	IO	E16	I/O
0	IO	F13	I/O
0	IO	F14	I/O
0	IO	G7	I/O
0	IO/VREF_0	C11	VREF
0	IO_L01N_0	B17	I/O
0	IO_L01P_0	C17	I/O
0	IO_L03N_0/VREF_0	A18	VREF
0	IO_L03P_0	A19	I/O
0	IO_L04N_0	A17	I/O
0	IO_L04P_0	A16	I/O
0	IO_L06N_0	A15	I/O
0	IO_L06P_0	B15	I/O
0	IO_L07N_0	C14	I/O
0	IO_L07P_0	D14	I/O
0	IO_L09N_0/VREF_0	A13	VREF
0	IO_L09P_0	A14	I/O
0	IO_L10N_0	B13	I/O
0	IO_L10P_0	C13	I/O
0	IO_L12N_0	C12	I/O

Table 152: FG400 Package Pinout ***(Cont'd)***

Bank	XC3S1200E XC3S1600E Pin Name	FG400 Ball	Type
0	IO_L12P_0	D12	I/O
0	IO_L13N_0	E12	I/O
0	IO_L13P_0	F12	I/O
0	IO_L15N_0/GCLK5	G11	GCLK
0	IO_L15P_0/GCLK4	F11	GCLK
0	IO_L16N_0/GCLK7	E10	GCLK
0	IO_L16P_0/GCLK6	E11	GCLK
0	IO_L18N_0/GCLK11	A9	GCLK
0	IO_L18P_0/GCLK10	A10	GCLK
0	IO_L19N_0	F9	I/O
0	IO_L19P_0	E9	I/O
0	IO_L21N_0	C9	I/O
0	IO_L21P_0	D9	I/O
0	IO_L22N_0/VREF_0	B8	VREF
0	IO_L22P_0	B9	I/O
0	IO_L24N_0/VREF_0	F7	VREF
0	IO_L24P_0	F8	I/O
0	IO_L25N_0	A6	I/O
0	IO_L25P_0	A7	I/O
0	IO_L27N_0	B5	I/O
0	IO_L27P_0	B6	I/O
0	IO_L28N_0	D6	I/O
0	IO_L28P_0	C6	I/O
0	IO_L30N_0/VREF_0	C5	VREF
0	IO_L30P_0	D5	I/O
0	IO_L31N_0	A2	I/O
0	IO_L31P_0	B2	I/O
0	IO_L32N_0/HSWAP	D4	DUAL
0	IO_L32P_0	C4	I/O
0	IP	B18	INPUT
0	IP	E5	INPUT
0	IP_L02N_0	C16	INPUT
0	IP_L02P_0	D16	INPUT
0	IP_L05N_0	D15	INPUT
0	IP_L05P_0	C15	INPUT
0	IP_L08N_0	E14	INPUT
0	IP_L08P_0	E15	INPUT
0	IP_L11N_0	G14	INPUT
0	IP_L11P_0	G13	INPUT
0	IP_L14N_0	B11	INPUT
0	IP_L14P_0	B12	INPUT
0	IP_L17N_0/GCLK9	G10	GCLK

Table 152: FG400 Package Pinout ***(Cont'd)***

Bank	XC3S1200E XC3S1600E Pin Name	FG400 Ball	Type
3	IP	N5	INPUT
3	IP	P3	INPUT
3	IP	T4	INPUT
3	IP	W1	INPUT
3	IP/VREF_3	K5	VREF
3	IP/VREF_3	P6	VREF
3	VCCO_3	E2	VCCO
3	VCCO_3	H4	VCCO
3	VCCO_3	L2	VCCO
3	VCCO_3	L6	VCCO
3	VCCO_3	P4	VCCO
3	VCCO_3	U2	VCCO
GND	GND	A1	GND
GND	GND	A11	GND
GND	GND	A20	GND
GND	GND	B7	GND
GND	GND	B14	GND
GND	GND	C3	GND
GND	GND	C18	GND
GND	GND	D10	GND
GND	GND	F6	GND
GND	GND	F15	GND
GND	GND	G2	GND
GND	GND	G12	GND
GND	GND	G19	GND
GND	GND	H8	GND
GND	GND	J9	GND
GND	GND	J11	GND
GND	GND	K1	GND
GND	GND	K8	GND
GND	GND	K10	GND
GND	GND	K12	GND
GND	GND	K17	GND
GND	GND	L4	GND
GND	GND	L9	GND
GND	GND	L11	GND
GND	GND	L13	GND
GND	GND	L20	GND
GND	GND	M10	GND
GND	GND	M12	GND
GND	GND	N13	GND
GND	GND	P2	GND
GND	GND	P9	GND

Table 152: FG400 Package Pinout ***(Cont'd)***

Bank	XC3S1200E XC3S1600E Pin Name	FG400 Ball	Type
GND	GND	P19	GND
GND	GND	R6	GND
GND	GND	R15	GND
GND	GND	U11	GND
GND	GND	V3	GND
GND	GND	V18	GND
GND	GND	W7	GND
GND	GND	W14	GND
GND	GND	Y1	GND
GND	GND	Y10	GND
GND	GND	Y20	GND
VCCAUX	DONE	V17	CONFIG
VCCAUX	PROG_B	C2	CONFIG
VCCAUX	TCK	D17	JTAG
VCCAUX	TDI	B3	JTAG
VCCAUX	TDO	B19	JTAG
VCCAUX	TMS	E17	JTAG
VCCAUX	VCCAUX	D11	VCCAUX
VCCAUX	VCCAUX	H12	VCCAUX
VCCAUX	VCCAUX	J7	VCCAUX
VCCAUX	VCCAUX	K4	VCCAUX
VCCAUX	VCCAUX	L17	VCCAUX
VCCAUX	VCCAUX	M14	VCCAUX
VCCAUX	VCCAUX	N9	VCCAUX
VCCAUX	VCCAUX	U10	VCCAUX
VCCINT	VCCINT	H9	VCCINT
VCCINT	VCCINT	H11	VCCINT
VCCINT	VCCINT	H13	VCCINT
VCCINT	VCCINT	J8	VCCINT
VCCINT	VCCINT	J10	VCCINT
VCCINT	VCCINT	J12	VCCINT
VCCINT	VCCINT	K9	VCCINT
VCCINT	VCCINT	K11	VCCINT
VCCINT	VCCINT	L10	VCCINT
VCCINT	VCCINT	L12	VCCINT
VCCINT	VCCINT	M9	VCCINT
VCCINT	VCCINT	M11	VCCINT
VCCINT	VCCINT	M13	VCCINT
VCCINT	VCCINT	N8	VCCINT
VCCINT	VCCINT	N10	VCCINT
VCCINT	VCCINT	N12	VCCINT