AMD Xilinx - XC3S250E-5PQG208C Datasheet

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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	612
Number of Logic Elements/Cells	5508
Total RAM Bits	221184
Number of I/O	158
Number of Gates	250000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s250e-5pqg208c

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/01/05	1.0	Initial Xilinx release.
03/21/05	1.1	Added XC3S250E in CP132 package to Table 2. Corrected number of differential I/O pairs for CP132 package. Added package markings for QFP packages (Figure 2) and CP132/CPG132 packages (Figure 4).
11/23/05	2.0	Added differential HSTL and SSTL I/O standards. Updated Table 2 to indicate number of input-only pins. Added Production Stepping information, including example top marking diagrams.
03/22/06	3.0	Upgraded data sheet status to Preliminary. Added XC3S100E in CP132 package and updated I/O counts for the XC3S1600E in FG320 package (Table 2). Added information about dual markings for –5C and –4I product combinations to Package Marking.
11/09/06	3.4	Added 66 MHz PCI support and links to the Xilinx PCI LogiCORE data sheet. Indicated that Stepping 1 parts are Production status. Promoted Module 1 to Production status. Synchronized all modules to v3.4.
04/18/08	3.7	Added XC3S500E VQG100 package. Added reference to XA Automotive version. Updated links.
08/26/09	3.8	Added paragraph to Configuration indicating the device supports MultiBoot configuration. Added package sizes to Table 2. Described the speed grade and temperature range guarantee for devices having a single mark in paragraph 3 under Package Marking. Deleted Pb-Free Packaging example under Ordering Information. Revised information under Production Stepping. Revised description of Table 3.
10/29/12	4.0	Added Notice of Disclaimer. This product is not recommended for new designs. Updated Table 2 footprint size of PQ208.

Notice of Disclaimer

Input Delay Functions

Each IOB has a programmable delay block that optionally delays the input signal. In Figure 6, the signal path has a coarse delay element that can be bypassed. The input signal then feeds a 6-tap delay line. The coarse and tap delays vary; refer to timing reports for specific delay values. All six taps are available via a multiplexer for use as an asynchronous input directly into the FPGA fabric. In this way, the delay is programmable in 12 steps. Three of the six taps are also available via a multiplexer to the D inputs of the synchronous storage elements. The delay inserted in the path to the storage element can be varied in six steps. The first, coarse delay element is common to both asynchronous and synchronous paths, and must be either used or not used for both paths.

The delay values are set up in the silicon once at configuration time—they are non-modifiable in device operation.

The primary use for the input delay element is to adjust the input delay path to ensure that there is no hold time requirement when using the input flip-flop(s) with a global clock. The default value is chosen automatically by the Xilinx software tools as the value depends on device size and the specific device edge where the flip-flop resides. The value set by the Xilinx ISE software is indicated in the Map report generated by the implementation tools, and the resulting effects on input timing are reported using the Timing Analyzer tool.

If the design uses a DCM in the clock path, then the delay element can be safely set to zero because the Delay-Locked Loop (DLL) compensation automatically ensures that there is still no input hold time requirement.

Both asynchronous and synchronous values can be modified, which is useful where extra delay is required on clock or data inputs, for example, in interfaces to various types of RAM.

These delay values are defined through the IBUF_DELAY_VALUE and the IFD_DELAY_VALUE parameters. The default IBUF_DELAY_VALUE is 0, bypassing the delay elements for the asynchronous input. The user can set this parameter to 0-12. The default IFD_DELAY_VALUE is AUTO. IBUF_DELAY_VALUE and IFD_DELAY_VALUE are independent for each input. If the same input pin uses both registered and non-registered input paths, both parameters can be used, but they must both be in the same half of the total delay (both either bypassing or using the coarse delay element).

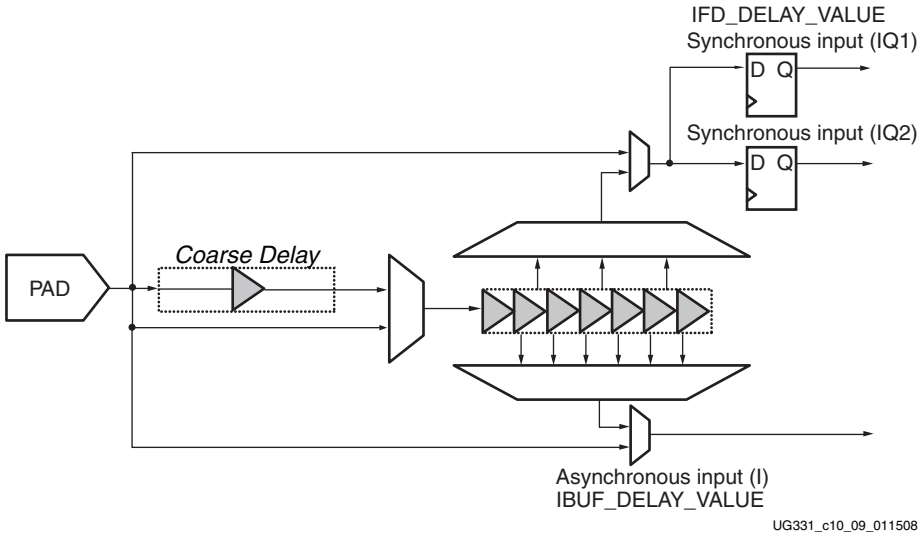


Figure 6: **Programmable Fixed Input Delay Elements**

Storage Element Functions

There are three pairs of storage elements in each IOB, one pair for each of the three paths. It is possible to configure each of these storage elements as an edge-triggered D-type flip-flop (FD) or a level-sensitive latch (LD).

The storage-element pair on either the Output path or the Three-State path can be used together with a special multiplexer to produce Double-Data-Rate (DDR) transmission. This is accomplished by taking data synchronized to the clock signal's rising edge and converting it to bits synchronized on both the rising and the falling edge. The combination of two registers and a multiplexer is referred to as a Double-Data-Rate D-type flip-flop (ODDR2).

Table 4 describes the signal paths associated with the storage element.

Table 4: **Storage Element Signal Description**

Storage Element Signal	Description	Function
D	Data input	Data at this input is stored on the active edge of CK and enabled by CE. For latch operation when the input is enabled, data passes directly to the output Q.
Q	Data output	The data on this output reflects the state of the storage element. For operation as a latch in transparent mode, Q mirrors the data at D.
CK	Clock input	Data is loaded into the storage element on this input's active edge with CE asserted.
CE	Clock Enable input	When asserted, this input enables CK. If not connected, CE defaults to the asserted state.
SR	Set/Reset input	This input forces the storage element into the state specified by the SRHIGH/SRLOW attributes. The SYNC/ASYNC attribute setting determines if the SR input is synchronized to the clock or not. If both SR and REV are active at the same time, the storage element gets a value of 0.
REV	Reverse input	This input is used together with SR. It forces the storage element into the state opposite from what SR does. The SYNC/ASYNC attribute setting determines whether the REV input is synchronized to the clock or not. If both SR and REV are active at the same time, the storage element gets a value of 0.

As shown in Figure 5, the upper registers in both the output and three-state paths share a common clock. The OTCLK1 clock signal drives the CK clock inputs of the upper registers on the output and three-state paths. Similarly, OTCLK2 drives the CK inputs for the lower registers on the output and three-state paths. The upper and lower registers on the input path have independent clock lines: ICLK1 and ICLK2.

The OCE enable line controls the CE inputs of the upper and lower registers on the output path. Similarly, TCE controls the CE inputs for the register pair on the three-state path and ICE does the same for the register pair on the input path.

The Set/Reset (SR) line entering the IOB controls all six registers, as is the Reverse (REV) line.

In addition to the signal polarity controls described in IOB Overview, each storage element additionally supports the controls described in Table 5.

Table 5: **Storage Element Options**

Option Switch	Function	Specificity
FF/Latch	Chooses between an edge-triggered flip-flop or a level-sensitive latch	Independent for each storage element
SYNC/ASYNC	Determines whether the SR set/reset control is synchronous or asynchronous	Independent for each storage element
SRHIGH/SRLOW	Determines whether SR acts as a Set, which forces the storage element to a logic 1 (SRHIGH) or a Reset, which forces a logic 0 (SRLOW)	Independent for each storage element, except when using ODDR2. In the latter case, the selection for the upper element will apply to both elements.
INIT1/INIT0	When Global Set/Reset (GSR) is asserted or after configuration this option specifies the initial state of the storage element, either set (INIT1) or reset (INIT0). By default, choosing SRLOW also selects INIT0; choosing SRHIGH also selects INIT1.	Independent for each storage element, except when using ODDR2, which uses two IOBs. In the ODDR2 case, selecting INIT0 for one IOBs applies to both elements within the IOB, although INIT1 could be selected for the elements in the other IOB.

initialized distributed RAM contents are not disturbed during the configuration process.

The distributed RAM is useful for smaller amounts of memory. Larger memory requirements can use the dedicated 18Kbit RAM blocks (see Block RAM).

Shift Registers

For additional information, refer to the “Using Look-Up Tables as Shift Registers (SRL16)” chapter in UG331.

It is possible to program each SLICEM LUT as a 16-bit shift register (see Figure 28). Used in this way, each LUT can delay serial data anywhere from 1 to 16 clock cycles without using any of the dedicated flip-flops. The resulting programmable delays can be used to balance the timing of data pipelines.

The SLICEM LUTs cascade from the G-LUT to the F-LUT through the DIFMUX (see Figure 15). SHIFTIN and SHIFTOUT lines cascade a SLICEM to the SLICEM below to form larger shift registers. The four SLICEM LUTs of a single CLB can be combined to produce delays up to 64 clock cycles. It is also possible to combine shift registers across more than one CLB.

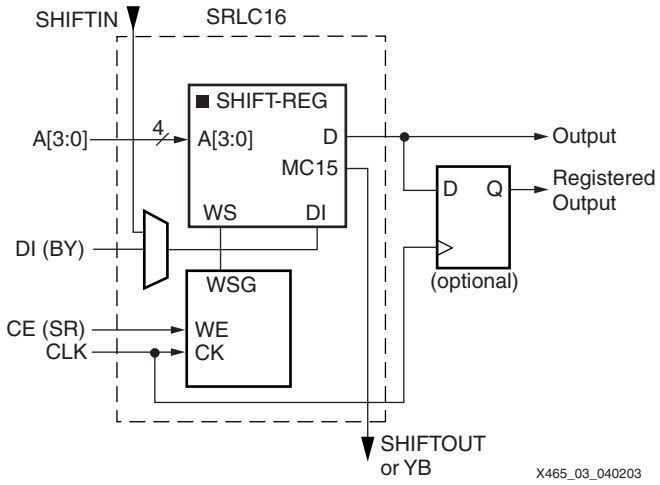


Figure 28: **Logic Cell SRL16 Structure**

Each shift register provides a shift output MC15 for the last bit in each LUT, in addition to providing addressable access to any bit in the shift register through the normal D output. The address inputs A[3:0] are the same as the distributed RAM address lines, which come from the LUT inputs F[4:1] or G[4:1]. At the end of the shift register, the CLB flip-flop can be used to provide one more shift delay for the addressable bit.

The shift register element is known as the SRL16 (Shift Register LUT 16-bit), with a ‘C’ added to signify a cascade ability (Q15 output) and ‘E’ to indicate a Clock Enable. See Figure 29 for an example of the SRLC16E component.

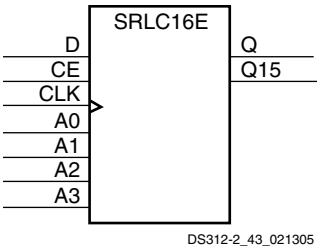


Figure 29: **SRL16 Shift Register Component with Cascade and Clock Enable**

The functionality of the shift register is shown in Table 20. The SRL16 shifts on the rising edge of the clock input when the Clock Enable control is High. This shift register cannot be initialized either during configuration or during operation except by shifting data into it. The clock enable and clock inputs are shared between the two LUTs in a SLICEM. The clock enable input is automatically kept active if unused.

Table 20: **SRL16 Shift Register Function**

Inputs				Outputs	
Am	**CLK**	**CE**	**D**	**Q**	**Q15**
Am	X	0	X	Q[Am]	Q[15]
Am	↑	1	D	Q[Am-1]	Q[15]

Notes:

1. m = 0, 1, 2, 3.

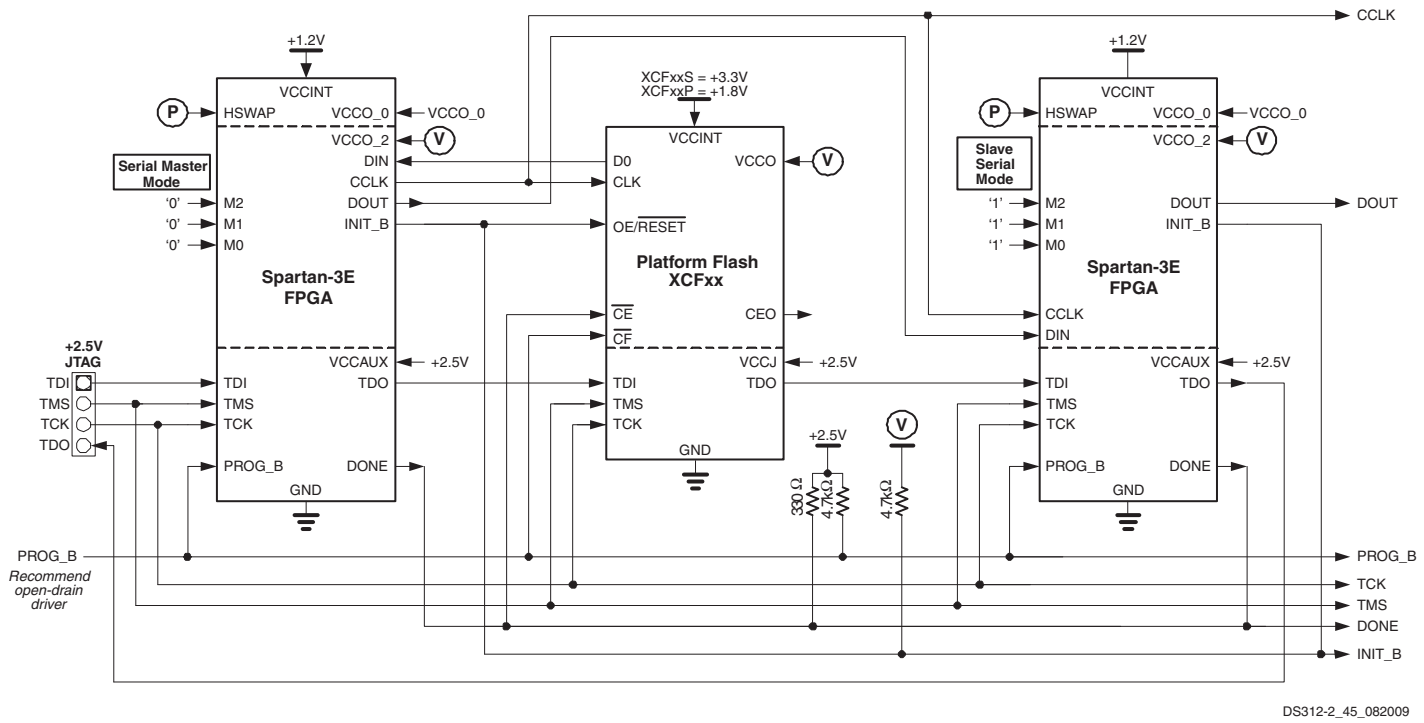


Figure 52: **Daisy-Chaining from Master Serial Mode**

Daisy-Chaining

If the application requires multiple FPGAs with different configurations, then configure the FPGAs using a daisy chain, as shown in Figure 52. Use Master Serial mode (M[2:0] = <0:0:0>) for the FPGA connected to the Platform Flash PROM and Slave Serial mode (M[2:0] = <1:1:1>) for all other FPGAs in the daisy-chain. After the master FPGA—the FPGA on the left in the diagram—finishes loading its configuration data from the Platform Flash, the master device supplies data using its DOUT output pin to the next device in the daisy-chain, on the falling CCLK edge.

JTAG Interface

Both the Spartan-3E FPGA and the Platform Flash PROM have a four-wire IEEE 1149.1/1532 JTAG port. Both devices share the TCK clock input and the TMS mode select input. The devices may connect in either order on the JTAG chain with the TDO output of one device feeding the TDI input of the following device in the chain. The TDO output of the last device in the JTAG chain drives the JTAG connector.

The JTAG interface on Spartan-3E FPGAs is powered by the 2.5V V_{CCAUX} supply. Consequently, the PROM's V_{CCJ} supply input must also be 2.5V. To create a 3.3V JTAG interface, please refer to application note XAPP453: *The 3.3V Configuration of Spartan-3 FPGAs* for additional information.

In-System Programming Support

Both the FPGA and the Platform Flash PROM are in-system programmable via the JTAG chain. Download support is provided by the Xilinx iMPACT programming software and the associated Xilinx Parallel Cable IV or Platform Cable USB programming cables.

Storing Additional User Data in Platform Flash

After configuration, the FPGA application can continue to use the Master Serial interface pins to communicate with the Platform Flash PROM. If desired, use a larger Platform Flash PROM to hold additional non-volatile application data, such as MicroBlaze processor code, or other user data such as serial numbers and Ethernet MAC IDs. The FPGA first configures from Platform Flash PROM. Then using FPGA logic after configuration, the FPGA copies MicroBlaze code from Platform Flash into external DDR SDRAM for code execution.

See XAPP694: *Reading User Data from Configuration PROMs* and XAPP482: *MicroBlaze Platform Flash/PROM Boot Loader and User Data Storage* for specific details on how to implement such an interface.

SPI Serial Flash Mode

For additional information, refer to the “Master SPI Mode” chapter in UG332.

In SPI Serial Flash mode (M[2:0] = <0:0:1>), the Spartan-3E FPGA configures itself from an attached industry-standard SPI serial Flash PROM, as illustrated in Figure 53 and Figure 54. The FPGA supplies the CCLK output clock from its internal oscillator to the clock input of the attached SPI Flash PROM.

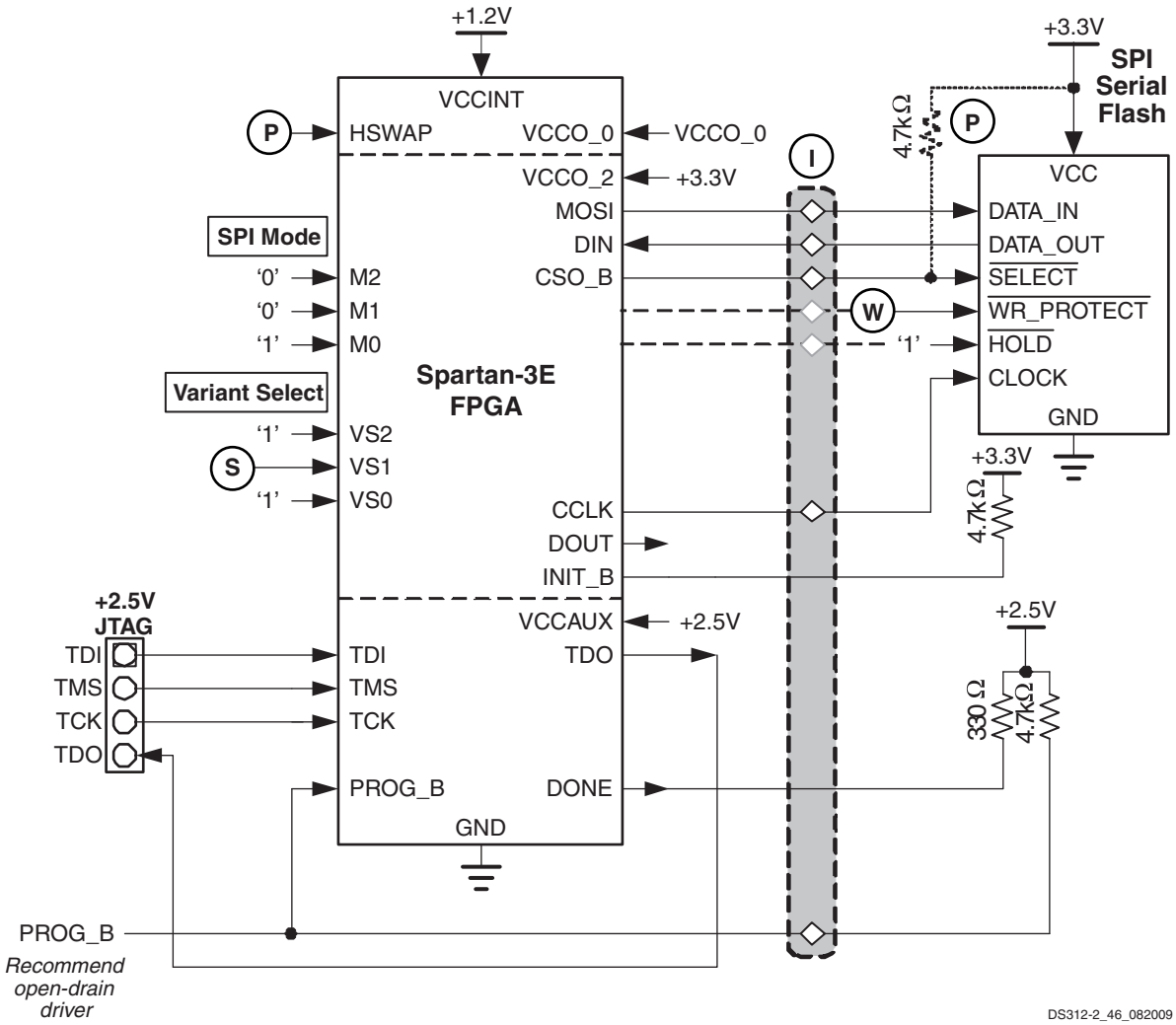


Figure 53: **SPI Flash PROM Interface for PROMs Supporting READ (0x03) and FAST_READ (0x0B) Commands**

Ⓢ Although SPI is a standard four-wire interface, various available SPI Flash PROMs use different command protocols. The FPGA’s variant select pins, VS[2:0], define how the FPGA communicates with the SPI Flash, including which SPI Flash command the FPGA issues to start the read operation and the number of dummy bytes inserted before the FPGA expects to receive valid data from the SPI Flash. Table 53 shows the available SPI Flash PROMs expected to operate with Spartan-3E FPGAs. Other compatible devices might work but have not been tested for suitability with Spartan-3E FPGAs. All other VS[2:0] values are reserved for future use. Consult the data sheet for the desired SPI Flash device to determine its suitability. The basic timing requirements and waveforms are provided in Serial Peripheral Interface (SPI) Configuration Timing in Module 3.

Figure 53 shows the general connection diagram for those SPI Flash PROMs that support the 0x03 READ command or the 0x0B FAST READ commands.

Figure 54 shows the connection diagram for Atmel DataFlash serial PROMs, which also use an SPI-based protocol. ‘B’-series DataFlash devices are limited to FPGA applications operating over the commercial temperature range. Industrial temperature range applications must use ‘C’- or ‘D’-series DataFlash devices, which have a shorter DataFlash select setup time, because of the faster FPGA CCLK frequency at cold temperatures.

Daisy-Chaining

If the application requires multiple FPGAs with different configurations, then configure the FPGAs using a daisy chain, as shown in Figure 57. Daisy-chaining from a single SPI serial Flash PROM is supported in Stepping 1 devices. It is not supported in Stepping 0 devices. Use SPI Flash mode (M[2:0] = <0:0:1>) for the FPGA connected to the Platform Flash PROM and Slave Serial mode (M[2:0] = <1:1:1>) for all other FPGAs in the daisy-chain. After the master FPGA—the FPGA on the left in the diagram—finishes loading its configuration data from the SPI Flash PROM, the master device uses its DOUT output pin to supply data to the next device in the daisy-chain, on the falling CCLK edge.

Design Note

SPI mode daisy chains are supported only in Stepping 1 silicon versions.

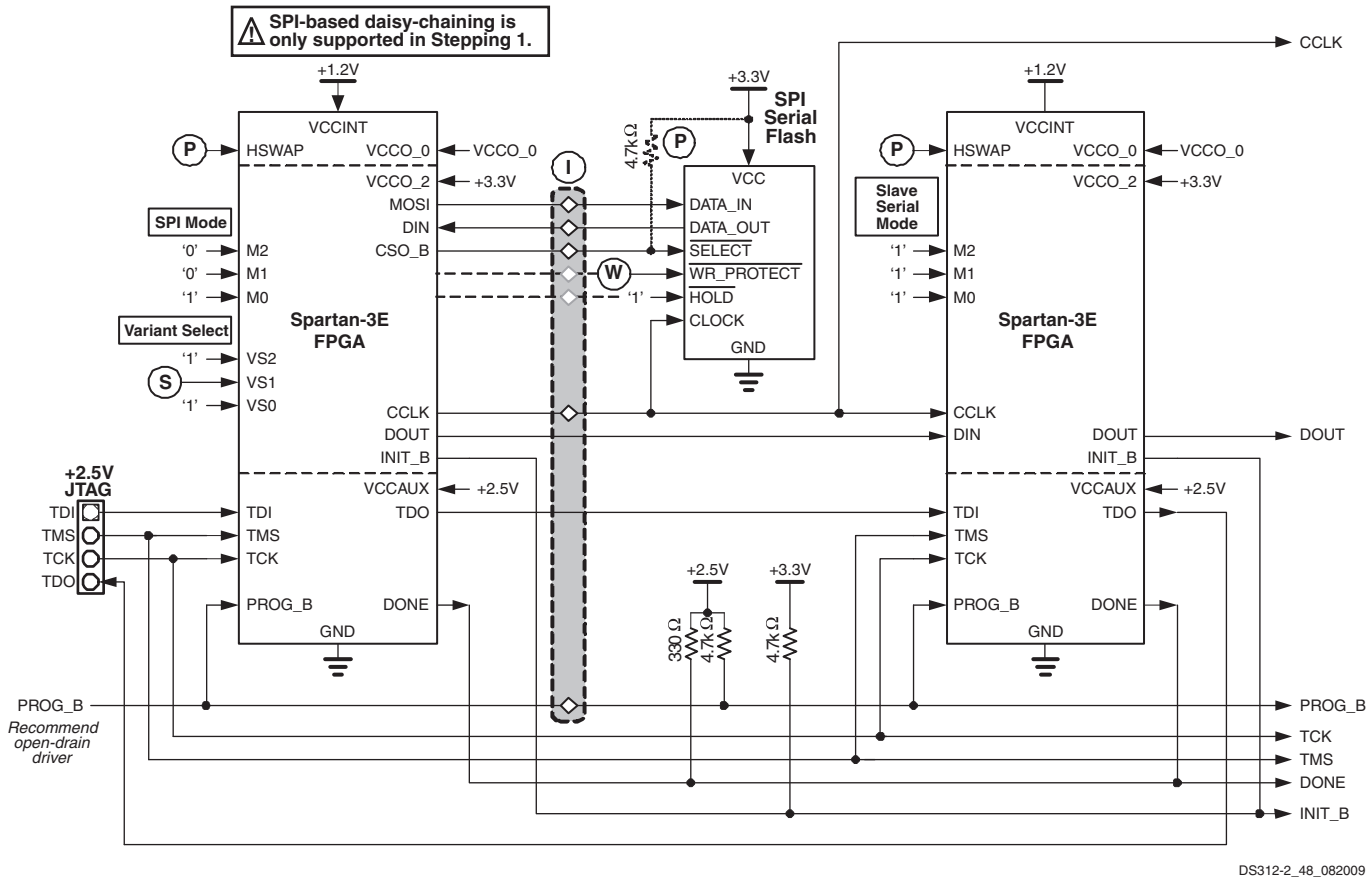


Figure 57: **Daisy-Chaining from SPI Flash Mode (Stepping 1)**

Programming Support

For successful daisy-chaining, the ***DONE_cycle*** configuration option must be set to cycle 5 or sooner. The default cycle is 4. See Table 69 and the Start-Up section for additional information.

(I) In production applications, the SPI Flash PROM is usually pre-programmed before it is mounted on the printed circuit board. The Xilinx ISE development software produces industry-standard programming files that can be used with third-party gang programmers. Consult your specific SPI Flash vendor for recommended production programming solutions.

In-system programming support is available from some third-party PROM programmers using a socket adapter with attached wires. To gain access to the SPI Flash signals, drive the FPGA's PROG_B input Low with an open-drain driver. This action places all FPGA I/O pins, including those attached to the SPI Flash, in high-impedance (Hi-Z). If the HSWAP input is Low, the I/Os have pull-up resistors to the V_{CCO} input on their respective I/O bank. The external programming hardware then has direct access to the SPI Flash pins. The programming access points are highlighted in the gray box in Figure 53, Figure 54, and Figure 57.

Beginning with the Xilinx ISE 8.2i software release, the iMPACT programming utility provides direct, in-system prototype programming support for STMicro M25P-series

This addressing flexibility allows the FPGA to share the parallel Flash PROM with an external or embedded processor. Depending on the specific processor architecture, the processor boots either from the top or bottom of memory. The FPGA is flexible and boots from the opposite end of memory from the processor. Only the processor or the FPGA can boot at any given time. The FPGA can configure first, holding the processor in reset or the processor can boot first, asserting the FPGA's PROG_B pin.

The mode select pins, M[2:0], are sampled when the FPGA's INIT_B output goes High and must be at defined logic levels during this time. After configuration, when the FPGA's DONE output goes High, the mode pins are available as full-featured user-I/O pins.

(P) Similarly, the FPGA's HSWAP pin must be Low to enable pull-up resistors on all user-I/O pins or High to disable the pull-up resistors. The HSWAP control must remain at a constant logic level throughout FPGA configuration. After configuration, when the FPGA's DONE output goes High, the HSWAP pin is available as full-featured user-I/O pin and is powered by the VCCO_0 supply.

The RDWR_B and CSI_B must be Low throughout the configuration process. After configuration, these pins also become user I/O.

In a single-FPGA application, the FPGA's CSO_B and CCLK pins are not used but are actively driving during the configuration process. The BUSY pin is not used but also actively drives during configuration and is available as a user I/O after configuration.

After configuration, all of the interface pins except DONE and PROG_B are available as user I/Os. Furthermore, the bidirectional SelectMAP configuration peripheral interface (see Slave Parallel Mode) is available after configuration. To continue using SelectMAP mode, set the ***Persist*** bitstream generator option to ***Yes***. An external host can then read and verify configuration data.

The Persist option will maintain A20-A23 as configuration pins although they are not used in SelectMAP mode.

Table 59: **Byte-Wide Peripheral Interface (BPI) Connections**

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
HSWAP (P)	Input	**User I/O Pull-Up Control**. When Low during configuration, enables pull-up resistors in all I/O pins to respective I/O bank V_{CCO} input. 0: Pull-ups during configuration 1: No pull-ups	Drive at valid logic level throughout configuration.	User I/O
M[2:0] (A)	Input	**Mode Select**. Selects the FPGA configuration mode. See Design Considerations for the HSWAP, M[2:0], and VS[2:0] Pins.	M2 = 0, M1 = 1. Set M0 = 0 to start at address 0, increment addresses. Set M0 = 1 to start at address 0xFFFFFF and decrement addresses. Sampled when INIT_B goes High.	User I/O
CSI_B	Input	**Chip Select Input**. Active Low.	Must be Low throughout configuration.	User I/O. If bitstream option ***Persist=Yes***, becomes part of SelectMap parallel peripheral interface.
RDWR_B	Input	**Read/Write Control**. Active Low write enable. Read functionality typically only used after configuration, if bitstream option ***Persist=Yes***.	Must be Low throughout configuration.	User I/O. If bitstream option ***Persist=Yes***, becomes part of SelectMap parallel peripheral interface.
LDC0	Output	PROM Chip Enable	Connect to PROM chip-select input (CE#). FPGA drives this signal Low throughout configuration.	User I/O. If the FPGA does not access the PROM after configuration, drive this pin High to deselect the PROM. A[23:0], D[7:0], LDC[2:1], and HDC then become available as user I/O.
LDC1	Output	PROM Output Enable	Connect to the PROM output-enable input (OE#). The FPGA drives this signal Low throughout configuration.	User I/O

Table 59: **Byte-Wide Peripheral Interface (BPI) Connections *(Cont'd)***

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
DONE	Open-drain bidirectional I/O	**FPGA Configuration Done**. Low during configuration. Goes High when FPGA successfully completes configuration. Requires external 330 Ω pull-up resistor to 2.5V.	Low indicates that the FPGA is not yet configured.	Pulled High via external pull-up. When High, indicates that the FPGA is successfully configured.
PROG_B	Input	**Program FPGA**. Active Low. When asserted Low for 500 ns or longer, forces the FPGA to restart its configuration process by clearing configuration memory and resetting the DONE and INIT_B pins once PROG_B returns High. Recommend external 4.7 kΩ pull-up resistor to 2.5V. Internal pull-up value may be weaker (see Table 78). If driving externally with a 3.3V output, use an open-drain or open-collector driver or use a current limiting series resistor.	Must be High to allow configuration to start.	Drive PROG_B Low and release to reprogram FPGA. Hold PROG_B to force FPGA I/O pins into Hi-Z, allowing direct programming access to Flash PROM pins.

Voltage Compatibility

The FPGA's parallel Flash interface signals are within I/O Banks 1 and 2. The majority of parallel Flash PROMs use a single 3.3V supply voltage. Consequently, in most cases, the FPGA's VCCO_1 and VCCO_2 supply voltages must also be 3.3V to match the parallel Flash PROM. There are some 1.8V parallel Flash PROMs available and the FPGA interfaces with these devices if the VCCO_1 and VCCO_2 supplies are also 1.8V.

Power-On Precautions if PROM Supply is Last in Sequence

Like SPI Flash PROMs, parallel Flash PROMs typically require some amount of internal initialization time when the supply voltage reaches its minimum value.

The PROM supply voltage also connects to the FPGA's VCCO_2 supply input. In many systems, the PROM supply feeding the FPGA's VCCO_2 input is valid before the FPGA's other V_{CCINT} and V_{CCAUX} supplies, and consequently, there is no issue. However, if the PROM supply is last in the sequence, a potential race occurs between the FPGA and the parallel Flash PROM. See Power-On Precautions if 3.3V Supply is Last in Sequence for a similar description of the issue for SPI Flash PROMs.

Supported Parallel NOR Flash PROM Densities

Table 60 indicates the smallest usable parallel Flash PROM to program a single Spartan-3E FPGA. Parallel Flash density is specified in bits but addressed as bytes. The FPGA presents up to 24 address lines during configuration but not all are required for single FPGA applications. Table 60 shows the minimum required number of address lines between the FPGA and parallel Flash PROM. The actual number of address line required depends on the density of the attached parallel Flash PROM.

A multiple-FPGA daisy-chained application requires a parallel Flash PROM large enough to contain the sum of the FPGA file sizes. An application can also use a larger-density parallel Flash PROM to hold additional data beyond just FPGA configuration data. For example, the parallel Flash PROM can also contain the application code for a MicroBlaze RISC processor core implemented within the Spartan-3E FPGA. After configuration, the MicroBlaze processor can execute directly from external Flash or can copy the code to other, faster system memory before executing the code.

Table 60: **Number of Bits to Program a Spartan-3E FPGA and Smallest Parallel Flash PROM**

Spartan-3E FPGA	Uncompressed File Sizes (bits)	Smallest Usable Parallel Flash PROM	Minimum Required Address Lines
XC3S100E	581,344	1 Mbit	A[16:0]
XC3S250E	1,353,728	2 Mbit	A[17:0]
XC3S500E	2,270,208	4 Mbit	A[18:0]
XC3S1200E	3,841,184	4 Mbit	A[18:0]
XC3S1600E	5,969,696	8 Mbit	A[19:0]

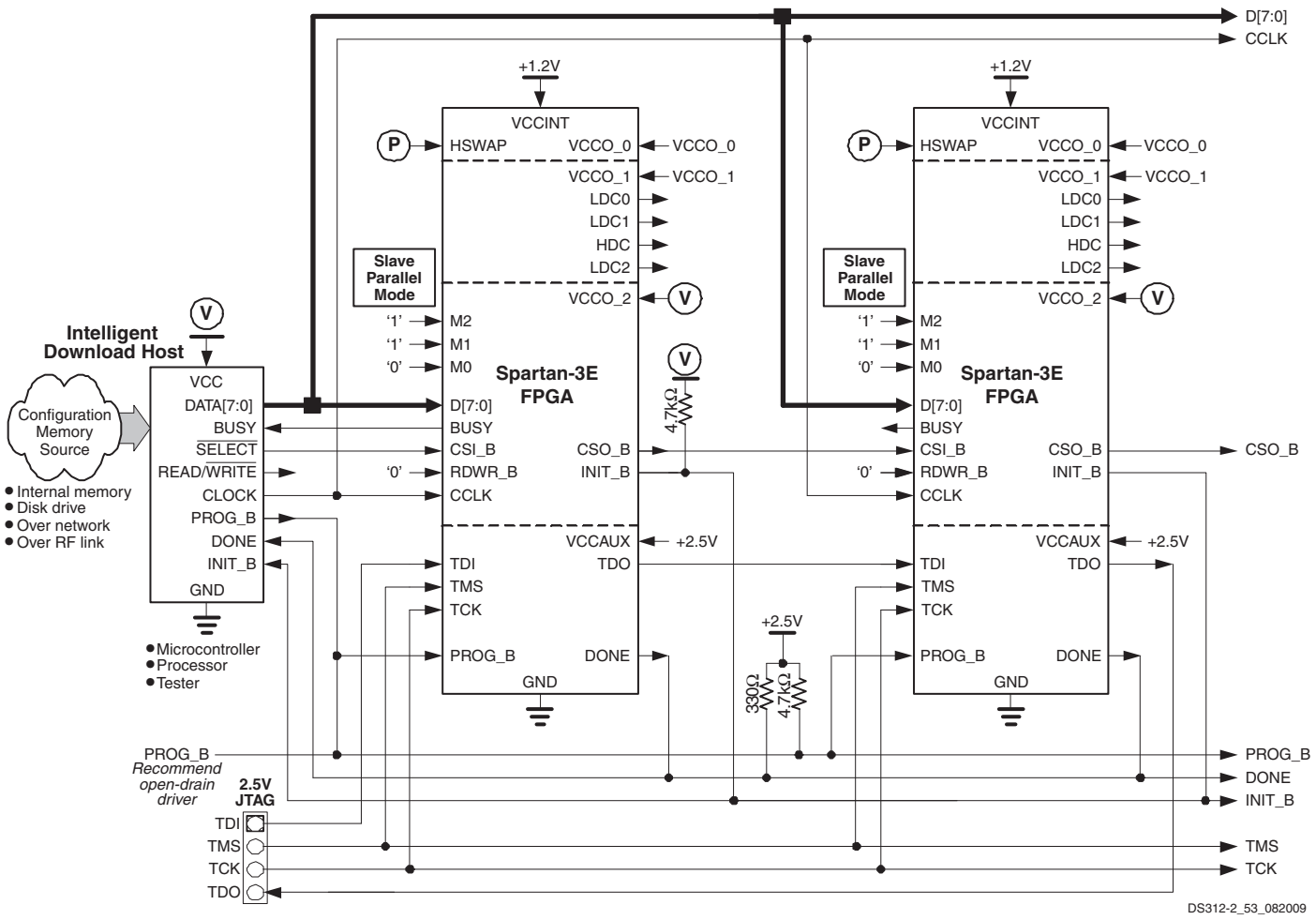


Figure 62: **Daisy-Chaining using Slave Parallel Mode**

Slave Serial Mode

For additional information, refer to the “Slave Serial Mode” chapter in UG332.

In Slave Serial mode (M[2:0] = <1:1:1>), an external host such as a microprocessor or microcontroller writes serial configuration data into the FPGA, using the synchronous serial interface shown in Figure 63. The serial configuration data is presented on the FPGA’s DIN input pin with sufficient setup time before each rising edge of the externally generated CCLK clock input.

The intelligent host starts the configuration process by pulsing PROG_B and monitoring that the INIT_B pin goes High, indicating that the FPGA is ready to receive its first data. The host then continues supplying data and clock signals until either the DONE pin goes High, indicating a successful configuration, or until the INIT_B pin goes Low, indicating a configuration error. The configuration process requires more clock cycles than indicated from the configuration file size. Additional clocks are required during the FPGA’s start-up sequence, especially if the FPGA is programmed to wait for selected Digital Clock Managers (DCMs) to lock to their respective clock inputs (see Start-Up, page 105).

Maximum Bitstream Size for Daisy-Chains

The maximum bitstream length supported by Spartan-3E FPGAs in serial daisy-chains is 4,294,967,264 bits (4 Gbits), roughly equivalent to a daisy-chain with 720 XC3S1600E FPGAs. This is a limit only for serial daisy-chains where configuration data is passed via the FPGA's DOUT pin. There is no such limit for JTAG chains.

Configuration Sequence

For additional information including I/O behavior before and during configuration, refer to the "Sequence of Events" chapter in UG332.

The Spartan-3E configuration process is three-stage process that begins after the FPGA powers on (a POR event) or after the PROG_B input is asserted. Power-On Reset (POR) occurs after the V_{CCINT}, V_{CCAUX}, and the V_{CCO} Bank 2 supplies reach their respective input threshold levels. After either a POR or PROG_B event, the three-stage configuration process begins.

1. The FPGA clears (initializes) the internal configuration memory.
2. Configuration data is loaded into the internal memory.
3. The user-application is activated by a start-up process.

Figure 66 is a generalized block diagram of the Spartan-3E configuration logic, showing the interaction of different device inputs and Bitstream Generator (BitGen) options. A flow diagram for the configuration sequence of the Serial and Parallel modes appears in Figure 66. Figure 67 shows the Boundary-Scan or JTAG configuration sequence.

Initialization

Configuration automatically begins after power-on or after asserting the FPGA PROG_B pin, unless delayed using the FPGA's INIT_B pin. The FPGA holds the open-drain INIT_B signal Low while it clears its internal configuration memory. Externally holding the INIT_B pin Low forces the configuration sequencer to wait until INIT_B again goes High.

The FPGA signals when the memory-clearing phase is complete by releasing the open-drain INIT_B pin, allowing the pin to go High via the external pull-up resistor to VCCO_2.

Loading Configuration Data

After initialization, configuration data is written to the FPGA's internal memory. The FPGA holds the Global Set/Reset (GSR) signal active throughout configuration, holding all FPGA flip-flops in a reset state. The FPGA signals when the entire configuration process completes by releasing the DONE pin, allowing it to go High.

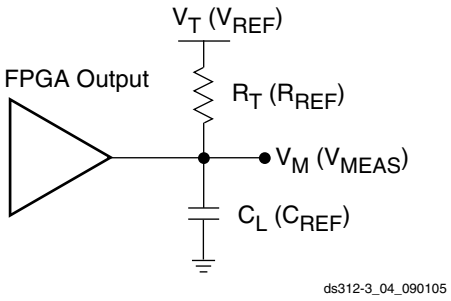
The FPGA configuration sequence can also be initiated by asserting PROG_B. Once released, the FPGA begins clearing its internal configuration memory, and progresses through the remainder of the configuration process.

Timing Measurement Methodology

When measuring timing parameters at the programmable I/Os, different signal standards call for different test conditions. Table 95 lists the conditions to use for each standard.

The method for measuring Input timing is as follows: A signal that swings between a Low logic level of V_L and a High logic level of V_H is applied to the Input under test. Some standards also require the application of a bias voltage to the V_{REF} pins of a given bank to properly set the input-switching threshold. The measurement point of the Input signal (V_M) is commonly located halfway between V_L and V_H.

The Output test setup is shown in Figure 72. A termination voltage V_T is applied to the termination resistor R_T, the other end of which is connected to the Output. For each standard, R_T and V_T generally take on the standard values recommended for minimizing signal reflections. If the standard does not ordinarily use terminations (e.g., LVCMOS, LVTTL), then R_T is set to 1MΩ to indicate an open connection, and V_T is set to zero. The same measurement point (V_M) that was used at the Input is also used at the Output.



Notes:

1. The names shown in parentheses are used in the IBIS file.

Figure 72: **Output Test Setup**

Table 95: **Test Methods for Timing Measurement at I/Os**

Signal Standard (IOSTANDARD)		Inputs			Outputs		Inputs and Outputs
		V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
Single-Ended							
LVTTL		-	0	3.3	1M	0	1.4
LVCMOS33		-	0	3.3	1M	0	1.65
LVCMOS25		-	0	2.5	1M	0	1.25
LVCMOS18		-	0	1.8	1M	0	0.9
LVCMOS15		-	0	1.5	1M	0	0.75
LVCMOS12		-	0	1.2	1M	0	0.6
PCI33_3	Rising	-	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
PCI66_3	Rising	-	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
HSTL_I_18		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
HSTL_III_18		1.1	V_{REF} – 0.5	V_{REF} + 0.5	50	1.8	V_{REF}
SSTL18_I		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
SSTL2_I		1.25	V_{REF} – 0.75	V_{REF} + 0.75	50	1.25	V_{REF}
Differential							
LVDS_25		-	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
BLVDS_25		-	V_{ICM} – 0.125	V_{ICM} + 0.125	1M	0	V_{ICM}
MINI_LVDS_25		-	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
LVPECL_25		-	V_{ICM} – 0.3	V_{ICM} + 0.3	1M	0	V_{ICM}
RSDS_25		-	V_{ICM} – 0.1	V_{ICM} + 0.1	50	1.2	V_{ICM}

Package Thermal Characteristics

The power dissipated by an FPGA application has implications on package selection and system design. The power consumed by a Spartan-3E FPGA is reported using either the XPower Estimator or the XPower Analyzer calculator integrated in the Xilinx ISE® development software. Table 130 provides the thermal characteristics for the various Spartan-3E package offerings.

The junction-to-case thermal resistance (θ_{JC}) indicates the difference between the temperature measured on the package body (case) and the die junction temperature per watt of power consumption. The junction-to-board (θ_{JB}) value similarly reports the difference between the board and junction temperature. The junction-to-ambient (θ_{JA}) value reports the temperature difference per watt between the ambient environment and the junction temperature. The θ_{JA} value is reported at different air velocities, measured in linear feet per minute (LFM). The Still Air (0 LFM) column shows the θ_{JA} value in a system without a fan. The thermal resistance drops with increasing air flow.

Table 130: **Spartan-3E Package Thermal Characteristics**

Device	Package	Junction-to-Case (θ_{JC})	Junction-to-Board (θ_{JB})	Junction-to-Ambient (θ_{JA}) at Different Air Flows				Units
				Still Air (0 LFM)	250 LFM	500 LFM	750 LFM	
XC3S100E	VQ100	13.0	30.9	49.0	40.7	37.9	37.0	°C/Watt
XC3S250E		11.0	25.9	43.3	36.0	33.6	32.7	°C/Watt
XC3S500E		9.8		40.0	33.3	31.0	30.2	°C/Watt
XC3S100E	CP132	19.3	42.0	62.1	55.3	52.8	51.2	°C/Watt
XC3S250E		11.8	28.1	48.3	41.8	39.5	38.0	°C/Watt
XC3S500E		8.5	21.3	41.5	35.2	32.9	31.5	°C/Watt
XC3S100E	TQ144	8.2	31.9	52.1	40.5	34.6	32.5	°C/Watt
XC3S250E		7.2	25.7	37.6	29.2	25.0	23.4	°C/Watt
XC3S250E	PQ208	9.8	29.0	37.0	27.3	24.1	22.4	°C/Watt
XC3S500E		8.5	26.8	36.1	26.6	23.6	21.8	°C/Watt
XC3S250E	FT256	12.4	27.7	35.8	29.3	28.4	28.1	°C/Watt
XC3S500E		9.6	22.2	31.1	25.0	24.0	23.6	°C/Watt
XC3S1200E		6.5	16.4	26.2	20.5	19.3	18.9	°C/Watt
XC3S500E	FG320	9.8	15.6	26.1	20.6	19.4	18.6	°C/Watt
XC3S1200E		8.2	12.5	23.0	17.7	16.4	15.7	°C/Watt
XC3S1600E		7.1	10.6	21.1	15.9	14.6	13.8	°C/Watt
XC3S1200E	FG400	7.5	12.4	22.3	17.2	16.0	15.3	°C/Watt
XC3S1600E		6.0	10.4	20.3	15.2	14.0	13.3	°C/Watt
XC3S1600E	FG484	5.7	9.4	18.8	12.5	11.3	10.8	°C/Watt

Table 131: **VQ100 Package Pinout *(Cont'd)***

Bank	XC3S100E XC3S250E XC3S500E Pin Name	VQ100 Pin Number	Type
3	IO_L02P_3	P4	I/O
3	IO_L03N_3/LHCLK1	P10	LHCLK
3	IO_L03P_3/LHCLK0	P9	LHCLK
3	IO_L04N_3/LHCLK3	P12	LHCLK
3	IO_L04P_3/LHCLK2	P11	LHCLK
3	IO_L05N_3/LHCLK5	P16	LHCLK
3	IO_L05P_3/LHCLK4	P15	LHCLK
3	IO_L06N_3/LHCLK7	P18	LHCLK
3	IO_L06P_3/LHCLK6	P17	LHCLK
3	IO_L07N_3	P23	I/O
3	IO_L07P_3	P22	I/O
3	IP	P13	INPUT
3	VCCO_3	P8	VCCO
3	VCCO_3	P20	VCCO
GND	GND	P7	GND
GND	GND	P14	GND
GND	GND	P19	GND
GND	GND	P29	GND
GND	GND	P37	GND
GND	GND	P52	GND
GND	GND	P59	GND
GND	GND	P64	GND
GND	GND	P72	GND
GND	GND	P81	GND
GND	GND	P87	GND
GND	GND	P93	GND
VCCAUX	DONE	P51	CONFIG
VCCAUX	PROG_B	P1	CONFIG
VCCAUX	TCK	P77	JTAG
VCCAUX	TDI	P100	JTAG
VCCAUX	TDO	P76	JTAG
VCCAUX	TMS	P75	JTAG
VCCAUX	VCCAUX	P21	VCCAUX
VCCAUX	VCCAUX	P46	VCCAUX
VCCAUX	VCCAUX	P74	VCCAUX
VCCAUX	VCCAUX	P96	VCCAUX
VCCINT	VCCINT	P6	VCCINT
VCCINT	VCCINT	P28	VCCINT
VCCINT	VCCINT	P56	VCCINT
VCCINT	VCCINT	P80	VCCINT

FT256 Footprint

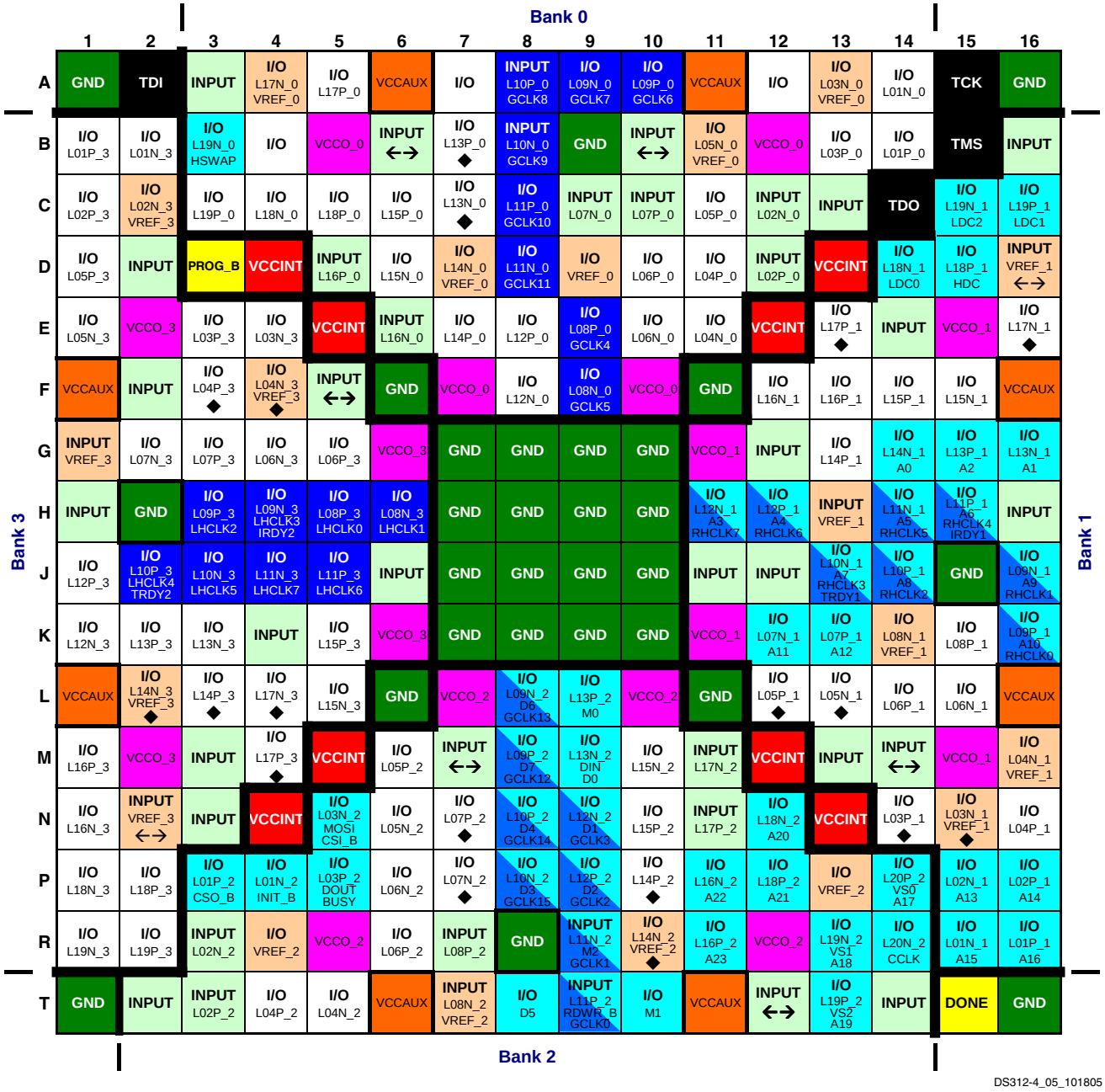


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Figure 85: **FT256 Package Footprint (top view)**

2	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	8	**VCCINT:** Internal core supply voltage (+1.2V)
28	**GND:** Ground	16	**VCCO:** Output voltage supply for bank	8	**VCCAUX:** Auxiliary supply voltage (+2.5V)
6 ↔	**Migration Difference:** For flexible package migration, use these pins as inputs.	18 (◆)	Unconnected pins on XC3S250E		

User I/Os by Bank

Table 149 and Table 150 indicate how the available user-I/O pins are distributed between the four I/O banks on the FG320 package.

Table 149: **User I/Os Per Bank for XC3S500E in the FG320 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF(1)	CLK(2)
Top	0	58	29	14	1	6	8
Right	1	58	22	10	21	5	0(2)
Bottom	2	58	17	13	24	4	0(2)
Left	3	58	34	11	0	5	8
TOTAL		**232**	**102**	**48**	**46**	**20**	**16**

Notes:

1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

Table 150: **User I/Os Per Bank for XC3S1200E and XC3S1600E in the FG320 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF(1)	CLK(2)
Top	0	61	34	12	1	6	8
Right	1	63	25	12	21	5	0(2)
Bottom	2	63	23	11	24	5	0(2)
Left	3	63	38	12	0	5	8
TOTAL		**250**	**120**	**47**	**46**	**21**	**16**

Notes:

1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

FG400 Footprint

Left Half of Package (top view)

156 **I/O:** Unrestricted, general-purpose user I/O

62 **INPUT:** Unrestricted, general-purpose input pin

46 **DUAL:** Configuration pin, then possible user I/O

24 **VREF:** User I/O or input voltage reference for bank

16 **CLK:** User I/O, input, or clock buffer input

2 **CONFIG:** Dedicated configuration pins

4 **JTAG:** Dedicated JTAG port pins

42 **GND:** Ground

24 **VCCO:** Output voltage supply for bank

16 **VCCINT:** Internal core supply voltage (+1.2V)

8 **VCCAUX:** Auxiliary supply voltage (+2.5V)

0 **N.C.:** Not connected

Bank 0

	1	2	3	4	5	6	7	8	9	10
A	GND	I/O L31N_0	I/O	INPUT L29N_0	INPUT L29P_0	I/O L25N_0	I/O L25P_0	I/O	I/O L18N_0 GCLK11	I/O L18P_0 GCLK10
B	I/O L03P_3	I/O L31P_0	TDI	VCCO_0	I/O L27N_0	I/O L27P_0	GND	I/O L22N_0 VREF_0	I/O L22P_0	VCCO_0
C	I/O L03N_3	PROG_B	GND	I/O L32P_0	I/O L30N_0 VREF_0	I/O L28P_0	I/O	INPUT L23N_0	I/O L21N_0	I/O
D	I/O L04P_3	I/O L01N_3	I/O L01P_3	I/O L32N_0 HSWAP	I/O L30P_0	I/O L28N_0	VCCO_0	INPUT L23P_0	I/O L21P_0	GND
E	I/O L04N_3	VCCO_3	I/O L02N_3 VREF_3	I/O L02P_3	INPUT	INPUT L26N_0	INPUT L26P_0	I/O	I/O L19P_0	I/O L16N_0 GCLK7
F	I/O L06N_3	I/O L06P_3	I/O L05N_3	I/O L05P_3	INPUT	GND	I/O L24N_0 VREF_0	I/O L24P_0	I/O L19N_0	VCCO_0
G	INPUT	GND	I/O L07P_3	I/O L07N_3	I/O L08N_3	INPUT	I/O	INPUT L20P_0	INPUT L20N_0	INPUT L17N_0 GCLK9
H	INPUT	I/O L09P_3	I/O L09N_3 VREF_3	VCCO_3	I/O L08P_3	I/O L10P_3	I/O L10N_3	GND	VCCINT	INPUT L17P_0 GCLK8
J	I/O L12N_3	I/O L12P_3	I/O L11P_3	I/O L11N_3	INPUT	I/O L13N_3	VCCAUX	VCCINT	GND	VCCINT
K	GND	I/O L14N_3 LHCLK1	I/O L14P_3 LHCLK0	VCCAUX	INPUT VREF_3	I/O L13P_3	I/O L15P_3 LHCLK2	GND	VCCINT	GND
L	I/O L16N_3 LHCLK5	VCCO_3	I/O L17N_3 LHCLK7	GND	INPUT	VCCO_3	I/O L15N_3 LHCLK3 IRDY2	INPUT	GND	VCCINT
M	I/O L16P_3 LHCLK4 TRDY2	INPUT	I/O L17P_3 LHCLK6	I/O L19N_3	I/O L19P_3	I/O L20P_3	I/O L18N_3	I/O L18P_3	VCCINT	GND
N	I/O L21P_3	I/O L21N_3	I/O L23P_3	I/O L23N_3	INPUT	I/O L20N_3 VREF_3	I/O L22P_3	VCCINT	VCCAUX	VCCINT
P	I/O L24P_3	GND	INPUT	VCCO_3	I/O L25P_3	INPUT VREF_3	I/O L22N_3	I/O	GND	I/O L16N_2 D3 GCLK15
R	I/O L24N_3	I/O L26P_3	I/O L27P_3	I/O L27N_3	I/O L25N_3	GND	I/O L09N_2 VREF_2	INPUT L11N_2	I/O	I/O L16P_2 D4 GCLK14
T	I/O L28N_3 VREF_3	I/O L26N_3	I/O L29N_3	INPUT	I/O L06P_2	I/O L06N_2	I/O L09P_2	INPUT L11P_2	INPUT L14P_2	INPUT L14N_2 VREF_2
U	I/O L28P_3	VCCO_3	I/O L29P_3	I/O L01P_2 CSO_B	I/O L03P_2 DOUT BUSY	INPUT L05P_2	I/O L07N_2	VCCO_2	I/O L12N_2	VCCAUX
V	I/O L30N_3	I/O L30P_3	GND	I/O L01N_2 INIT_B	I/O L03N_2 MOSI CSI_B	INPUT L05N_2	I/O L07P_2	I/O L10N_2	I/O L12P_2	I/O L18P_2 D2 GCLK2
W	INPUT	INPUT L02P_2	INPUT	I/O L04P_2	VCCO_2	INPUT L08P_2	GND	I/O L10P_2	I/O L15P_2 D7 GCLK12	I/O L15N_2 D6 GCLK13
Y	GND	INPUT L02N_2	I/O VREF_2	I/O L04N_2	I/O	INPUT L08N_2	I/O	I/O L13N_2	I/O L13P_2	GND

Bank 3

Bank 2

DS312-4_08_101905

Figure 87: **FG400 Package Footprint (top view)**

Table 154: **FG484 Package Pinout *(Cont'd)***

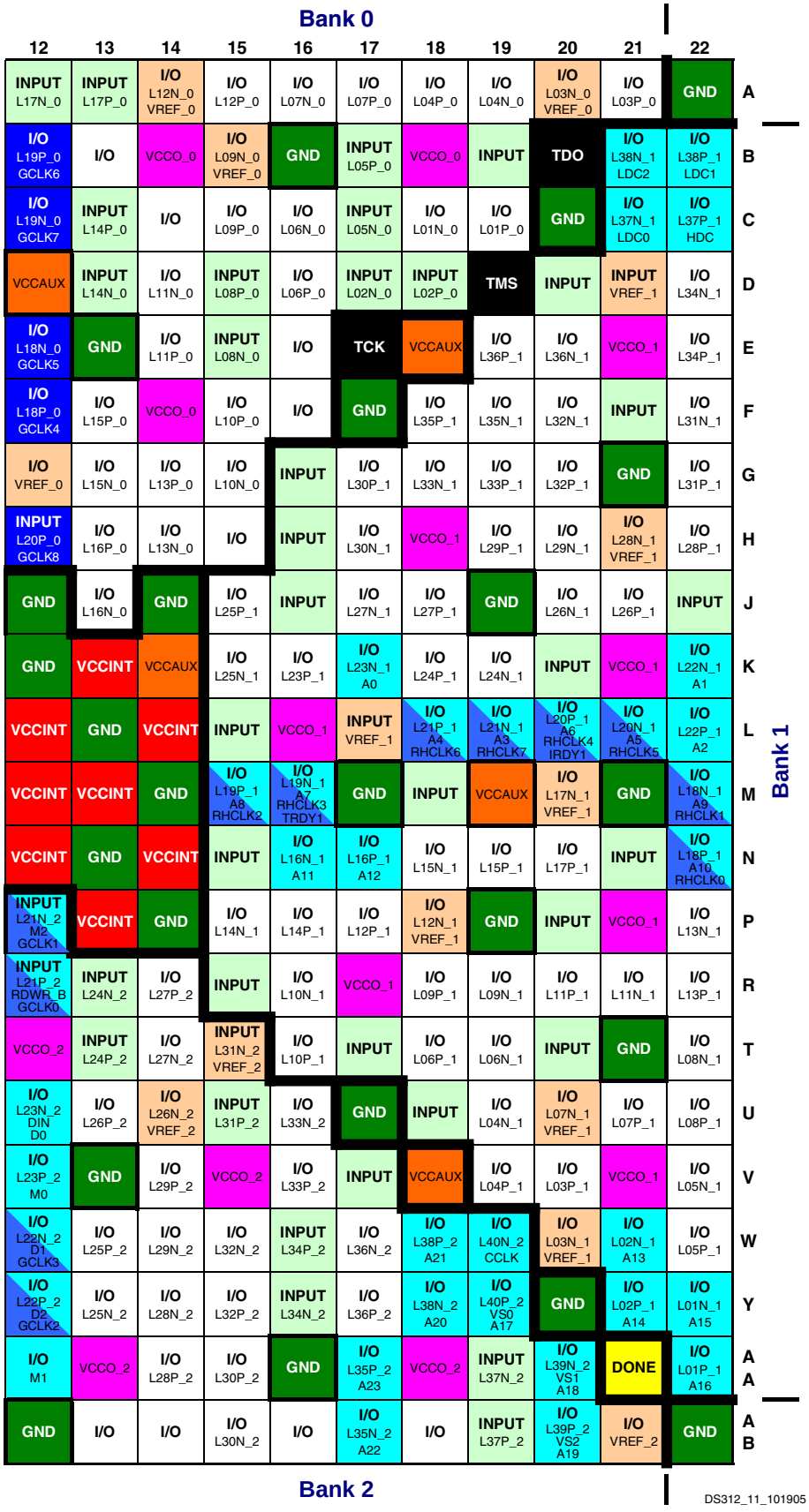
Bank	XC3S1600E Pin Name	FG484 Ball	Type
2	IO_L19N_2/D6/GCLK13	U11	DUAL/ GCLK
2	IO_L19P_2/D7/GCLK12	V11	DUAL/ GCLK
2	IO_L20N_2/D3/GCLK15	T11	DUAL/ GCLK
2	IO_L20P_2/D4/GCLK14	R11	DUAL/ GCLK
2	IO_L22N_2/D1/GCLK3	W12	DUAL/ GCLK
2	IO_L22P_2/D2/GCLK2	Y12	DUAL/ GCLK
2	IO_L23N_2/DIN/D0	U12	DUAL
2	IO_L23P_2/M0	V12	DUAL
2	IO_L25N_2	Y13	I/O
2	IO_L25P_2	W13	I/O
2	IO_L26N_2/VREF_2	U14	VREF
2	IO_L26P_2	U13	I/O
2	IO_L27N_2	T14	I/O
2	IO_L27P_2	R14	I/O
2	IO_L28N_2	Y14	I/O
2	IO_L28P_2	AA14	I/O
2	IO_L29N_2	W14	I/O
2	IO_L29P_2	V14	I/O
2	IO_L30N_2	AB15	I/O
2	IO_L30P_2	AA15	I/O
2	IO_L32N_2	W15	I/O
2	IO_L32P_2	Y15	I/O
2	IO_L33N_2	U16	I/O
2	IO_L33P_2	V16	I/O
2	IO_L35N_2/A22	AB17	DUAL
2	IO_L35P_2/A23	AA17	DUAL
2	IO_L36N_2	W17	I/O
2	IO_L36P_2	Y17	I/O
2	IO_L38N_2/A20	Y18	DUAL
2	IO_L38P_2/A21	W18	DUAL
2	IO_L39N_2/VS1/A18	AA20	DUAL
2	IO_L39P_2/VS2/A19	AB20	DUAL
2	IO_L40N_2/CCLK	W19	DUAL
2	IO_L40P_2/VS0/A17	Y19	DUAL
2	IP	V17	INPUT
2	IP	AB2	INPUT
2	IP_L02N_2	AA4	INPUT
2	IP_L02P_2	Y4	INPUT
2	IP_L05N_2	Y6	INPUT
2	IP_L05P_2	AA6	INPUT

Table 154: **FG484 Package Pinout *(Cont'd)***

Bank	XC3S1600E Pin Name	FG484 Ball	Type
2	IP_L08N_2	AB7	INPUT
2	IP_L08P_2	AB6	INPUT
2	IP_L15N_2	Y10	INPUT
2	IP_L15P_2	W10	INPUT
2	IP_L18N_2/VREF_2	AA11	VREF
2	IP_L18P_2	Y11	INPUT
2	IP_L21N_2/M2/GCLK1	P12	DUAL/ GCLK
2	IP_L21P_2/RDWR_B/ GCLK0	R12	DUAL/ GCLK
2	IP_L24N_2	R13	INPUT
2	IP_L24P_2	T13	INPUT
2	IP_L31N_2/VREF_2	T15	VREF
2	IP_L31P_2	U15	INPUT
2	IP_L34N_2	Y16	INPUT
2	IP_L34P_2	W16	INPUT
2	IP_L37N_2	AA19	INPUT
2	IP_L37P_2	AB19	INPUT
2	VCCO_2	T12	VCCO
2	VCCO_2	U9	VCCO
2	VCCO_2	V15	VCCO
2	VCCO_2	AA5	VCCO
2	VCCO_2	AA9	VCCO
2	VCCO_2	AA13	VCCO
2	VCCO_2	AA18	VCCO
3	IO_L01N_3	C1	I/O
3	IO_L01P_3	C2	I/O
3	IO_L02N_3/VREF_3	D2	VREF
3	IO_L02P_3	D3	I/O
3	IO_L03N_3	E3	I/O
3	IO_L03P_3	E4	I/O
3	IO_L04N_3	E1	I/O
3	IO_L04P_3	D1	I/O
3	IO_L05N_3	F4	I/O
3	IO_L05P_3	F3	I/O
3	IO_L06N_3	G5	I/O
3	IO_L06P_3	G4	I/O
3	IO_L07N_3	F1	I/O
3	IO_L07P_3	G1	I/O
3	IO_L08N_3/VREF_3	G6	VREF
3	IO_L08P_3	G7	I/O
3	IO_L09N_3	H4	I/O
3	IO_L09P_3	H5	I/O
3	IO_L10N_3	H2	I/O
3	IO_L10P_3	H3	I/O

FG484 Footprint

Right Half of Package (top view)



DS312_11_101905

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/01/05	1.0	Initial Xilinx release.
03/21/05	1.1	Added XC3S250E in the CP132 package to Table 129. Corrected number of differential I/O pairs on CP132. Added pinout and footprint information for the CP132, FG400, and FG484 packages. Removed IRDY and TRDY pins from the VQ100, TQ144, and PQ208 packages.
11/23/05	2.0	Corrected title of Table 153. Updated differential pair numbering for some pins in Bank 0 of the FG400 package, affecting Table 152 and Figure 87. Pin functionality and ball assignment were not affected. Added Package Thermal Characteristics section. Added package mass values to Table 125.
03/22/06	3.0	Included I/O pins, not just input-only pins under the VREF description in Table 124. Clarified that some global clock inputs are Input-only pins in Table 124. Added information on the XC3S100E in the CP132 package, affecting Table 129, Table 130, Table 133, Table 134, Table 136, and Figure 81. Ball A12 on the XC3S1600E in the FG320 package a full I/O pin, not an Input-only pin. Corrected the I/O counts for the XC3S1600E in the FG320 package, affecting Table 129, Table 150, Table 151, and Figure 86. Corrected pin type for XC3S1600E balls N14 and N15 in Table 148.
05/19/06	3.1	Minor text edits.
11/09/06	3.4	Added package thermal data for the XC3S100E in the CP132 package to Table 130. Corrected pin migration arrows for balls E17 and F4 between the XC3S500E and XC3S1600E in Table 151. Promoted Module 4 to Production status. Synchronized all modules to v3.4.
03/16/07	3.5	Minor formatting changes.
05/29/07	3.6	Corrected ‘Lxx’ to ‘Lxxy’ in Table 124. Noted that some GCLK and VREF pins are on INPUT pins in Table 124 and Table 129. Added link before Table 127 to Material Declaration Data Sheets.
04/18/08	3.7	Added XC3S500E VQG100 package. Added Material Declaration Data Sheet links in Table 127. Updated Thermal Characteristics in Table 130. Updated links.
08/26/09	3.8	Minor typographical updates.
10/29/12	4.0	Added Notice of Disclaimer. This product is not recommended for new designs. Updated the XC3S250E-FT256 in Table 129.

Notice of Disclaimer