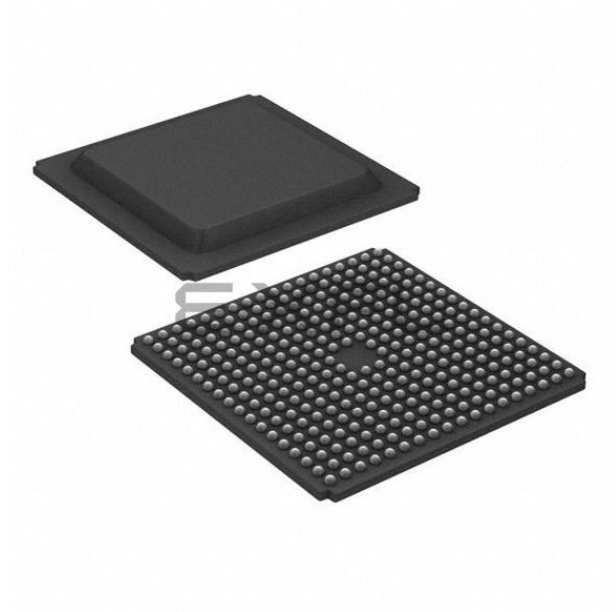
AMD Xilinx - XC3S500E-4FG320I Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1164
Number of Logic Elements/Cells	10476
Total RAM Bits	368640
Number of I/O	232
Number of Gates	500000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	320-BGA
Supplier Device Package	320-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s500e-4fg320i

Architectural Overview

The Spartan-3E family architecture consists of five fundamental programmable functional elements:

- **Configurable Logic Blocks (CLBs)** contain flexible Look-Up Tables (LUTs) that implement logic plus storage elements used as flip-flops or latches. CLBs perform a wide variety of logical functions as well as store data.
- **Input/Output Blocks (IOBs)** control the flow of data between the I/O pins and the internal logic of the device. Each IOB supports bidirectional data flow plus 3-state operation. Supports a variety of signal standards, including four high-performance differential standards. Double Data-Rate (DDR) registers are included.
- **Block RAM** provides data storage in the form of 18-Kbit dual-port blocks.
- **Multiplier Blocks** accept two 18-bit binary numbers as inputs and calculate the product.
- **Digital Clock Manager (DCM) Blocks** provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase-shifting clock signals.

These elements are organized as shown in Figure 1. A ring of IOBs surrounds a regular array of CLBs. Each device has two columns of block RAM except for the XC3S100E, which has one column. Each RAM column consists of several 18-Kbit RAM blocks. Each block RAM is associated with a dedicated multiplier. The DCMs are positioned in the center with two at the top and two at the bottom of the device. The XC3S100E has only one DCM at the top and bottom, while the XC3S1200E and XC3S1600E add two DCMs in the middle of the left and right sides.

The Spartan-3E family features a rich network of traces that interconnect all five functional elements, transmitting signals among them. Each functional element has an associated switch matrix that permits multiple connections to the routing.

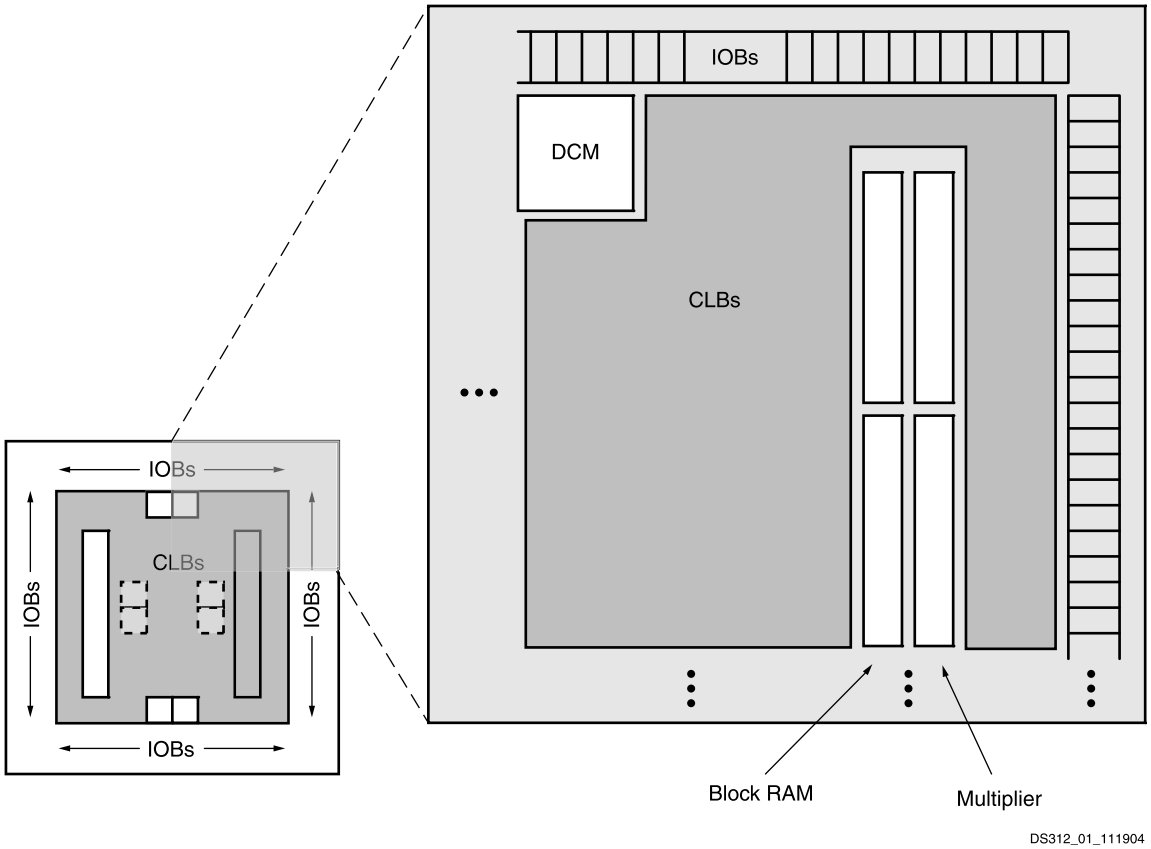

Figure 1: **Spartan-3E Family Architecture**

Configurable Logic Block (CLB) and Slice Resources

For additional information, refer to the “Using Configurable Logic Blocks (CLBs)” chapter in UG331.

CLB Overview

The Configurable Logic Blocks (CLBs) constitute the main logic resource for implementing synchronous as well as combinatorial circuits. Each CLB contains four slices, and each slice contains two Look-Up Tables (LUTs) to implement logic and two dedicated storage elements that can be used as flip-flops or latches. The LUTs can be used as a 16x1 memory (RAM16) or as a 16-bit shift register (SRL16), and additional multiplexers and carry logic simplify wide logic and arithmetic functions. Most general-purpose logic in a design is automatically mapped to the slice resources in the CLBs. Each CLB is identical, and the Spartan-3E family CLB structure is identical to that for the Spartan-3 family.

CLB Array

The CLBs are arranged in a regular array of rows and columns as shown in Figure 14.

Each density varies by the number of rows and columns of CLBs (see Table 9).

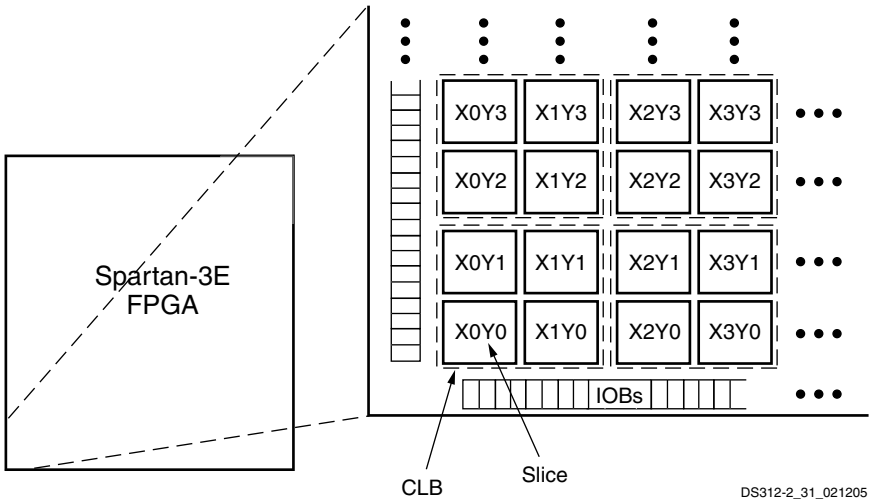

Figure 14: **CLB Locations**

Table 9: **Spartan-3E CLB Resources**

Device	CLB Rows	CLB Columns	CLB Total(1)	Slices	LUTs / Flip-Flops	Equivalent Logic Cells	RAM16 / SRL16	Distributed RAM Bits
XC3S100E	22	16	240	960	1,920	2,160	960	15,360
XC3S250E	34	26	612	2,448	4,896	5,508	2,448	39,168
XC3S500E	46	34	1,164	4,656	9,312	10,476	4,656	74,496
XC3S1200E	60	46	2,168	8,672	17,344	19,512	8,672	138,752
XC3S1600E	76	58	3,688	14,752	29,504	33,192	14,752	236,032

Notes:

1. The number of CLBs is less than the multiple of the rows and columns because the block RAM/multiplier blocks and the DCMs are embedded in the array (see Figure 1 in Module 1).

Slices

Each CLB comprises four interconnected slices, as shown in Figure 16. These slices are grouped in pairs. Each pair is organized as a column with an independent carry chain. The left pair supports both logic and memory functions and its slices are called SLICEM. The right pair supports logic only and its slices are called SLICEL. Therefore half the LUTs support both logic and memory (including both RAM16 and SRL16 shift registers) while half support logic only, and the two types alternate throughout the array columns. The SLICEL reduces the size of the CLB and lowers the cost of the device, and can also provide a performance advantage over the SLICEM.

Table 14: **Carry Logic Functions *(Cont'd)***

Function	Description
CY0G	Carry generation for top half of slice. Fixed selection of: · G1 or G2 inputs to the LUT (both equal 1 when a carry is to be generated) · GAND gate for multiplication · BY input for carry initialization · Fixed 1 or 0 input for use as a simple Boolean function
CYMUXF	Carry generation or propagation mux for bottom half of slice. Dynamic selection via CYSELF of: · CYINIT carry propagation (CYSELF = 1) · CY0F carry generation (CYSELF = 0)
CYMUXG	Carry generation or propagation mux for top half of slice. Dynamic selection via CYSELF of: · CYMUXF carry propagation (CYSELG = 1) · CY0G carry generation (CYSELG = 0)
CYSELF	Carry generation or propagation select for bottom half of slice. Fixed selection of: · F-LUT output (typically XOR result) · Fixed 1 to always propagate
CYSELG	Carry generation or propagation select for top half of slice. Fixed selection of: · G-LUT output (typically XOR result) · Fixed 1 to always propagate
XORF	Sum generation for bottom half of slice. Inputs from: · F-LUT · CYINIT carry signal from previous stage Result is sent to either the combinatorial or registered output for the top of the slice.
XORG	Sum generation for top half of slice. Inputs from: · G-LUT · CYMUXF carry signal from previous stage Result is sent to either the combinatorial or registered output for the top of the slice.
FAND	Multiplier partial product for bottom half of slice. Inputs: · F-LUT F1 input · F-LUT F2 input Result is sent through CY0F to become the carry generate signal into CYMUXF
GAND	Multiplier partial product for top half of slice. Inputs: · G-LUT G1 input · G-LUT G2 input Result is sent through CY0G to become the carry generate signal into CYMUXG

The basic usage of the carry logic is to generate a half-sum in the LUT via an XOR function, which generates or propagates a carry out COUT via the carry mux CYMUXF (or CYMUXG), and then complete the sum with the dedicated XORF (or XORG) gate and the carry input CIN. This structure allows two bits of an arithmetic function in each slice. The CYMUXF (or CYMUXG) can be instantiated using the MUXCY element, and the XORF (or XORG) can be instantiated using the XORCY element.

The FAND (or GAND) gate is used for partial product multiplication and can be instantiated using the MULT_AND component. Partial products are generated by two-input AND gates and then added. The carry logic is efficient for the adder, but one of the inputs must be outside the LUT as shown in Figure 23.

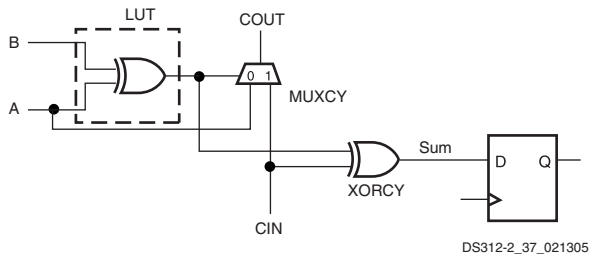

Figure 23: **Using the MUXCY and XORCY in the Carry Logic**

The FAND (or GAND) gate is used to duplicate one of the partial products, while the LUT generates both partial products and the XOR function, as shown in Figure 24.

Multiplier/Block RAM Interaction

Each multiplier is located adjacent to an 18 Kbit block RAM and shares some interconnect resources. Configuring an 18 Kbit block RAM for 36-bit wide data (512 x 36 mode) prevents use of the associated dedicated multiplier.

The upper 16 bits of the 'A' multiplicand input are shared with the upper 16 bits of the block RAM's Port A Data input. Similarly, the upper 16 bits of the 'B' multiplicand input are shared with Port B's data input. See also Figure 48, page 62.

Table 27 defines each port of the MULT18X18SIO primitive.

Table 27: **MULT18X18SIO Embedded Multiplier Primitives Description**

Signal Name	Direction	Function
A[17:0]	Input	The primary 18-bit two's complement value for multiplication. The block multiplies by this value asynchronously if the optional AREG and PREG registers are omitted. When AREG and/or PREG are used, the value provided on this port is qualified by the rising edge of CLK, subject to the appropriate register controls.
B[17:0]	Input	The second 18-bit two's complement value for multiplication if the B_INPUT attribute is set to DIRECT. The block multiplies by this value asynchronously if the optional BREG and PREG registers are omitted. When BREG and/or PREG are used, the value provided on this port is qualified by the rising edge of CLK, subject to the appropriate register controls.
BCIN[17:0]	Input	The second 18-bit two's complement value for multiplication if the B_INPUT attribute is set to CASCADE. The block multiplies by this value asynchronously if the optional BREG and PREG registers are omitted. When BREG and/or PREG are used, the value provided on this port is qualified by the rising edge of CLK, subject to the appropriate register controls.
P[35:0]	Output	The 36-bit two's complement product resulting from the multiplication of the two input values applied to the multiplier. If the optional AREG, BREG and PREG registers are omitted, the output operates asynchronously. Use of PREG causes this output to respond to the rising edge of CLK with the value qualified by CEP and RSTP. If PREG is omitted, but AREG and BREG are used, this output responds to the rising edge of CLK with the value qualified by CEA, RSTA, CEB, and RSTB. If PREG is omitted and only one of AREG or BREG is used, this output responds to both asynchronous and synchronous events.
BCOUT[17:0]	Output	The value being applied to the second input of the multiplier. When the optional BREG register is omitted, this output responds asynchronously in response to changes at the B[17:0] or BCIN[17:0] ports according to the setting of the B_INPUT attribute. If BREG is used, this output responds to the rising edge of CLK with the value qualified by CEB and RSTB.
CEA	Input	Clock enable qualifier for the optional AREG register. The value provided on the A[17:0] port is captured by AREG in response to a rising edge of CLK when this signal is High, provided that RSTA is Low.
RSTA	Input	Synchronous reset for the optional AREG register. AREG content is forced to the value zero in response to a rising edge of CLK when this signal is High.
CEB	Input	Clock enable qualifier for the optional BREG register. The value provided on the B[17:0] or BCIN[17:0] port is captured by BREG in response to a rising edge of CLK when this signal is High, provided that RSTB is Low.
RSTB	Input	Synchronous reset for the optional BREG register. BREG content is forced to the value zero in response to a rising edge of CLK when this signal is High.
CEP	Input	Clock enable qualifier for the optional PREG register. The value provided on the output of the multiplier port is captured by PREG in response to a rising edge of CLK when this signal is High, provided that RSTP is Low.
RSTP	Input	Synchronous reset for the optional PREG register. PREG content is forced to the value zero in response to a rising edge of CLK when this signal is High.

Notes:

1. The control signals CLK, CEA, RSTA, CEB, RSTB, CEP, and RSTP have the option of inverted polarity.

Clocking Infrastructure

For additional information, refer to the “Using Global Clock Resources” chapter in UG331.

The Spartan-3E clocking infrastructure, shown in Figure 45, provides a series of low-capacitance, low-skew interconnect lines well-suited to carrying high-frequency signals throughout the FPGA. The infrastructure also includes the clock inputs and BUFGMUX clock buffers/multiplexers. The Xilinx Place-and-Route (PAR) software automatically routes high-fanout clock signals using these resources.

Clock Inputs

Clock pins accept external clock signals and connect directly to DCMs and BUFGMUX elements. Each Spartan-3E FPGA has:

- 16 Global Clock inputs (GCLK0 through GCLK15) located along the top and bottom edges of the FPGA
- 8 Right-Half Clock inputs (RHCLK0 through RHCLK7) located along the right edge
- 8 Left-Half Clock inputs (LHCLK0 through LHCLK7) located along the left edge

Clock inputs optionally connect directly to DCMs using dedicated connections. Table 30, Table 31, and Table 32 show the clock inputs that best feed a specific DCM within a given Spartan-3E part number. Different Spartan-3E FPGA densities have different numbers of DCMs. The XC3S1200E and XC3S1600E are the only two densities with the left- and right-edge DCMs.

Each clock input is also optionally a user-I/O pin and connects to internal interconnect. Some clock pad pins are input-only pins as indicated in Module 4, Pinout Descriptions.

Design Note

Avoid using global clock input GCLK1 as it is always shared with the M2 mode select pin. Global clock inputs GCLK0, GCLK2, GCLK3, GCLK12, GCLK13, GCLK14, and GCLK15 have shared functionality in some configuration modes.

Clock Buffers/Multiplexers

Clock Buffers/Multiplexers either drive clock input signals directly onto a clock line (BUFG) or optionally provide a multiplexer to switch between two unrelated, possibly asynchronous clock signals (BUFGMUX).

Each BUFGMUX element, shown in Figure 46, is a 2-to-1 multiplexer. The select line, S, chooses which of the two inputs, I0 or I1, drives the BUFGMUX’s output signal, O, as described in Table 40. The switching from one clock to the other is glitch-less, and done in such a way that the output High and Low times are never shorter than the shortest High or Low time of either input clock. The two clock inputs can be asynchronous with regard to each other, and the S input can change at any time, except for a short setup time prior to the rising edge of the presently selected clock (I0 or I1). This setup time is specified as TGSI in Table 101, page 136. Violating this setup time requirement possibly results in an undefined runt pulse output.

Table 40: **BUFGMUX Select Mechanism**

S Input	O Output
0	I0 Input
1	I1 Input

The BUFG clock buffer primitive drives a single clock signal onto the clock network and is essentially the same element as a BUFGMUX, just without the clock select mechanism. Similarly, the BUFGCE primitive creates an enabled clock buffer using the BUFGMUX select mechanism.

The I0 and I1 inputs to an BUFGMUX element originate from clock input pins, DCMs, or Double-Line interconnect, as shown in Figure 46. As shown in Figure 45, there are 24 BUFGMUX elements distributed around the four edges of the device. Clock signals from the four BUFGMUX elements at the top edge and the four at the bottom edge are truly global and connect to all clocking quadrants. The eight left-edge BUFGMUX elements only connect to the two clock quadrants in the left half of the device. Similarly, the eight right-edge BUFGMUX elements only connect to the right half of the device.

BUFGMUX elements are organized in pairs and share I0 and I1 connections with adjacent BUFGMUX elements from a common clock switch matrix as shown in Figure 46. For example, the input on I0 of one BUFGMUX is also a shared input to I1 of the adjacent BUFGMUX.

The clock switch matrix for the left- and right-edge BUFGMUX elements receive signals from any of the three following sources: an LHCLK or RHCLK pin as appropriate, a Double-Line interconnect, or a DCM in the XC3S1200E and XC3S1600E devices.

Also, in a multi-FPGA daisy-chain configuration of more than two devices, all intermediate FPGAs between the first and last devices must be Spartan-3E or Virtex-5 FPGAs. The last FPGA in the chain can be from any Xilinx FPGA family.

BPI Mode Interaction with Right and Bottom Edge Global Clock Inputs

Some of the BPI mode configuration pins are shared with global clock inputs along the right and bottom edges of the device (Bank 1 and Bank 2, respectively). These pins are not easily reclaimable for clock inputs after configuration, especially if the FPGA application access the parallel NOR Flash after configuration. Table 64 summarizes the shared pins.

Table 64: **Shared BPI Configuration Mode and Global Buffer Input Pins**

Device Edge	Global Buffer Input Pin	BPI Mode Configuration Pin
Bottom	GCLK0	RDWR_B
	GCLK2	D2
	GCLK3	D1
	GCLK12	D7
	GCLK13	D6
	GCLK14	D4
	GCLK15	D3
Right	RHCLK0	A10
	RHCLK1	A9
	RHCLK2	A8
	RHCLK3	A7
	RHCLK4	A6
	RHCLK5	A5
	RHCLK6	A4
	RHCLK7	A3

Production Stepping

The Spartan-3E FPGA family uses production stepping to indicate improved capabilities or enhanced features.

Stepping 1 is, by definition, a functional superset of Stepping 0. Furthermore, configuration bitstreams generated for Stepping 0 are compatible with Stepping 1.

Designs operating on the Stepping 0 devices perform similarly on a Stepping 1 device.

Differences Between Steppings

Table 71 summarizes the feature and performance differences between Stepping 0 devices and Stepping 1 devices.

Table 71: **Differences between Spartan-3E Production Stepping Levels**

	Stepping 0	Stepping 1
Production status	Production from 2005 to 2007	Production starting March 2006
Speed grade and operating conditions	-4C only	-4C, -4I, -5C
JTAG ID code	Different revision fields. See Table 67.	
DCM DLL maximum input frequency	90 MHz (200 MHz for XC3S1200E)	240 MHz (-4 speed grade) 275 MHz (-5 speed grade)
DCM DFS output frequency range(s)	Split ranges at 5 – 90 MHz and 220 – 307 MHz (single range 5 – 307 MHz for XC3S1200E)	Continuous range: 5 – 311 MHz (-4) 5 – 333 MHz (-5)
Supports multi-FPGA daisy-chain configurations from SPI Flash	No, single FPGA only	Yes
JTAG configuration supported when FPGA in BPI mode with a valid image in the attached parallel NOR Flash PROM	No(1)	Yes
JTAG EXTEST, INTEST, SAMPLE support	Yes: XC3S100E, XC3S250E, XC3S500E No(2): XC3S1200E, XC3S1600E	Yes All Devices
Power sequencing when using HSWAP Pull-Up	Requires V_{CCINT} before V_{CCAUX}	Any sequence
PCI compliance	No	Yes

Notes:

1. Workarounds exist. See Stepping 0 Limitations when Reprogramming via JTAG if FPGA Set for BPI Configuration.
2. JTAG BYPASS and JTAG configuration are supported

Ordering a Later Stepping

-5C and -4I devices, and -4C devices (with date codes 0901 (2009) and later) always support the Stepping 1 feature set independent of the stepping code. Optionally, to order only Stepping 1 for the -4C devices, append an “S1” suffix to the standard ordering code, where ‘1’ is the stepping number, as indicated in Table 72.

Table 72: **Spartan-3E Optional Stepping Ordering**

Stepping Number	Suffix Code	Status
0	None	Production
1	S1	Production

Software Version Requirements

Production Spartan-3E applications must be processed using the Xilinx ISE 8.1i, Service Pack 3 or later development software, using the v1.21 or later speed files. The ISE 8.1i software implements critical bitstream generator updates.

For additional information on Spartan-3E development software and known issues, see the following Answer Record:

- Xilinx Answer #22253
  http://www.xilinx.com/support/answers/22253.htm

Switching Characteristics

All Spartan-3E FPGAs ship in two speed grades: -4 and the higher performance -5. Switching characteristics in this document may be designated as Advance, Preliminary, or Production, as shown in Table 84. Each category is defined as follows:

Advance: These specifications are based on simulations only and are typically available soon after establishing FPGA specifications. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These specifications are based on complete early silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting preliminary delays is greatly reduced compared to Advance data.

Production: These specifications are approved once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Software Version Requirements

Production-quality systems must use FPGA designs compiled using a speed file designated as PRODUCTION status. FPGAs designs using a less mature speed file designation should only be used during system prototyping or pre-production qualification. FPGA designs with speed files designated as Advance or Preliminary should not be used in a production-quality system.

Whenever a speed file designation changes, as a device matures toward Production status, rerun the latest Xilinx ISE software on the FPGA design to ensure that the FPGA design incorporates the latest timing information and software updates.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all Spartan-3E devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.**

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Timing parameters and their representative values are selected for inclusion below either because they are important as general design requirements or they indicate fundamental device performance characteristics. The Spartan-3E speed files (v1.27), part of the Xilinx Development Software, are the original source for many but not all of the values. The speed grade designations for these files are shown in Table 84. For more complete, more precise, and worst-case data, use the values reported by the Xilinx static timing analyzer (TRACE in the Xilinx development software) and back-annotated to the simulation netlist.

Table 84: **Spartan-3E v1.27 Speed Grade Designations**

Device	Advance	Preliminary	Production
XC3S100E			-MIN, -4, -5
XC3S250E			-MIN, -4, -5
XC3S500E			-MIN, -4, -5
XC3S1200E			-MIN, -4, -5
XC3S1600E			-MIN, -4, -5

Table 85 provides the history of the Spartan-3E speed files since all devices reached Production status.

Table 85: **Spartan-3E Speed File Version History**

Version	ISE Release	Description
1.27	9.2.03i	Added XA Automotive.
1.26	8.2.02i	Added -0/-MIN speed grade, which includes minimum values.
1.25	8.2.01i	Added XA Automotive devices to speed file. Improved model for left and right DCMs.
1.23	8.2i	Updated input setup/hold values based on default IFD_DELAY_VALUE settings.
1.21	8.1.03i	All Spartan-3E FPGAs and all speed grades elevated to Production status.

I/O Timing

Table 86: **Pin-to-Pin Clock-to-Output Times for the IOB Output Path**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max[2]	Max[2]	
Clock-to-Output Times						
$T_{ICKOFDCM}$	When reading from the Output Flip-Flop (OFF), the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is used.	LVCMOS25[3], 12 mA output drive, Fast slew rate, with DCM[4]	XC3S100E	2.66	2.79	ns
			XC3S250E	3.00	3.45	ns
			XC3S500E	3.01	3.46	ns
			XC3S1200E	3.01	3.46	ns
			XC3S1600E	3.00	3.45	ns
T_{ICKOF}	When reading from OFF, the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is not used.	LVCMOS25[3], 12 mA output drive, Fast slew rate, without DCM	XC3S100E	5.60	5.92	ns
			XC3S250E	4.91	5.43	ns
			XC3S500E	4.98	5.51	ns
			XC3S1200E	5.36	5.94	ns
			XC3S1600E	5.45	6.05	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 95 and are based on the operating conditions set forth in Table 77 and Table 80.
2. For minimums, use the values reported by the Xilinx timing analyzer.
3. This clock-to-output time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or a standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. If the former is true, *add* the appropriate Input adjustment from Table 91. If the latter is true, *add* the appropriate Output adjustment from Table 94.
4. DCM output jitter is included in all measurements.

Table 99: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	-5		-4		Units
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{SHCKO}	Time from the active edge at the CLK input to data appearing on the distributed RAM output	-	2.05	-	2.35	ns
Setup Times						
T_{DS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the distributed RAM	0.40	-	0.46	-	ns
T_{AS}	Setup time of the F/G address inputs before the active transition at the CLK input of the distributed RAM	0.46	-	0.52	-	ns
T_{WS}	Setup time of the write enable input before the active transition at the CLK input of the distributed RAM	0.34	-	0.40	-	ns
Hold Times						
T_{DH}	Hold time of the BX, BY data inputs after the active transition at the CLK input of the distributed RAM	0.13	-	0.15	-	ns
T_{AH}, T_{WH}	Hold time of the F/G address inputs or the write enable input after the active transition at the CLK input of the distributed RAM	0	-	0	-	ns
Clock Pulse Width						
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	0.88	-	1.01	-	ns

Table 100: **CLB Shift Register Switching Characteristics**

Symbol	Description	-5		-4		Units
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{REG}	Time from the active edge at the CLK input to data appearing on the shift register output	-	3.62	-	4.16	ns
Setup Times						
T_{SRLDS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the shift register	0.41	-	0.46	-	ns
Hold Times						
T_{SRLDH}	Hold time of the BX or BY data input after the active transition at the CLK input of the shift register	0.14	-	0.16	-	ns
Clock Pulse Width						
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	0.88	-	1.01	-	ns

Clock Buffer/Multiplexer Switching Characteristics

Table 101: **Clock Distribution Switching Characteristics**

Description	Symbol	Maximum		Units
		Speed Grade		
		-5	-4	
Global clock buffer (BUFG, BUFGMUX, BUFGCE) I input to O-output delay	T_{GIO}	1.46	1.46	ns
Global clock multiplexer (BUFGMUX) select S-input setup to I0 and I1 inputs. Same as BUFGCE enable CE-input	T_{GSI}	0.55	0.63	ns
Frequency of signals distributed on global buffers (all sides)	F_{BUFG}	333	311	MHz

Block RAM Timing

Table 103: **Block RAM Timing**

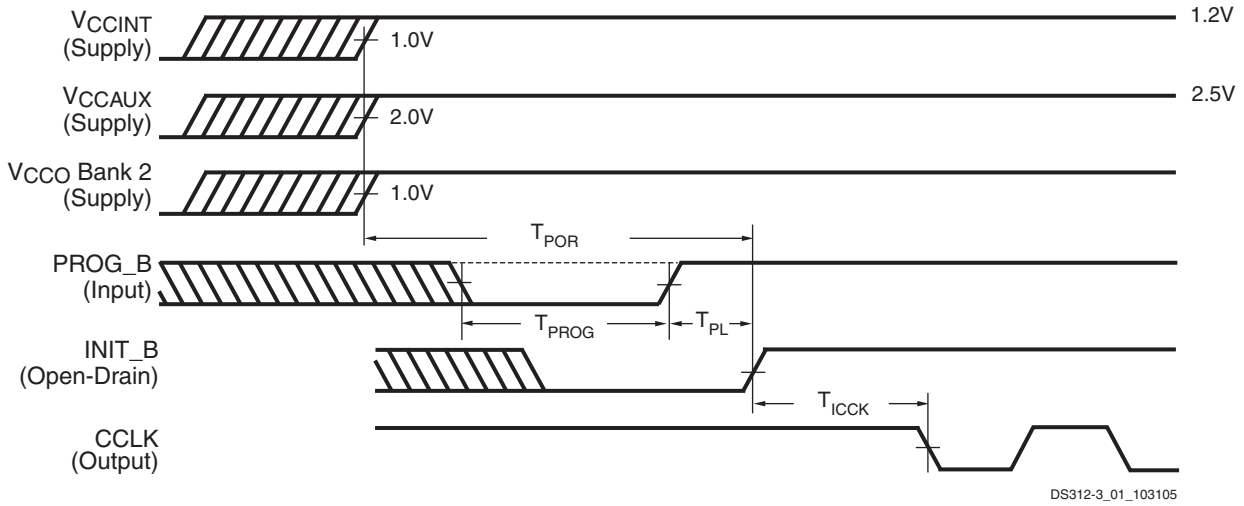
Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{BCKO}	When reading from block RAM, the delay from the active transition at the CLK input to data appearing at the DOUT output	-	2.45	-	2.82	ns
Setup Times						
T_{BACK}	Setup time for the ADDR inputs before the active transition at the CLK input of the block RAM	0.33	-	0.38	-	ns
T_{BDCK}	Setup time for data at the DIN inputs before the active transition at the CLK input of the block RAM	0.23	-	0.23	-	ns
T_{BECK}	Setup time for the EN input before the active transition at the CLK input of the block RAM	0.67	-	0.77	-	ns
T_{BWCK}	Setup time for the WE input before the active transition at the CLK input of the block RAM	1.09	-	1.26	-	ns
Hold Times						
T_{BCKA}	Hold time on the ADDR inputs after the active transition at the CLK input	0.12	-	0.14	-	ns
T_{BCKD}	Hold time on the DIN inputs after the active transition at the CLK input	0.12	-	0.13	-	ns
T_{BCKE}	Hold time on the EN input after the active transition at the CLK input	0	-	0	-	ns
T_{BCKW}	Hold time on the WE input after the active transition at the CLK input	0	-	0	-	ns
Clock Timing						
T_{BPWH}	High pulse width of the CLK signal	1.39	-	1.59	-	ns
T_{BPWL}	Low pulse width of the CLK signal	1.39	-	1.59	-	ns
Clock Frequency						
F_{BRAM}	Block RAM clock frequency. RAM read output value written back into RAM, for shift-registers and circular buffers. Write-only or read-only performance is faster.	0	270	0	230	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 77.

Configuration and JTAG Timing

General Configuration Power-On/Reconfigure Timing



Notes:

1. The V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies may be applied in any order.
2. The Low-going pulse on PROG_B is optional after power-on but necessary for reconfiguration without a power cycle.
3. The rising edge of INIT_B samples the voltage levels applied to the mode pins (M0 - M2).

Figure 73: **Waveforms for Power-On and the Beginning of Configuration**

Table 111: **Power-On Timing and the Beginning of Configuration**

Symbol	Description	Device	All Speed Grades		Units
			Min	Max	
T_{POR}(2)	The time from the application of V_{CCINT}, V_{CCAUX}, and V_{CCO} Bank 2 supply voltage ramps (whichever occurs last) to the rising transition of the INIT_B pin	XC3S100E	-	5	ms
		XC3S250E	-	5	ms
		XC3S500E	-	5	ms
		XC3S1200E	-	5	ms
		XC3S1600E	-	7	ms
T_{PROG}	The width of the low-going pulse on the PROG_B pin	All	0.5	-	µs
T_{PL}(2)	The time from the rising edge of the PROG_B pin to the rising transition on the INIT_B pin	XC3S100E	-	0.5	ms
		XC3S250E	-	0.5	ms
		XC3S500E	-	1	ms
		XC3S1200E	-	2	ms
		XC3S1600E	-	2	ms
T_{INIT}	Minimum Low pulse width on INIT_B output	All	250	-	ns
T_{ICCK}(3)	The time from the rising edge of the INIT_B pin to the generation of the configuration clock signal at the CCLK output pin	All	0.5	4.0	µs

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 77. This means power must be applied to all V_{CCINT}, V_{CCO}, and V_{CCAUX} lines.
2. Power-on reset and the clearing of configuration memory occurs during this period.
3. This specification applies only to the Master Serial, SPI, BPI-Up, and BPI-Down modes.

Table 119: **Configuration Timing Requirements for Attached SPI Serial Flash**

Symbol	Description	Requirement	Units
T_{CCS}	SPI serial Flash PROM chip-select time	$T_{CCS} \leq T_{MCCL1} - T_{CCO}$	ns
T_{DSU}	SPI serial Flash PROM data input setup time	$T_{DSU} \leq T_{MCCL1} - T_{CCO}$	ns
T_{DH}	SPI serial Flash PROM data input hold time	$T_{DH} \leq T_{MCCH1}$	ns
T_V	SPI serial Flash PROM data clock-to-output time	$T_V \leq T_{MCCLn} - T_{DCC}$	ns
f_C or f_R	Maximum SPI serial Flash PROM clock frequency (also depends on specific read command used)	$f_C \geq \frac{1}{T_{CCLKn(min)}}$	MHz

Notes:

1. These requirements are for successful FPGA configuration in SPI mode, where the FPGA provides the CCLK frequency. The post configuration timing can be different to support the specific needs of the application loaded into the FPGA and the resulting clock source.
2. Subtract additional printed circuit board routing delay as required by the application.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/01/05	1.0	Initial Xilinx release.
11/23/05	2.0	Added AC timing information and additional DC specifications.
03/22/06	3.0	Upgraded data sheet status to Preliminary. Finalized production timing parameters. All speed grades for all Spartan-3E FPGAs are now Production status using the v1.21 speed files, as shown in Table 84. Expanded description in Note 2, Table 78. Updated pin-to-pin and clock-to-output timing based on final characterization, shown in Table 86. Updated system-synchronous input setup and hold times based on final characterization, shown in Table 87 and Table 88. Updated other I/O timing in Table 90. Provided input and output adjustments for LVPECL_25, DIFF_SSTL and DIFF_HSTL I/O standards that supersede the v1.21 speed file values, in Table 91 and Table 94. Reduced I/O three-state and set/reset delays in Table 93. Added XC3S100E FPGA in CP132 package to Table 96. Increased T_{AS} slice flip-flop timing by 100 ps in Table 98. Updated distributed RAM timing in Table 99 and SRL16 timing in Table 100. Updated global clock timing, removed left/right clock buffer limits in Table 101. Updated block RAM timing in Table 103. Added DCM parameters for remainder of Step 0 device; added improved Step 1 DCM performance to Table 104, Table 105, Table 106, and Table 107. Added minimum INIT_B pulse width specification, T_{INIT}, in Table 111. Increased data hold time for Slave Parallel mode to 1.0 ns (T_{SMCCD}) in Table 117. Improved the DCM performance for the XC3S1200E, Stepping 0 in Table 104, Table 105, Table 106, and Table 107. Corrected links in Table 118 and Table 120. Added MultiBoot timing specifications to Table 122.
04/07/06	3.1	Improved SSO limits for LVDS_25, MINI_LVDS_25, and RSDS_25 I/O standards in the QFP packages (Table 97). Removed potentially confusing Note 2 from Table 78.
05/19/06	3.2	Clarified that 100 mV of hysteresis applies to LVCMOS33 and LVCMOS25 I/O standards (Note 4, Table 80). Other minor edits.
05/30/06	3.2.1	Corrected various typos and incorrect links.
11/09/06	3.4	Improved absolute maximum voltage specifications in Table 73, providing additional overshoot allowance. Widened the recommended voltage range for PCI and PCI-X standards in Table 80. Clarified Note 2, Table 83. Improved various timing specifications for v1.26 speed file. Added Table 85 to summarize the history of speed file releases after which time all devices became Production status. Added absolute minimum values for Table 86, Table 92, and Table 93. Updated pin-to-pin setup and hold timing based on default IFD_DELAY_VALUE settings in Table 87, Table 88, and Table 90. Added Table 89 about source-synchronous input capture sample window. Promoted Module 3 to Production status. Synchronized all modules to v3.4.
03/16/07	3.5	Based on extensive 90 nm production data, improved (reduced) the maximum quiescent current limits for the I_{CCINTQ}, I_{CCAUXQ}, and I_{CCOQ} specifications in Table 79 by an average of 50%.
05/29/07	3.6	Added note to Table 74 and Table 75 regarding HSWAP in step 0 devices. Updated t_{RPW_CLB} in Table 98 to match value in speed file. Improved CLKOUT_FREQ_CLK90 to 200 MHz for Stepping 1 in Table 105.
04/18/08	3.7	Clarified that Stepping 0 was offered only for -4C and removed Stepping 0 -5 specifications. Added reference to XAPP459 in Table 73 and Table 77. Improved recommended max V_{CCO} to 3.465V (3.3V + 5%) in Table 77. Removed minimum input capacitance from Table 78. Updated Recommended Operating Conditions for LVCMOS and PCI I/O standards in Table 80. Removed Absolute Minimums from Table 86, Table 92 and Table 93 and added footnote recommending use of Timing Analyzer for minimum values. Updated T_{PSFD} and T_{PHFD} in Table 87 to match current speed file. Update T_{RPW_IOB} in Table 88 to match current speed file and CLB equivalent spec. Added XC3S500E VQG100 to Table 96. Replaced $T_{MULCKID}$ with T_{MSCKD} for A, B, and P registers in Table 102. Updated CLKOUT_PER_JITT_FX in Table 107. Updated MAX_STEPS equation in Table 109. Updated Figure 77 and Table 120 to correct CCLK active edge. Updated links.

Date	Version	Revision
08/26/09	3.8	Added reference to XAPP459 in Table 73 note 2. Updated BPI timing in Figure 77, Table 119, and Table 120. Removed V_{REF} requirements for differential HSTL and differential SSTL in Table 95. Added Spread Spectrum paragraph. Revised hold times for $T_{IOICKPD}$ in Table 88 and setup times for T_{DICK} in Table 98. Added note 4 to Table 106 and note 3 to Table 107, and updated note 6 for Table 107 to add input jitter.
10/29/12	4.0	Added Notice of Disclaimer. This product is not recommended for new designs. Revised note 2 in Table 73. Revised note 2 and V_{IN} description in Table 77, and added note 5. Added note 3 to Table 78.

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Table 124: **Types of Pins on Spartan-3E FPGAs *(Cont'd)***

Type / Color Code	Description	Pin Name(s) in Type[1]
VCCAUX	Dedicated auxiliary power supply pin. The number of VCCAUX pins depends on the package used. All must be connected to +2.5V. See the Powering Spartan-3E FPGAs section in Module 2 for details.	VCCAUX
VCCINT	Dedicated internal core logic power supply pin. The number of VCCINT pins depends on the package used. All must be connected to +1.2V. See the Powering Spartan-3E FPGAs section in Module 2 for details.	VCCINT
VCCO	Along with all the other VCCO pins in the same bank, this pin supplies power to the output buffers within the I/O bank and sets the input threshold voltage for some I/O standards. See the Powering Spartan-3E FPGAs section in Module 2 for details.	VCCO_#
N.C.	This package pin is not connected in this specific device/package combination but may be connected in larger devices in the same package.	N.C.

Notes:

1. # = I/O bank number, an integer between 0 and 3.
2. IRDY/TRDY designations are for PCI designs; refer to PCI documentation for details.

Differential Pair Labeling

I/Os with Lxxy_# are part of a differential pair. 'L' indicates differential capability. The 'xx' field is a two-digit integer, unique to each bank that identifies a differential pin-pair. The 'y' field is either 'P' for the true signal or 'N' for the inverted signal in the differential pair. The '#' field is the I/O bank number.

The pin name suffix has the following significance. Figure 79 provides a specific example showing a differential input to and a differential output from Bank 1.

'L' indicates that the pin is part of a differential pair.

'xx' is a two-digit integer, unique for each bank, that identifies a differential pin-pair.

'y' is replaced by 'P' for the true signal or 'N' for the inverted. These two pins form one differential pin-pair.

'#' is an integer, 0 through 3, indicating the associated I/O bank.

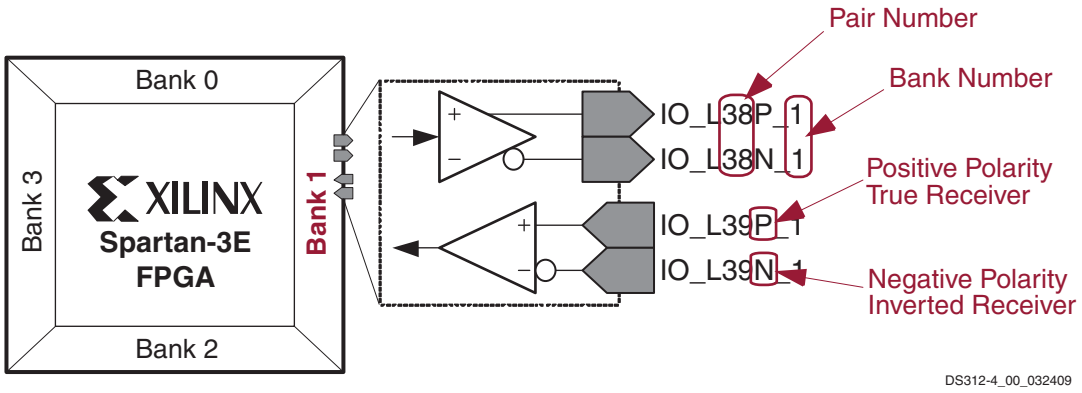

Figure 79: **Differential Pair Labeling**

CP132 Footprint

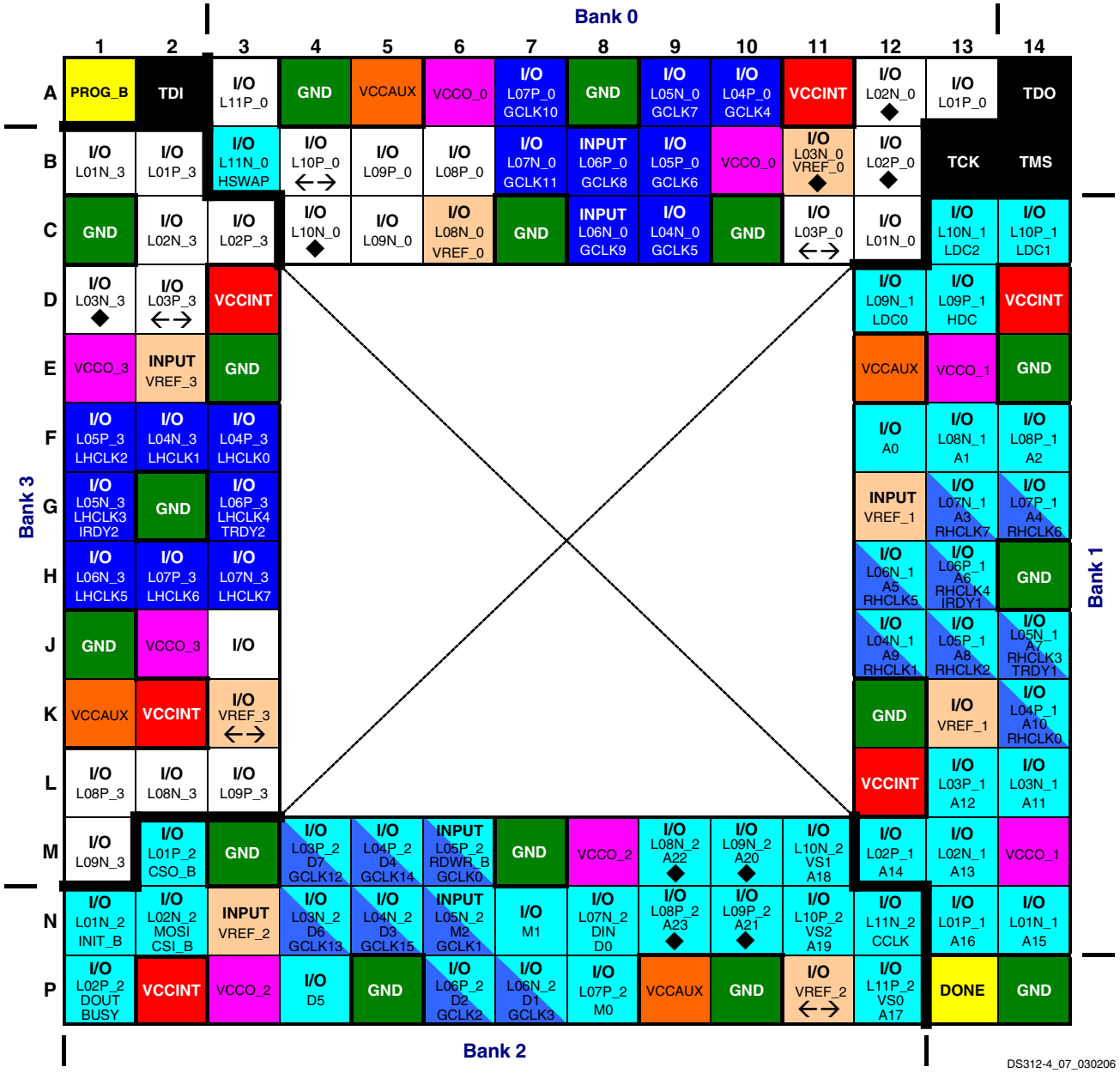

Figure 81: **CP132 Package Footprint (top view)**

16-22	**I/O:** Unrestricted, general-purpose user I/O	42-46	**DUAL:** Configuration pin, then possible user I/O	7-8	**VREF:** User I/O or input voltage reference for bank
0-2	**INPUT:** Unrestricted, general-purpose input pin	16	**CLK:** User I/O, input, or global buffer input	8	**VCCO:** Output voltage supply for bank
2	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	6	**VCCINT:** Internal core supply voltage (+1.2V)
9	**N.C.:** Unconnected balls on the XC3S100E FPGA (◆)	16	**GND:** Ground	4	**VCCAUX:** Auxiliary supply voltage (+2.5V)

FT256: 256-ball Fine-pitch, Thin Ball Grid Array

The 256-ball fine-pitch, thin ball grid array package, FT256, supports three different Spartan-3E FPGAs, including the XC3S250E, the XC3S500E, and the XC3S1200E.

Table 143 lists all the package pins. They are sorted by bank number and then by pin name of the largest device. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

The highlighted rows indicate pinout differences between the XC3S250E, the XC3S500E, and the XC3S1200E FPGAs. The XC3S250E has 18 unconnected balls, indicated as N.C. (No Connection) in Table 143 and with the black diamond character (◆) in Table 143 and Figure 83.

If the table row is highlighted in tan, then this is an instance where an unconnected pin on the XC3S250E FPGA maps to a VREF pin on the XC3S500E and XC3S1200E FPGA. If the FPGA application uses an I/O standard that requires a VREF voltage reference, connect the highlighted pin to the VREF voltage supply, even though this does not actually connect to the XC3S250E FPGA. This VREF connection on the board allows future migration to the larger devices without modifying the printed-circuit board.

All other balls have nearly identical functionality on all three devices. Table 147 summarizes the Spartan-3E footprint migration differences for the FT256 package.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx web site at:

http://www.xilinx.com/support/documentation/data_sheets/s3e_pin.zip

Pinout Table

Table 143: **FT256 Package Pinout**

Bank	XC3S250E Pin Name	XC3S500E Pin Name	XC3S1200E Pin Name	FT256 Ball	Type
0	IO	IO	IO	A7	I/O
0	IO	IO	IO	A12	I/O
0	IO	IO	IO	B4	I/O
0	IP	IP	IO	B6	***250E:*** INPUT ***500E:*** INPUT ***1200E:*** I/O
0	IP	IP	IO	B10	***250E:*** INPUT ***500E:*** INPUT ***1200E:*** I/O
0	IO/VREF_0	IO/VREF_0	IO/VREF_0	D9	VREF
0	IO_L01N_0	IO_L01N_0	IO_L01N_0	A14	I/O
0	IO_L01P_0	IO_L01P_0	IO_L01P_0	B14	I/O
0	IO_L03N_0/VREF_0	IO_L03N_0/VREF_0	IO_L03N_0/VREF_0	A13	VREF
0	IO_L03P_0	IO_L03P_0	IO_L03P_0	B13	I/O
0	IO_L04N_0	IO_L04N_0	IO_L04N_0	E11	I/O
0	IO_L04P_0	IO_L04P_0	IO_L04P_0	D11	I/O
0	IO_L05N_0/VREF_0	IO_L05N_0/VREF_0	IO_L05N_0/VREF_0	B11	VREF
0	IO_L05P_0	IO_L05P_0	IO_L05P_0	C11	I/O
0	IO_L06N_0	IO_L06N_0	IO_L06N_0	E10	I/O
0	IO_L06P_0	IO_L06P_0	IO_L06P_0	D10	I/O
0	IO_L08N_0/GCLK5	IO_L08N_0/GCLK5	IO_L08N_0/GCLK5	F9	GCLK
0	IO_L08P_0/GCLK4	IO_L08P_0/GCLK4	IO_L08P_0/GCLK4	E9	GCLK
0	IO_L09N_0/GCLK7	IO_L09N_0/GCLK7	IO_L09N_0/GCLK7	A9	GCLK
0	IO_L09P_0/GCLK6	IO_L09P_0/GCLK6	IO_L09P_0/GCLK6	A10	GCLK
0	IO_L11N_0/GCLK11	IO_L11N_0/GCLK11	IO_L11N_0/GCLK11	D8	GCLK
0	IO_L11P_0/GCLK10	IO_L11P_0/GCLK10	IO_L11P_0/GCLK10	C8	GCLK
0	IO_L12N_0	IO_L12N_0	IO_L12N_0	F8	I/O

Table 148: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S500E Pin Name	XC3S1200E Pin Name	XC3S1600E Pin Name	FG320 Ball	Type
2	IO_L20P_2	IO_L20P_2	IO_L20P_2	T12	I/O
2	N.C. (◆)	IO_L21N_2	IO_L21N_2	P12	**500E:** N.C. **1200E:** I/O **1600E:** I/O
2	N.C. (◆)	IO_L21P_2	IO_L21P_2	N12	**500E:** N.C. **1200E:** I/O **1600E:** I/O
2	IO_L22N_2/A22	IO_L22N_2/A22	IO_L22N_2/A22	R13	DUAL
2	IO_L22P_2/A23	IO_L22P_2/A23	IO_L22P_2/A23	P13	DUAL
2	IO_L24N_2/A20	IO_L24N_2/A20	IO_L24N_2/A20	R14	DUAL
2	IO_L24P_2/A21	IO_L24P_2/A21	IO_L24P_2/A21	T14	DUAL
2	IO_L25N_2/VS1/A18	IO_L25N_2/VS1/A18	IO_L25N_2/VS1/A18	U15	DUAL
2	IO_L25P_2/VS2/A19	IO_L25P_2/VS2/A19	IO_L25P_2/VS2/A19	V15	DUAL
2	IO_L26N_2/CCLK	IO_L26N_2/CCLK	IO_L26N_2/CCLK	U16	DUAL
2	IO_L26P_2/VS0/A17	IO_L26P_2/VS0/A17	IO_L26P_2/VS0/A17	T16	DUAL
2	IP	IP	IP	V2	INPUT
2	IP	IP	IP	V16	INPUT
2	IP_L02N_2	IP_L02N_2	IP_L02N_2	V3	INPUT
2	IP_L02P_2	IP_L02P_2	IP_L02P_2	V4	INPUT
2	IP_L08N_2	IP_L08N_2	IP_L08N_2	R7	INPUT
2	IP_L08P_2	IP_L08P_2	IP_L08P_2	T7	INPUT
2	IP_L11N_2/VREF_2	IP_L11N_2/VREF_2	IP_L11N_2/VREF_2	V8	VREF
2	IP_L11P_2	IP_L11P_2	IP_L11P_2	U8	INPUT
2	IP_L14N_2/M2/GCLK1	IP_L14N_2/M2/GCLK1	IP_L14N_2/M2/GCLK1	T10	DUAL/GCLK
2	IP_L14P_2/RDWR_B/ GCLK0	IP_L14P_2/RDWR_B/ GCLK0	IP_L14P_2/RDWR_B/ GCLK0	U10	DUAL/GCLK
2	IP_L17N_2	IP_L17N_2	IP_L17N_2	U11	INPUT
2	IP_L17P_2	IP_L17P_2	IP_L17P_2	T11	INPUT
2	IP_L23N_2	IP_L23N_2	IP_L23N_2	U14	INPUT
2	IP_L23P_2	IP_L23P_2	IP_L23P_2	V14	INPUT
2	VCCO_2	VCCO_2	VCCO_2	M8	VCCO
2	VCCO_2	VCCO_2	VCCO_2	M11	VCCO
2	VCCO_2	VCCO_2	VCCO_2	T6	VCCO
2	VCCO_2	VCCO_2	VCCO_2	T13	VCCO
2	VCCO_2	VCCO_2	VCCO_2	V10	VCCO
3	N.C. (◆)	IO	IO	D4	**500E:** N.C. **1200E:** I/O **1600E:** I/O
3	IO_L01N_3	IO_L01N_3	IO_L01N_3	C2	I/O
3	IO_L01P_3	IO_L01P_3	IO_L01P_3	C1	I/O
3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	IO_L02N_3/VREF_3	D2	VREF
3	IO_L02P_3	IO_L02P_3	IO_L02P_3	D1	I/O
3	IO_L03N_3	IO_L03N_3	IO_L03N_3	E1	I/O
3	IO_L03P_3	IO_L03P_3	IO_L03P_3	E2	I/O

Table 152: **FG400 Package Pinout *(Cont'd)***

Bank	XC3S1200E XC3S1600E Pin Name	FG400 Ball	Type
3	IP	N5	INPUT
3	IP	P3	INPUT
3	IP	T4	INPUT
3	IP	W1	INPUT
3	IP/VREF_3	K5	VREF
3	IP/VREF_3	P6	VREF
3	VCCO_3	E2	VCCO
3	VCCO_3	H4	VCCO
3	VCCO_3	L2	VCCO
3	VCCO_3	L6	VCCO
3	VCCO_3	P4	VCCO
3	VCCO_3	U2	VCCO
GND	GND	A1	GND
GND	GND	A11	GND
GND	GND	A20	GND
GND	GND	B7	GND
GND	GND	B14	GND
GND	GND	C3	GND
GND	GND	C18	GND
GND	GND	D10	GND
GND	GND	F6	GND
GND	GND	F15	GND
GND	GND	G2	GND
GND	GND	G12	GND
GND	GND	G19	GND
GND	GND	H8	GND
GND	GND	J9	GND
GND	GND	J11	GND
GND	GND	K1	GND
GND	GND	K8	GND
GND	GND	K10	GND
GND	GND	K12	GND
GND	GND	K17	GND
GND	GND	L4	GND
GND	GND	L9	GND
GND	GND	L11	GND
GND	GND	L13	GND
GND	GND	L20	GND
GND	GND	M10	GND
GND	GND	M12	GND
GND	GND	N13	GND
GND	GND	P2	GND
GND	GND	P9	GND

Table 152: **FG400 Package Pinout *(Cont'd)***

Bank	XC3S1200E XC3S1600E Pin Name	FG400 Ball	Type
GND	GND	P19	GND
GND	GND	R6	GND
GND	GND	R15	GND
GND	GND	U11	GND
GND	GND	V3	GND
GND	GND	V18	GND
GND	GND	W7	GND
GND	GND	W14	GND
GND	GND	Y1	GND
GND	GND	Y10	GND
GND	GND	Y20	GND
VCCAUX	DONE	V17	CONFIG
VCCAUX	PROG_B	C2	CONFIG
VCCAUX	TCK	D17	JTAG
VCCAUX	TDI	B3	JTAG
VCCAUX	TDO	B19	JTAG
VCCAUX	TMS	E17	JTAG
VCCAUX	VCCAUX	D11	VCCAUX
VCCAUX	VCCAUX	H12	VCCAUX
VCCAUX	VCCAUX	J7	VCCAUX
VCCAUX	VCCAUX	K4	VCCAUX
VCCAUX	VCCAUX	L17	VCCAUX
VCCAUX	VCCAUX	M14	VCCAUX
VCCAUX	VCCAUX	N9	VCCAUX
VCCAUX	VCCAUX	U10	VCCAUX
VCCINT	VCCINT	H9	VCCINT
VCCINT	VCCINT	H11	VCCINT
VCCINT	VCCINT	H13	VCCINT
VCCINT	VCCINT	J8	VCCINT
VCCINT	VCCINT	J10	VCCINT
VCCINT	VCCINT	J12	VCCINT
VCCINT	VCCINT	K9	VCCINT
VCCINT	VCCINT	K11	VCCINT
VCCINT	VCCINT	L10	VCCINT
VCCINT	VCCINT	L12	VCCINT
VCCINT	VCCINT	M9	VCCINT
VCCINT	VCCINT	M11	VCCINT
VCCINT	VCCINT	M13	VCCINT
VCCINT	VCCINT	N8	VCCINT
VCCINT	VCCINT	N10	VCCINT
VCCINT	VCCINT	N12	VCCINT