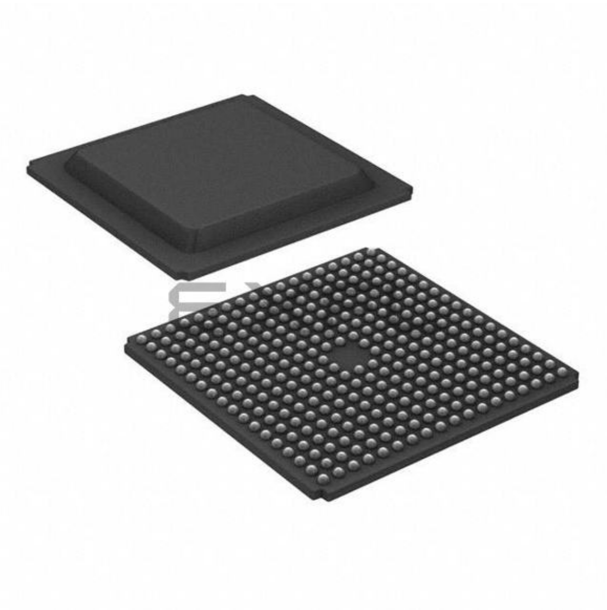

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1164
Number of Logic Elements/Cells	10476
Total RAM Bits	368640
Number of I/O	232
Number of Gates	500000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	320-BGA
Supplier Device Package	320-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s500e-4fgg320i

Package Marking

Figure 2 provides a top marking example for Spartan-3E FPGAs in the quad-flat packages. Figure 3 shows the top marking for Spartan-3E FPGAs in BGA packages except the 132-ball chip-scale package (CP132 and CPG132). The markings for the BGA packages are nearly identical to those for the quad-flat packages, except that the marking is rotated with respect to the ball A1 indicator. Figure 4 shows the top marking for Spartan-3E FPGAs in the CP132 and CPG132 packages.

On the QFP and BGA packages, the optional numerical Stepping Code follows the Lot Code.

The "5C" and "4I" part combinations can have a dual mark of "5C/4I". Devices with a single mark are only guaranteed for the marked speed grade and temperature range. All "5C" and "4I" part combinations use the Stepping 1 production silicon.

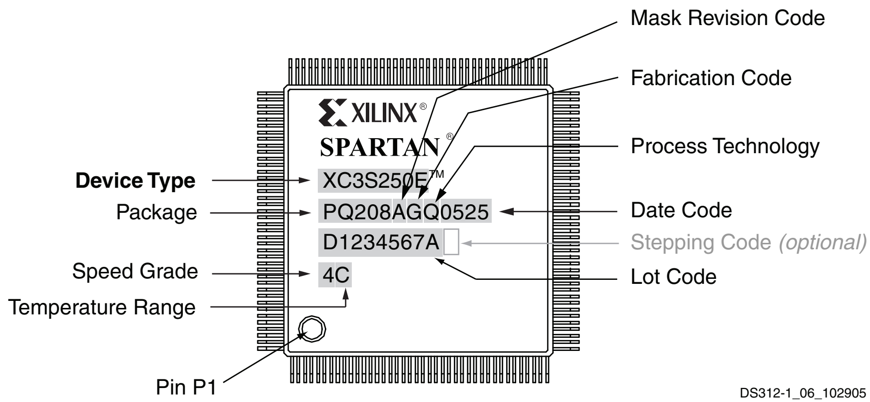


Figure 2: **Spartan-3E QFP Package Marking Example**

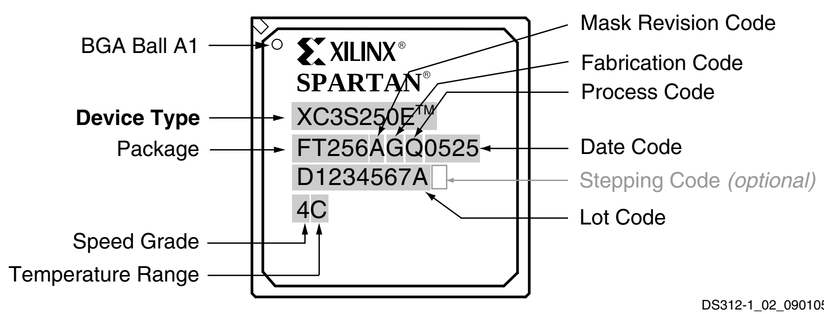


Figure 3: **Spartan-3E BGA Package Marking Example**

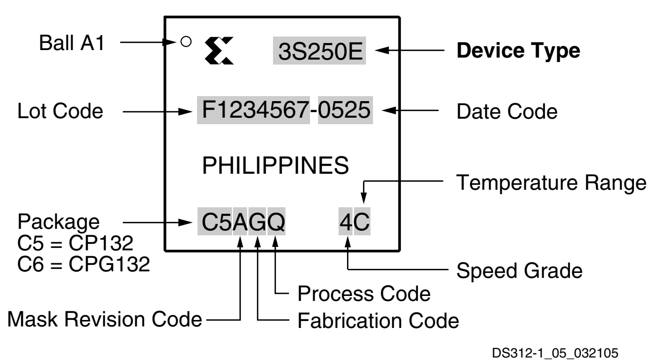


Figure 4: **Spartan-3E CP132 and CPG132 Package Marking Example**

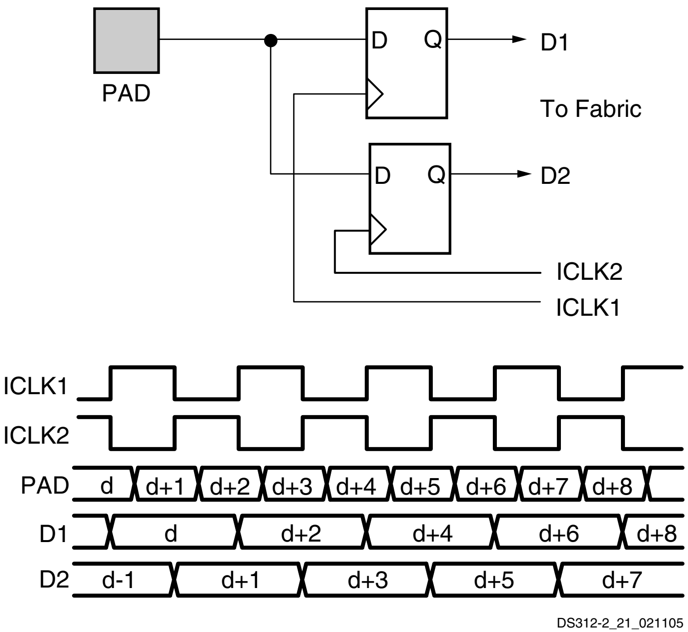


Figure 8: **Input DDR (without Cascade Feature)**

In the Spartan-3E device, the signal D2 can be cascaded into the storage element of the adjacent slave IOB. There it is re-registered to ICLK1, and only then fed to the FPGA fabric where it is now already in the same time domain as D1. Here, the FPGA fabric uses only the clock ICLK1 to process the received data. See Figure 9 for a graphical illustration of this function.

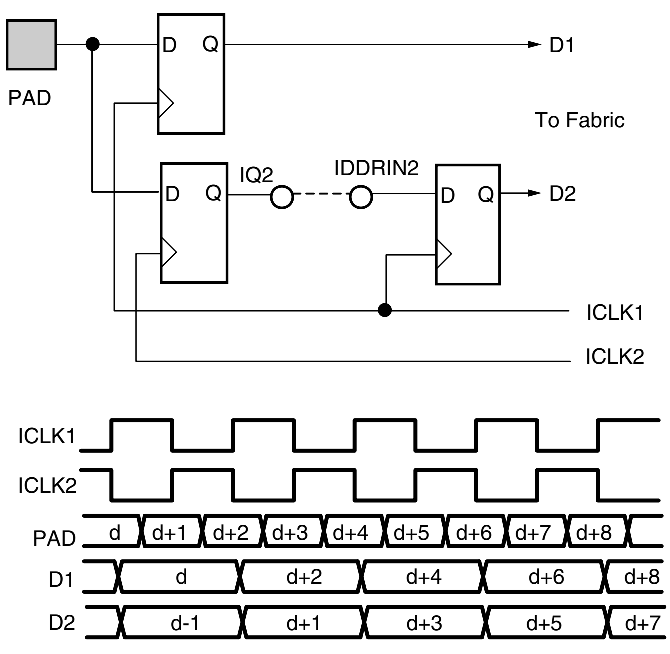


Figure 9: **Input DDR Using Spartan-3E Cascade Feature**

ODDR2

As a DDR output pair, the master IOB registers data coming from the FPGA fabric on the rising edge of OCLK1 (= D1) and the rising edge of OCLK2 (= D2), which is typically the same as the falling edge of OCLK1. These two bits of data are multiplexed by the DDR mux and forwarded to the output pin. The D2 data signal must be re-synchronized from the OCLK1 clock domain to the OCLK2 domain using FPGA slice flip-flops. Placement is critical at high frequencies, because the time available is only one half a clock cycle. See Figure 10 for a graphical illustration of this function.

The C0 or C1 alignment feature of the ODDR2 flip-flop, originally introduced in the Spartan-3E FPGA family, is not recommended or supported in the ISE development software. The ODDR2 flip-flop without the alignment feature remains fully supported. Without the alignment feature, the ODDR2 feature behaves equivalent to the ODDR flip-flop on previous Xilinx FPGA families.

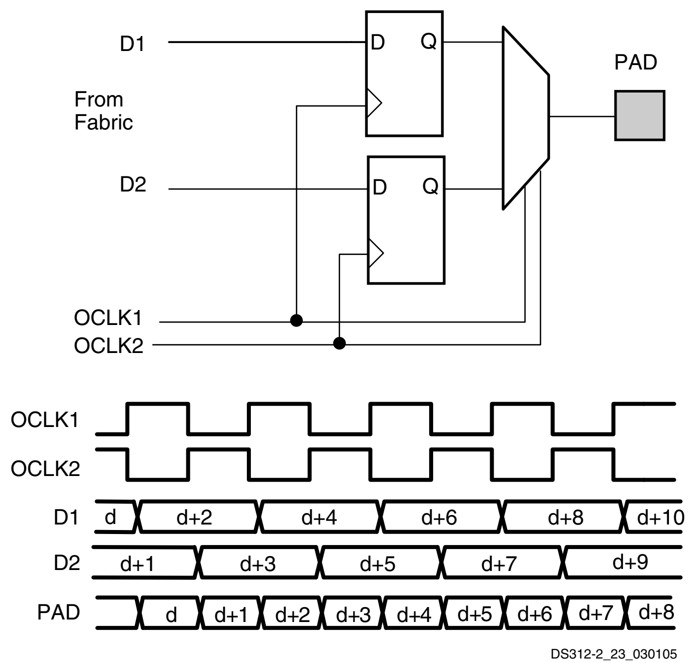


Figure 10: **Output DDR**

SelectIO Signal Standards

The Spartan-3E I/Os feature inputs and outputs that support a wide range of I/O signaling standards (Table 6 and Table 7). The majority of the I/Os also can be used to form differential pairs to support any of the differential signaling standards (Table 7).

To define the I/O signaling standard in a design, set the IOSTANDARD attribute to the appropriate setting. Xilinx provides a variety of different methods for applying the IOSTANDARD for maximum flexibility. For a full description of different methods of applying attributes to control IOSTANDARD, refer to the Xilinx Software Manuals and Help.

Table 30: **Direct Clock Input Connections and Optional External Feedback to Associated DCMs**

Package	Differential Pair		Differential Pair			Differential Pair		Differential Pair	
	N	P	N	P		N	P	N	P
	Pin Number for Single-Ended Input					Pin Number for Single-Ended Input			
VQ100	P91	P90	P89	P88		P86	P85	P84	P83
CP132	B7	A7	C8	B8		A9	B9	C9	A10
TQ144	P131	P130	P129	P128		P126	P125	P123	P122
PQ208	P186	P185	P184	P183		P181	P180	P178	P177
FT256	D8	C8	B8	A8		A9	A10	F9	E9
FG320	D9	C9	B9	B8		A10	B10	E10	D10
FG400	A9	A10	G10	H10		E10	E11	G11	F11
FG484	B11	C11	H11	H12		C12	B12	E12	F12

Associated Global Buffers

GCLK11 GCLK10 GCLK9 GCLK8

Top Left DCM
XC3S100: N/A
XC3S250E, XC3S500E: DCM_X0Y1
XC3S1200E, XC3S1600E: DCM_X1Y3

BUFGMUX_X1Y10 BUFGMUX_X1Y11 BUFGMUX_X2Y10 BUFGMUX_X2Y11

GCLK7 GCLK6 GCLK5 GCLK4

Top Right DCM
XC3S100: DCM_X0Y1
XC3S250E, XC3S500E: DCM_X1Y1
XC3S1200E, XC3S1600E: DCM_X2Y3

H G F E

Clock Line (see Table 41)

D C B A

Bottom Left DCM
XC3S100: N/A
XC3S250E, XC3S500E: DCM_X0Y0
XC3S1200E, XC3S1600E: DCM_X1Y0

GCLK12 GCLK13 GCLK14 GCLK15

BUFGMUX_X1Y0 BUFGMUX_X1Y1 BUFGMUX_X2Y0 BUFGMUX_X2Y1

Bottom Right DCM
XC3S100: DCM_X0Y0
XC3S250E, XC3S500E: DCM_X1Y0
XC3S1200E, XC3S1600E: DCM_X2Y0

GCLK0 GCLK1 GCLK2 GCLK3

Associated Global Buffers

Package	Differential Pair		Differential Pair			Differential Pair		Differential Pair	
	P	N	P	N		P	N	P	N
	Pin Number for Single-Ended Input					Pin Number for Single-Ended Input			
VQ100	P32	P33	P35	P36		P38	P39	P40	P41
CP132	M4	N4	M5	N5		M6	N6	P6	P7
TQ144	P50	P51	P53	P54		P56	P57	P58	P59
PQ208	P74	P75	P77	P78		P80	P81	P82	P83
FT256	M8	L8	N8	P8		T9	R9	P9	N9
FG320	N9	M9	U9	V9		U10	T10	R10	P10
FG400	W9	W10	R10	P10		P11	P12	V10	V11
FG484	V11	U11	R11	T11		R12	P12	Y12	W12

FIXED Phase Shift Mode

The FIXED phase shift mode shifts the DCM outputs by a fixed amount (T_{PS}), controlled by the user-specified PHASE_SHIFT attribute. The PHASE_SHIFT value (shown as P in Figure 44) must be an integer ranging from –255 to +255. PHASE_SHIFT specifies a phase shift delay as a fraction of the T_{CLKIN}. The phase shift behavior is different between ISE 8.1, Service Pack 3 and prior software versions, as described below.

Design Note

Prior to ISE 8.1i, Service Pack 3, the FIXED phase shift feature operated differently than the Spartan-3 DCM design primitive and simulation model. Designs using software prior to ISE 8.1i, Service Pack 3 require recompilation using the latest ISE software release. The following Answer Record contains additional information:

http://www.xilinx.com/support/answers/23153.htm.

FIXED Phase Shift using ISE 8.1i, Service Pack 3 and later: See Equation 2. The value corresponds to a phase shift range of –360° to +360°, which matches behavior of the Spartan-3 DCM design primitive and simulation model.

$$t_{PS} = \left(\frac{PHASESHIFT}{256}\right) \bullet T_{CLKIN} \qquad \textit{Eq 2}$$

FIXED Phase Shift prior to ISE 8.1i, Service Pack 3: See Equation 3. The value corresponds to a phase shift range of –180° to +180° degrees, which is different from the Spartan-3 DCM design primitive and simulation model. Designs created prior to ISE 8.1i, Service Pack 3 must be recompiled using the most recent ISE development software.

$$t_{PS} = \left(\frac{PHASESHIFT}{512}\right) \bullet T_{CLKIN} \qquad \textit{Eq 3}$$

When the PHASE_SHIFT value is zero, CLKFB and CLKIN are in phase, the same as when the PS unit is disabled. When the PHASE_SHIFT value is positive, the DCM outputs are shifted later in time with respect to CLKIN input. When the attribute value is negative, the DCM outputs are shifted earlier in time with respect to CLKIN.

Figure 44b illustrates the relationship between CLKFB and CLKIN in the Fixed Phase mode. In the Fixed Phase mode, the PSEN, PSCLK, and PSINCDEC inputs are not used and must be tied to GND.

Equation 2 or Equation 3 applies only to FIXED phase shift mode. The VARIABLE phase shift mode operates differently.

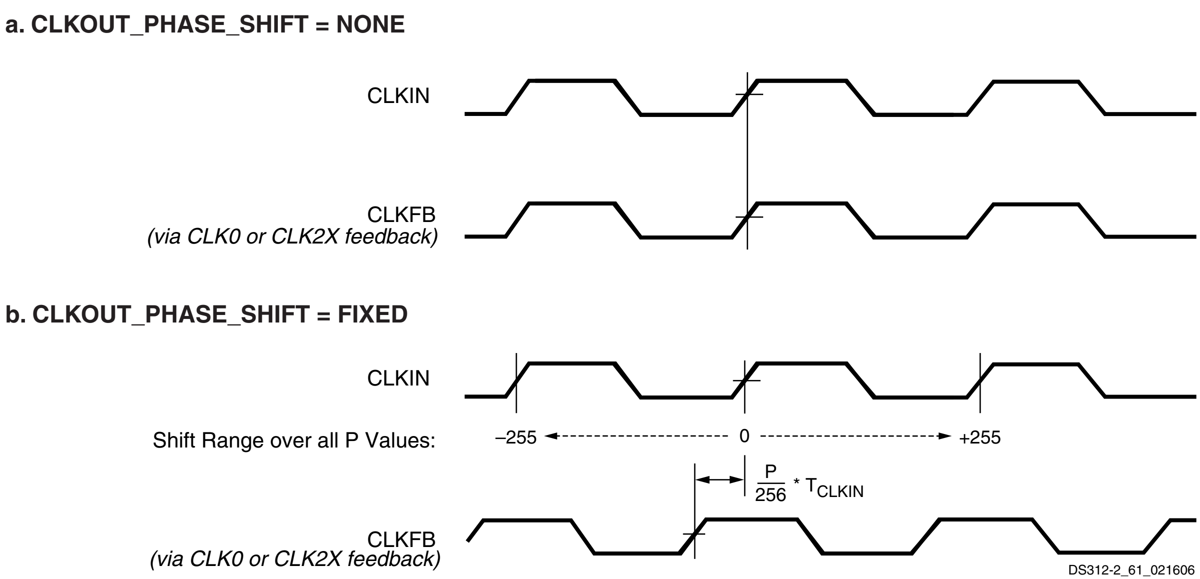
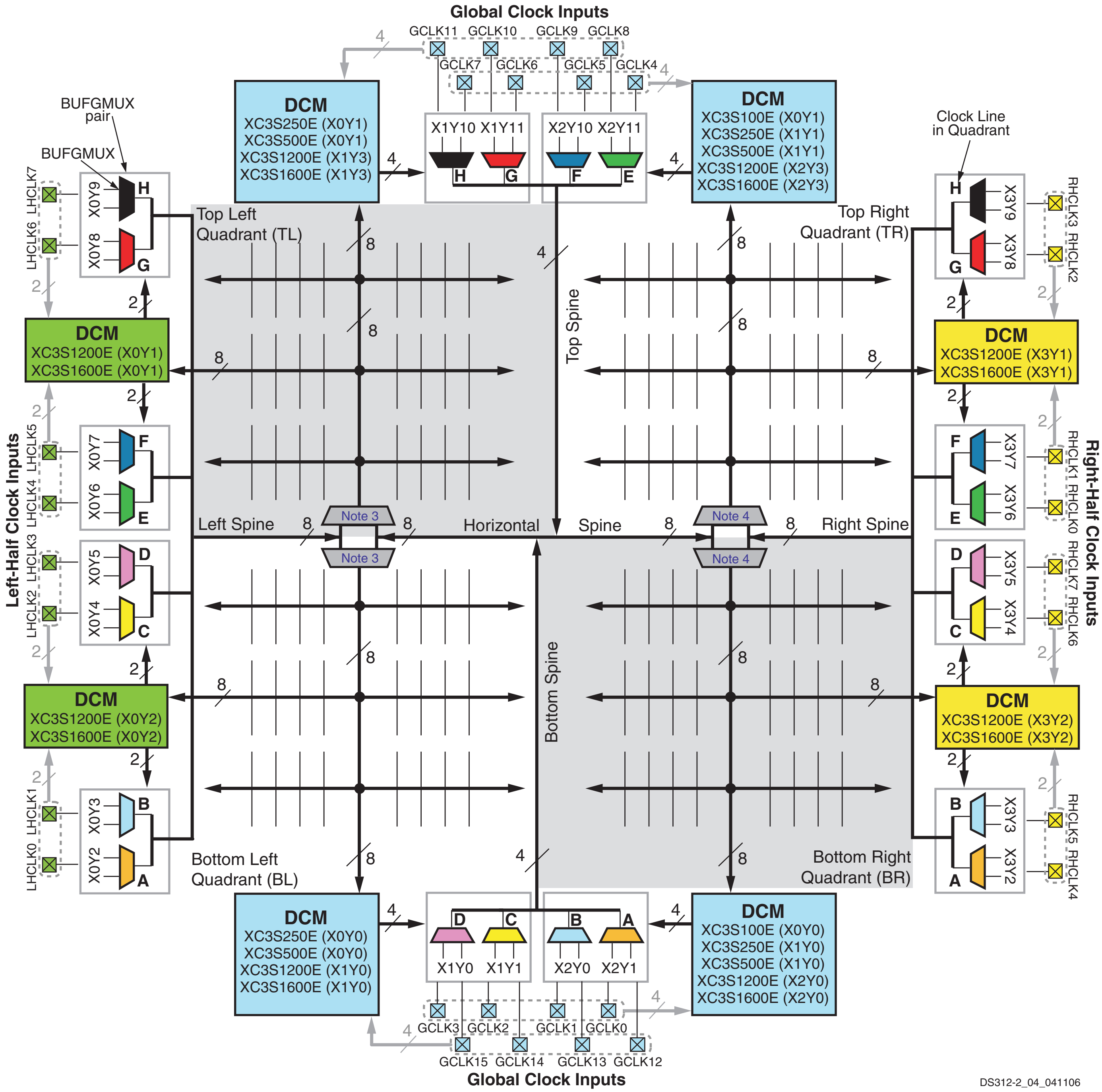


Figure 44: **NONE and FIXED Phase Shifter Waveforms (ISE 8.1i, Service Pack 3 and later)**



Notes:

1. The diagram presents electrical connectivity. The diagram locations do not necessarily match the physical location on the device, although the coordinate locations shown are correct.
2. Number of DCMs and locations of these DCM varies for different device densities. The left and right DCMs are only in the XC3S1200E and XC3S1600E. The XC3S100E has only two DCMs, one on the top right and one on the bottom right of the die.
3. See Figure 47a, which shows how the eight clock lines are multiplexed on the left-hand side of the device.
4. See Figure 47b, which shows how the eight clock lines are multiplexed on the right-hand side of the device.
5. For best direct clock inputs to a particular clock buffer, not a DCM, see Table 41.
6. For best direct clock inputs to a particular DCM, not a BUFGMUX, see Table 30, Table 31, and Table 32. Direct pin inputs to a DCM are shown in gray.

Figure 45: **Spartan-3E Internal Quadrant-Based Clock Network (Electrical Connectivity View)**

Configuration Bitstream Image Sizes

A specific Spartan-3E part type always requires a constant number of configuration bits, regardless of design complexity, as shown in Table 45. The configuration file size for a multiple-FPGA daisy-chain design roughly equals the sum of the individual file sizes.

Table 45: **Number of Bits to Program a Spartan-3E FPGA (Uncompressed Bitstreams)**

Spartan-3E FPGA	Number of Configuration Bits
XC3S100E	581,344
XC3S250E	1,353,728
XC3S500E	2,270,208
XC3S1200E	3,841,184
XC3S1600E	5,969,696

Pin Behavior During Configuration

For additional information, refer to the “Configuration Pins and Behavior during Configuration” chapter in UG332.

Table 46 shows how various pins behave during the FPGA configuration process. The actual behavior depends on the values applied to the M2, M1, and M0 mode select pins and the HSWAP pin. The mode select pins determine which of the I/O pins are borrowed during configuration and how they function. In JTAG configuration mode, no user-I/O pins are borrowed for configuration.

All user-I/O pins, input-only pins, and dual-purpose pins that are not actively involved in the currently-select configuration mode are high impedance (floating, three-stated, Hi-Z) during the configuration process. These pins are indicated in Table 46 as gray shaded table entries or cells.

The HSWAP input controls whether all user-I/O pins, input-only pins, and dual-purpose pins have a pull-up resistor to the supply rail or not. When HSWAP is Low, each pin has an internal pull-up resistor that is active throughout configuration. After configuration, pull-up and pull-down resistors are available in the FPGA application as described in Pull-Up and Pull-Down Resistors.

The yellow-shaded table entries or cells represent pins where the pull-up resistor is always enabled during configuration, regardless of the HSWAP input. The post-configuration behavior of these pins is defined by Bitstream Generator options as defined in Table 69.

Table 46: **Pin Behavior during Configuration**

Pin Name	Master Serial	SPI (Serial Flash)	BPI (Parallel NOR Flash)	JTAG	Slave Parallel	Slave Serial	I/O Bank[3]
IO* (user-I/O) IP* (input-only)							-
TDI	TDI	TDI	TDI	TDI	TDI	TDI	V_{CCAUX}
TMS	TMS	TMS	TMS	TMS	TMS	TMS	V_{CCAUX}
TCK	TCK	TCK	TCK	TCK	TCK	TCK	V_{CCAUX}
TDO	TDO	TDO	TDO	TDO	TDO	TDO	V_{CCAUX}
PROG_B	PROG_B	PROG_B	PROG_B	PROG_B	PROG_B	PROG_B	V_{CCAUX}
DONE	DONE	DONE	DONE	DONE	DONE	DONE	V_{CCAUX}
HSWAP	HSWAP	HSWAP	HSWAP	HSWAP	HSWAP	HSWAP	0
M2	0	0	0	1	1	1	2
M1	0	0	1	0	1	1	2
M0	0	1	0 = Up 1 = Down	1	0	1	2
CCLK	CCLK (I/O)	CCLK (I/O)	CCLK (I/O)		CCLK (I)	CCLK (I)	2
INIT_B	INIT_B	INIT_B	INIT_B		INIT_B	INIT_B	2
CSO_B		CSO_B	CSO_B		CSO_B		2
DOUT/BUSY	DOUT	DOUT	BUSY		BUSY	DOUT	2
MOSI/CSI_B		MOSI	CSI_B		CSI_B		2
D7			D7		D7		2
D6			D6		D6		2
D5			D5		D5		2
D4			D4		D4		2
D3			D3		D3		2
D2			D2		D2		2
D1			D1		D1		2

Daisy-Chaining

If the application requires multiple FPGAs with different configurations, then configure the FPGAs using a daisy chain, as shown in Figure 57. Daisy-chaining from a single SPI serial Flash PROM is supported in Stepping 1 devices. It is not supported in Stepping 0 devices. Use SPI Flash mode (M[2:0] = <0:0:1>) for the FPGA connected to the Platform Flash PROM and Slave Serial mode (M[2:0] = <1:1:1>) for all other FPGAs in the daisy-chain. After the master FPGA—the FPGA on the left in the diagram—finishes loading its configuration data from the SPI Flash PROM, the master device uses its DOUT output pin to supply data to the next device in the daisy-chain, on the falling CCLK edge.

Design Note

SPI mode daisy chains are supported only in Stepping 1 silicon versions.

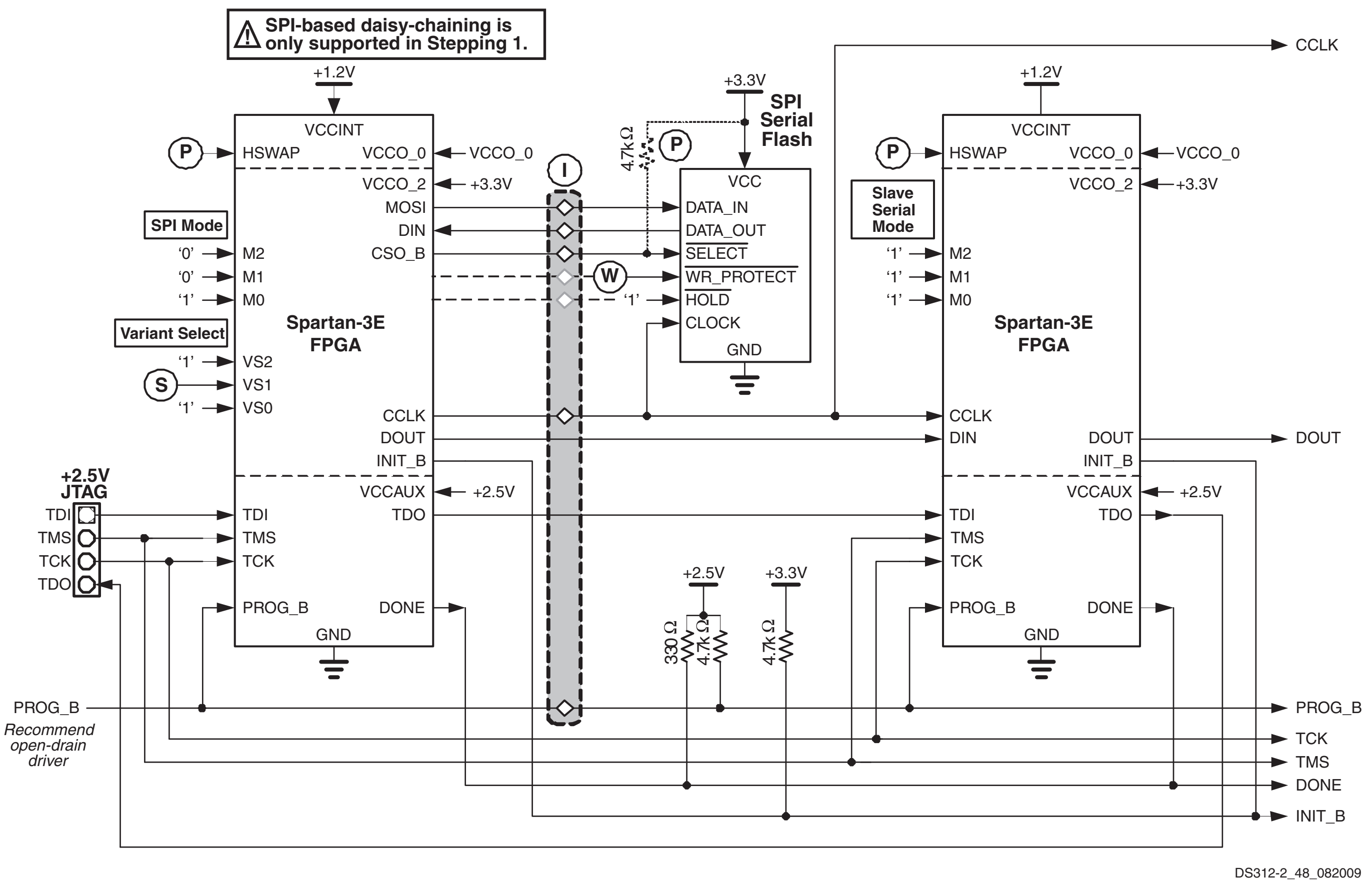


Figure 57: **Daisy-Chaining from SPI Flash Mode (Stepping 1)**

Programming Support

For successful daisy-chaining, the ***DONE_cycle*** configuration option must be set to cycle 5 or sooner. The default cycle is 4. See Table 69 and the Start-Up section for additional information.

Ⓘ In production applications, the SPI Flash PROM is usually pre-programmed before it is mounted on the printed circuit board. The Xilinx ISE development software produces industry-standard programming files that can be used with third-party gang programmers. Consult your specific SPI Flash vendor for recommended production programming solutions.

In-system programming support is available from some third-party PROM programmers using a socket adapter with attached wires. To gain access to the SPI Flash signals, drive the FPGA's PROG_B input Low with an open-drain driver. This action places all FPGA I/O pins, including those attached to the SPI Flash, in high-impedance (Hi-Z). If the HSWAP input is Low, the I/Os have pull-up resistors to the V_{CCO} input on their respective I/O bank. The external programming hardware then has direct access to the SPI Flash pins. The programming access points are highlighted in the gray box in Figure 53, Figure 54, and Figure 57.

Beginning with the Xilinx ISE 8.2i software release, the iMPACT programming utility provides direct, in-system prototype programming support for STMicro M25P-series

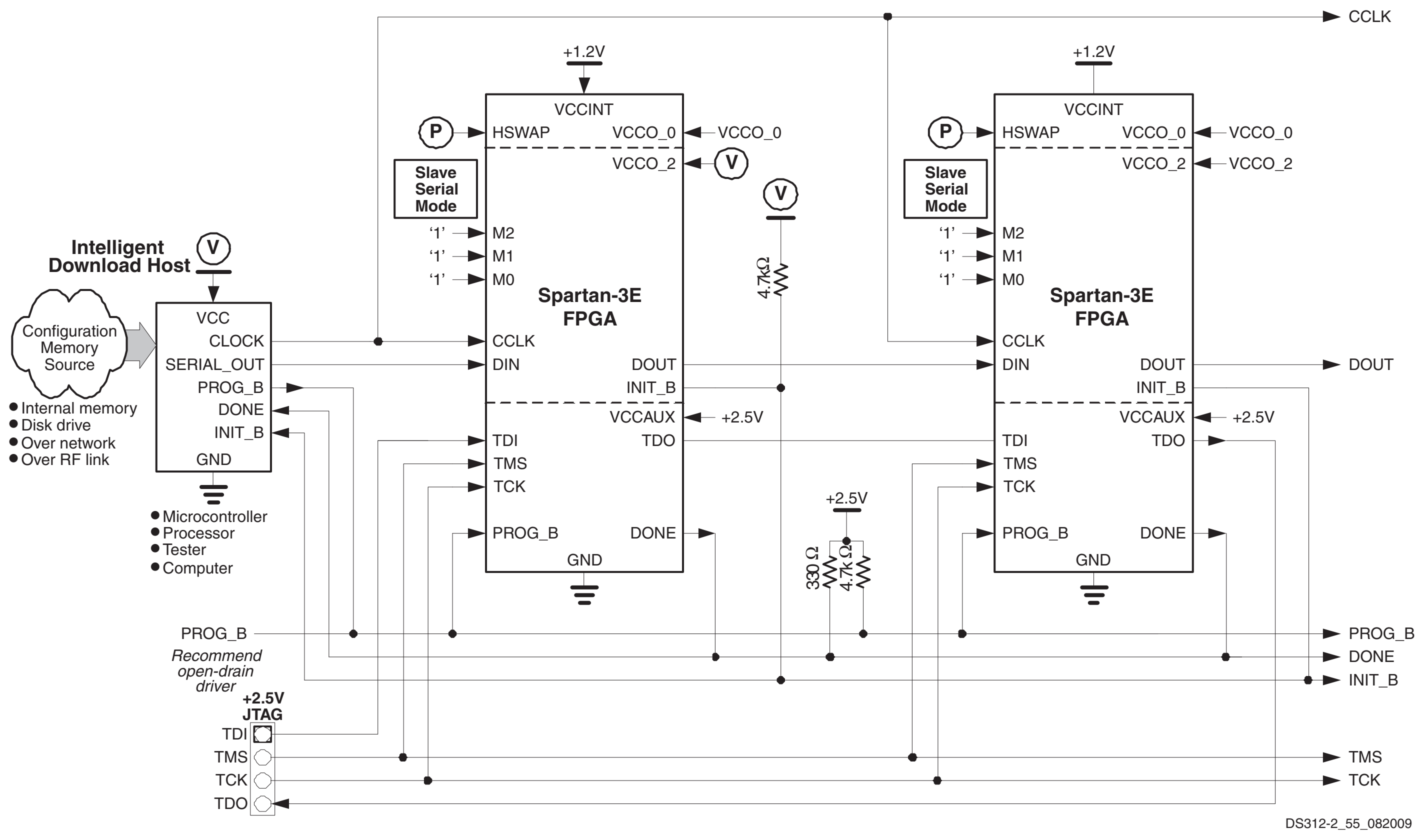


Figure 64: **Daisy-Chaining using Slave Serial Mode**

JTAG Mode

For additional information, refer to the “JTAG Configuration Mode and Boundary-Scan” chapter in UG332.

The Spartan-3E FPGA has a dedicated four-wire IEEE 1149.1/1532 JTAG port that is always available any time the FPGA is powered and regardless of the mode pin settings. However, when the FPGA mode pins are set for JTAG mode (M[2:0] = <1:0:1>), the FPGA waits to be configured via the JTAG port after a power-on event or when PROG_B is asserted. Selecting the JTAG mode simply disables the other configuration modes. No other pins are required as part of the configuration interface.

Figure 65 illustrates a JTAG-only configuration interface. The JTAG interface is easily cascaded to any number of FPGAs by connecting the TDO output of one device to the TDI input of the next device in the chain. The TDO output of the last device in the chain loops back to the port connector.

Design Note

If using software versions prior to ISE 9.1.01i, avoid configuring the FPGA using JTAG if...

- the mode pins are set for a Master mode
- the attached Master mode PROM contains a valid FPGA configuration bitstream.

The FPGA bitstream may be corrupted and the DONE pin may go High. The following Answer Record contains additional information.

http://www.xilinx.com/support/answers/22255.htm

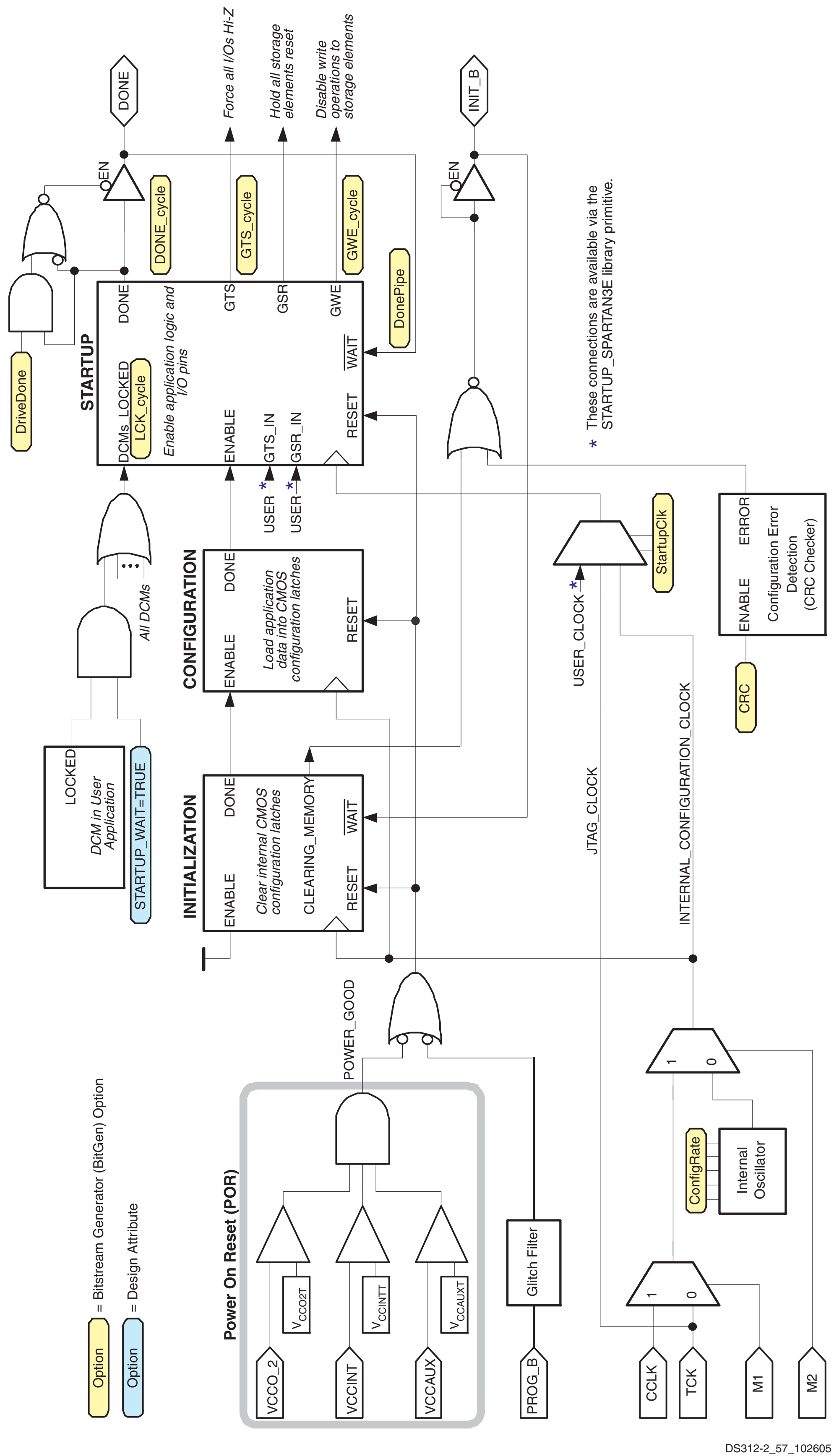


Figure 66: **Generalized Spartan-3E FPGA Configuration Logic Block Diagram**

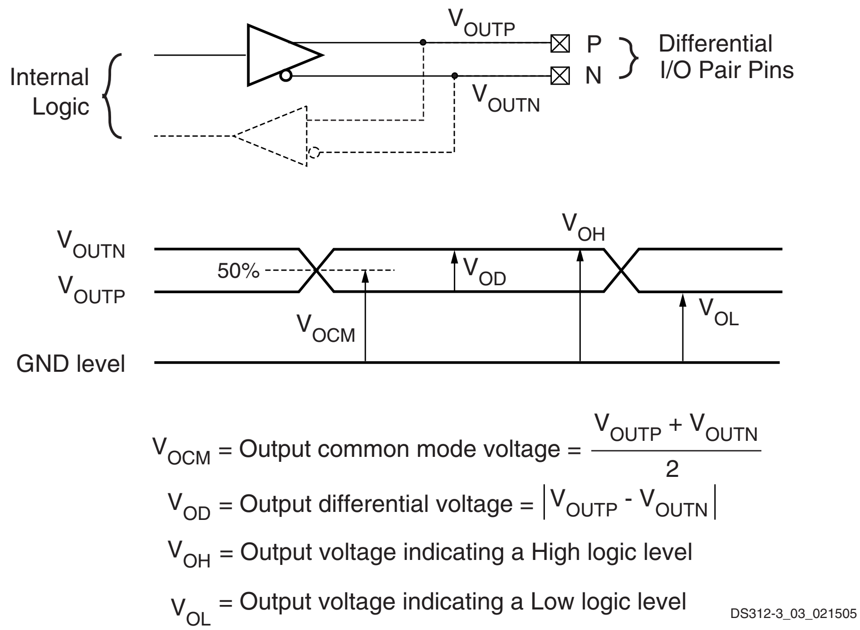


Figure 70: **Differential Output Voltages**

Table 83: **DC Characteristics of User I/Os Using Differential Signal Standards**

IOSTANDARD Attribute	V_{OD}			ΔV_{OD}		V_{OCM}			ΔV_{OCM}		V_{OH}	V_{OL}
	Min (mV)	Typ (mV)	Max (mV)	Min (mV)	Max (mV)	Min (V)	Typ (V)	Max (V)	Min (mV)	Max (mV)	Min (V)	Max (V)
LVDS_25	250	350	450	–	–	1.125	–	1.375	–	–	–	–
BLVDS_25	250	350	450	–	–	–	1.20	–	–	–	–	–
MINI_LVDS_25	300	–	600	–	50	1.0	–	1.4	–	50	–	–
RSDS_25	100	–	400	–	–	1.1	–	1.4	–	–	–	–
DIFF_HSTL_I_18	–	–	–	–	–	–	–	–	–	–	$V_{CCO} - 0.4$	0.4
DIFF_HSTL_III_18	–	–	–	–	–	–	–	–	–	–	$V_{CCO} - 0.4$	0.4
DIFF_SSTL18_I	–	–	–	–	–	–	–	–	–	–	$V_{TT} + 0.475$	$V_{TT} - 0.475$
DIFF_SSTL2_I	–	–	–	–	–	–	–	–	–	–	$V_{TT} + 0.61$	$V_{TT} - 0.61$

Notes:
1. The numbers in this table are based on the conditions set forth in Table 77 and Table 82.
2. Output voltage measurements for all differential standards are made with a termination resistor (R_T) of 100Ω across the N and P pins of the differential signal pair. The exception is for BLVDS, shown in Figure 71.
3. At any given time, no more than two of the following differential output standards may be assigned to an I/O bank: LVDS_25, RSDS_25, MINI_LVDS_25

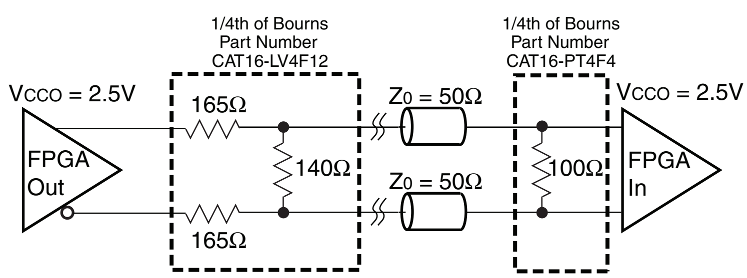


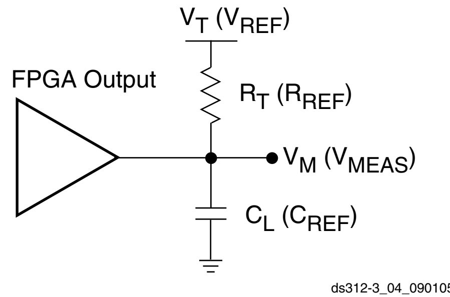
Figure 71: **External Termination Resistors for BLVDS Transmitter and BLVDS Receiver**

Timing Measurement Methodology

When measuring timing parameters at the programmable I/Os, different signal standards call for different test conditions. Table 95 lists the conditions to use for each standard.

The method for measuring Input timing is as follows: A signal that swings between a Low logic level of V_L and a High logic level of V_H is applied to the Input under test. Some standards also require the application of a bias voltage to the V_{REF} pins of a given bank to properly set the input-switching threshold. The measurement point of the Input signal (V_M) is commonly located halfway between V_L and V_H.

The Output test setup is shown in Figure 72. A termination voltage V_T is applied to the termination resistor R_T, the other end of which is connected to the Output. For each standard, R_T and V_T generally take on the standard values recommended for minimizing signal reflections. If the standard does not ordinarily use terminations (e.g., LVCMOS, LVTTL), then R_T is set to 1MΩ to indicate an open connection, and V_T is set to zero. The same measurement point (V_M) that was used at the Input is also used at the Output.



Notes:

1. The names shown in parentheses are used in the IBIS file.

Figure 72: **Output Test Setup**

Table 95: **Test Methods for Timing Measurement at I/Os**

Signal Standard (IOSTANDARD)		Inputs			Outputs		Inputs and Outputs
		V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
Single-Ended							
LVTTL		-	0	3.3	1M	0	1.4
LVCMOS33		-	0	3.3	1M	0	1.65
LVCMOS25		-	0	2.5	1M	0	1.25
LVCMOS18		-	0	1.8	1M	0	0.9
LVCMOS15		-	0	1.5	1M	0	0.75
LVCMOS12		-	0	1.2	1M	0	0.6
PCI33_3	Rising	-	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
PCI66_3	Rising	-	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
HSTL_I_18		0.9	$V_{REF} - 0.5$	$V_{REF} + 0.5$	50	0.9	V_{REF}
HSTL_III_18		1.1	$V_{REF} - 0.5$	$V_{REF} + 0.5$	50	1.8	V_{REF}
SSTL18_I		0.9	$V_{REF} - 0.5$	$V_{REF} + 0.5$	50	0.9	V_{REF}
SSTL2_I		1.25	$V_{REF} - 0.75$	$V_{REF} + 0.75$	50	1.25	V_{REF}
Differential							
LVDS_25		-	$V_{ICM} - 0.125$	$V_{ICM} + 0.125$	50	1.2	V_{ICM}
BLVDS_25		-	$V_{ICM} - 0.125$	$V_{ICM} + 0.125$	1M	0	V_{ICM}
MINI_LVDS_25		-	$V_{ICM} - 0.125$	$V_{ICM} + 0.125$	50	1.2	V_{ICM}
LVPECL_25		-	$V_{ICM} - 0.3$	$V_{ICM} + 0.3$	1M	0	V_{ICM}
RSDS_25		-	$V_{ICM} - 0.1$	$V_{ICM} + 0.1$	50	1.2	V_{ICM}

Table 121: **Configuration Timing Requirements for Attached Parallel NOR Flash**

Symbol	Description	Requirement	Units
T_{CE} (t_{ELQV})	Parallel NOR Flash PROM chip-select time	$T_{CE} \leq T_{INITADDR}$	ns
T_{OE} (t_{GLQV})	Parallel NOR Flash PROM output-enable time	$T_{OE} \leq T_{INITADDR}$	ns
T_{ACC} (t_{AVQV})	Parallel NOR Flash PROM read access time	$T_{ACC} \leq 0.5 T_{CCLKn(min)} - T_{CCO} - T_{DCC} - PCB$	ns
T_{BYTE} (t_{FLQV}, t_{FHQV})	For x8/x16 PROMs only: BYTE# to output valid time(3)	$T_{BYTE} \leq T_{INITADDR}$	ns

Notes:

1. These requirements are for successful FPGA configuration in BPI mode, where the FPGA provides the CCLK frequency. The post configuration timing can be different to support the specific needs of the application loaded int o the FPGA and the resulting clock source.
2. Subtract additional printed circuit board routing delay as required by the application.
3. The initial BYTE# timing can be extended using an external, appropriately sized pull-down resistor on the FPGA's LDC2 pin. The resistor value also depends on whether the FPGA's HSWAP pin is High or Low.

Table 122: **MultiBoot Trigger (MBT) Timing**

Symbol	Description	Minimum	Maximum	Units
T_{MBT}	MultiBoot Trigger (MBT) Low pulse width required to initiate MultiBoot reconfiguration	300	∞	ns

Notes:

1. MultiBoot re-configuration starts on the rising edge after MBT is Low for at least the prescribed minimum period.

Table 133: **CP132 Package Pinout *(Cont'd)***

Bank	XC3S100E Pin Name	XC3S250E XC3S500E Pin Name	CP132 Ball	Type
0	VCCO_0	VCCO_0	B10	VCCO
1	IO/A0	IO/A0	F12	DUAL
1	IO/VREF_1	IO/VREF_1	K13	VREF
1	IO_L01N_1/A15	IO_L01N_1/A15	N14	DUAL
1	IO_L01P_1/A16	IO_L01P_1/A16	N13	DUAL
1	IO_L02N_1/A13	IO_L02N_1/A13	M13	DUAL
1	IO_L02P_1/A14	IO_L02P_1/A14	M12	DUAL
1	IO_L03N_1/A11	IO_L03N_1/A11	L14	DUAL
1	IO_L03P_1/A12	IO_L03P_1/A12	L13	DUAL
1	IO_L04N_1/A9/RHCLK1	IO_L04N_1/A9/RHCLK1	J12	RHCLK/DUAL
1	IO_L04P_1/A10/RHCLK0	IO_L04P_1/A10/RHCLK0	K14	RHCLK/DUAL
1	IO_L05N_1/A7/RHCLK3/TRDY1	IO_L05N_1/A7/RHCLK3/TRDY1	J14	RHCLK/DUAL
1	IO_L05P_1/A8/RHCLK2	IO_L05P_1/A8/RHCLK2	J13	RHCLK/DUAL
1	IO_L06N_1/A5/RHCLK5	IO_L06N_1/A5/RHCLK5	H12	RHCLK/DUAL
1	IO_L06P_1/A6/RHCLK4/IRDY1	IO_L06P_1/A6/RHCLK4/IRDY1	H13	RHCLK/DUAL
1	IO_L07N_1/A3/RHCLK7	IO_L07N_1/A3/RHCLK7	G13	RHCLK/DUAL
1	IO_L07P_1/A4/RHCLK6	IO_L07P_1/A4/RHCLK6	G14	RHCLK/DUAL
1	IO_L08N_1/A1	IO_L08N_1/A1	F13	DUAL
1	IO_L08P_1/A2	IO_L08P_1/A2	F14	DUAL
1	IO_L09N_1/LDC0	IO_L09N_1/LDC0	D12	DUAL
1	IO_L09P_1/HDC	IO_L09P_1/HDC	D13	DUAL
1	IO_L10N_1/LDC2	IO_L10N_1/LDC2	C13	DUAL
1	IO_L10P_1/LDC1	IO_L10P_1/LDC1	C14	DUAL
1	IP/VREF_1	IP/VREF_1	G12	VREF
1	VCCO_1	VCCO_1	E13	VCCO
1	VCCO_1	VCCO_1	M14	VCCO
2	IO/D5	IO/D5	P4	DUAL
2	IO/M1	IO/M1	N7	DUAL
2	IP/VREF_2	IO/VREF_2	P11	***100E:*** VREF(INPUT) ***Others:*** VREF(I/O)
2	IO_L01N_2/INIT_B	IO_L01N_2/INIT_B	N1	DUAL
2	IO_L01P_2/CSO_B	IO_L01P_2/CSO_B	M2	DUAL
2	IO_L02N_2/MOSI/CSI_B	IO_L02N_2/MOSI/CSI_B	N2	DUAL
2	IO_L02P_2/DOUT/BUSY	IO_L02P_2/DOUT/BUSY	P1	DUAL
2	IO_L03N_2/D6/GCLK13	IO_L03N_2/D6/GCLK13	N4	DUAL/GCLK
2	IO_L03P_2/D7/GCLK12	IO_L03P_2/D7/GCLK12	M4	DUAL/GCLK
2	IO_L04N_2/D3/GCLK15	IO_L04N_2/D3/GCLK15	N5	DUAL/GCLK
2	IO_L04P_2/D4/GCLK14	IO_L04P_2/D4/GCLK14	M5	DUAL/GCLK
2	IO_L06N_2/D1/GCLK3	IO_L06N_2/D1/GCLK3	P7	DUAL/GCLK
2	IO_L06P_2/D2/GCLK2	IO_L06P_2/D2/GCLK2	P6	DUAL/GCLK
2	IO_L07N_2/DIN/D0	IO_L07N_2/DIN/D0	N8	DUAL
2	IO_L07P_2/M0	IO_L07P_2/M0	P8	DUAL
2	N.C. (◆)	IO_L08N_2/A22	M9	***100E:*** N.C. ***Others:*** DUAL

Table 137: **TQ144 Package Pinout *(Cont'd)***

Bank	XC3S100E Pin Name	XC3S250E Pin Name	TQ144 Pin	Type
GND	GND	GND	P27	GND
GND	GND	GND	P37	GND
GND	GND	GND	P46	GND
GND	GND	GND	P55	GND
GND	GND	GND	P61	GND
GND	GND	GND	P73	GND
GND	GND	GND	P90	GND
GND	GND	GND	P99	GND
GND	GND	GND	P118	GND
GND	GND	GND	P127	GND
GND	GND	GND	P133	GND
VCCAUX	DONE	DONE	P72	CONFIG
VCCAUX	PROG_B	PROG_B	P1	CONFIG
VCCAUX	TCK	TCK	P110	JTAG
VCCAUX	TDI	TDI	P144	JTAG
VCCAUX	TDO	TDO	P109	JTAG
VCCAUX	TMS	TMS	P108	JTAG
VCCAUX	VCCAUX	VCCAUX	P30	VCCAUX
VCCAUX	VCCAUX	VCCAUX	P65	VCCAUX
VCCAUX	VCCAUX	VCCAUX	P102	VCCAUX
VCCAUX	VCCAUX	VCCAUX	P137	VCCAUX
VCCINT	VCCINT	VCCINT	P9	VCCINT
VCCINT	VCCINT	VCCINT	P45	VCCINT
VCCINT	VCCINT	VCCINT	P80	VCCINT
VCCINT	VCCINT	VCCINT	P115	VCCINT

PQ208: 208-pin Plastic Quad Flat Package

The 208-pin plastic quad flat package, PQ208, supports two different Spartan-3E FPGAs, including the XC3S250E and the XC3S500E.

Table 141 lists all the PQ208 package pins. They are sorted by bank number and then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at:

http://www.xilinx.com/support/documentation/data_sheets/s3e_pin.zip

Pinout Table

Table 141: **PQ208 Package Pinout**

Bank	XC3S250E XC3S500E Pin Name	PQ208 Pin	Type
0	IO	P187	I/O
0	IO/VREF_0	P179	VREF
0	IO_L01N_0	P161	I/O
0	IO_L01P_0	P160	I/O
0	IO_L02N_0/VREF_0	P163	VREF
0	IO_L02P_0	P162	I/O
0	IO_L03N_0	P165	I/O
0	IO_L03P_0	P164	I/O
0	IO_L04N_0/VREF_0	P168	VREF
0	IO_L04P_0	P167	I/O
0	IO_L05N_0	P172	I/O
0	IO_L05P_0	P171	I/O
0	IO_L07N_0/GCLK5	P178	GCLK
0	IO_L07P_0/GCLK4	P177	GCLK
0	IO_L08N_0/GCLK7	P181	GCLK
0	IO_L08P_0/GCLK6	P180	GCLK
0	IO_L10N_0/GCLK11	P186	GCLK
0	IO_L10P_0/GCLK10	P185	GCLK
0	IO_L11N_0	P190	I/O
0	IO_L11P_0	P189	I/O
0	IO_L12N_0/VREF_0	P193	VREF
0	IO_L12P_0	P192	I/O
0	IO_L13N_0	P197	I/O
0	IO_L13P_0	P196	I/O
0	IO_L14N_0/VREF_0	P200	VREF
0	IO_L14P_0	P199	I/O
0	IO_L15N_0	P203	I/O

Table 141: **PQ208 Package Pinout *(Cont'd)***

Bank	XC3S250E XC3S500E Pin Name	PQ208 Pin	Type
0	IO_L15P_0	P202	I/O
0	IO_L16N_0/HSWAP	P206	DUAL
0	IO_L16P_0	P205	I/O
0	IP	P159	INPUT
0	IP	P169	INPUT
0	IP	P194	INPUT
0	IP	P204	INPUT
0	IP_L06N_0	P175	INPUT
0	IP_L06P_0	P174	INPUT
0	IP_L09N_0/GCLK9	P184	GCLK
0	IP_L09P_0/GCLK8	P183	GCLK
0	VCCO_0	P176	VCCO
0	VCCO_0	P191	VCCO
0	VCCO_0	P201	VCCO
1	IO_L01N_1/A15	P107	DUAL
1	IO_L01P_1/A16	P106	DUAL
1	IO_L02N_1/A13	P109	DUAL
1	IO_L02P_1/A14	P108	DUAL
1	IO_L03N_1/VREF_1	P113	VREF
1	IO_L03P_1	P112	I/O
1	IO_L04N_1	P116	I/O
1	IO_L04P_1	P115	I/O
1	IO_L05N_1/A11	P120	DUAL
1	IO_L05P_1/A12	P119	DUAL
1	IO_L06N_1/VREF_1	P123	VREF
1	IO_L06P_1	P122	I/O
1	IO_L07N_1/A9/RHCLK1	P127	RHCLK/DUAL
1	IO_L07P_1/A10/RHCLK0	P126	RHCLK/DUAL
1	IO_L08N_1/A7/RHCLK3	P129	RHCLK/DUAL
1	IO_L08P_1/A8/RHCLK2	P128	RHCLK/DUAL
1	IO_L09N_1/A5/RHCLK5	P133	RHCLK/DUAL
1	IO_L09P_1/A6/RHCLK4	P132	RHCLK/DUAL
1	IO_L10N_1/A3/RHCLK7	P135	RHCLK/DUAL
1	IO_L10P_1/A4/RHCLK6	P134	RHCLK/DUAL
1	IO_L11N_1/A1	P138	DUAL
1	IO_L11P_1/A2	P137	DUAL
1	IO_L12N_1/A0	P140	DUAL
1	IO_L12P_1	P139	I/O
1	IO_L13N_1	P145	I/O
1	IO_L13P_1	P144	I/O
1	IO_L14N_1	P147	I/O
1	IO_L14P_1	P146	I/O

Table 148: **FG320 Package Pinout *(Cont'd)***

Bank	XC3S500E Pin Name	XC3S1200E Pin Name	XC3S1600E Pin Name	FG320 Ball	Type
3	N.C. (◆)	IO_L22P_3	IO_L22P_3	P3	**500E:** N.C. **1200E:** I/O **1600E:** I/O
3	IO_L23N_3	IO_L23N_3	IO_L23N_3	R2	I/O
3	IO_L23P_3	IO_L23P_3	IO_L23P_3	R3	I/O
3	IO_L24N_3	IO_L24N_3	IO_L24N_3	T1	I/O
3	IO_L24P_3	IO_L24P_3	IO_L24P_3	T2	I/O
3	IP	IP	IP	D3	INPUT
3	IO	IP	IP	F4	**500E:** I/O **1200E:** INPUT **1600E:** INPUT
3	IP	IP	IP	F5	INPUT
3	IP	IP	IP	G1	INPUT
3	IP	IP	IP	J7	INPUT
3	IP	IP	IP	K2	INPUT
3	IP	IP	IP	K7	INPUT
3	IP	IP	IP	M1	INPUT
3	IP	IP	IP	N1	INPUT
3	IP	IP	IP	N2	INPUT
3	IP	IP	IP	R1	INPUT
3	IP	IP	IP	U1	INPUT
3	IP/VREF_3	IP/VREF_3	IP/VREF_3	J6	VREF
3	IO/VREF_3	IP/VREF_3	IP/VREF_3	R4	**500E:** VREF(I/O) **1200E:** VREF(INPUT) **1600E:** VREF(INPUT)
3	VCCO_3	VCCO_3	VCCO_3	F3	VCCO
3	VCCO_3	VCCO_3	VCCO_3	H7	VCCO
3	VCCO_3	VCCO_3	VCCO_3	K1	VCCO
3	VCCO_3	VCCO_3	VCCO_3	L7	VCCO
3	VCCO_3	VCCO_3	VCCO_3	N3	VCCO
GND	GND	GND	GND	A1	GND
GND	GND	GND	GND	A18	GND
GND	GND	GND	GND	B2	GND
GND	GND	GND	GND	B17	GND
GND	GND	GND	GND	C10	GND
GND	GND	GND	GND	G7	GND
GND	GND	GND	GND	G12	GND
GND	GND	GND	GND	H8	GND
GND	GND	GND	GND	H9	GND
GND	GND	GND	GND	H10	GND
GND	GND	GND	GND	H11	GND
GND	GND	GND	GND	J3	GND
GND	GND	GND	GND	J8	GND
GND	GND	GND	GND	J11	GND

User I/Os by Bank

Table 149 and Table 150 indicate how the available user-I/O pins are distributed between the four I/O banks on the FG320 package.

Table 149: **User I/Os Per Bank for XC3S500E in the FG320 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF[1]	CLK[2]
Top	0	58	29	14	1	6	8
Right	1	58	22	10	21	5	0[2]
Bottom	2	58	17	13	24	4	0[2]
Left	3	58	34	11	0	5	8
TOTAL		**232**	**102**	**48**	**46**	**20**	**16**

Notes:
1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

Table 150: **User I/Os Per Bank for XC3S1200E and XC3S1600E in the FG320 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF[1]	CLK[2]
Top	0	61	34	12	1	6	8
Right	1	63	25	12	21	5	0[2]
Bottom	2	63	23	11	24	5	0[2]
Left	3	63	38	12	0	5	8
TOTAL		**250**	**120**	**47**	**46**	**21**	**16**

Notes:
1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

Table 155: **User I/Os Per Bank for the XC3S1600E in the FG484 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF[1]	CLK[2]
Top	0	94	56	22	1	7	8
Right	1	94	50	16	21	7	0[2]
Bottom	2	94	45	18	24	7	0[2]
Left	3	94	63	16	0	7	8
TOTAL		**376**	**214**	**72**	**46**	**28**	**16**

Notes:

1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

Footprint Migration Differences

The XC3S1600E FPGA is the only Spartan-3E device offered in the FG484 package.

FG484 Footprint

Right Half of Package (top view)

Bank 0

	12	13	14	15	16	17	18	19	20	21	22
A	INPUT L17N_0	INPUT L17P_0	I/O L12N_0 VREF_0	I/O L12P_0	I/O L07N_0	I/O L07P_0	I/O L04P_0	I/O L04N_0	I/O L03N_0 VREF_0	I/O L03P_0	GND
B	I/O L19P_0 GCLK6	I/O	VCCO_0	I/O L09N_0 VREF_0	GND	INPUT L05P_0	VCCO_0	INPUT	TDO	I/O L38N_1 LDC2	I/O L38P_1 LDC1
C	I/O L19N_0 GCLK7	INPUT L14P_0	I/O	I/O L09P_0	I/O L06N_0	INPUT L05N_0	I/O L01N_0	I/O L01P_0	GND	I/O L37N_1 LDC0	I/O L37P_1 HDC
D	VCCAUX	INPUT L14N_0	I/O L11N_0	INPUT L08P_0	I/O L06P_0	INPUT L02N_0	INPUT L02P_0	TMS	INPUT	INPUT VREF_1	I/O L34N_1
E	I/O L18N_0 GCLK5	GND	I/O L11P_0	INPUT L08N_0	I/O	TCK	VCCAUX	I/O L36P_1	I/O L36N_1	VCCO_1	I/O L34P_1
F	I/O L18P_0 GCLK4	I/O L15P_0	VCCO_0	I/O L10P_0	I/O	GND	I/O L35P_1	I/O L35N_1	I/O L32N_1	INPUT	I/O L31N_1
G	I/O VREF_0	I/O L15N_0	I/O L13P_0	I/O L10N_0	INPUT	I/O L30P_1	I/O L33N_1	I/O L33P_1	I/O L32P_1	GND	I/O L31P_1
H	INPUT L20P_0 GCLK8	I/O L16P_0	I/O L13N_0	I/O	INPUT	I/O L30N_1	VCCO_1	I/O L29P_1	I/O L29N_1	I/O L28N_1 VREF_1	I/O L28P_1
J	GND	I/O L16N_0	GND	I/O L25P_1	INPUT	I/O L27N_1	I/O L27P_1	GND	I/O L26N_1	I/O L26P_1	INPUT
K	GND	VCCINT	VCCAUX	I/O L25N_1	I/O L23P_1	I/O L23N_1 A0	I/O L24P_1	I/O L24N_1	INPUT	VCCO_1	I/O L22N_1 A1
L	VCCINT	GND	VCCINT	INPUT	VCCO_1	INPUT VREF_1	I/O L21P_1 A4 RHCLK6	I/O L21N_1 A3 RHCLK7	I/O L20P_1 A6 RHCLK4 IRDY1	I/O L20N_1 A5 RHCLK5	I/O L22P_1 A2
M	VCCINT	VCCINT	GND	I/O L19P_1 A8 RHCLK2	I/O L19N_1 A7 RHCLK3 TRDY1	GND	INPUT	VCCAUX	I/O L17N_1 VREF_1	GND	I/O L18N_1 A9 RHCLK1
N	VCCINT	GND	VCCINT	INPUT	I/O L16N_1 A11	I/O L16P_1 A12	I/O L15N_1	I/O L15P_1	I/O L17P_1	INPUT	I/O L18P_1 A10 RHCLK0
P	INPUT L21N_2 M2 GCLK1	VCCINT	GND	I/O L14N_1	I/O L14P_1	I/O L12P_1	I/O L12N_1 VREF_1	GND	INPUT	VCCO_1	I/O L13N_1
R	INPUT L21P_2 RDWR_B GCLK0	INPUT L24N_2	I/O L27P_2	INPUT	I/O L10N_1	VCCO_1	I/O L09P_1	I/O L09N_1	I/O L11P_1	I/O L11N_1	I/O L13P_1
T	VCCO_2	INPUT L24P_2	I/O L27N_2	INPUT L31N_2 VREF_2	I/O L10P_1	INPUT	I/O L06P_1	I/O L06N_1	INPUT	GND	I/O L08N_1
U	I/O L23N_2 DIN D0	I/O L26P_2	I/O L26N_2 VREF_2	INPUT L31P_2	I/O L33N_2	GND	INPUT	I/O L04N_1	I/O L07N_1 VREF_1	I/O L07P_1	I/O L08P_1
V	I/O L23P_2 M0	GND	I/O L29P_2	VCCO_2	I/O L33P_2	INPUT	VCCAUX	I/O L04P_1	I/O L03P_1	VCCO_1	I/O L05N_1
W	I/O L22N_2 D1 GCLK3	I/O L25P_2	I/O L29N_2	I/O L32N_2	INPUT L34P_2	I/O L36N_2	I/O L38P_2 A21	I/O L40N_2 CCLK	I/O L03N_1 VREF_1	I/O L02N_1 A13	I/O L05P_1
Y	I/O L22P_2 D2 GCLK2	I/O L25N_2	I/O L28N_2	I/O L32P_2	INPUT L34N_2	I/O L36P_2	I/O L38N_2 A20	I/O L40P_2 VS0 A17	GND	I/O L02P_1 A14	I/O L01N_1 A15
AA	I/O M1	VCCO_2	I/O L28P_2	I/O L30P_2	GND	I/O L35P_2 A23	VCCO_2	INPUT L37N_2	I/O L39N_2 VS1 A18	DONE	I/O L01P_1 A16
AB	GND	I/O	I/O	I/O L30N_2	I/O	I/O L35N_2 A22	I/O	INPUT L37P_2	I/O L39P_2 VS2 A19	I/O VREF_2	GND

Bank 1

Bank 2

DS312_11_101905

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/01/05	1.0	Initial Xilinx release.
03/21/05	1.1	Added XC3S250E in the CP132 package to Table 129. Corrected number of differential I/O pairs on CP132. Added pinout and footprint information for the CP132, FG400, and FG484 packages. Removed IRDY and TRDY pins from the VQ100, TQ144, and PQ208 packages.
11/23/05	2.0	Corrected title of Table 153. Updated differential pair numbering for some pins in Bank 0 of the FG400 package, affecting Table 152 and Figure 87. Pin functionality and ball assignment were not affected. Added Package Thermal Characteristics section. Added package mass values to Table 125.
03/22/06	3.0	Included I/O pins, not just input-only pins under the VREF description in Table 124. Clarified that some global clock inputs are Input-only pins in Table 124. Added information on the XC3S100E in the CP132 package, affecting Table 129, Table 130, Table 133, Table 134, Table 136, and Figure 81. Ball A12 on the XC3S1600E in the FG320 package a full I/O pin, not an Input-only pin. Corrected the I/O counts for the XC3S1600E in the FG320 package, affecting Table 129, Table 150, Table 151, and Figure 86. Corrected pin type for XC3S1600E balls N14 and N15 in Table 148.
05/19/06	3.1	Minor text edits.
11/09/06	3.4	Added package thermal data for the XC3S100E in the CP132 package to Table 130. Corrected pin migration arrows for balls E17 and F4 between the XC3S500E and XC3S1600E in Table 151. Promoted Module 4 to Production status. Synchronized all modules to v3.4.
03/16/07	3.5	Minor formatting changes.
05/29/07	3.6	Corrected 'Lxx' to 'Lxxy' in Table 124. Noted that some GCLK and VREF pins are on INPUT pins in Table 124 and Table 129. Added link before Table 127 to Material Declaration Data Sheets.
04/18/08	3.7	Added XC3S500E VQG100 package. Added Material Declaration Data Sheet links in Table 127. Updated Thermal Characteristics in Table 130. Updated links.
08/26/09	3.8	Minor typographical updates.
10/29/12	4.0	Added Notice of Disclaimer. This product is not recommended for new designs. Updated the XC3S250E-FT256 in Table 129.

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