AMD Xilinx - XC3S500E-4PQ208C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1164
Number of Logic Elements/Cells	10476
Total RAM Bits	368640
Number of I/O	158
Number of Gates	500000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s500e-4pq208c

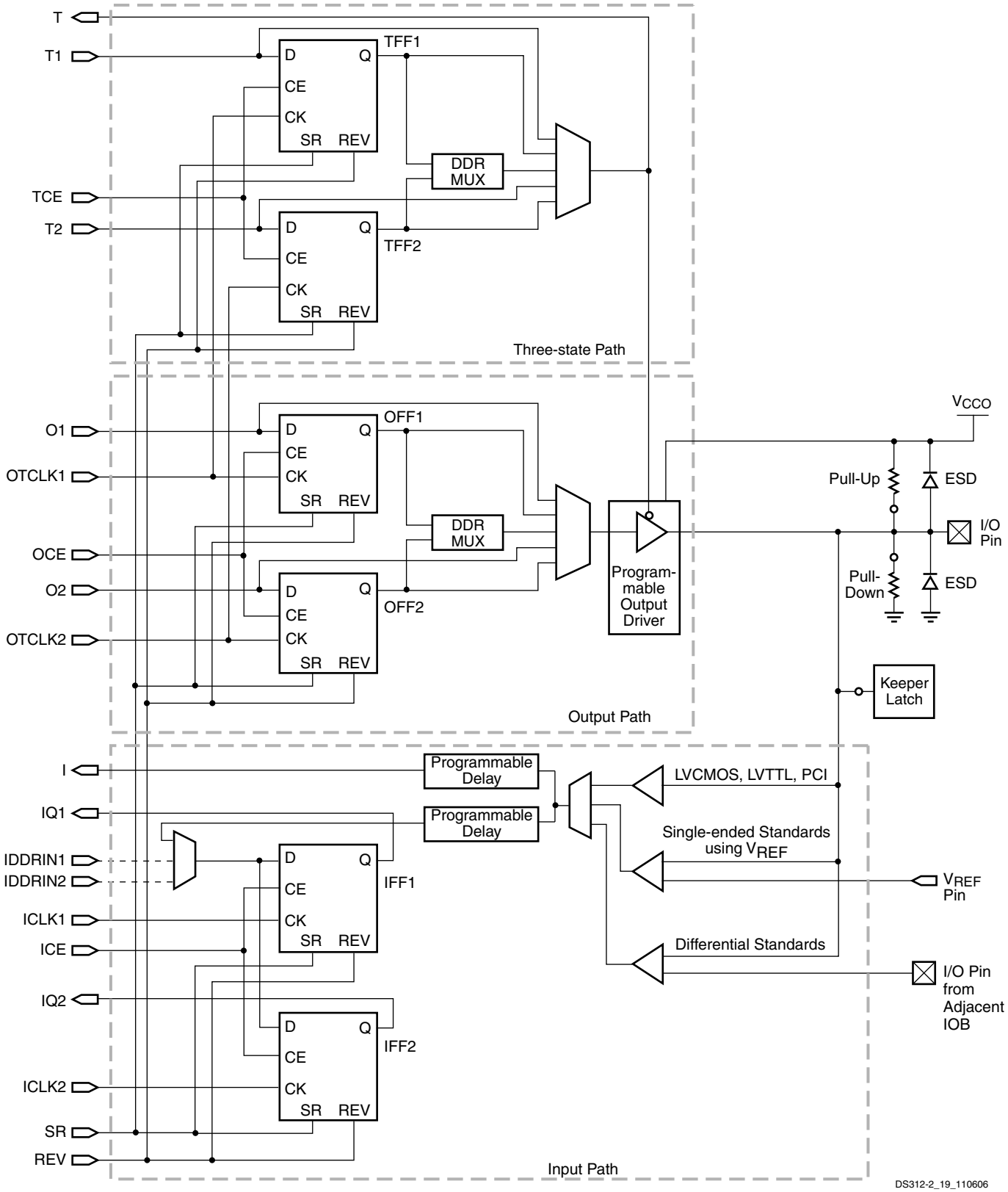


Figure 5: **Simplified IOB Diagram**

IOBs Organized into Banks

The Spartan-3E architecture organizes IOBs into four I/O banks as shown in Figure 13. Each bank maintains separate V_{CCO} and V_{REF} supplies. The separate supplies allow each bank to independently set V_{CCO}. Similarly, the V_{REF} supplies can be set for each bank. Refer to Table 6 and Table 7 for V_{CCO} and V_{REF} requirements.

When working with Spartan-3E devices, most of the differential I/O standards are compatible and can be combined within any given bank. Each bank can support any two of the following differential standards: LVDS_25 outputs, MINI_LVDS_25 outputs, and RSDS_25 outputs. As an example, LVDS_25 outputs, RSDS_25 outputs, and any other differential inputs while using on-chip differential termination are a valid combination. A combination not allowed is a single bank with LVDS_25 outputs, RSDS_25 outputs, and MINI_LVDS_25 outputs.

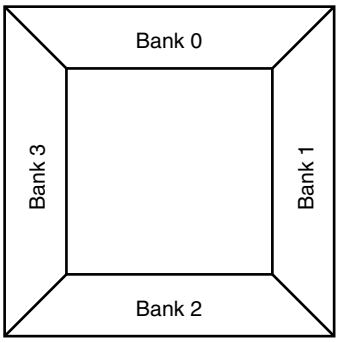


Figure 13: **Spartan-3E I/O Banks (top view)**

I/O Banking Rules

When assigning I/Os to banks, these V_{CCO} rules must be followed:

1. All V_{CCO} pins on the FPGA must be connected even if a bank is unused.
2. All V_{CCO} lines associated within a bank must be set to the same voltage level.
3. The V_{CCO} levels used by all standards assigned to the I/Os of any given bank must agree. The Xilinx development software checks for this. Table 6 and Table 7 describe how different standards use the V_{CCO} supply.
4. If a bank does not have any V_{CCO} requirements, connect V_{CCO} to an available voltage, such as 2.5V or 3.3V. Some configuration modes might place additional V_{CCO} requirements. Refer to Configuration for more information.

If any of the standards assigned to the Inputs of the bank use V_{REF}, then the following additional rules must be observed:

1. All V_{REF} pins must be connected within a bank.
2. All V_{REF} lines associated with the bank must be set to the same voltage level.
3. The V_{REF} levels used by all standards assigned to the Inputs of the bank must agree. The Xilinx development software checks for this. Table 6 describes how different standards use the V_{REF} supply.

If V_{REF} is not required to bias the input switching thresholds, all associated V_{REF} pins within the bank can be used as user I/Os or input pins.

Package Footprint Compatibility

Sometimes, applications outgrow the logic capacity of a specific Spartan-3E FPGA. Fortunately, the Spartan-3E family is designed so that multiple part types are available in pin-compatible package footprints, as described in Module 4, Pinout Descriptions. In some cases, there are subtle differences between devices available in the same footprint. These differences are outlined for each package, such as pins that are unconnected on one device but connected on another in the same package or pins that are dedicated inputs on one package but full I/O on another. When designing the printed circuit board (PCB), plan for potential future upgrades and package migration.

The Spartan-3E family is not pin-compatible with any previous Xilinx FPGA family.

Dedicated Inputs

Dedicated Inputs are IOBs used only as inputs. Pin names designate a Dedicated Input if the name starts with *IP*, for example, IP or IP_Lxxx_x. Dedicated inputs retain the full functionality of the IOB for input functions with a single exception for differential inputs (IP_Lxxx_x). For the differential Dedicated Inputs, the on-chip differential termination is not available. To replace the on-chip differential termination, choose a differential pair that supports outputs (IO_Lxxx_x) or use an external 100Ω termination resistor on the board.

ESD Protection

Clamp diodes protect all device pads against damage from Electro-Static Discharge (ESD) as well as excessive voltage transients. Each I/O has two clamp diodes: one diode extends P-to-N from the pad to V_{CCO} and a second diode extends N-to-P from the pad to GND. During operation, these diodes are normally biased in the off state. These clamp diodes are always connected to the pad, regardless of the signal standard selected. The presence of diodes limits the ability of Spartan-3E I/Os to tolerate high signal voltages. The V_{IN} absolute maximum rating in Table 73 of Module 3, DC and Switching Characteristics specifies the voltage range that I/Os can tolerate.

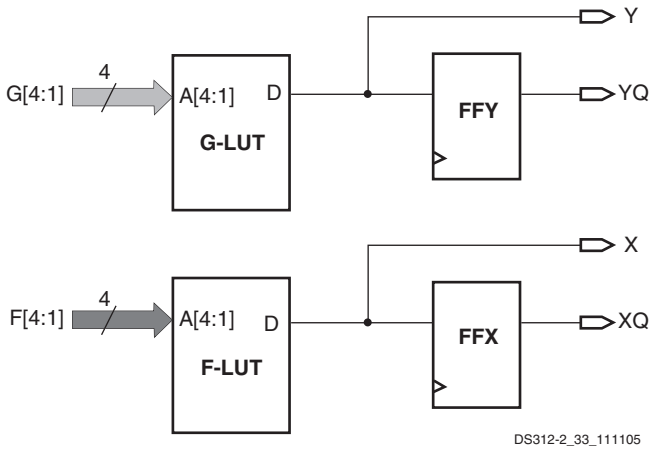


Figure 18: **LUT Resources in a Slice**

Wide Multiplexers

For additional information, refer to the “Using Dedicated Multiplexers” chapter in UG331.

Wide-function multiplexers effectively combine LUTs in order to permit more complex logic operations. Each slice has two of these multiplexers with F5MUX in the bottom portion of the slice and FiMUX in the top portion. The F5MUX multiplexes the two LUTs in a slice. The FiMUX multiplexes two CLB inputs which connect directly to the F5MUX and FiMUX results from the same slice or from other slices. See Figure 19.

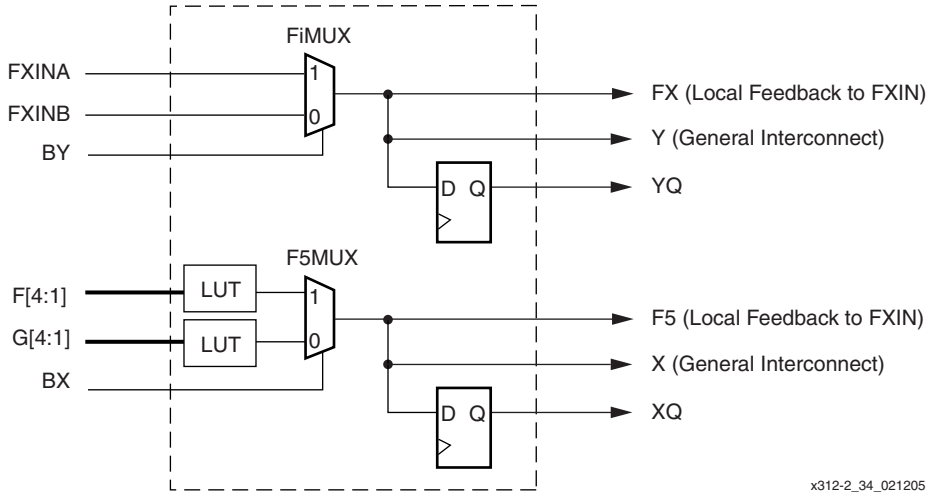
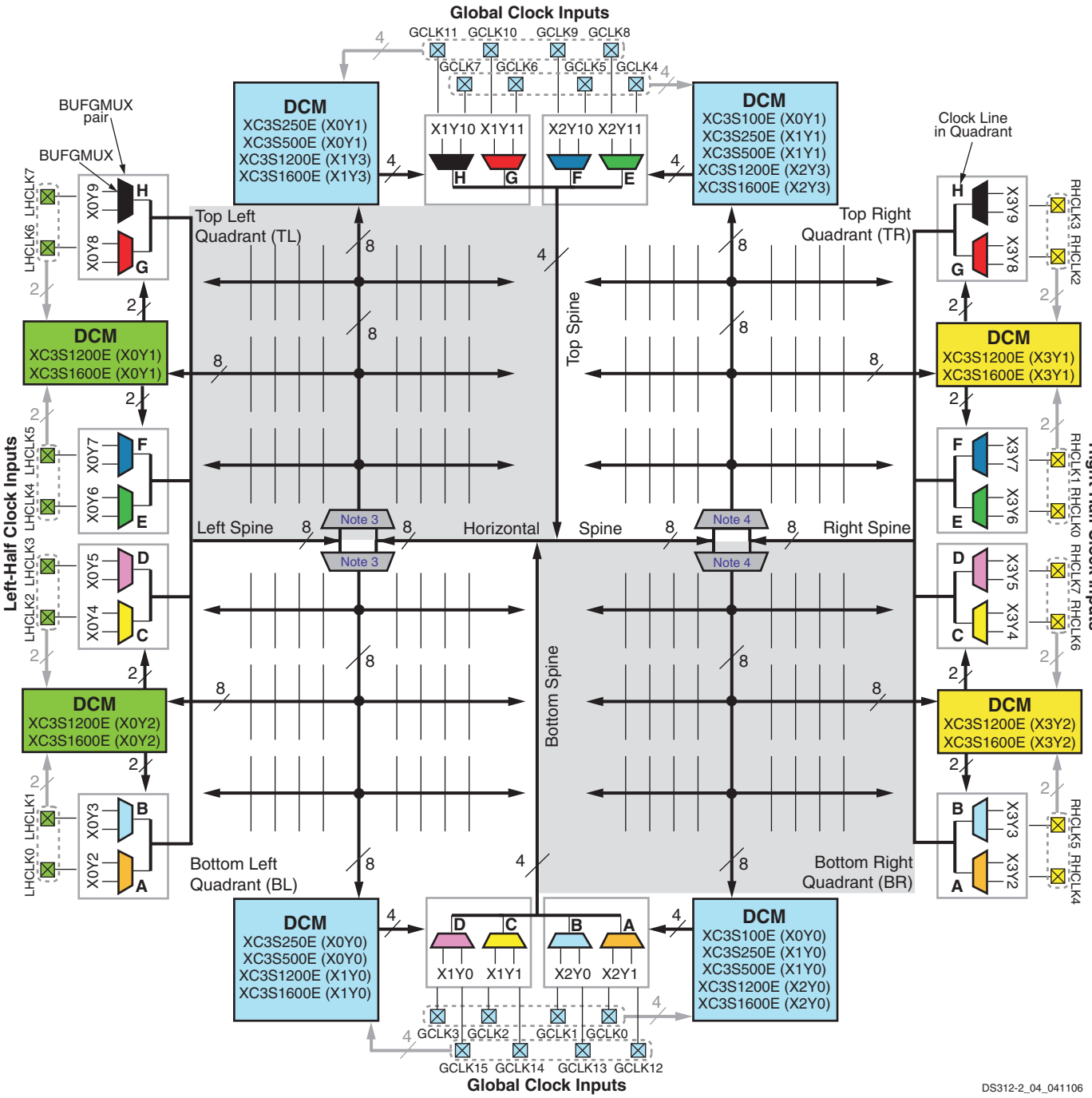


Figure 19: **Dedicated Multiplexers in Spartan-3E CLB**

Depending on the slice, FiMUX takes on the name F6MUX, F7MUX, or F8MUX. The designation indicates the number of inputs possible without restriction on the function. For example, an F7MUX can generate any function of seven inputs. Figure 20 shows the names of the multiplexers in each position in the Spartan-3E CLB. The figure also includes the direct connections within the CLB, along with the F7MUX connection to the CLB below.

Each mux can create logic functions of more inputs than indicated by its name. The F5MUX, for example, can generate any function of five inputs, with four inputs duplicated to two LUTs and the fifth input controlling the mux. Because each LUT can implement independent 2:1 muxes, the F5MUX can combine them to create a 4:1 mux, which is a six-input function. If the two LUTs have completely independent sets of inputs, some functions of all nine inputs can be implemented. Table 11 shows the connections for each multiplexer and the number of inputs possible for different types of functions.



Notes:

1. The diagram presents electrical connectivity. The diagram locations do not necessarily match the physical location on the device, although the coordinate locations shown are correct.
2. Number of DCMs and locations of these DCM varies for different device densities. The left and right DCMs are only in the XC3S1200E and XC3S1600E. The XC3S100E has only two DCMs, one on the top right and one on the bottom right of the die.
3. See Figure 47a, which shows how the eight clock lines are multiplexed on the left-hand side of the device.
4. See Figure 47b, which shows how the eight clock lines are multiplexed on the right-hand side of the device.
5. For best direct clock inputs to a particular clock buffer, not a DCM, see Table 41.
6. For best direct clock inputs to a particular DCM, not a BUFGMUX, see Table 30, Table 31, and Table 32. Direct pin inputs to a DCM are shown in gray.

Figure 45: **Spartan-3E Internal Quadrant-Based Clock Network (Electrical Connectivity View)**

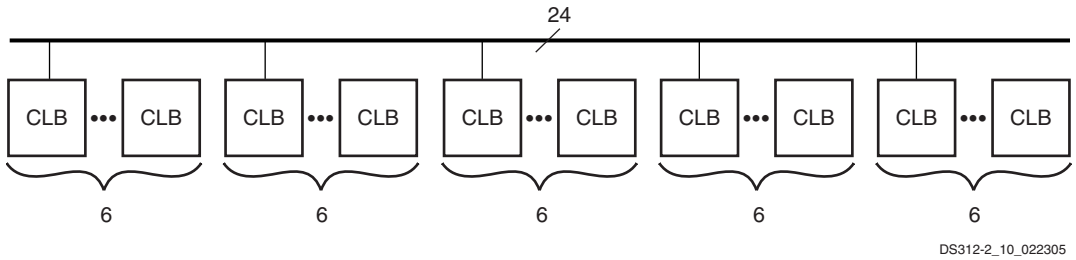
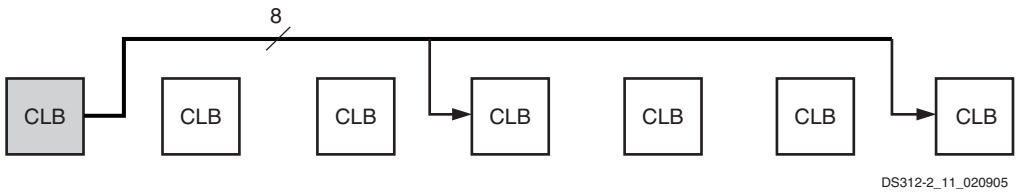
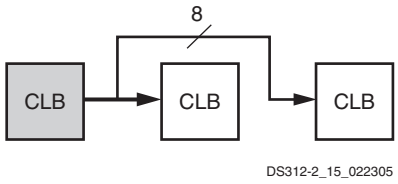
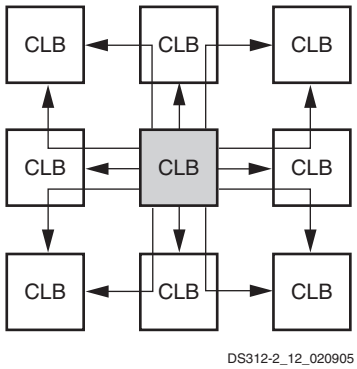
Horizontal and Vertical Long Lines (horizontal channel shown as an example)	
Horizontal and Vertical Hex Lines (horizontal channel shown as an example)	
Horizontal and Vertical Double Lines (horizontal channel shown as an example)	
Direct Connections	

Figure 50: **Interconnect Types between Two Adjacent Interconnect Tiles**

The four types of general-purpose interconnect available in each channel, shown in Figure 50, are described below.

Long Lines

Each set of 24 long line signals spans the die both horizontally and vertically and connects to one out of every six interconnect tiles. At any tile, four of the long lines drive or receive signals from a switch matrix. Because of their low capacitance, these lines are well-suited for carrying high-frequency signals with minimal loading effects (e.g. skew). If all global clock lines are already committed and additional clock signals remain to be assigned, long lines serve as a good alternative.

Hex Lines

Each set of eight hex lines are connected to one out of every three tiles, both horizontally and vertically. Thirty-two hex lines are available between any given interconnect tile. Hex lines are only driven from one end of the route.

Double Lines

Each set of eight double lines are connected to every other tile, both horizontally and vertically. in all four directions. Thirty-two double lines available between any given interconnect tile. Double lines are more connections and more flexibility, compared to long line and hex lines.

(W) Table 54 shows the connections between the SPI Flash PROM and the FPGA's SPI configuration interface. Each SPI Flash PROM vendor uses slightly different signal naming. The SPI Flash PROM's write protect and hold controls are not used by the FPGA during configuration. However, the $\overline{\text{HOLD}}$ pin must be High during the configuration process. The PROM's write protect input must be High in order to write or program the Flash memory.

Table 54: **Example SPI Flash PROM Connections and Pin Naming**

SPI Flash Pin	FPGA Connection	STMicro	NexFlash	Silicon Storage Technology	Atmel DataFlash
DATA_IN	MOSI	D	DI	SI	SI
DATA_OUT	DIN	Q	DO	SO	SO
$\overline{\text{SELECT}}$	CSO_B	$\overline{\text{S}}$	$\overline{\text{CS}}$	CE#	$\overline{\text{CS}}$
CLOCK	CCLK	C	CLK	SCK	SCK
$\overline{\text{WR\_PROTECT}}$ (W)	Not required for FPGA configuration. Must be High to program SPI Flash. Optional connection to FPGA user I/O after configuration.	$\overline{\text{W}}$	$\overline{\text{WP}}$	WP#	$\overline{\text{WP}}$
$\overline{\text{HOLD}}$ (see Figure 53)	Not required for FPGA configuration but must be High during configuration. Optional connection to FPGA user I/O after configuration. Not applicable to Atmel DataFlash.	$\overline{\text{HOLD}}$	$\overline{\text{HOLD}}$	HOLD#	N/A
$\overline{\text{RESET}}$ (see Figure 54)	Only applicable to Atmel DataFlash. Not required for FPGA configuration but must be High during configuration. Optional connection to FPGA user I/O after configuration. Do not connect to FPGA's PROG_B as this will prevent direct programming of the DataFlash.	N/A	N/A	N/A	$\overline{\text{RESET}}$
RDY/$\overline{\text{BUSY}}$ (see Figure 54)	Only applicable to Atmel DataFlash and only available on certain packages. Not required for FPGA configuration. Output from DataFlash PROM. Optional connection to FPGA user I/O after configuration.	N/A	N/A	N/A	RDY/$\overline{\text{BUSY}}$

The mode select pins, M[2:0], and the variant select pins, VS[2:0] are sampled when the FPGA's INIT_B output goes High and must be at defined logic levels during this time. After configuration, when the FPGA's DONE output goes High, these pins are all available as full-featured user-I/O pins.

(P) Similarly, the FPGA's HSWAP pin must be Low to enable pull-up resistors on all user-I/O pins or High to disable the pull-up resistors. The HSWAP control must remain at a constant logic level throughout FPGA configuration. After configuration, when the FPGA's DONE output goes High, the HSWAP pin is available as full-featured user-I/O pin and is powered by the VCCO_0 supply.

In a single-FPGA application, the FPGA's DOUT pin is not used but is actively driving during the configuration process.

Table 55: **Serial Peripheral Interface (SPI) Connections**

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
HSWAP (P)	Input	**User I/O Pull-Up Control**. When Low during configuration, enables pull-up resistors in all I/O pins to respective I/O bank V_{CCO} input. 0: Pull-ups during configuration 1: No pull-ups	Drive at valid logic level throughout configuration.	User I/O
M[2:0]	Input	**Mode Select**. Selects the FPGA configuration mode. See Design Considerations for the HSWAP, M[2:0], and VS[2:0] Pins.	M2 = 0, M1 = 0, M0 = 1. Sampled when INIT_B goes High.	User I/O

SPI serial Flash PROMs and the Atmel AT45DB-series Data Flash PROMs using the Platform Cable USB, Xilinx Parallel IV, or other compatible programming cable.

Byte-Wide Peripheral Interface (BPI) Parallel Flash Mode

For additional information, refer to the “Master BPI Mode” chapter in UG332.

In Byte-wide Peripheral Interface (BPI) mode (M[2:0] = <0:1:0> or <0:1:1>), a Spartan-3E FPGA configures itself from an industry-standard parallel NOR Flash PROM, as illustrated in Figure 58. The FPGA generates up to a 24-bit address lines to access an attached parallel Flash. Only 20 address lines are generated for Spartan-3E FPGAs in the TQ144 package. Similarly, the XC3S100E FPGA in the CP132 package only has 20 address lines while the XC3S250E and XC3S500E FPGAs in the same package have 24 address lines. When using the VQ100 package, the BPI mode is not available when using parallel NOR Flash, but is supported using parallel Platform Flash (XCFxxP).

The BPI configuration interface is primarily designed for standard parallel NOR Flash PROMs and supports both byte-wide (x8) and byte-wide/halfword (x8/x16) PROMs. The interface functions with halfword-only (x16) PROMs, but the upper byte in a portion of the PROM remains unused. For configuration, the BPI interface does not require any specific Flash PROM features, such as boot block or a specific sector size.

The BPI interface also functions with Xilinx parallel Platform Flash PROMs (XCFxxP), although the FPGA’s address lines are left unconnected.

The BPI interface also works equally wells with other asynchronous memories that use a similar SRAM-style interface such as SRAM, NVRAM, EEPROM, EPROM, or masked ROM.

NAND Flash memory is commonly used in memory cards for digital cameras. Spartan-3E FPGAs do not configure directly from NAND Flash memories.

The FPGA’s internal oscillator controls the interface timing and the FPGA supplies the clock on the CCLK output pin. However, the CCLK signal is not used in single FPGA applications. Similarly, the FPGA drives three pins Low during configuration (LDC[2:0]) and one pin High during configuration (HDC) to the PROM’s control inputs.

This addressing flexibility allows the FPGA to share the parallel Flash PROM with an external or embedded processor. Depending on the specific processor architecture, the processor boots either from the top or bottom of memory. The FPGA is flexible and boots from the opposite end of memory from the processor. Only the processor or the FPGA can boot at any given time. The FPGA can configure first, holding the processor in reset or the processor can boot first, asserting the FPGA's PROG_B pin.

The mode select pins, M[2:0], are sampled when the FPGA's INIT_B output goes High and must be at defined logic levels during this time. After configuration, when the FPGA's DONE output goes High, the mode pins are available as full-featured user-I/O pins.

(P) Similarly, the FPGA's HSWAP pin must be Low to enable pull-up resistors on all user-I/O pins or High to disable the pull-up resistors. The HSWAP control must remain at a constant logic level throughout FPGA configuration. After configuration, when the FPGA's DONE output goes High, the HSWAP pin is available as full-featured user-I/O pin and is powered by the VCCO_0 supply.

The RDWR_B and CSI_B must be Low throughout the configuration process. After configuration, these pins also become user I/O.

In a single-FPGA application, the FPGA's CSO_B and CCLK pins are not used but are actively driving during the configuration process. The BUSY pin is not used but also actively drives during configuration and is available as a user I/O after configuration.

After configuration, all of the interface pins except DONE and PROG_B are available as user I/Os. Furthermore, the bidirectional SelectMAP configuration peripheral interface (see Slave Parallel Mode) is available after configuration. To continue using SelectMAP mode, set the ***Persist*** bitstream generator option to ***Yes***. An external host can then read and verify configuration data.

The Persist option will maintain A20-A23 as configuration pins although they are not used in SelectMAP mode.

Table 59: **Byte-Wide Peripheral Interface (BPI) Connections**

Pin Name	FPGA Direction	Description	During Configuration	After Configuration
HSWAP (P)	Input	**User I/O Pull-Up Control**. When Low during configuration, enables pull-up resistors in all I/O pins to respective I/O bank V_{CCO} input. 0: Pull-ups during configuration 1: No pull-ups	Drive at valid logic level throughout configuration.	User I/O
M[2:0] (A)	Input	**Mode Select**. Selects the FPGA configuration mode. See Design Considerations for the HSWAP, M[2:0], and VS[2:0] Pins.	M2 = 0, M1 = 1. Set M0 = 0 to start at address 0, increment addresses. Set M0 = 1 to start at address 0xFFFFFF and decrement addresses. Sampled when INIT_B goes High.	User I/O
CSI_B	Input	**Chip Select Input**. Active Low.	Must be Low throughout configuration.	User I/O. If bitstream option ***Persist=Yes***, becomes part of SelectMap parallel peripheral interface.
RDWR_B	Input	**Read/Write Control**. Active Low write enable. Read functionality typically only used after configuration, if bitstream option ***Persist=Yes***.	Must be Low throughout configuration.	User I/O. If bitstream option ***Persist=Yes***, becomes part of SelectMap parallel peripheral interface.
LDC0	Output	PROM Chip Enable	Connect to PROM chip-select input (CE#). FPGA drives this signal Low throughout configuration.	User I/O. If the FPGA does not access the PROM after configuration, drive this pin High to deselect the PROM. A[23:0], D[7:0], LDC[2:1], and HDC then become available as user I/O.
LDC1	Output	PROM Output Enable	Connect to the PROM output-enable input (OE#). The FPGA drives this signal Low throughout configuration.	User I/O

Start-Up

At the end of configuration, the FPGA automatically pulses the Global Set/Reset (GSR) signal, placing all flip-flops in a known state. After configuration completes, the FPGA switches over to the user application loaded into the FPGA. The sequence and timing of how the FPGA switches over is programmable as is the clock source controlling the sequence.

The default start-up sequence appears in Figure 68, where the Global Three-State signal (GTS) is released one clock cycle after DONE goes High. This sequence allows the DONE signal to enable or disable any external logic used during configuration before the user application in the FPGA starts driving output signals. One clock cycle later, the Global Write Enable (GWE) signal is released. This allows signals to propagate within the FPGA before any clocked storage elements such as flip-flops and block ROM are enabled.

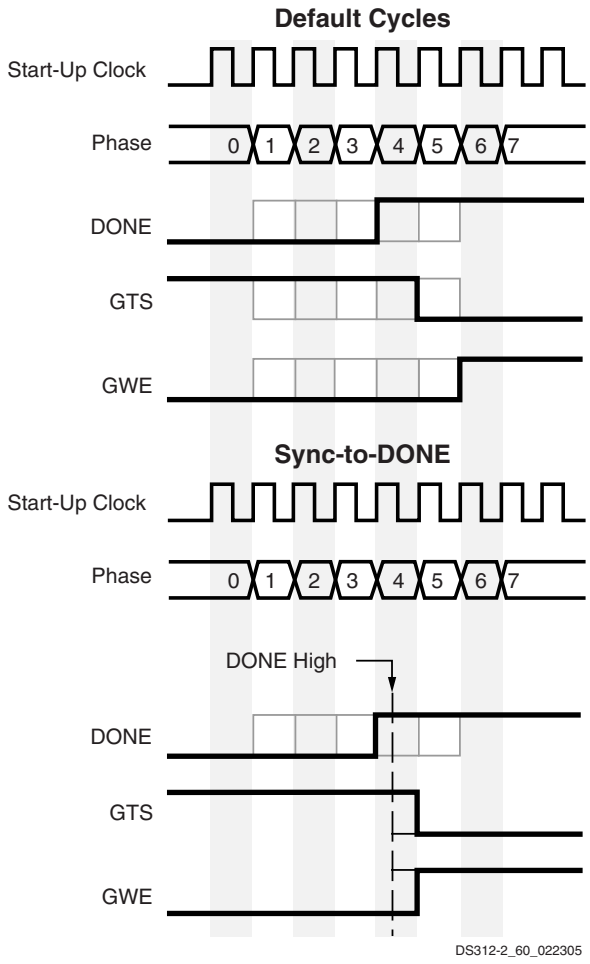


Figure 68: **Default Start-Up Sequence**

The function of the dual-purpose I/O pins, such as M[2:0], VS[2:0], HSWAP, and A[23:0], also changes when the DONE pin goes High. When DONE is High, these pins become user I/Os. Like all user-I/O pins, GTS controls when the dual-purpose pins can drive out.

The relative timing of configuration events is programmed via the Bitstream Generator (BitGen) options in the Xilinx development software. For example, the GTS and GWE events can be programmed to wait for all the DONE pins to High on all the devices in a multiple-FPGA daisy-chain, forcing the FPGAs to start synchronously. Similarly, the start-up sequence can be paused at any stage, waiting for selected DCMs to lock to their respective input clock signals. See also Stabilizing DCM Clocks Before User Mode.

By default, the start-up sequence is synchronized to CCLK. Alternatively, the start-up sequence can be synchronized to a user-specified clock from within the FPGA application using the STARTUP_SPARTAN3E library primitive and by setting the ***StartupClk*** bitstream generator option. The FPGA application can optionally assert the GSR and GTS signals via the STARTUP_SPARTAN3E primitive. For JTAG configuration, the start-up sequence can be synchronized to the TCK clock input.

General DC Characteristics for I/O Pins

Table 78: **General DC Characteristics of User I/O, Dual-Purpose, and Dedicated Pins**

Symbol	Description	Test Conditions	Min	Typ	Max	Units
I_L (3)	Leakage current at User I/O, Input-only, Dual-Purpose, and Dedicated pins	Driver is in a high-impedance state, V_{IN} = 0V or V_{CCO} max, sample-tested	–10	–	+10	µA
I_{RPU} (2)	Current through pull-up resistor at User I/O, Dual-Purpose, Input-only, and Dedicated pins	V_{IN} = 0V, V_{CCO} = 3.3V	–0.36	–	–1.24	mA
		V_{IN} = 0V, V_{CCO} = 2.5V	–0.22	–	–0.80	mA
		V_{IN} = 0V, V_{CCO} = 1.8V	–0.10	–	–0.42	mA
		V_{IN} = 0V, V_{CCO} = 1.5V	–0.06	–	–0.27	mA
		V_{IN} = 0V, V_{CCO} = 1.2V	–0.04	–	–0.22	mA
R_{PU} (2)	Equivalent pull-up resistor value at User I/O, Dual-Purpose, Input-only, and Dedicated pins (based on I_{RPU} per Note 2)	V_{IN} = 0V, V_{CCO} = 3.0V to 3.465V	2.4	–	10.8	kΩ
		V_{IN} = 0V, V_{CCO} = 2.3V to 2.7V	2.7	–	11.8	kΩ
		V_{IN} = 0V, V_{CCO} = 1.7V to 1.9V	4.3	–	20.2	kΩ
		V_{IN} = 0V, V_{CCO} =1.4V to 1.6V	5.0	–	25.9	kΩ
		V_{IN} = 0V, V_{CCO} = 1.14V to 1.26V	5.5	–	32.0	kΩ
I_{RPD} (2)	Current through pull-down resistor at User I/O, Dual-Purpose, Input-only, and Dedicated pins	V_{IN} = V_{CCO}	0.10	–	0.75	mA
R_{PD} (2)	Equivalent pull-down resistor value at User I/O, Dual-Purpose, Input-only, and Dedicated pins (based on I_{RPD} per Note 2)	V_{IN} = V_{CCO} = 3.0V to 3.465V	4.0	–	34.5	kΩ
		V_{IN} = V_{CCO} = 2.3V to 2.7V	3.0	–	27.0	kΩ
		V_{IN} = V_{CCO} = 1.7V to 1.9V	2.3	–	19.0	kΩ
		V_{IN} = V_{CCO} = 1.4V to 1.6V	1.8	–	16.0	kΩ
		V_{IN} = V_{CCO} = 1.14V to 1.26V	1.5	–	12.6	kΩ
I_{REF}	V_{REF} current per pin	All V_{CCO} levels	–10	–	+10	µA
C_{IN}	Input capacitance	–	–	–	10	pF
R_{DT}	Resistance of optional differential termination circuit within a differential I/O pair. Not available on Input-only pairs.	V_{OCM} Min ≤ V_{ICM} ≤ V_{OCM} Max V_{OD} Min ≤ V_{ID} ≤ V_{OD} Max V_{CCO} = 2.5V	–	120	–	Ω

Notes:

1. The numbers in this table are based on the conditions set forth in Table 77.
2. This parameter is based on characterization. The pull-up resistance R_{PU} = V_{CCO} / I_{RPU}. The pull-down resistance R_{PD} = V_{IN} / I_{RPD}.
3. For single-ended signals that are placed on a differential-capable I/O, V_{IN} of –0.2V to –0.5V is supported but can cause increased leakage between the two pins. See *Parasitic Leakage* in UG331, *Spartan-3 Generation FPGA User Guide*.

Quiescent Current Requirements

Table 79: **Quiescent Supply Current Characteristics**

Symbol	Description	Device	Typical	Commercial Maximum(1)	Industrial Maximum(1)	Units
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC3S100E	8	27	36	mA
		XC3S250E	15	78	104	mA
		XC3S500E	25	106	145	mA
		XC3S1200E	50	259	324	mA
		XC3S1600E	65	366	457	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC3S100E	0.8	1.0	1.5	mA
		XC3S250E	0.8	1.0	1.5	mA
		XC3S500E	0.8	1.0	1.5	mA
		XC3S1200E	1.5	2.0	2.5	mA
		XC3S1600E	1.5	2.0	2.5	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC3S100E	8	12	13	mA
		XC3S250E	12	22	26	mA
		XC3S500E	18	31	34	mA
		XC3S1200E	35	52	59	mA
		XC3S1600E	45	76	86	mA

Notes:

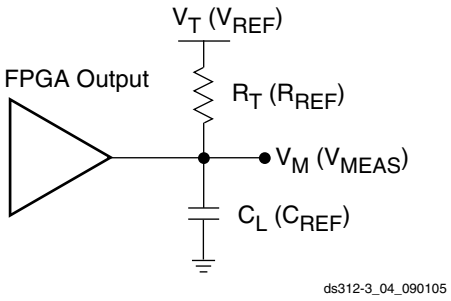
1. The maximum numbers in this table indicate the minimum current each power rail requires in order for the FPGA to power-on successfully.
2. The numbers in this table are based on the conditions set forth in Table 77.
3. Quiescent supply current is measured with all I/O drivers in a high-impedance state and with all pull-up/pull-down resistors at the I/O pads disabled. Typical values are characterized using typical devices at room temperature (T_J of 25°C at V_{CCINT} = 1.2 V, V_{CCO} = 3.3V, and V_{CCAUX} = 2.5V). The maximum limits are tested for each device at the respective maximum specified junction temperature and at maximum voltage limits with V_{CCINT} = 1.26V, V_{CCO} = 3.465V, and V_{CCAUX} = 2.625V. The FPGA is programmed with a "blank" configuration data file (i.e., a design with no functional elements instantiated). For conditions other than those described above, (e.g., a design including functional elements), measured quiescent current levels may be different than the values in the table. For more accurate estimates for a specific design, use the Xilinx® XPower tools.
4. There are two recommended ways to estimate the total power consumption (quiescent plus dynamic) for a specific design: a) The Spartan-3E XPower Estimator provides quick, approximate, typical estimates, and does not require a netlist of the design. b) XPower Analyzer uses a netlist as input to provide maximum estimates as well as more accurate typical estimates.

Timing Measurement Methodology

When measuring timing parameters at the programmable I/Os, different signal standards call for different test conditions. Table 95 lists the conditions to use for each standard.

The method for measuring Input timing is as follows: A signal that swings between a Low logic level of V_L and a High logic level of V_H is applied to the Input under test. Some standards also require the application of a bias voltage to the V_{REF} pins of a given bank to properly set the input-switching threshold. The measurement point of the Input signal (V_M) is commonly located halfway between V_L and V_H.

The Output test setup is shown in Figure 72. A termination voltage V_T is applied to the termination resistor R_T, the other end of which is connected to the Output. For each standard, R_T and V_T generally take on the standard values recommended for minimizing signal reflections. If the standard does not ordinarily use terminations (e.g., LVCMOS, LVTTL), then R_T is set to 1MΩ to indicate an open connection, and V_T is set to zero. The same measurement point (V_M) that was used at the Input is also used at the Output.



Notes:

1. The names shown in parentheses are used in the IBIS file.

Figure 72: **Output Test Setup**

Table 95: **Test Methods for Timing Measurement at I/Os**

Signal Standard (IOSTANDARD)		Inputs			Outputs		Inputs and Outputs
		V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
Single-Ended							
LVTTL		-	0	3.3	1M	0	1.4
LVCMOS33		-	0	3.3	1M	0	1.65
LVCMOS25		-	0	2.5	1M	0	1.25
LVCMOS18		-	0	1.8	1M	0	0.9
LVCMOS15		-	0	1.5	1M	0	0.75
LVCMOS12		-	0	1.2	1M	0	0.6
PCI33_3	Rising	-	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
PCI66_3	Rising	-	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
HSTL_I_18		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
HSTL_III_18		1.1	V_{REF} – 0.5	V_{REF} + 0.5	50	1.8	V_{REF}
SSTL18_I		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
SSTL2_I		1.25	V_{REF} – 0.75	V_{REF} + 0.75	50	1.25	V_{REF}
Differential							
LVDS_25		-	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
BLVDS_25		-	V_{ICM} – 0.125	V_{ICM} + 0.125	1M	0	V_{ICM}
MINI_LVDS_25		-	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
LVPECL_25		-	V_{ICM} – 0.3	V_{ICM} + 0.3	1M	0	V_{ICM}
RSDS_25		-	V_{ICM} – 0.1	V_{ICM} + 0.1	50	1.2	V_{ICM}

Configurable Logic Block (CLB) Timing

Table 98: **CLB (SLICEM) Timing**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{CKO}	When reading from the FFX (FFY) Flip-Flop, the time from the active transition at the CLK input to data appearing at the XQ (YQ) output	-	0.52	-	0.60	ns
Setup Times						
T_{AS}	Time from the setup of data at the F or G input to the active transition at the CLK input of the CLB	0.46	-	0.52	-	ns
T_{DICK}	Time from the setup of data at the BX or BY input to the active transition at the CLK input of the CLB	1.58	-	1.81	-	ns
Hold Times						
T_{AH}	Time from the active transition at the CLK input to the point where data is last held at the F or G input	0	-	0	-	ns
T_{CKDI}	Time from the active transition at the CLK input to the point where data is last held at the BX or BY input	0	-	0	-	ns
Clock Timing						
T_{CH}	The High pulse width of the CLB's CLK signal	0.70	-	0.80	-	ns
T_{CL}	The Low pulse width of the CLK signal	0.70	-	0.80	-	ns
F_{TOG}	Toggle frequency (for export control)	0	657	0	572	MHz
Propagation Times						
T_{ILO}	The time it takes for data to travel from the CLB's F (G) input to the X (Y) output	-	0.66	-	0.76	ns
Set/Reset Pulse Width						
T_{RPW_CLB}	The minimum allowable pulse width, High or Low, to the CLB's SR input	1.57	-	1.80	-	ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 77.

Table 105: **Switching Characteristics for the DLL *(Cont'd)***

Symbol	Description		Device	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Phase Alignment(4)								
CLKIN_CLKFB_PHASE	Phase offset between the CLKIN and CLKFB inputs		All	-	±200	-	±200	ps
CLKOUT_PHASE_DLL	Phase offset between DLL outputs	CLK0 to CLK2X (not CLK2X180)		-	±[1% of CLKIN period + 100]	-	±[1% of CLKIN period + 100]	ps
		All others		-	±[1% of CLKIN period + 200]	-	±[1% of CLKIN period + 200]	ps
Lock Time								
LOCK_DLL(3)	When using the DLL alone: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase	5 MHz ≤ F_{CLKIN} ≤ 15 MHz	All	-	5	-	5	ms
		F_{CLKIN} > 15 MHz		-	600	-	600	µs
Delay Lines								
DCM_DELAY_STEP	Finest delay resolution		All	20	40	20	40	ps

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 77 and Table 104.
2. Indicates the maximum amount of output jitter that the DCM adds to the jitter on the CLKIN input.
3. For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
4. Some jitter and duty-cycle specifications include 1% of input clock period or 0.01 UI.
   Example: The data sheet specifies a maximum jitter of ±[1% of CLKIN period + 150]. Assume the CLKIN frequency is 100 MHz. The equivalent CLKIN period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 150 ps] = ±250 ps.

Digital Frequency Synthesizer (DFS)

Table 106: **Recommended Operating Conditions for the DFS**

Symbol		Description		Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Input Frequency Ranges(2)								
F_{CLKIN}	CLKIN_FREQ_FX	Frequency for the CLKIN input		0.200	333(4)	0.200	333(4)	MHz
Input Clock Jitter Tolerance(3)								
CLKIN_CYC_JITT_FX_LF		Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency	F_{CLKFX} ≤ 150 MHz	-	±300	-	±300	ps
CLKIN_CYC_JITT_FX_HF			F_{CLKFX} > 150 MHz	-	±150	-	±150	ps
CLKIN_PER_JITT_FX		Period jitter at the CLKIN input		-	±1	-	±1	ns

Notes:

1. DFS specifications apply when either of the DFS outputs (CLKFX or CLKFX180) are used.
2. If both DFS and DLL outputs are used on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 104.
3. CLKIN input jitter beyond these limits may cause the DCM to lose lock.
4. To support double the maximum effective FCLKIN limit, set the CLKIN_DIVIDE_BY_2 attribute to TRUE. This attribute divides the incoming clock frequency by two as it enters the DCM.

Table 119: **Configuration Timing Requirements for Attached SPI Serial Flash**

Symbol	Description	Requirement	Units
T_{CCS}	SPI serial Flash PROM chip-select time	$T_{CCS} \leq T_{MCCL1} - T_{CCO}$	ns
T_{DSU}	SPI serial Flash PROM data input setup time	$T_{DSU} \leq T_{MCCL1} - T_{CCO}$	ns
T_{DH}	SPI serial Flash PROM data input hold time	$T_{DH} \leq T_{MCCH1}$	ns
T_V	SPI serial Flash PROM data clock-to-output time	$T_V \leq T_{MCCLn} - T_{DCC}$	ns
f_C or f_R	Maximum SPI serial Flash PROM clock frequency (also depends on specific read command used)	$f_C \geq \frac{1}{T_{CCLKn(min)}}$	MHz

Notes:

1. These requirements are for successful FPGA configuration in SPI mode, where the FPGA provides the CCLK frequency. The post configuration timing can be different to support the specific needs of the application loaded into the FPGA and the resulting clock source.
2. Subtract additional printed circuit board routing delay as required by the application.

Table 143: **FT256 Package Pinout *(Cont'd)***

Bank	XC3S250E Pin Name	XC3S500E Pin Name	XC3S1200E Pin Name	FT256 Ball	Type
0	IO_L12P_0	IO_L12P_0	IO_L12P_0	E8	I/O
0	N.C. (◆)	IO_L13N_0	IO_L13N_0	C7	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O
0	N.C. (◆)	IO_L13P_0	IO_L13P_0	B7	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O
0	IO_L14N_0/VREF_0	IO_L14N_0/VREF_0	IO_L14N_0/VREF_0	D7	VREF
0	IO_L14P_0	IO_L14P_0	IO_L14P_0	E7	I/O
0	IO_L15N_0	IO_L15N_0	IO_L15N_0	D6	I/O
0	IO_L15P_0	IO_L15P_0	IO_L15P_0	C6	I/O
0	IO_L17N_0/VREF_0	IO_L17N_0/VREF_0	IO_L17N_0/VREF_0	A4	VREF
0	IO_L17P_0	IO_L17P_0	IO_L17P_0	A5	I/O
0	IO_L18N_0	IO_L18N_0	IO_L18N_0	C4	I/O
0	IO_L18P_0	IO_L18P_0	IO_L18P_0	C5	I/O
0	IO_L19N_0/HSWAP	IO_L19N_0/HSWAP	IO_L19N_0/HSWAP	B3	DUAL
0	IO_L19P_0	IO_L19P_0	IO_L19P_0	C3	I/O
0	IP	IP	IP	A3	INPUT
0	IP	IP	IP	C13	INPUT
0	IP_L02N_0	IP_L02N_0	IP_L02N_0	C12	INPUT
0	IP_L02P_0	IP_L02P_0	IP_L02P_0	D12	INPUT
0	IP_L07N_0	IP_L07N_0	IP_L07N_0	C9	INPUT
0	IP_L07P_0	IP_L07P_0	IP_L07P_0	C10	INPUT
0	IP_L10N_0/GCLK9	IP_L10N_0/GCLK9	IP_L10N_0/GCLK9	B8	GCLK
0	IP_L10P_0/GCLK8	IP_L10P_0/GCLK8	IP_L10P_0/GCLK8	A8	GCLK
0	IP_L16N_0	IP_L16N_0	IP_L16N_0	E6	INPUT
0	IP_L16P_0	IP_L16P_0	IP_L16P_0	D5	INPUT
0	VCCO_0	VCCO_0	VCCO_0	B5	VCCO
0	VCCO_0	VCCO_0	VCCO_0	B12	VCCO
0	VCCO_0	VCCO_0	VCCO_0	F7	VCCO
0	VCCO_0	VCCO_0	VCCO_0	F10	VCCO
1	IO_L01N_1/A15	IO_L01N_1/A15	IO_L01N_1/A15	R15	DUAL
1	IO_L01P_1/A16	IO_L01P_1/A16	IO_L01P_1/A16	R16	DUAL
1	IO_L02N_1/A13	IO_L02N_1/A13	IO_L02N_1/A13	P15	DUAL
1	IO_L02P_1/A14	IO_L02P_1/A14	IO_L02P_1/A14	P16	DUAL
1	N.C. (◆)	IO_L03N_1/VREF_1	IO_L03N_1/VREF_1	N15	***250E:*** N.C. ***500E:*** VREF ***1200E:*** VREF
1	N.C. (◆)	IO_L03P_1	IO_L03P_1	N14	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O
1	IO_L04N_1/VREF_1	IO_L04N_1/VREF_1	IO_L04N_1/VREF_1	M16	VREF
1	IO_L04P_1	IO_L04P_1	IO_L04P_1	N16	I/O
1	N.C. (◆)	IO_L05N_1	IO_L05N_1	L13	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O

Table 143: **FT256 Package Pinout *(Cont'd)***

Bank	XC3S250E Pin Name	XC3S500E Pin Name	XC3S1200E Pin Name	FT256 Ball	Type
3	IO_L06P_3	IO_L06P_3	IO_L06P_3	G5	I/O
3	IO_L07N_3	IO_L07N_3	IO_L07N_3	G2	I/O
3	IO_L07P_3	IO_L07P_3	IO_L07P_3	G3	I/O
3	IO_L08N_3/LHCLK1	IO_L08N_3/LHCLK1	IO_L08N_3/LHCLK1	H6	LHCLK
3	IO_L08P_3/LHCLK0	IO_L08P_3/LHCLK0	IO_L08P_3/LHCLK0	H5	LHCLK
3	IO_L09N_3/LHCLK3/ IRDY2	IO_L09N_3/LHCLK3/ IRDY2	IO_L09N_3/LHCLK3/ IRDY2	H4	LHCLK
3	IO_L09P_3/LHCLK2	IO_L09P_3/LHCLK2	IO_L09P_3/LHCLK2	H3	LHCLK
3	IO_L10N_3/LHCLK5	IO_L10N_3/LHCLK5	IO_L10N_3/LHCLK5	J3	LHCLK
3	IO_L10P_3/LHCLK4/ TRDY2	IO_L10P_3/LHCLK4/ TRDY2	IO_L10P_3/LHCLK4/ TRDY2	J2	LHCLK
3	IO_L11N_3/LHCLK7	IO_L11N_3/LHCLK7	IO_L11N_3/LHCLK7	J4	LHCLK
3	IO_L11P_3/LHCLK6	IO_L11P_3/LHCLK6	IO_L11P_3/LHCLK6	J5	LHCLK
3	IO_L12N_3	IO_L12N_3	IO_L12N_3	K1	I/O
3	IO_L12P_3	IO_L12P_3	IO_L12P_3	J1	I/O
3	IO_L13N_3	IO_L13N_3	IO_L13N_3	K3	I/O
3	IO_L13P_3	IO_L13P_3	IO_L13P_3	K2	I/O
3	N.C. (◆)	IO_L14N_3/VREF_3	IO_L14N_3/VREF_3	L2	***250E:*** N.C. ***500E:*** VREF ***1200E:*** VREF
3	N.C. (◆)	IO_L14P_3	IO_L14P_3	L3	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O
3	IO_L15N_3	IO_L15N_3	IO_L15N_3	L5	I/O
3	IO_L15P_3	IO_L15P_3	IO_L15P_3	K5	I/O
3	IO_L16N_3	IO_L16N_3	IO_L16N_3	N1	I/O
3	IO_L16P_3	IO_L16P_3	IO_L16P_3	M1	I/O
3	N.C. (◆)	IO_L17N_3	IO_L17N_3	L4	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O
3	N.C. (◆)	IO_L17P_3	IO_L17P_3	M4	***250E:*** N.C. ***500E:*** I/O ***1200E:*** I/O
3	IO_L18N_3	IO_L18N_3	IO_L18N_3	P1	I/O
3	IO_L18P_3	IO_L18P_3	IO_L18P_3	P2	I/O
3	IO_L19N_3	IO_L19N_3	IO_L19N_3	R1	I/O
3	IO_L19P_3	IO_L19P_3	IO_L19P_3	R2	I/O
3	IP	IP	IP	D2	INPUT
3	IP	IP	IP	F2	INPUT
3	IO	IO	IP	F5	***250E:*** I/O ***500E:*** I/O ***1200E:*** INPUT
3	IP	IP	IP	H1	INPUT
3	IP	IP	IP	J6	INPUT
3	IP	IP	IP	K4	INPUT
3	IP	IP	IP	M3	INPUT

Table 154: **FG484 Package Pinout *(Cont'd)***

Bank	XC3S1600E Pin Name	FG484 Ball	Type
2	IO_L19N_2/D6/GCLK13	U11	DUAL/ GCLK
2	IO_L19P_2/D7/GCLK12	V11	DUAL/ GCLK
2	IO_L20N_2/D3/GCLK15	T11	DUAL/ GCLK
2	IO_L20P_2/D4/GCLK14	R11	DUAL/ GCLK
2	IO_L22N_2/D1/GCLK3	W12	DUAL/ GCLK
2	IO_L22P_2/D2/GCLK2	Y12	DUAL/ GCLK
2	IO_L23N_2/DIN/D0	U12	DUAL
2	IO_L23P_2/M0	V12	DUAL
2	IO_L25N_2	Y13	I/O
2	IO_L25P_2	W13	I/O
2	IO_L26N_2/VREF_2	U14	VREF
2	IO_L26P_2	U13	I/O
2	IO_L27N_2	T14	I/O
2	IO_L27P_2	R14	I/O
2	IO_L28N_2	Y14	I/O
2	IO_L28P_2	AA14	I/O
2	IO_L29N_2	W14	I/O
2	IO_L29P_2	V14	I/O
2	IO_L30N_2	AB15	I/O
2	IO_L30P_2	AA15	I/O
2	IO_L32N_2	W15	I/O
2	IO_L32P_2	Y15	I/O
2	IO_L33N_2	U16	I/O
2	IO_L33P_2	V16	I/O
2	IO_L35N_2/A22	AB17	DUAL
2	IO_L35P_2/A23	AA17	DUAL
2	IO_L36N_2	W17	I/O
2	IO_L36P_2	Y17	I/O
2	IO_L38N_2/A20	Y18	DUAL
2	IO_L38P_2/A21	W18	DUAL
2	IO_L39N_2/VS1/A18	AA20	DUAL
2	IO_L39P_2/VS2/A19	AB20	DUAL
2	IO_L40N_2/CCLK	W19	DUAL
2	IO_L40P_2/VS0/A17	Y19	DUAL
2	IP	V17	INPUT
2	IP	AB2	INPUT
2	IP_L02N_2	AA4	INPUT
2	IP_L02P_2	Y4	INPUT
2	IP_L05N_2	Y6	INPUT
2	IP_L05P_2	AA6	INPUT

Table 154: **FG484 Package Pinout *(Cont'd)***

Bank	XC3S1600E Pin Name	FG484 Ball	Type
2	IP_L08N_2	AB7	INPUT
2	IP_L08P_2	AB6	INPUT
2	IP_L15N_2	Y10	INPUT
2	IP_L15P_2	W10	INPUT
2	IP_L18N_2/VREF_2	AA11	VREF
2	IP_L18P_2	Y11	INPUT
2	IP_L21N_2/M2/GCLK1	P12	DUAL/ GCLK
2	IP_L21P_2/RDWR_B/ GCLK0	R12	DUAL/ GCLK
2	IP_L24N_2	R13	INPUT
2	IP_L24P_2	T13	INPUT
2	IP_L31N_2/VREF_2	T15	VREF
2	IP_L31P_2	U15	INPUT
2	IP_L34N_2	Y16	INPUT
2	IP_L34P_2	W16	INPUT
2	IP_L37N_2	AA19	INPUT
2	IP_L37P_2	AB19	INPUT
2	VCCO_2	T12	VCCO
2	VCCO_2	U9	VCCO
2	VCCO_2	V15	VCCO
2	VCCO_2	AA5	VCCO
2	VCCO_2	AA9	VCCO
2	VCCO_2	AA13	VCCO
2	VCCO_2	AA18	VCCO
3	IO_L01N_3	C1	I/O
3	IO_L01P_3	C2	I/O
3	IO_L02N_3/VREF_3	D2	VREF
3	IO_L02P_3	D3	I/O
3	IO_L03N_3	E3	I/O
3	IO_L03P_3	E4	I/O
3	IO_L04N_3	E1	I/O
3	IO_L04P_3	D1	I/O
3	IO_L05N_3	F4	I/O
3	IO_L05P_3	F3	I/O
3	IO_L06N_3	G5	I/O
3	IO_L06P_3	G4	I/O
3	IO_L07N_3	F1	I/O
3	IO_L07P_3	G1	I/O
3	IO_L08N_3/VREF_3	G6	VREF
3	IO_L08P_3	G7	I/O
3	IO_L09N_3	H4	I/O
3	IO_L09P_3	H5	I/O
3	IO_L10N_3	H2	I/O
3	IO_L10P_3	H3	I/O

Table 154: **FG484 Package Pinout *(Cont'd)***

Bank	XC3S1600E Pin Name	FG484 Ball	Type
GND	GND	E10	GND
GND	GND	E13	GND
GND	GND	F6	GND
GND	GND	F17	GND
GND	GND	G2	GND
GND	GND	G21	GND
GND	GND	J4	GND
GND	GND	J9	GND
GND	GND	J12	GND
GND	GND	J14	GND
GND	GND	J19	GND
GND	GND	K10	GND
GND	GND	K12	GND
GND	GND	L2	GND
GND	GND	L6	GND
GND	GND	L9	GND
GND	GND	L13	GND
GND	GND	M10	GND
GND	GND	M14	GND
GND	GND	M17	GND
GND	GND	M21	GND
GND	GND	N11	GND
GND	GND	N13	GND
GND	GND	P4	GND
GND	GND	P9	GND
GND	GND	P11	GND
GND	GND	P14	GND
GND	GND	P19	GND
GND	GND	T2	GND
GND	GND	T21	GND
GND	GND	U6	GND
GND	GND	U17	GND
GND	GND	V10	GND
GND	GND	V13	GND
GND	GND	Y3	GND
GND	GND	Y20	GND
GND	GND	AA7	GND
GND	GND	AA16	GND

Table 154: **FG484 Package Pinout *(Cont'd)***

Bank	XC3S1600E Pin Name	FG484 Ball	Type
GND	GND	AB1	GND
GND	GND	AB12	GND
GND	GND	AB22	GND
VCCAUX	DONE	AA21	CONFIG
VCCAUX	PROG_B	B1	CONFIG
VCCAUX	TCK	E17	JTAG
VCCAUX	TDI	B2	JTAG
VCCAUX	TDO	B20	JTAG
VCCAUX	TMS	D19	JTAG
VCCAUX	VCCAUX	D12	VCCAUX
VCCAUX	VCCAUX	E5	VCCAUX
VCCAUX	VCCAUX	E18	VCCAUX
VCCAUX	VCCAUX	K14	VCCAUX
VCCAUX	VCCAUX	L4	VCCAUX
VCCAUX	VCCAUX	M19	VCCAUX
VCCAUX	VCCAUX	N9	VCCAUX
VCCAUX	VCCAUX	V5	VCCAUX
VCCAUX	VCCAUX	V18	VCCAUX
VCCAUX	VCCAUX	W11	VCCAUX
VCCINT	VCCINT	J10	VCCINT
VCCINT	VCCINT	K9	VCCINT
VCCINT	VCCINT	K11	VCCINT
VCCINT	VCCINT	K13	VCCINT
VCCINT	VCCINT	L10	VCCINT
VCCINT	VCCINT	L11	VCCINT
VCCINT	VCCINT	L12	VCCINT
VCCINT	VCCINT	L14	VCCINT
VCCINT	VCCINT	M9	VCCINT
VCCINT	VCCINT	M11	VCCINT
VCCINT	VCCINT	M12	VCCINT
VCCINT	VCCINT	M13	VCCINT
VCCINT	VCCINT	N10	VCCINT
VCCINT	VCCINT	N12	VCCINT
VCCINT	VCCINT	N14	VCCINT
VCCINT	VCCINT	P13	VCCINT

User I/Os by Bank

Table 155 indicates how the 304 available user-I/O pins are distributed between the four I/O banks on the FG484 package.

Table 155: **User I/Os Per Bank for the XC3S1600E in the FG484 Package**

Package Edge	I/O Bank	Maximum I/O	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF[1]	CLK[2]
Top	0	94	56	22	1	7	8
Right	1	94	50	16	21	7	0[2]
Bottom	2	94	45	18	24	7	0[2]
Left	3	94	63	16	0	7	8
TOTAL		**376**	**214**	**72**	**46**	**28**	**16**

Notes:

1. Some VREF and CLK pins are on INPUT pins.
2. The eight global clock pins in this bank have optional functionality during configuration and are counted in the DUAL column.

Footprint Migration Differences

The XC3S1600E FPGA is the only Spartan-3E device offered in the FG484 package.